AHCAL – DIF Interface

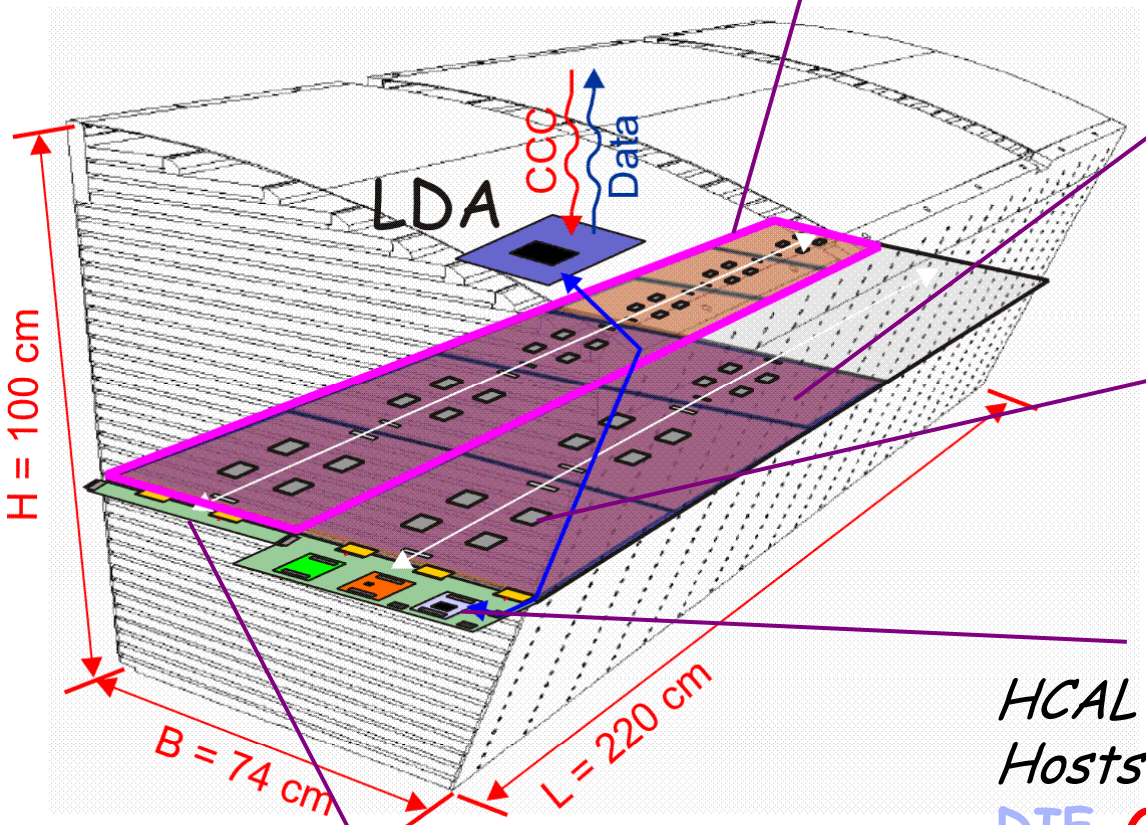
M. Reinecke

AHCAL Half Sector - Integration

FEB

AHCAL Slab

6 HBUs in a row



HBU

HCAL Base Unit

typ. 12 x 12 tiles

SPIROC

typ. 4 on a HBU

HEB

HCAL Endcap Board

Hosts mezzanine modules:

DIF, **CALIB** and **POWER**

HLD

HCAL Layer Distributor

HEB Interconnection Concept

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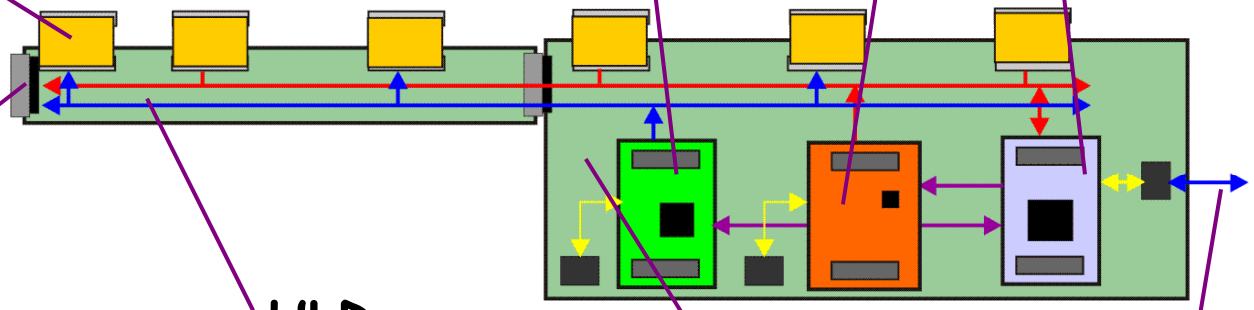
Flexlead and 80-pin connector
Interconnection to AHCAL-Layer (HBU)

POWER CALIB DIF



DIF-DIF conn.
Redundancy against failures of LDA

HLD
Changes Size from Layer to layer

HEB
Same Size for all 38 AHCAL layers

To LDA

DIF - *Detector Interface (Configuration and Operation)*
CALIB - *Light and/or Charge calibration and monitoring*
POWER - *Layer power and temperature monitors*

Mezzanine setup allows independent development of different groups.

Slabs of an AHCAL layer

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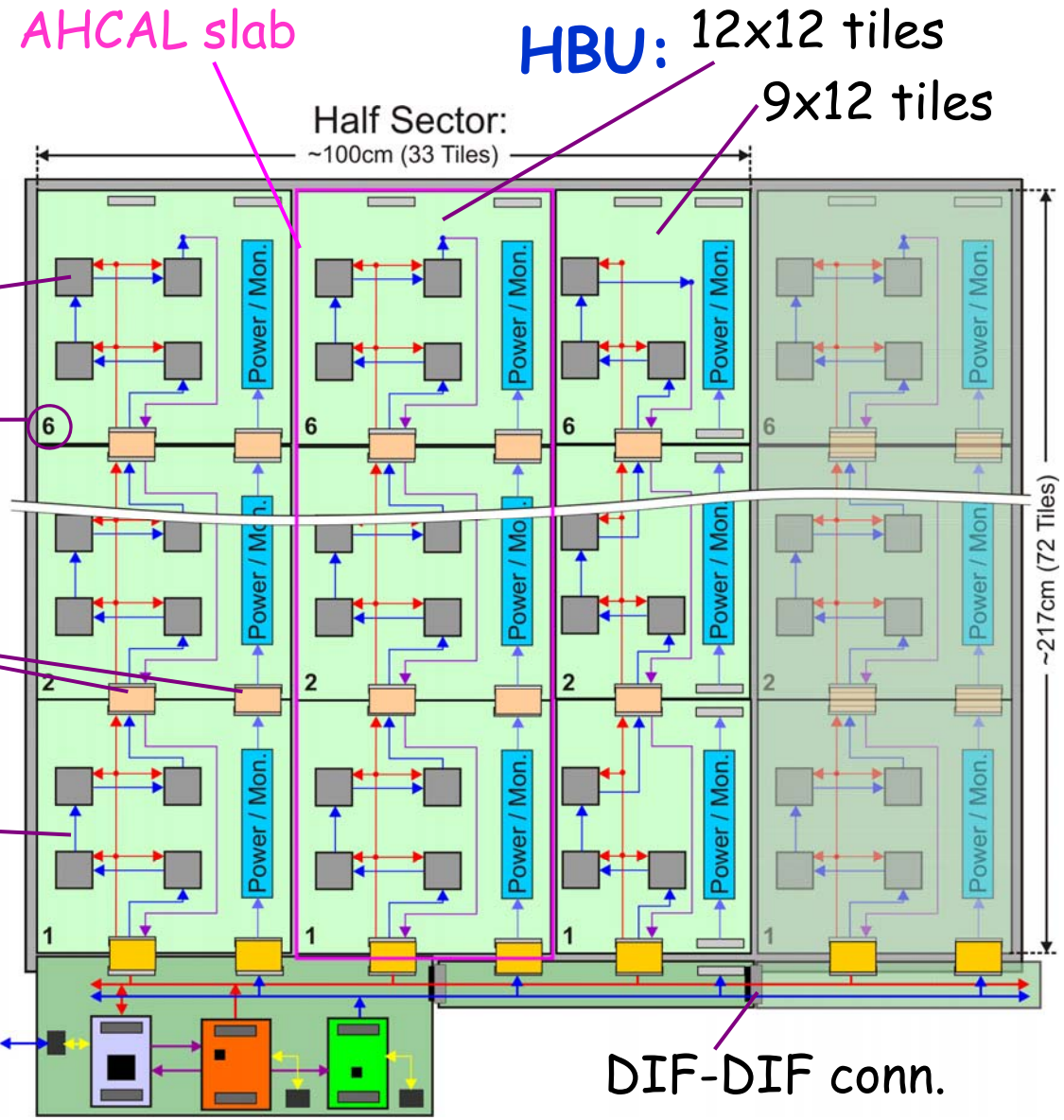
Number of channels per layer not constant!

24 SPIROCs in chain

6 HBUs in a row

Two flexleads for interconnection

Slow-Control and Readout token



DAQ and AHCAL Data Rate

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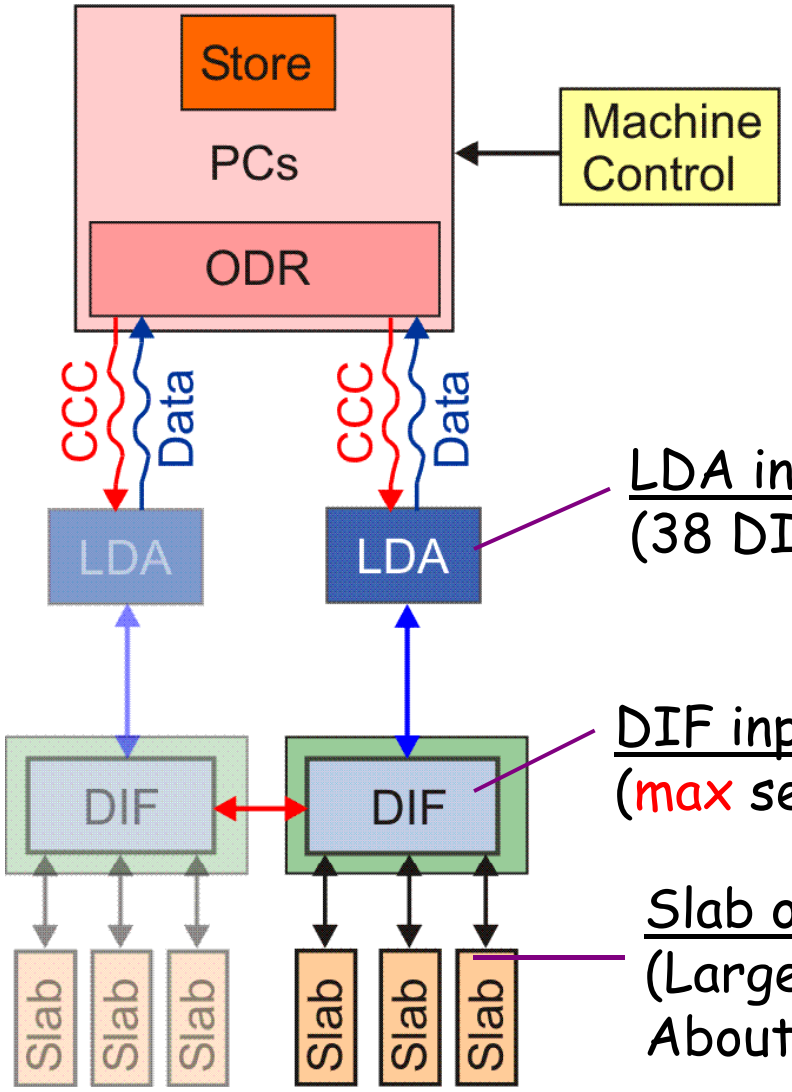


ODR: Off-Detector Receiver
LDA: Link/Data Aggregator
DIF: Detector (specific) Interface
CCC: Clock/Control/Config

LDA input data rate: max. 53MBit/bunch train
(38 DIFs connected)

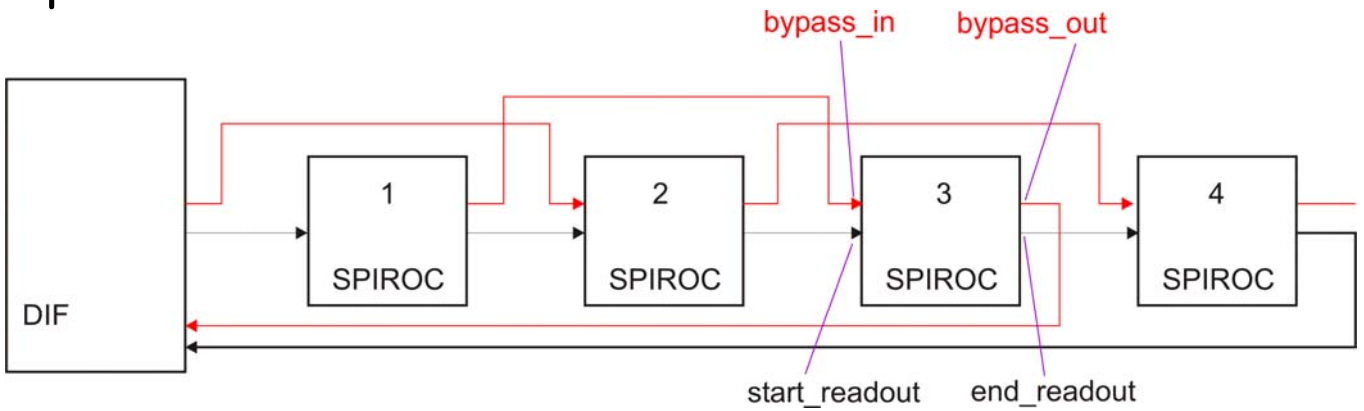
DIF input data rate: max 1.4MBit/bunch train.
(max setup: up to 3 slabs per DIF)

Slab output data rate: max. 460kBit.
(Largest slab: 24 SPIROCs in a readout chain,
About 19kbit data per SPIROC)

Failsafe Setup

Up to 24 SPIROCs (864 detector channels) in slow-control and readout chain (AHCAL).

A broken chip would disable the complete chain.
Proposal:



If agreed, needs implementation in next ASIC versions!

Power Cycling (SPIROC)

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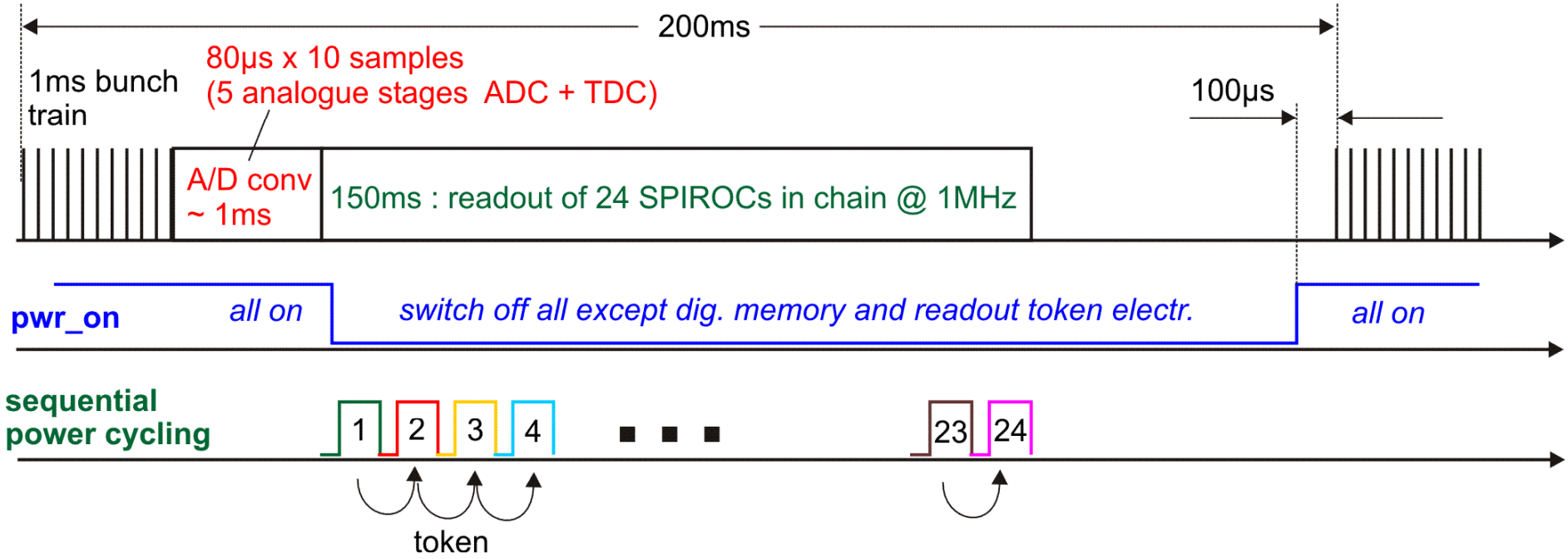

- SPIROC with 5 analogue stages : individual channel trigger, SIPM noise above threshold rate ≈ 300Hz.
- Power cycling <u>after</u> A/D conversion (sensitive analogue memory).
- Sequential power cycling of digital part (≈10% of total power) during readout, controlled by readout token.

Power Cycling II

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Assumption for SPIROC so far: 25μW per channel @ 1% duty cycle.

Proposed Power Cycle: 2.1ms all on (global signal ‚pwr_on')
+ 6ms digital part on (per SPIROC,
5848 bits @ 1MHz,
5 analogue stages)

⇒ ok!

But: Power budget is impaired if more than 5 analogue stages are needed (due to e.g. SiPM noise rate, trigger scheme).

To be checked: Switch off before A/D conversion.

SPIROC – DIF Signalling

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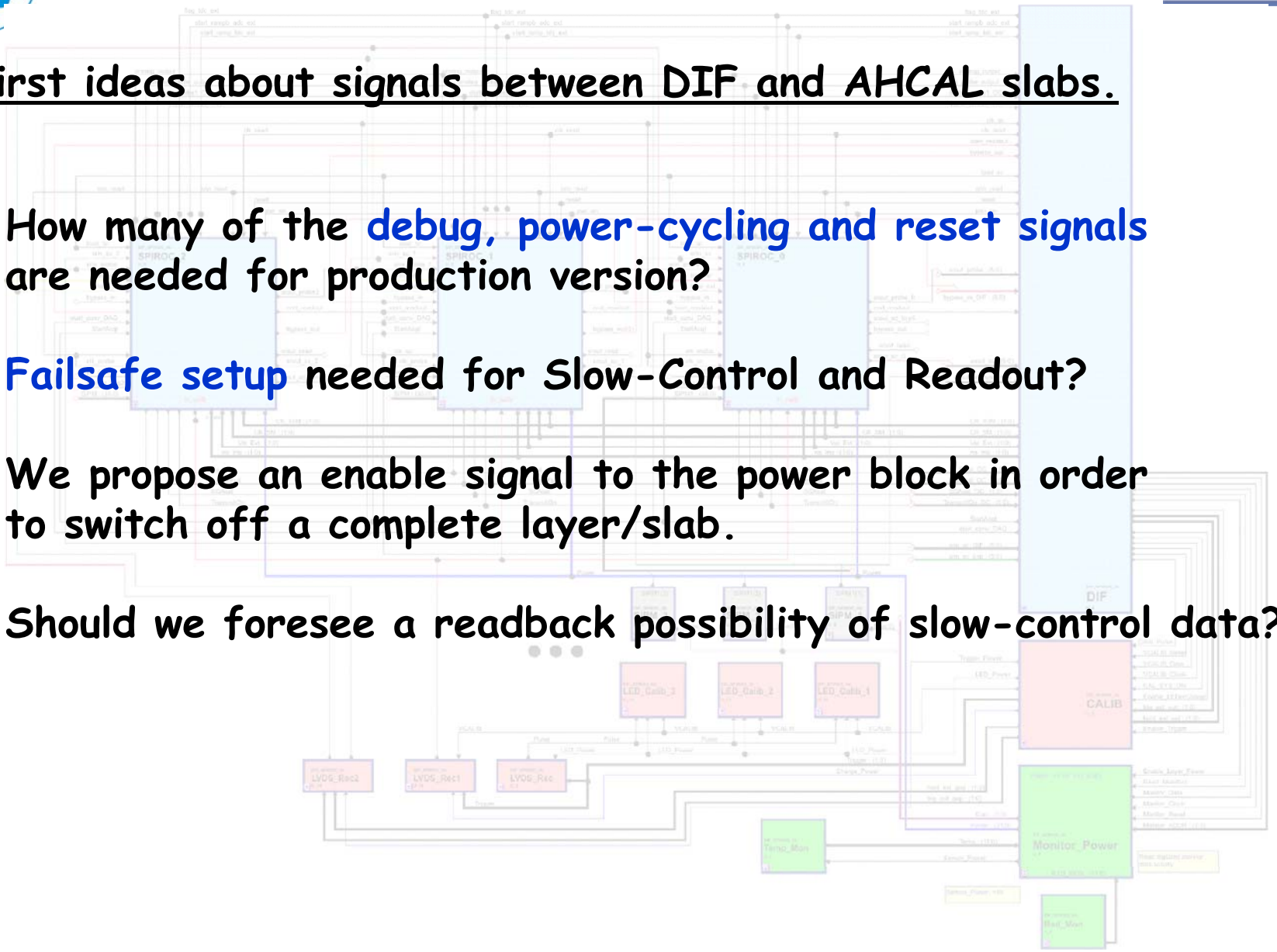
First ideas about signals between DIF and AHCAL slabs.

How many of the debug, power-cycling and reset signals are needed for production version?

Failsafe setup needed for Slow-Control and Readout?

We propose an enable signal to the power block in order to switch off a complete layer/slab.

Should we foresee a readback possibility of slow-control data?



DIF Signals – Common List

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A common signal list has been established:

- clarify differences and analogies of the detector concepts
- create a basis for the definition of the DIF tasks
- enable discussions on the necessity of individual signals

Category	Signal	Function	I/O for slab	Valid on	ECAL (SKIROC)	DHCAL (HARDROC)	AHCAL (SPIROC)
operation control							
	reset*	global reset of complete ASIC	I	low	LVCMOS	LVCMOS	LVCMOS
	RST_counter	reset for the BCID counter	I	high	LVCMOS	LVCMOS	LVCMOS
	Digital_pwr_on	power-cycling control for the digital part	I	high	LVCMOS	LVCMOS	LVCMOS
	Analog_pwr_on	power-cycling control for the analog part	I	high	LVCMOS	LVCMOS	LVCMOS
	DAC_pwr_on	power-cycling control for the DAC part	I	high	LVCMOS		LVCMOS
	ADC_pwr_on	power-cycling control for the ADC part	I	high	LVCMOS		LVCMOS
	start_acq	start data acquisition	I	high	LVCMOS	LVCMOS	LVCMOS
	start_conv_DAQ	start ADC conversion	I	high			LVCMOS
	no_trig	erase active analogue column	I	high			LVDS
	Val_Evt	external validation of event	I	high	LVDS	LVDS	LVDS
	trig_ext	external trigger	I	high	LVDS	LVDS	LVDS
	RAZ_Chn	reset for internal RS flip flops (discriminator outputs)	I	high	LVDS	LVDS	
slow control							
	clk_sc	slow-control shift-reg. clock 1MHz	I	rising	LVCMOS	LVCMOS	LVCMOS
	srin_sc (D_SC)	data input of slow control shift-reg.-chain	I	high	LVCMOS	LVCMOS	LVCMOS
	srout_sc (Q_SC)	output of slow-control shift-reg.-chain	O	high	LVCMOS	LVCMOS	LVCMOS
	load_sc	latch-command for slow control data	I	high			LVCMOS
	srin_sc_byp	bypass input of slow-control reg.	I	high			LVCMOS
	srout_sc_byp	bypass output of slow-control reg.	O	high			LVCMOS
readout							
	start_readout	token input of result data	I	high	LVCMOS	LVCMOS	LVCMOS

Redundancy

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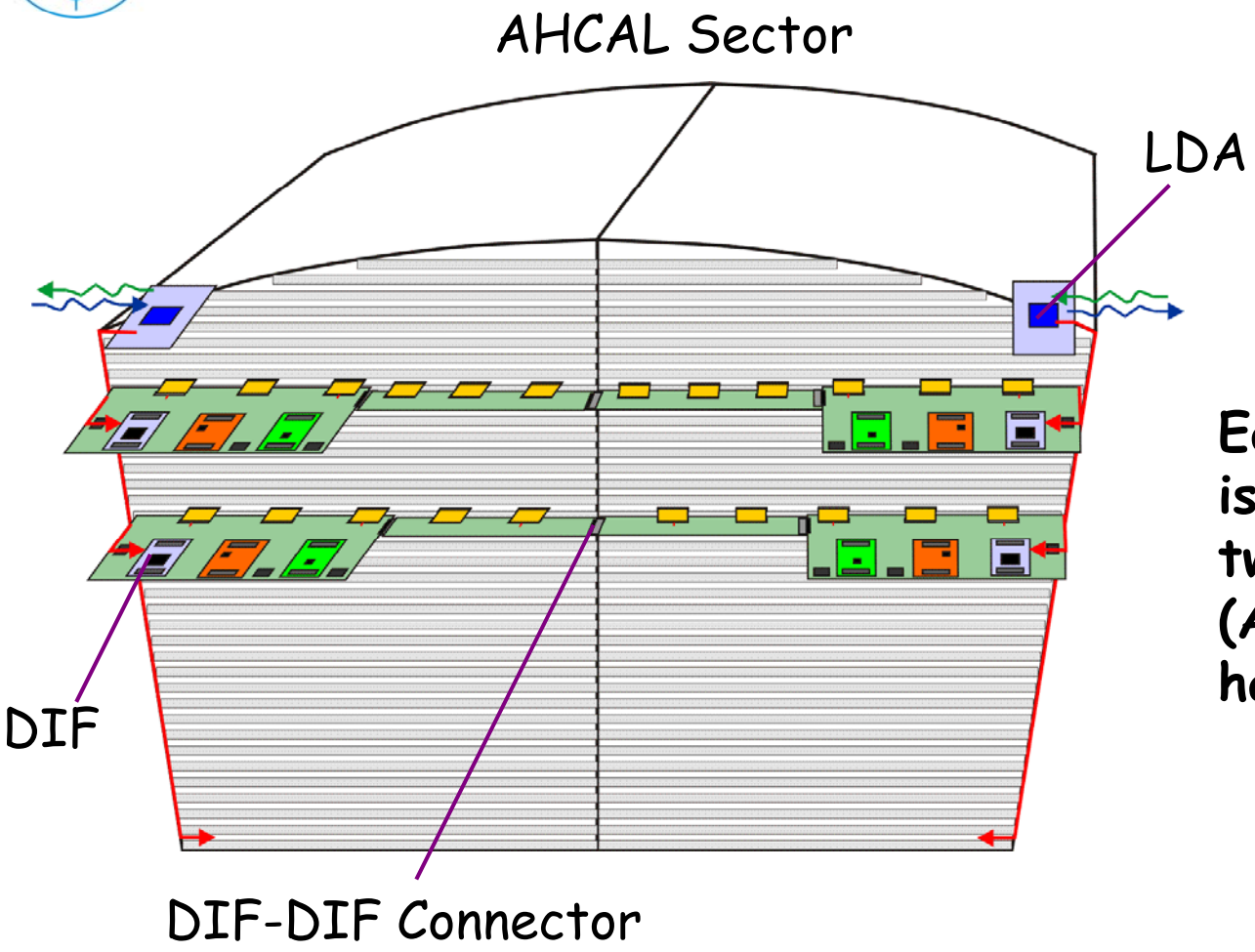

Each AHCAL slab is connected to two LDAs. (A broken DIF has to be replaced)

Redundancy proposal by M. Goodrick, Bart Hommels et al.

Conclusion

- First ideas about AHCAL-DIF setup have been collected.
  Now: discussions and coordination in DIF working group.

- The working group needs input and a final ‚ok' from ASIC designers and „ILC users" about a proposed concept.

- Next step: Agreement on protocol for data transfer for the readout- and slow-control data.