Guide

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- ODR-LDA-DIF-SLAB
- Multitude of Signals
- Multi-Purpose ECAL DIF Model for Lab & Testbeam :
  - Hardware = DIF + Adapter Card
  - Firmware = DIF + Personality
- Physical Arrangement for Prototypes
- SLAB signals :
  - ECAL with SPIROC / HARDROC +
  - Simulation
  - Special Lines:
    - Differential & Multi-Drop : Clocks,,, : Slab-end Termination
    - Multi Source : Readout Data, TXOn,,,
    - Bidirectional : RAM Full (also Multi Drop) – does "wired OR" – polarity?
  - Minimal Set
- Ext Trigger ??
- Clock and Control?? – needs CDR (PLL ?)
- Slow Control :
  - SPI, SPI-like, JTAG, I2C, I2C-like ??
  - Broadcast ?
  - Synchronous ?
- Chip Geographical Addresses : how: bonds, serial chain?
- Redundancy : how? What cost? Needed?

An ECAL DIF

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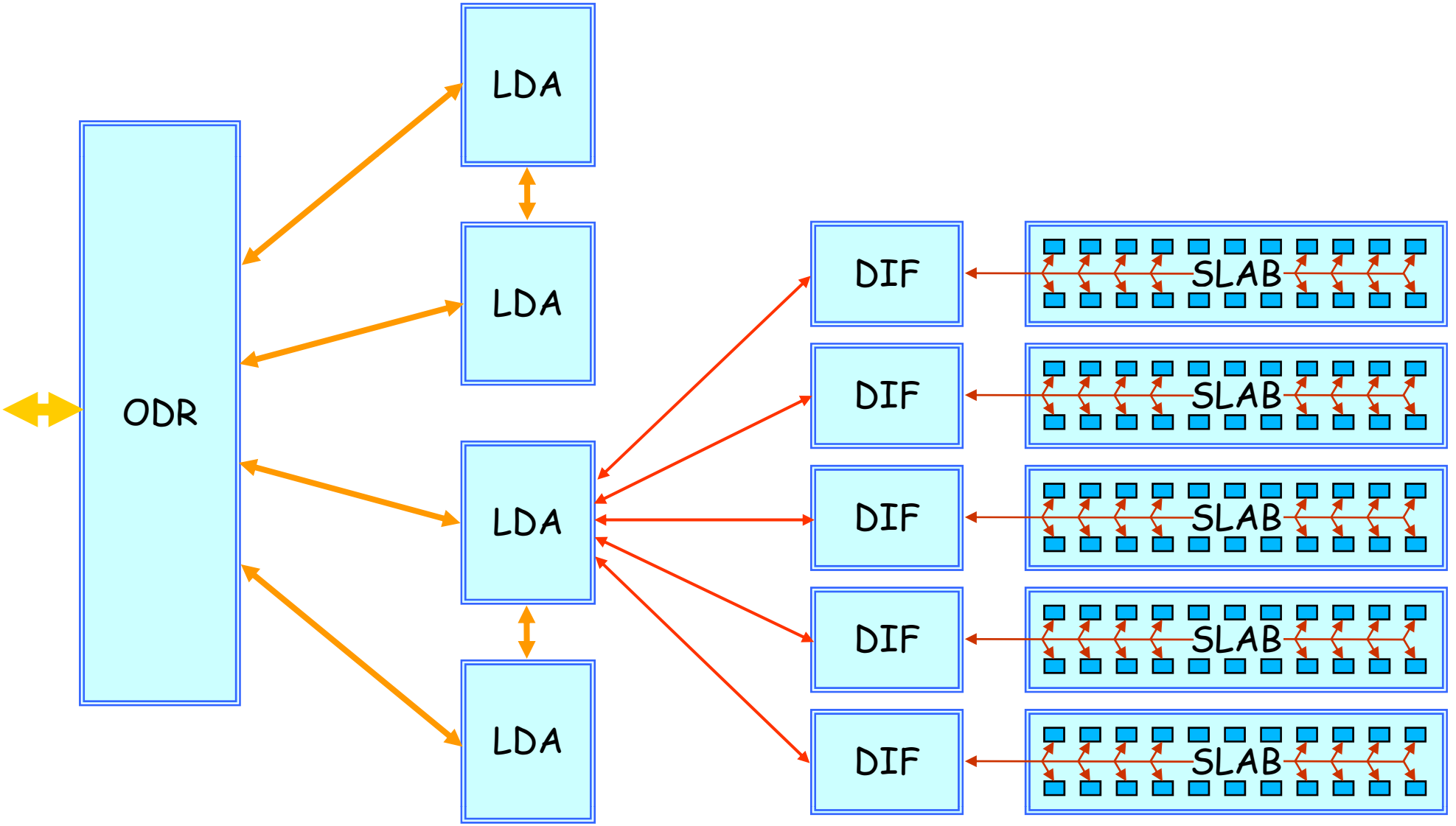
Control: ODR - LDA - DIF - VFE

Readout: VFE - DIF - LDA - ODR



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A Multi Function ECAL DIF

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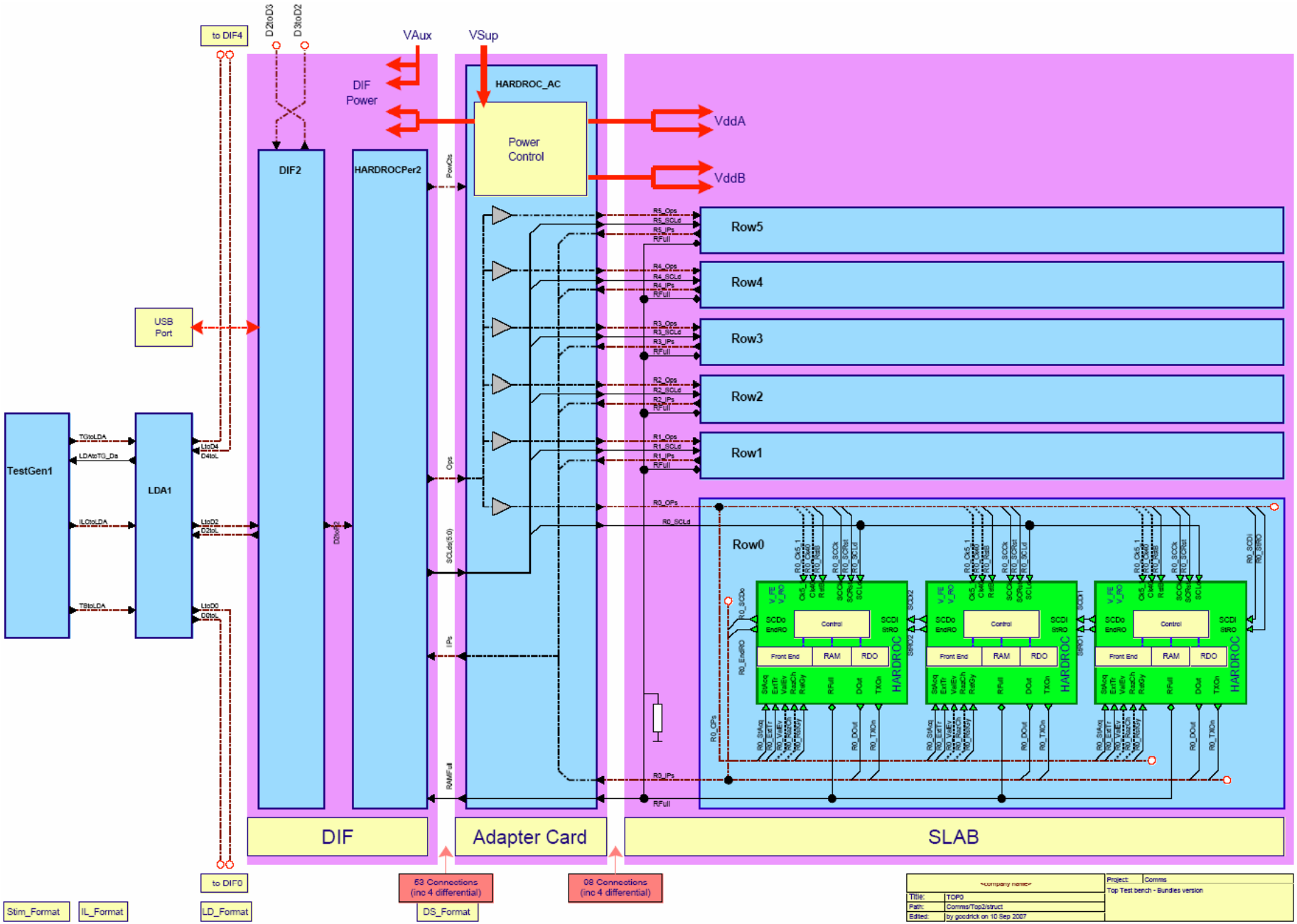

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A Multi Function ECAL DIF - Physical

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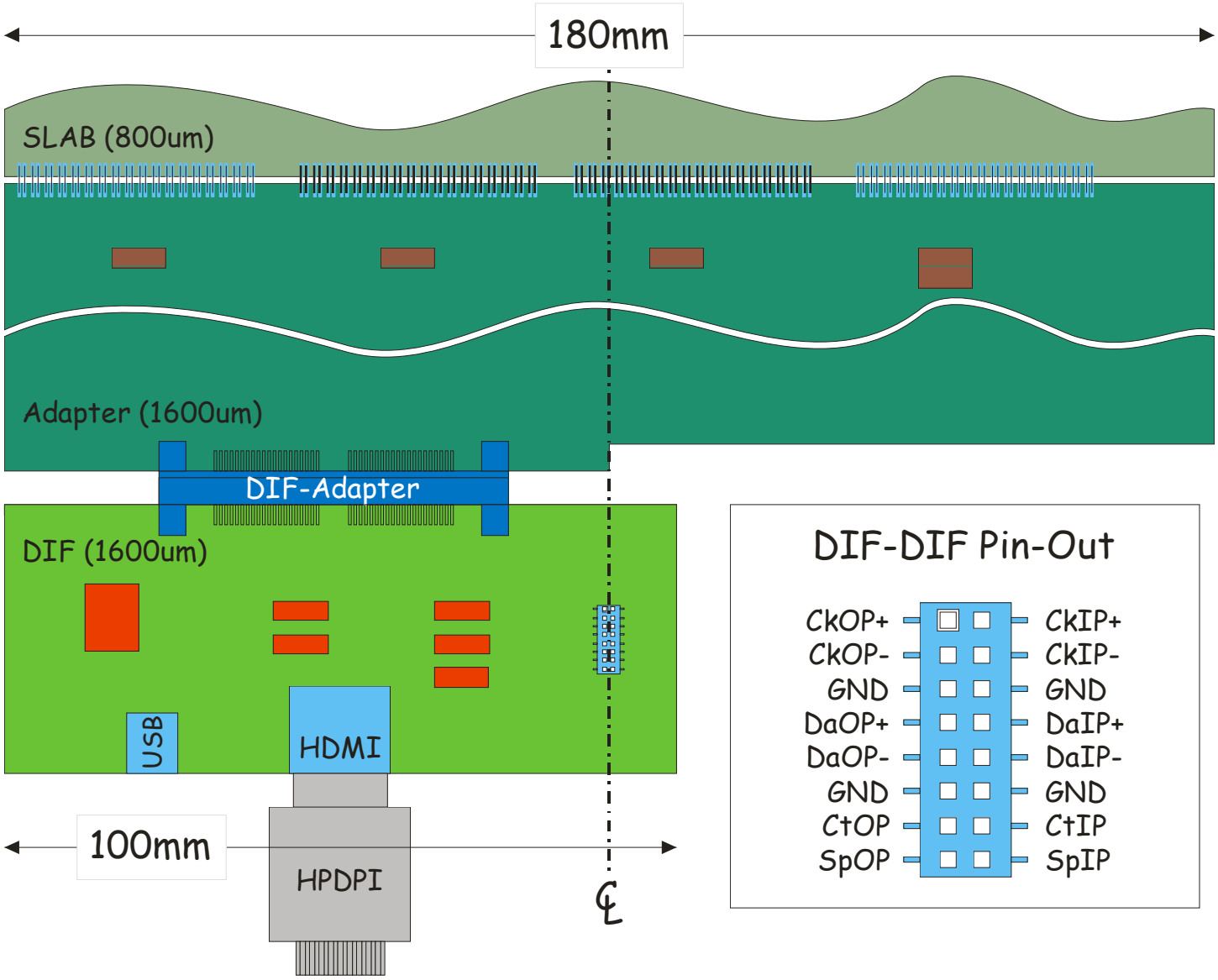

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A Multi Function ECAL DIF - Stacking

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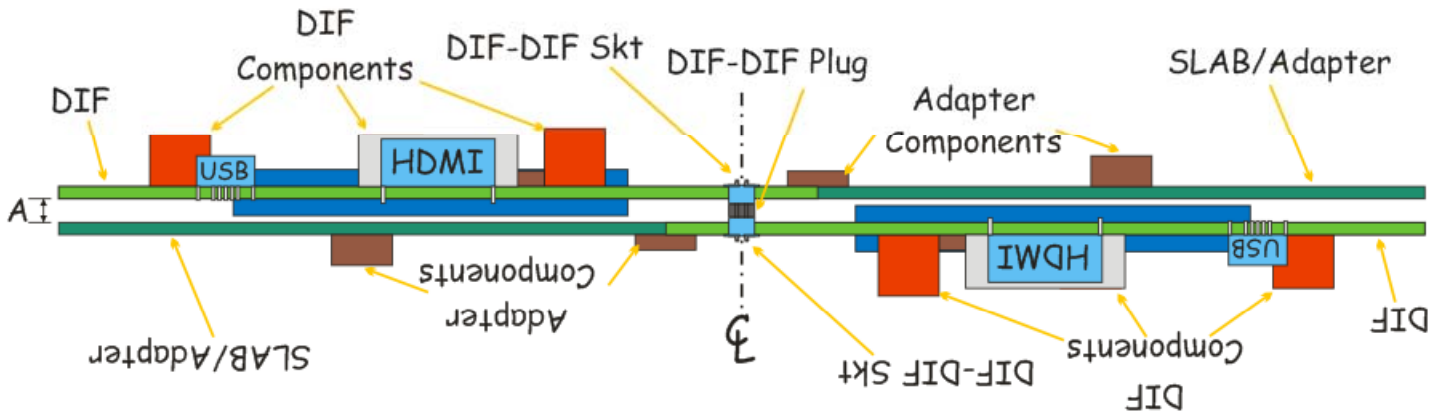

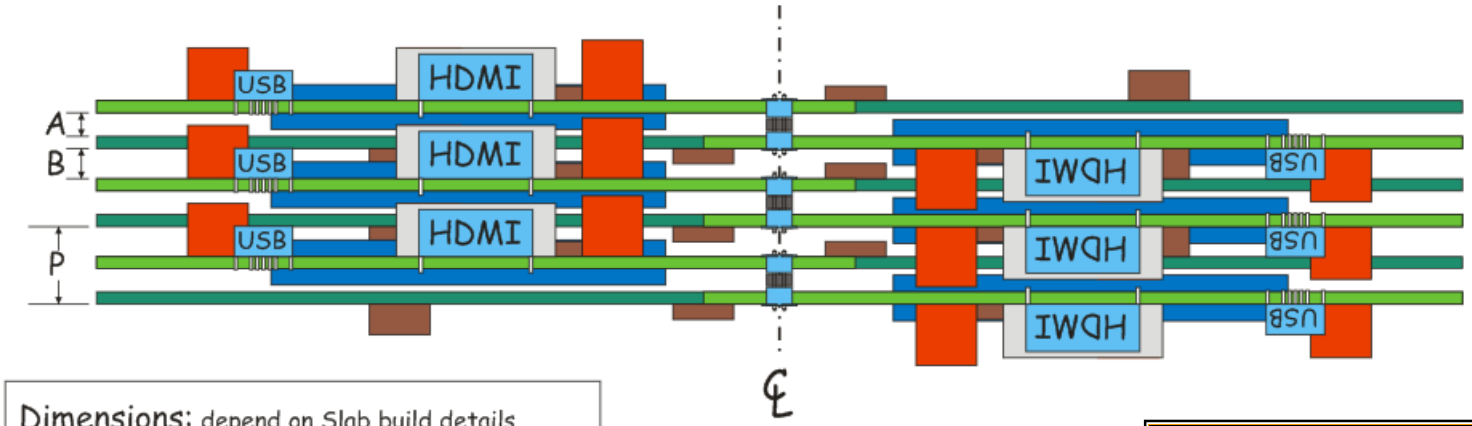

Dimensions: depend on Slab build details
A : (PCB-PCB of 2-sided module) 3.1 to 3.4mm
B : (PCB-PCB of adjacent modules) 3.95 to 3.65mm
P : (pitch of adjacent modules) 10.25mm

3 Double-Sided Slabs
(for 2.1 mm W thickness)

Shows Component Space
(plus Cooling and Power)

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Simulation – 1 Row of "HARDROCs"

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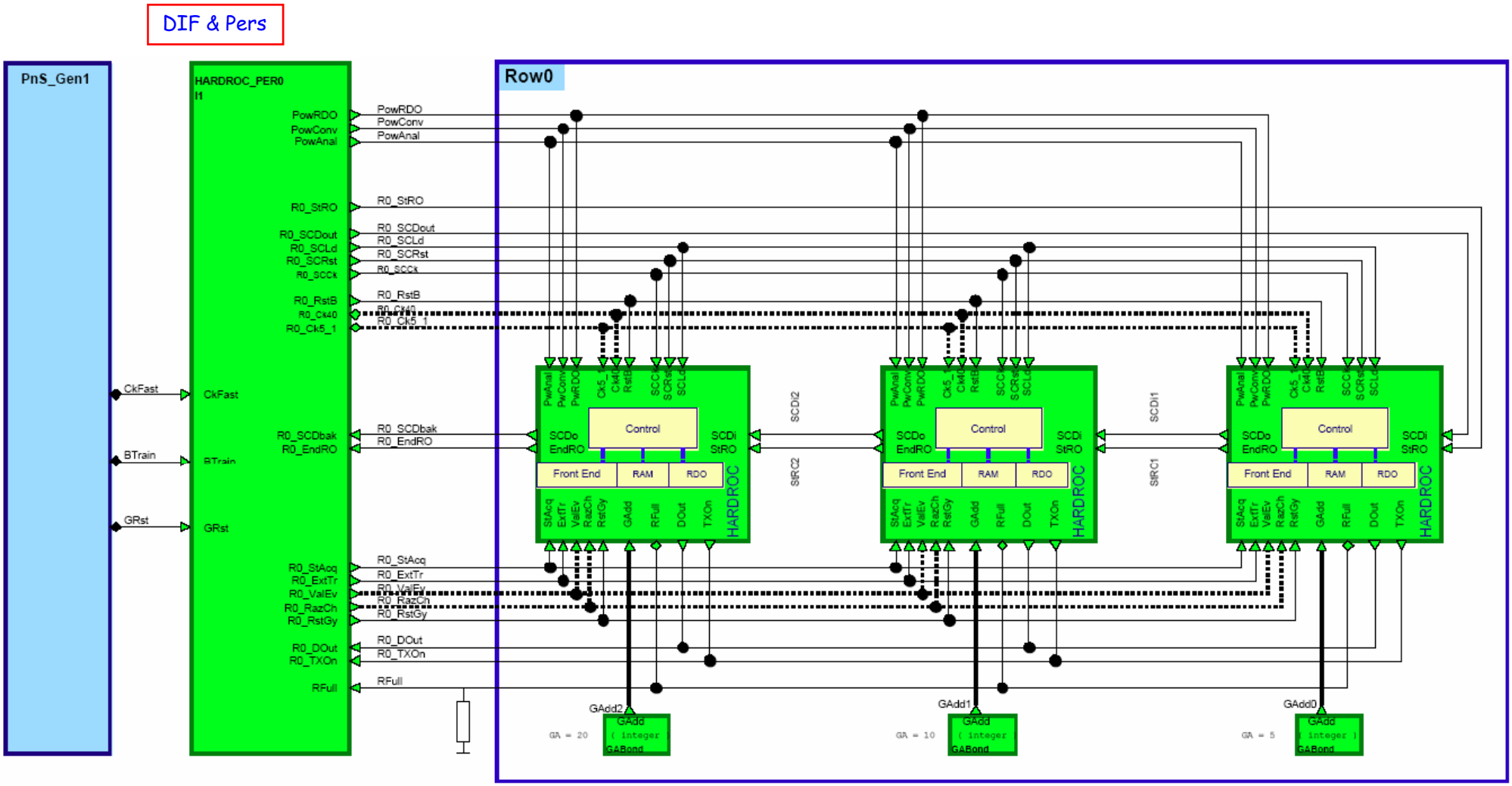

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SLAB Signals

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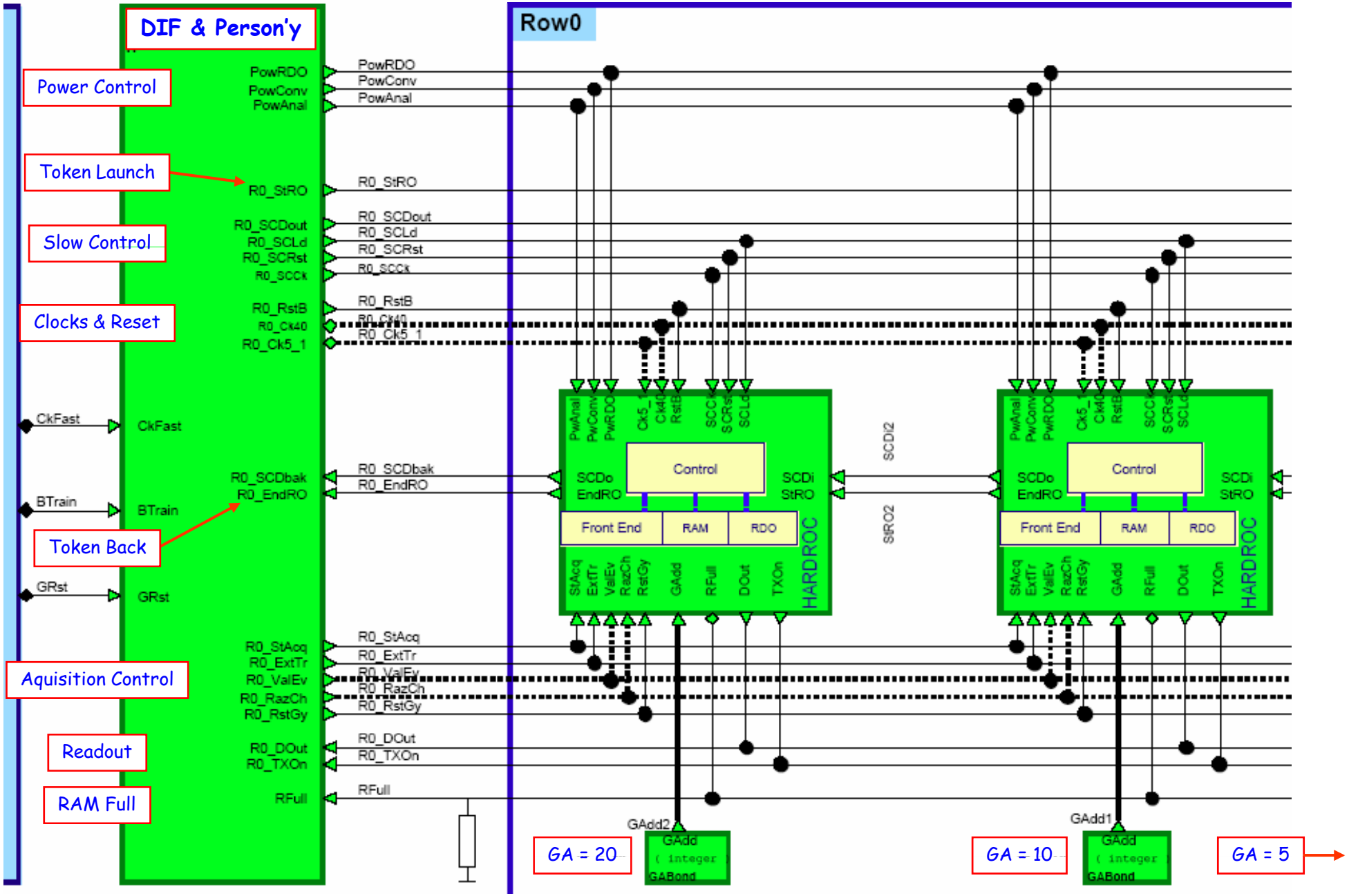

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Simulation - Overall

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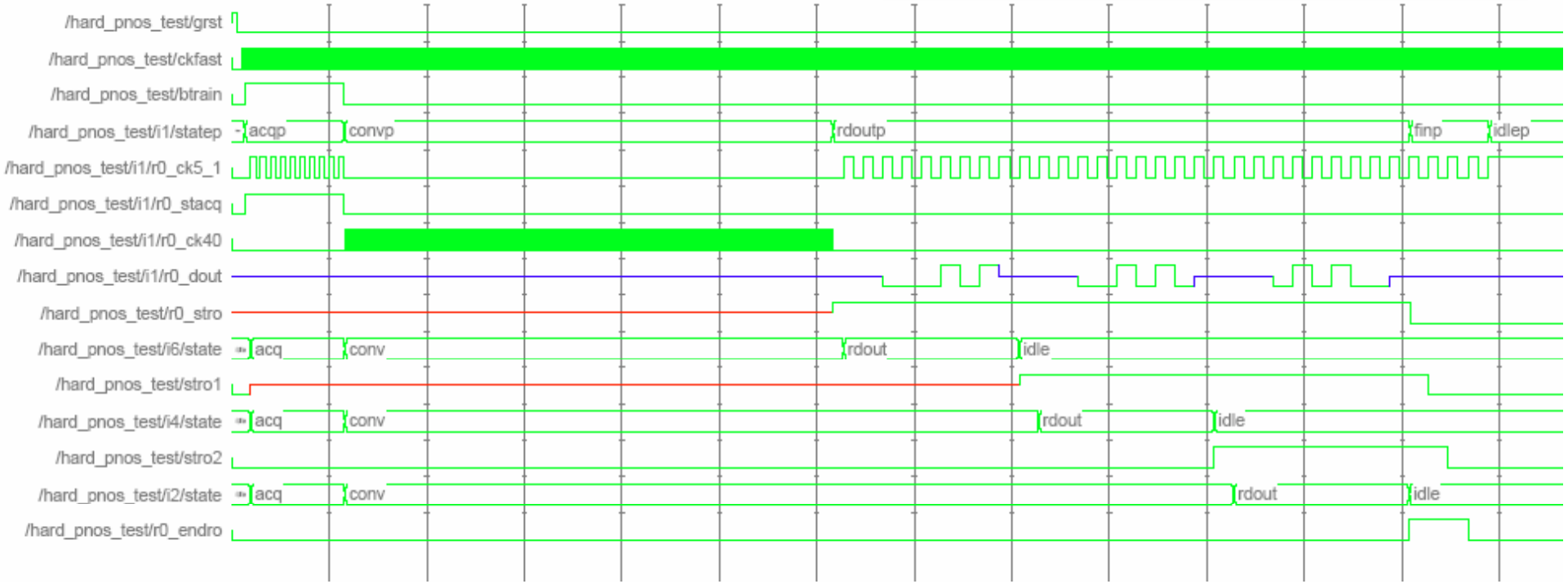
- Simplified and idealised VFE
- Acquisition, Conversion and Readout phases
- (no slow control, trigger,,,,)
- 50MHz, not 40MHz, to match LDA baseline

- Note dual speed of Ck5_1 clock
- TXOn signal not implemented yet



- Will progress to using the HARDROC VHDL
- Will add other signals
- Will add slow controls

Simulation – Acquisition Phase

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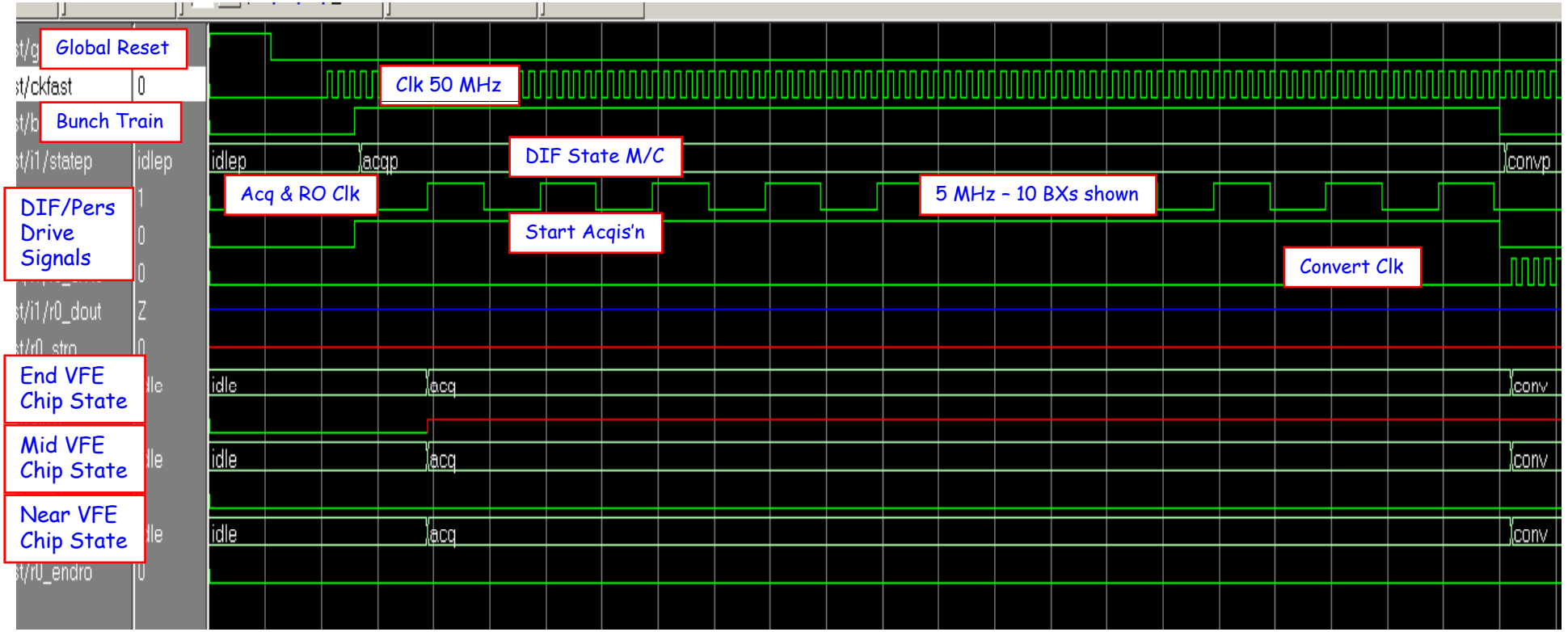
The first Ck5_1 clock edge with Bunch_Train TRUE causes VFEs to go into Acquire mode



The first Ck40 clock edge with Bunch_Train FALSE Causes VFEs to go into Convert mode

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Simulation – Convert Phase

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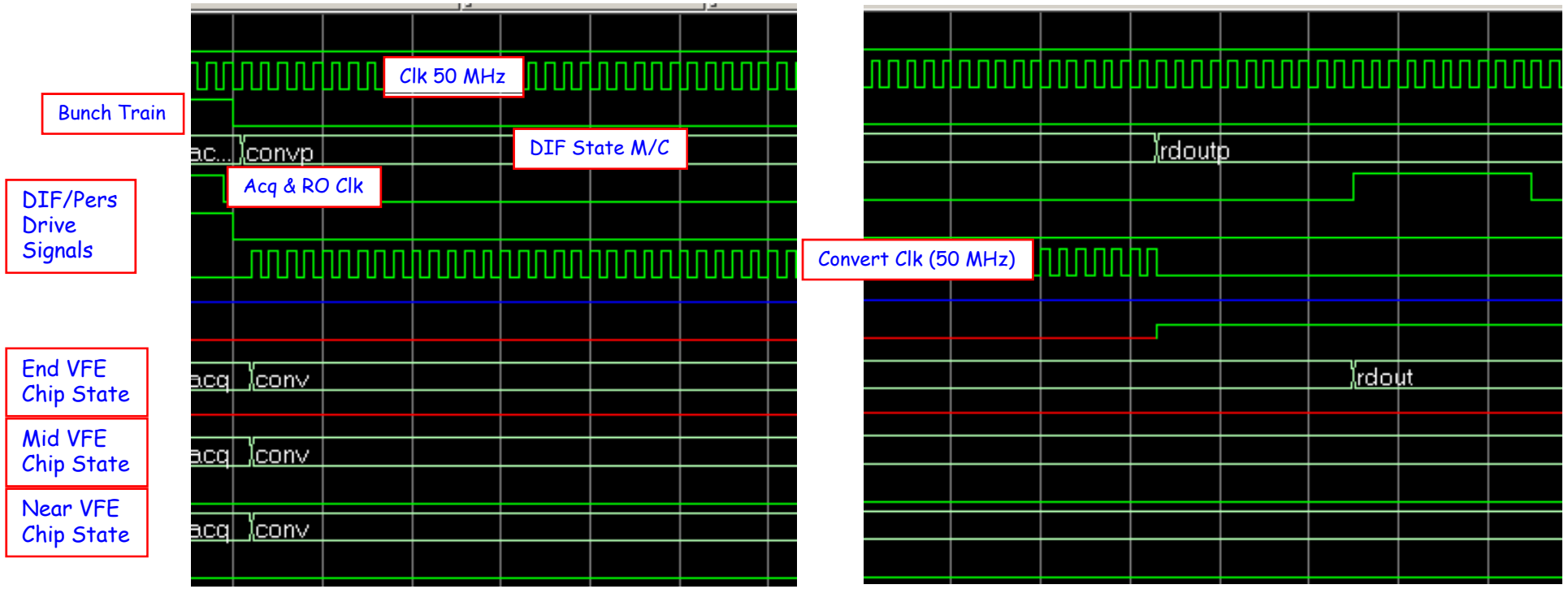
The DIF issues 4096 + n clocks to ensure all VFEs do conversion
The VFEs will in general finish conversion early, and can power-save



Simulation – Readout Phase

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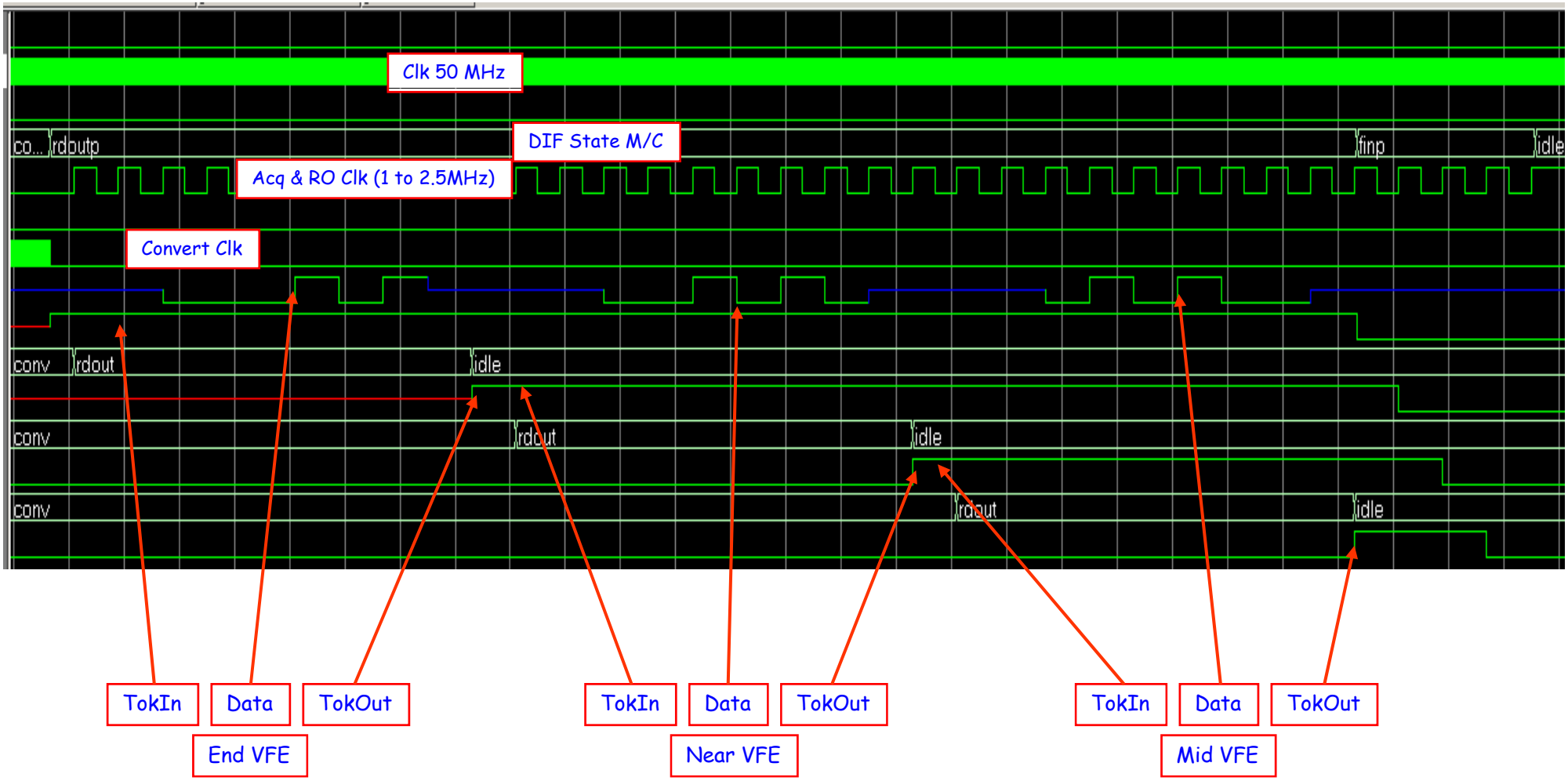
The first Ck5_1 clock edge with Token_In TRUE causes VFEs to go into Readout mode



Line Specs

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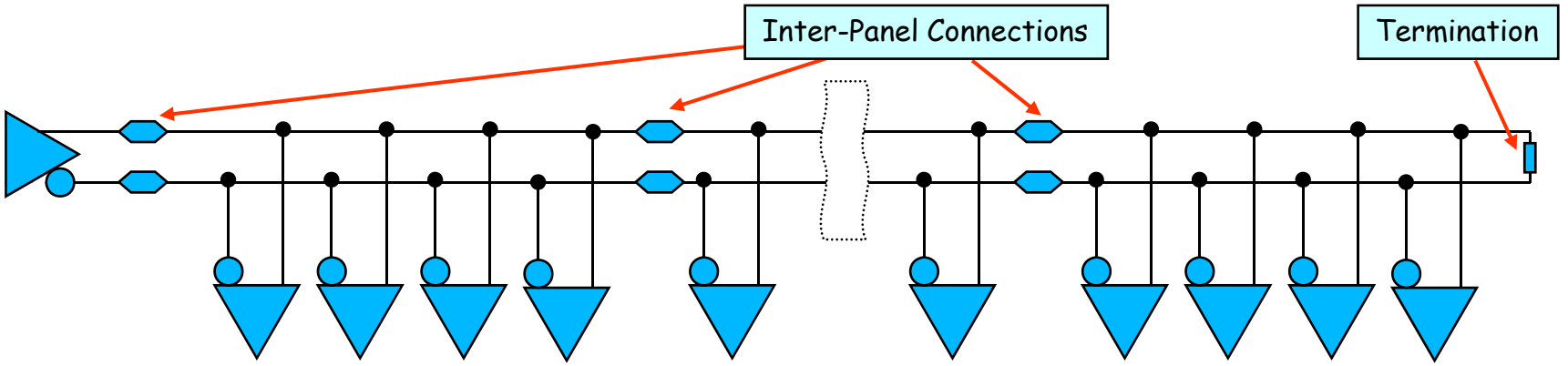
Differential & Multi-Drop Lines



Impedance will be low owing to board build capacitance
- so will probably need higher current driver to maintain signal swing

Line Specs

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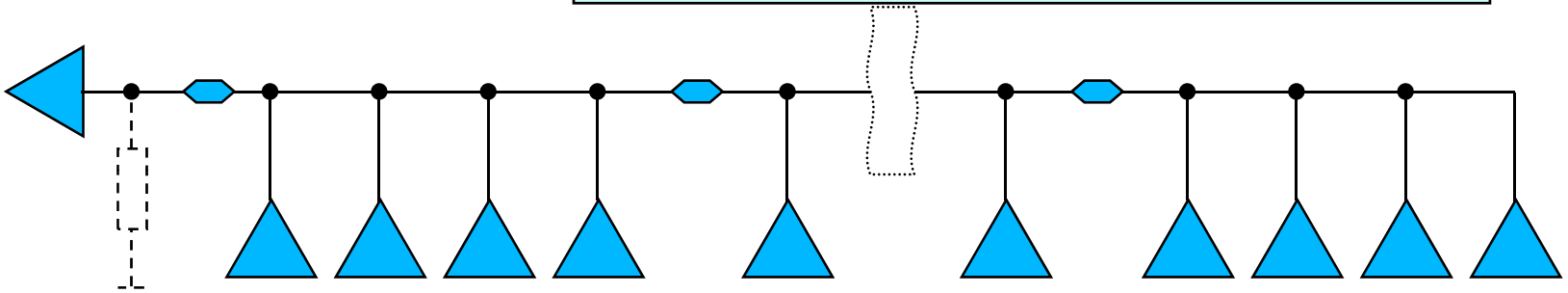
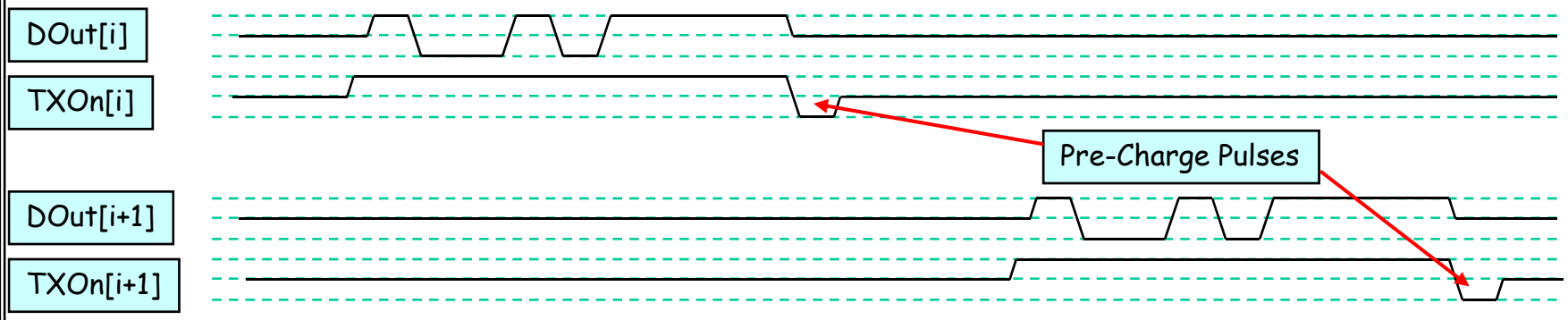
Multi-Source Signals

"Open Collector" solution possible, but is slow / power hungry



Signals where we need to know that no VFE is driving are special:

- Example is the TX_On signal used to validate the VFE Data_Out signals
- Need the Pull-down R, and "Open Collector" drivers (or equivalent)
- "Pre-charge" pulse needed to speed operation
- If the RX has "Bus-Hold", the Pull-down can be omitted or be higher value



Line Specs

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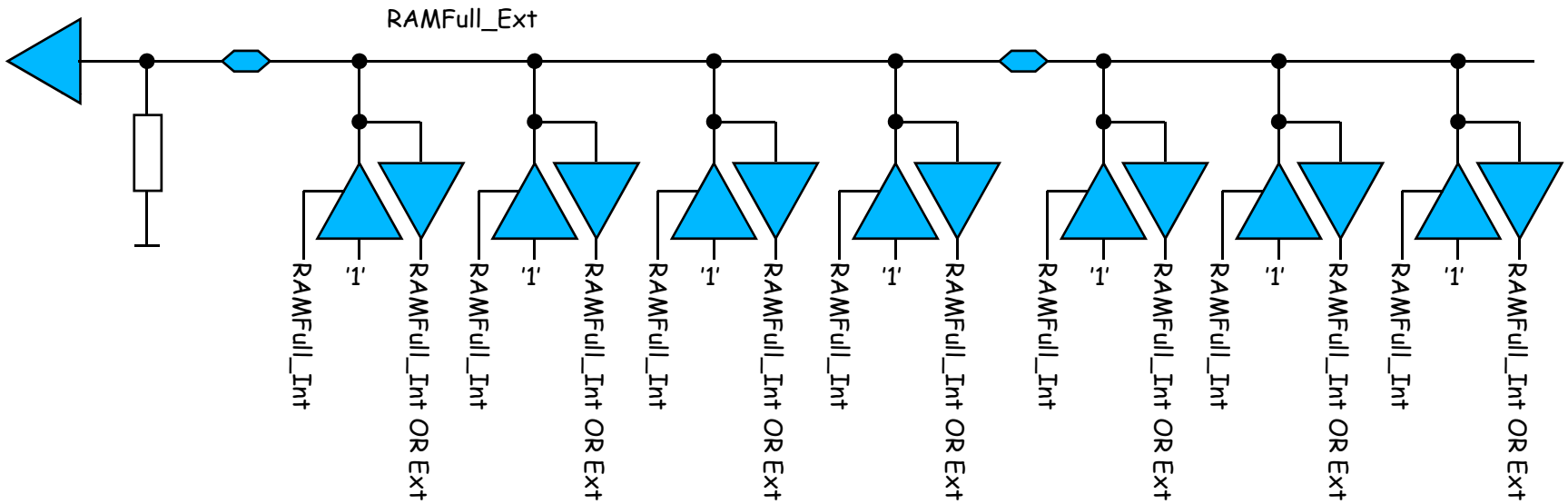
Bi-Directional (RAM_Full)

We can use a single line:
* each chip knows whether it has sourced the signal



Needs to give "Wired OR" of the drive signals

O/Ps Must be:
P-Channel Open Drain [1,Z]
(or Open Collector)
or Tri-state [0,1,Z]

The complementary solution may be better for the chip designers:
- Invert all signals
- Pull UP
- Drive with N-Channel [0,Z]

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Minimising SLAB Signals

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?? Why Minimise ??

- Inter – Panel connection is going to be DIFFICULT
  - Probably limited to a few per cm of panel width (so ~ 100 total inc power)
  - These connections are going to effect yield and reliability
- More signals = More Noise ??
- Redundancy schemes are likely to increase the number of signals by some factor (2, 1.5 ??)

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?? How ??

- In principle very few signals can be used to operate the VFEs
- Moving the functionality of the "Personality" into the VFE does this
- "Flexible Clock" line could be used for further reduction

Minimising SLAB Signals

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?? What Cost ??

- Need to freeze operation into Silicon – loss of flexibility
- Potentially more vulnerable to VFE failure

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?? Worth It ??

- Very large reduction in Signals
- Probably only way to have redundancy routing with acceptable connections

A Few Thoughts on Redundancy

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1. Do we need it? … can we live with, say, 1% dead Slabs ?
2. Detector Wafers and Interconnections fail, not ASICs
3. If the SLAB connections are in rows (6?), is a dead row important?
4. Could redundancy be done at the level of the Panel ?

Other Issues

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- Ext Trigger ?? & other prompt signals
- Clock and Control?? – needs CDR (PLL ?)
- Slow Control :
  - SPI, SPI-like, JTAG, I2C, I2C-like ??
  - Broadcast ?
  - Synchronous ?
- Chip Geographical Addresses : how: bonds, serial chain?
- Chip Temp Monitoring ?
- Chip Serial Numbers ?
- Panel Serial Numbers ?
- Current and Voltage Monitoring ?
- Maximising Reliability :
  - By design
  - By QA and Environmental Testing

Spare Slides Follow

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Heap of Slides from previous talks

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A Multi Function DIF

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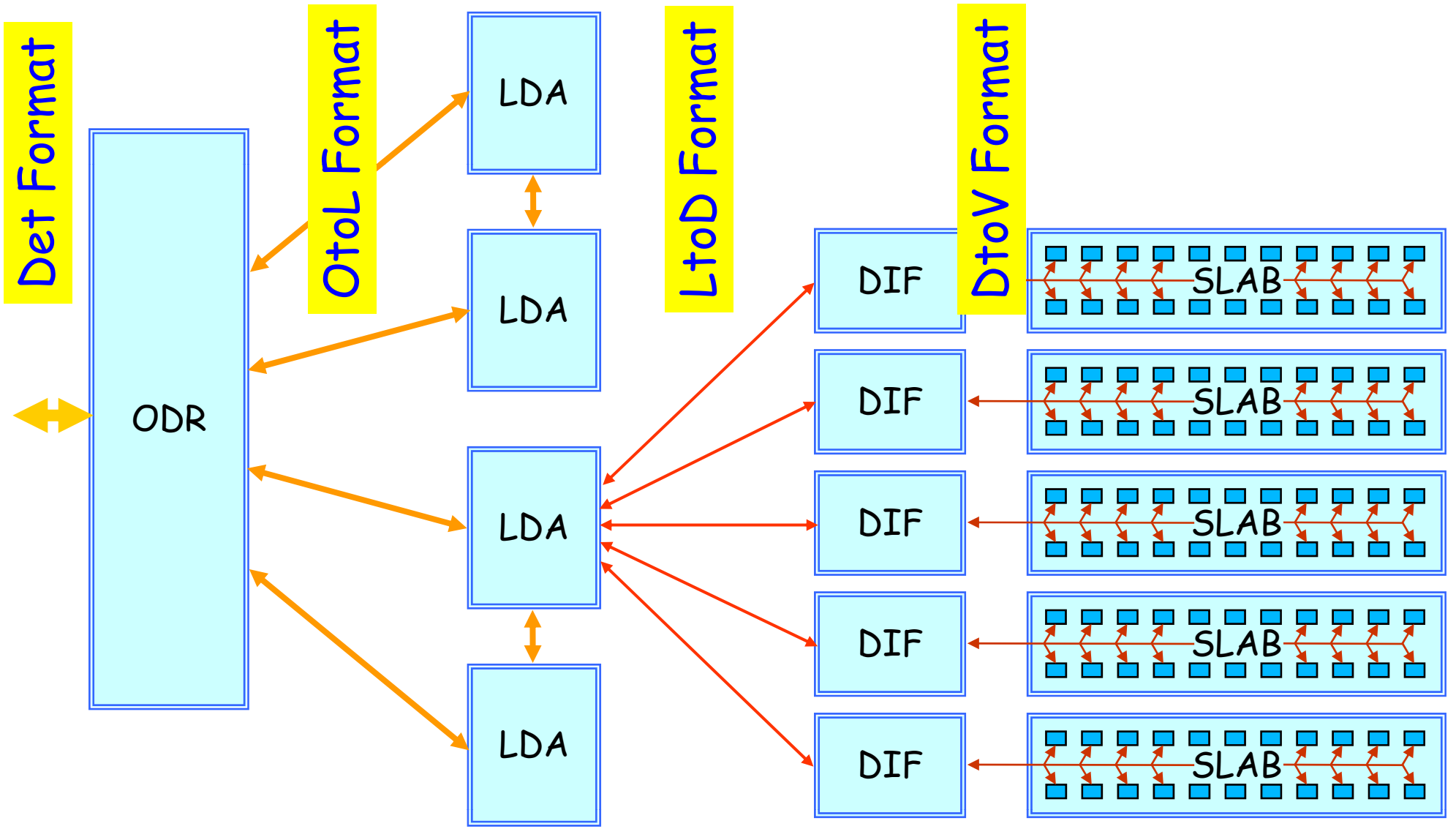
Different Formats at Different Levels



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A Multi Function DIF

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Environments

- Test Slab in the Lab – WP2.2 core work
- EUDET prototype in the lab
- EUDET prototype in Test Beam
- Next ASICs
- ILC environment

Control Requirements

- Clock
- Fast Controls
- Slow Controls
  - VFE – specific
  - Slab - specific
  - Broadcast

Data Path Requirements

- Accumulated Rates
- Adding Source Addresses
- Calibration ???

A Multi Function DIF

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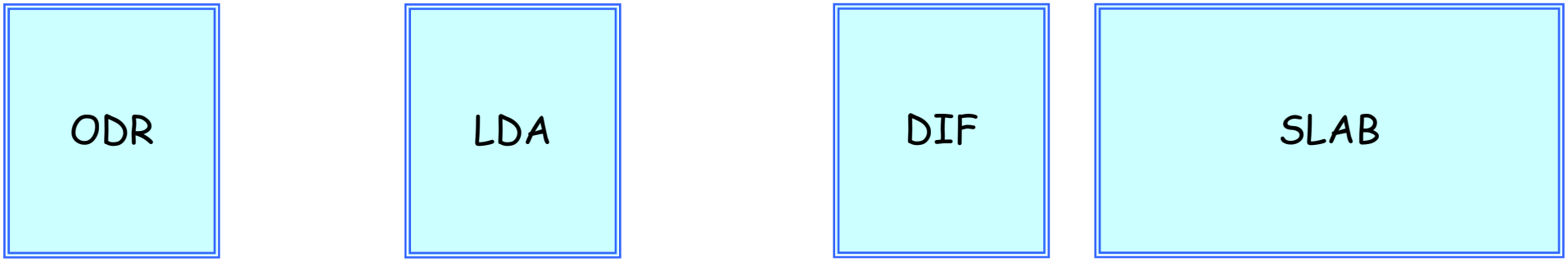
VFE – DIF – LDA – ODR chain: Architecture / Function / Hierarchy

- model as per Manchester workshop of 14-May-2007
- existing set-up mirrors this to some degree
- needed for prototype and EUDET slabs
- needed for final ECAL, HCAL and DAQ

It is very worthwhile adopting this model at this at this stage:

- behavioural description is key:
  - will check the viability of the scheme
  - will allow fine tuning of the model
  - will allow different flavours for different tasks (Test Panel, EUDET Prototype, …



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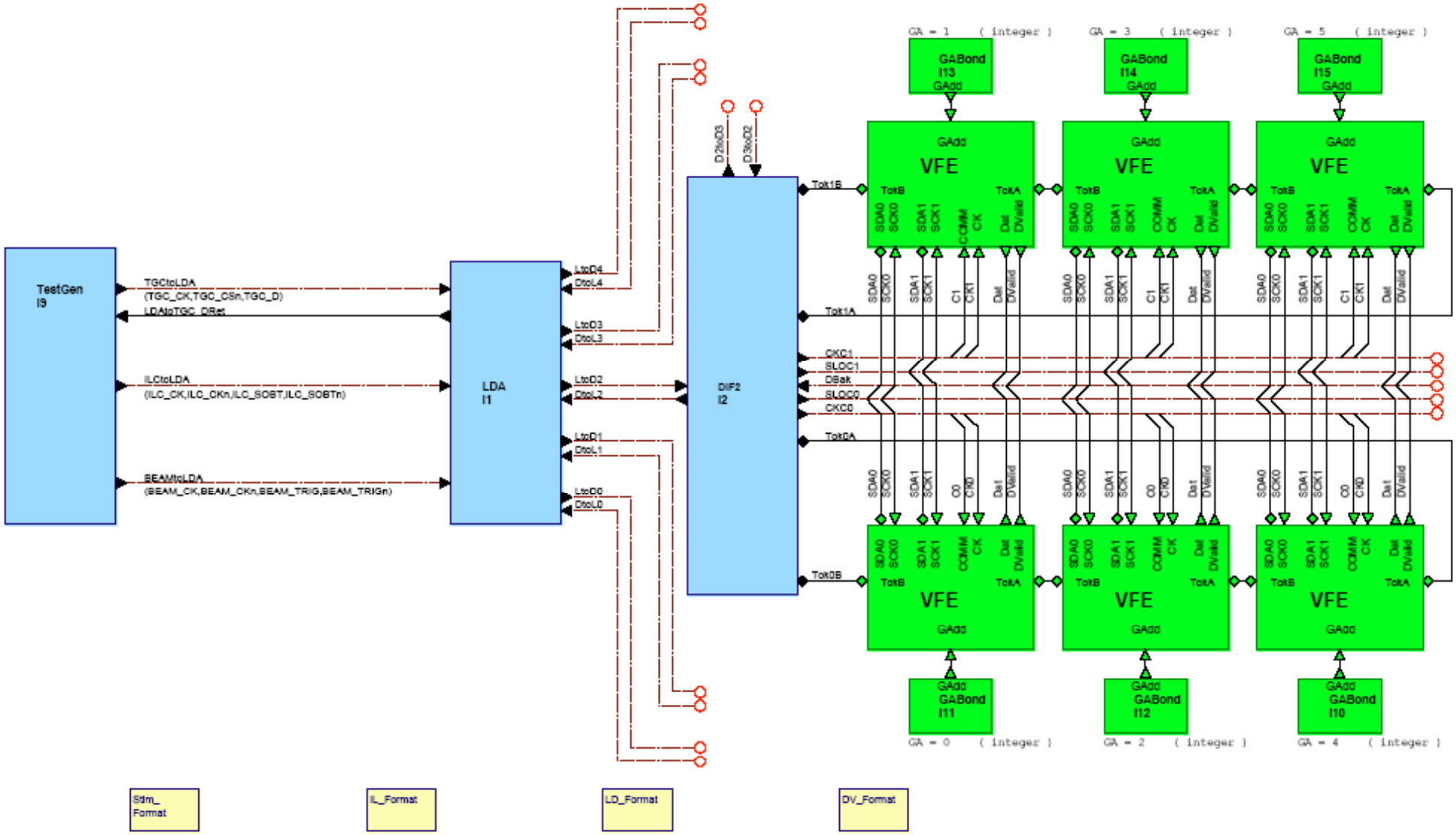

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A Multi Function DIF

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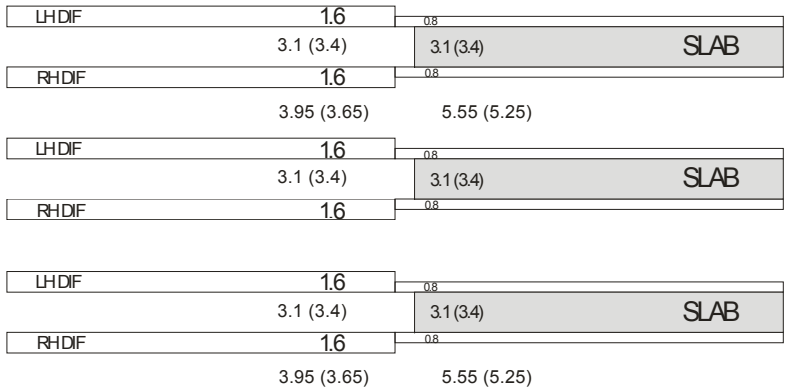
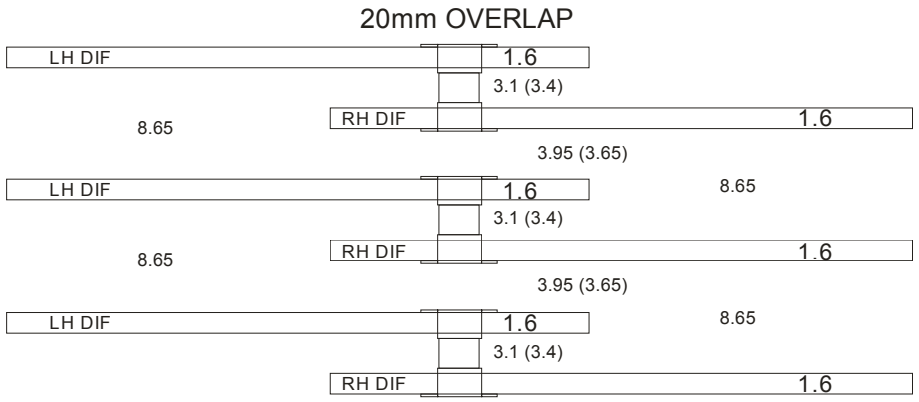
Card Spacing: based on Marc Anduze's ECAL Module design

NOMINAL SPACINGS

(ADAPTER CARDS IGNORED)



Side View



Rear View

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A Multi Function DIF

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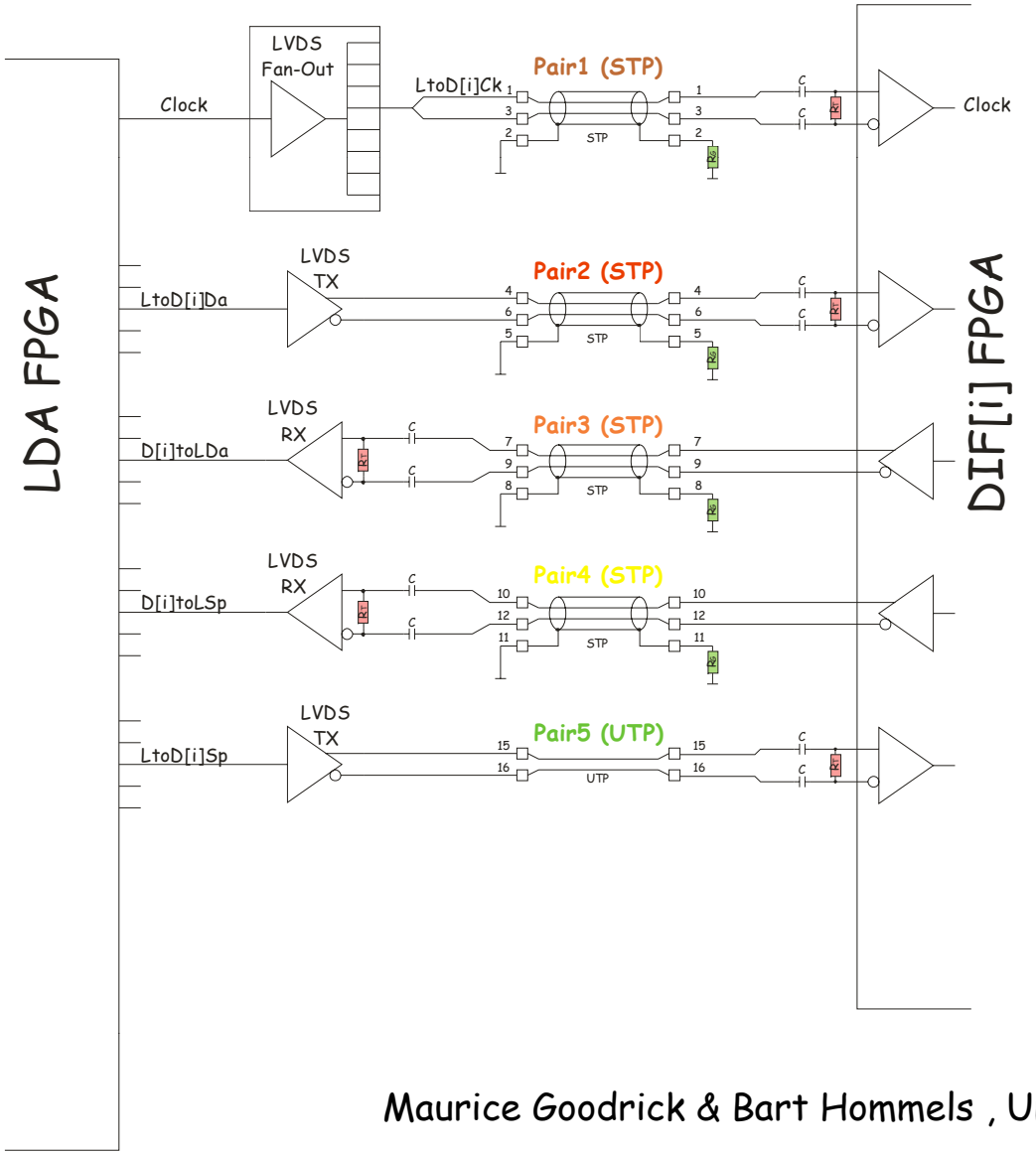
LDA-DIF Cable and Connector



Pair2 (STP)	Gnd	2	1	LtoD[i]Ck+	Pair1 (STP)
	LtoD[i]Da+	4	3	LtoD[i]Ck-	
	LtoD[i]Da-	6	5	Gnd	
	Gnd	8	7	D[i]toLDa+	Pair3 (STP)
Pair4 (STP)	D[i]toLSp+	10	9	D[i]toLDa-	
	D[i]toLSp-	12	11	Gnd	
	Pow2	14	13	Pow1	
	LtoD[i]Sp-	16	15	LtoD[i]Sp+	Pair5 (UTP)
	Pow3	18	17	Gnd	
			19	Pow4	

Possible Pinout for HDMI
(Based on SAMTEC HPDPI cable signal designation)

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