EUDET DAQ and DIF

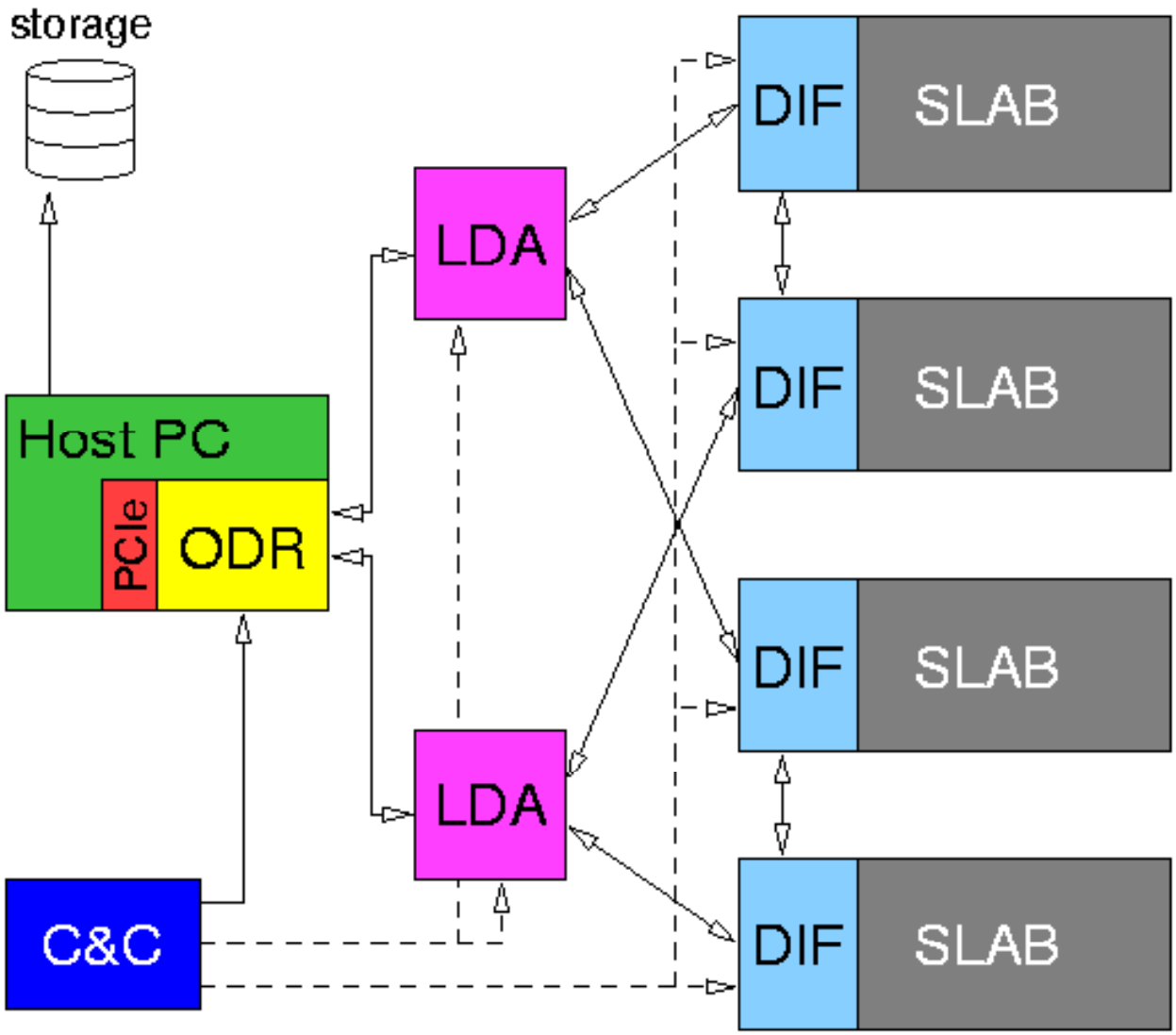
DAQ overview

DIF requirements and functionality

DIF-LDA link

DIF implementation

DAQ architecture



DIF: Detector InterFace

LDA: Link/Data Aggregator

ODR: Off-Detector Receiver

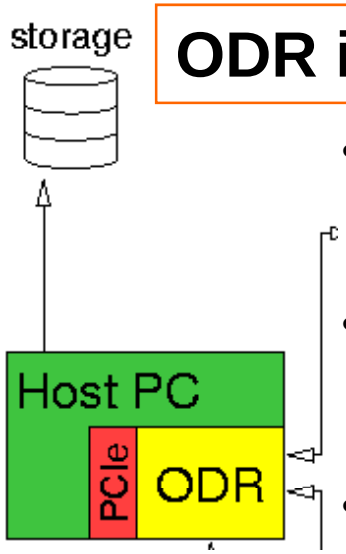
C&C: Clock & Controls

PCIe: PCI-Express

- Slab hosts VFE chips
- DIF connected to Slab
- LDA servicing DIFs
- LDAs read out by ODR
- PC hosts ODR, through PCIe
- C&C routes clock, controls

ODR and LDA

ODR is the interface between DAQ and the ‘PC-world’

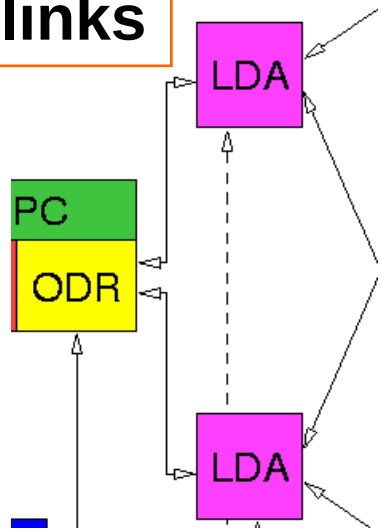


- ODR is a commercial FPGA board with high speed serial interfaces and a PCIe host bus
  (Virtex4-FX100, PCIe 8x, etc.)
- Customised firm- and software:
  DMA driver pulls data off the onboard RAM, writes to disk
- Performance studies & optimisation ongoing

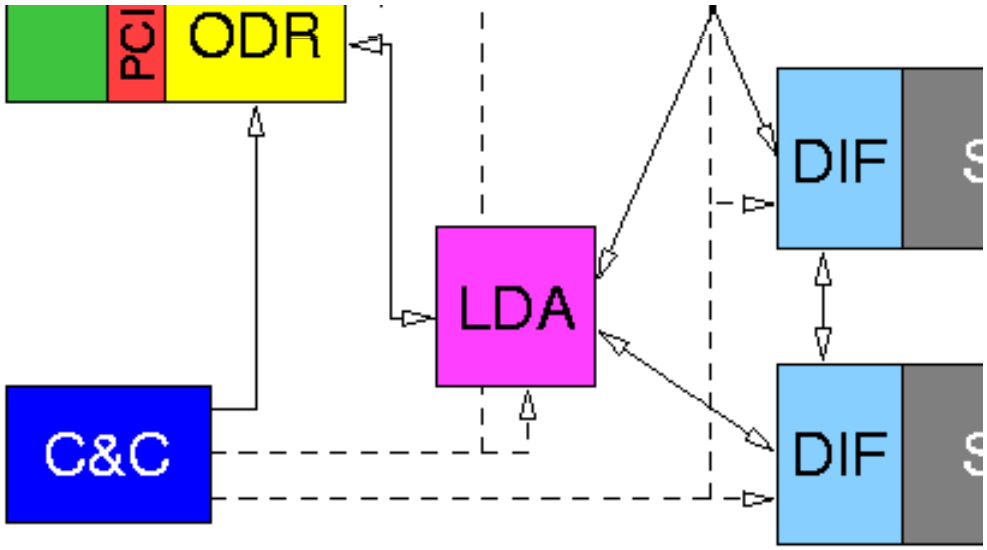
LDA interfaces many DIFs with few high-speed links

1st Prototype is (also) a commercial FPGA board with customised firmware and hardware add-ons:

- High-bandwidth link to ODR
- Many links towards DIFs



Clock & Controls Distribution



- C&C unit provides machine clock and fast signals to ODR, LDA (and DIF?)
- Clock jitter requirement seems not outrageous
  (at the moment)

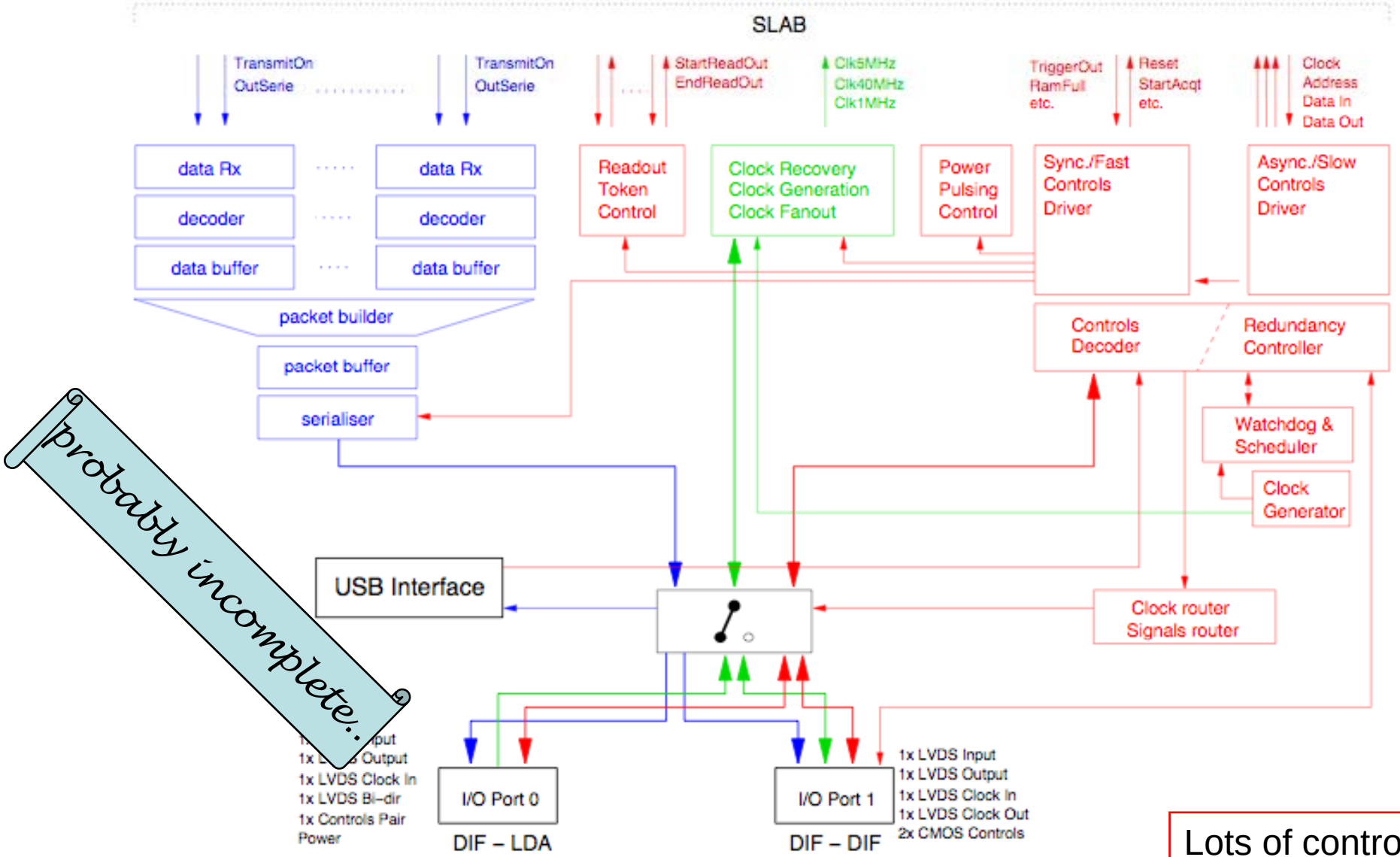
- Fast Controls: encoded commands on the LDA-DIF link
- Slow Controls/Configuration: transfers on LDA-DIF link
- Low-latency fast signals: distributed ‘directly’

Now…. let's have a closer look at the DIF

DIF Functionality

- Receive, regenerate and distribute **clocks**
- Receive, buffer, package and send **data** from VFE to LDA
- Receive and decode incoming **commands** and assert corresponding signals
- Receive, decode and store **block transfers**
- Control **power pulsing** and provide watchdog functionality
- Control the DIF-DIF **redundancy** connection
- Provide an **USB interface** for stand-alone running and debugging
- …..on top of that: all the things we did not think so far

Draft DIF block diagram



Lots of controls….

LDA-DIF link requirements

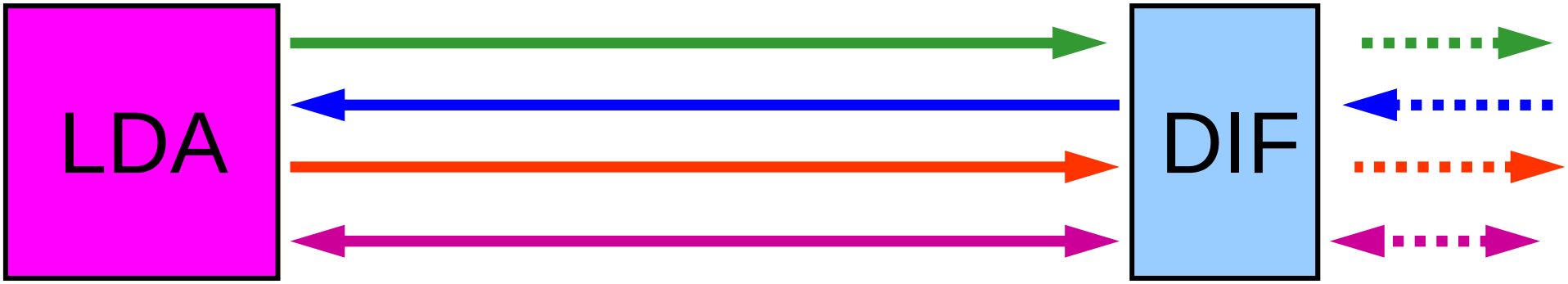
Clock: provide machine clk + synchronisation

- Byte-wide transfers in robust encoding

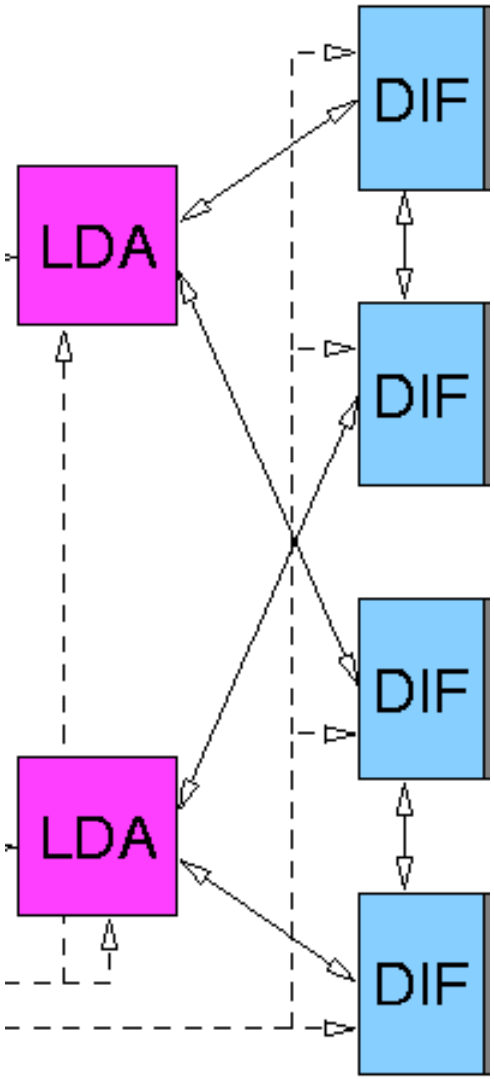
Data: large block transfers from DIF to LDA

Fast control commands: immediate action

‘Slow’ control command =
block transfer + fast control command



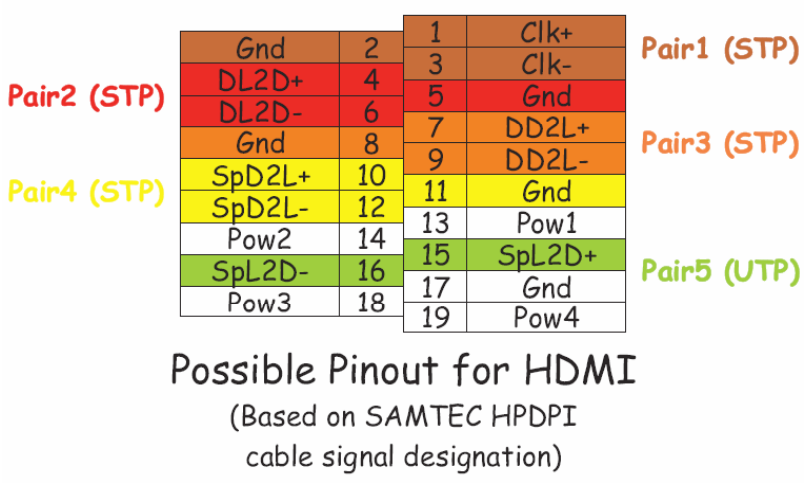
LDA-DIF link



LDA-DIF link:

- Serial link running at multiple of machine clock
- 50Mbps (raw) bandwidth minimum
- robust encoding (8B/10B or alike)
- anticipating 8…16 DIFs on an LDA, bandwidth permitting
- LDAs serve even/odd DIFs for redundancy

LDA-DIF physical interface



clock

data

control

spare data

spare control

LDA-DIF link physical form factor:

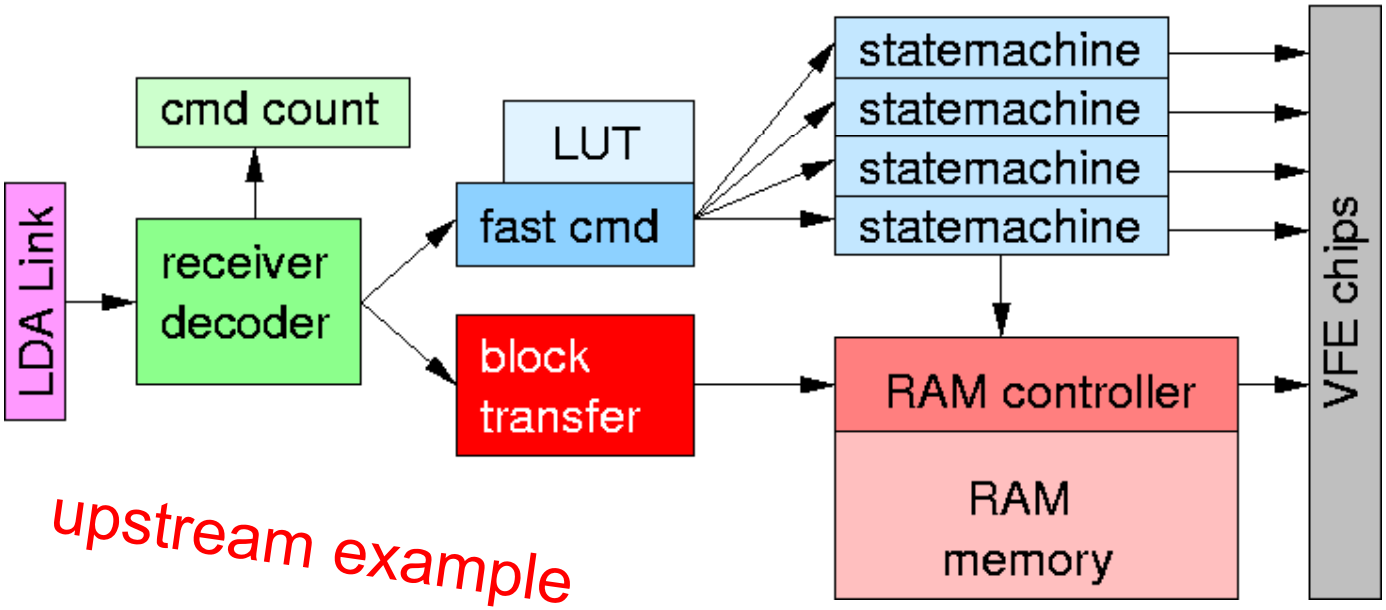
- Differential signals on shielded twisted pairs
- Few single-ended control lines
- HDMI connectors and cabling: commercially available in high quality

LDA-DIF link protocol ideas

- Fast commands: 8bit
- Configuration and Event data transfers:

  `[cmd][packet length][start address][byte 0]..[byte N]`

  Example: VFE configuration consists of a block transfer of configuration data + a fast command to load the config. data into the VFEs

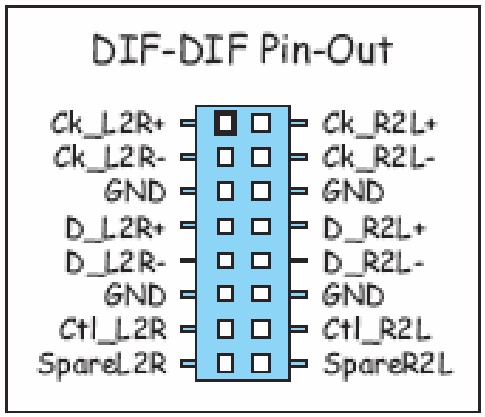


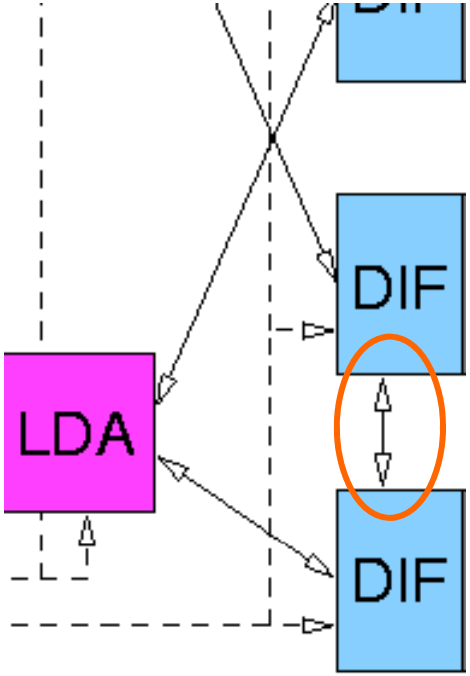
upstream example

robustness issues:

- acknowledge cmd rx: send cmd count
- upon cmd completion: send back cmd done
- keep track of cmd count
- link idle: send status bits

DIF-DIF link





- Redundancy against loss of LDA link
- Provides differential signals:
  - Clock in both directions
  - Data and Control connections
  - Two spares: one each direction
- Plus two single-ended control lines
- Single LDA-DIF link bandwidth sufficiently large for data of two DIFs

DIF implementation

- The Slab is an integral part of the detector
- The LDA and ODR are transparent wrt detector type

- The DIF and its interface to the slab is detector-specific
- Large parts of the DIF firmware can/*should*/***must*** be generalised
- *DIF hardware should support firmware* to profit from common developments
- DIF working group: AHCAL, ECAL, DHCAL + DAQ
- DIF wg to address common problems and share knowledge, experience, and VHDL code