Generic Silicon Detector R&D

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EUDET Annual Meeting 8. October 2007

SiIC Silicon Sensor Baseline

- **SiIC sensor baseline**
  - FZ p-on-n sensors: n-bulk material, p+ implants for strips
  - high resistivity (5-10 kOhm cm)
  - Readout strip pitch of 50µm
    - Possibly intermediate strips in between (resulting 25µm pitch)
    - Smaller pitch becomes very complicated (Pitch adapter, bonding, charge sharing,…)
  - Thickness around 100-300µm
    - mostly limited by readout chip capabilities (S/N ratio)
  - **Low current:** <1nA per strip

  (Due to long integration time: noise mostly defined by current and resistors)

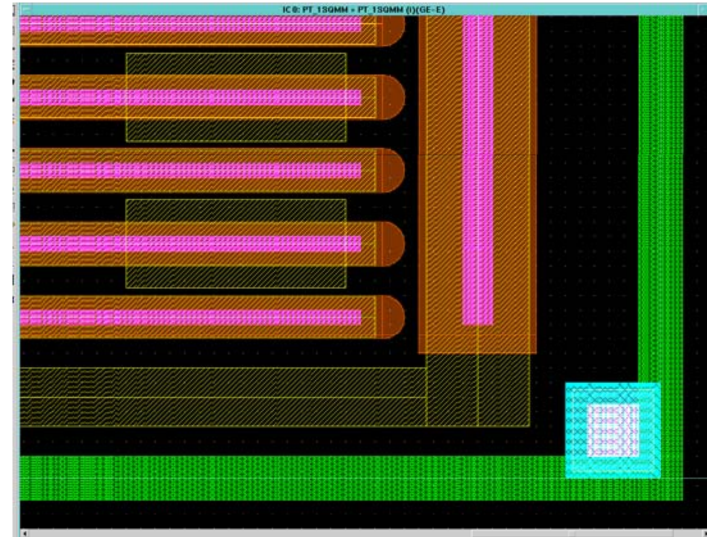
- **Baseline for inner layers:**
  - 6” inch, Double sided, AC coupled

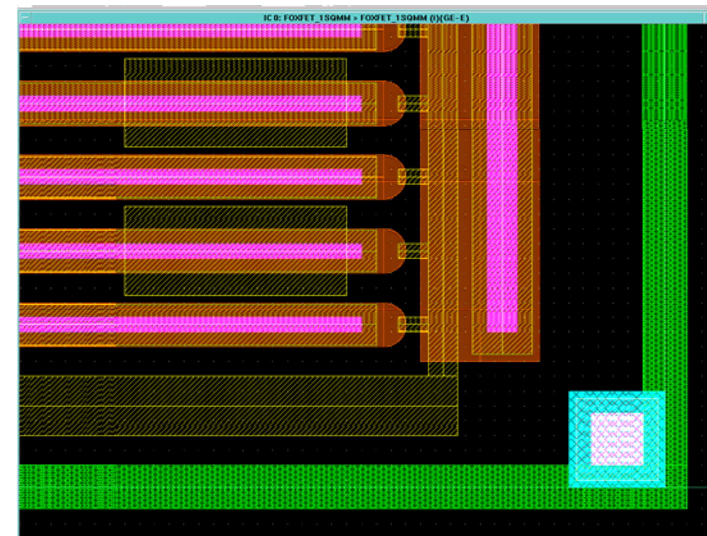
- **Baseline for outer layers:**
  - 8” (12”?) inch, Single sided, Preferably DC coupled (cheaper)

Sensor Baseline Details

Biasing Possibilities:

- bias resistor with **poly-silicon** (20 to 50 MOhm; not shown)
- **punch-through** (upper picture)
- **FOXFET** biasing structure (lower picture)





Advantages/disadvantages:

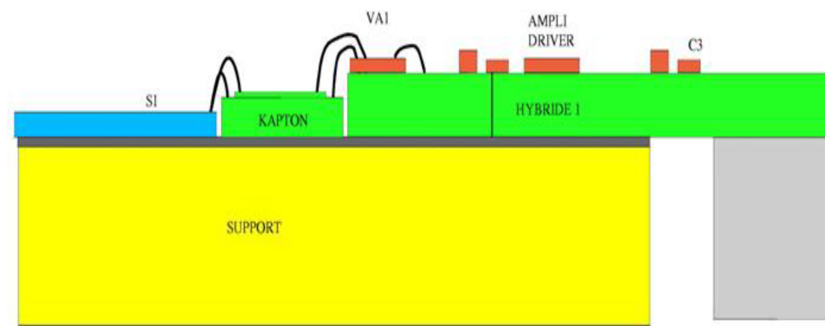
- Poly-Si radiation hard; PT and FOXFET not
- PT and FOXFET cheaper

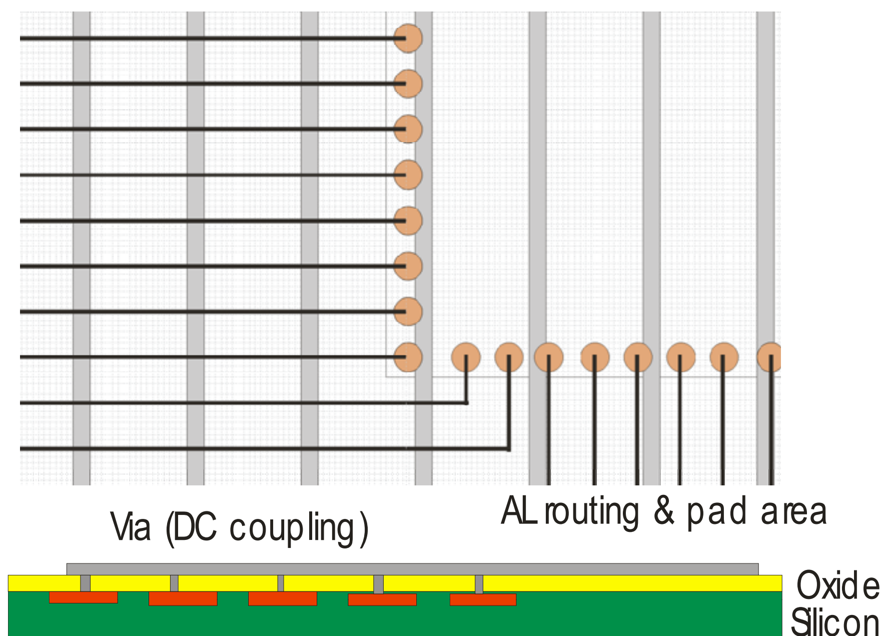
Minimize material budget

- Multiple scattering is crucial point for high-precision LC experiment

- Minimize multiple scattering by reduction of material budget
  - avoid old-fashioned way (pitch adapter, FE hybrid, readout chip)

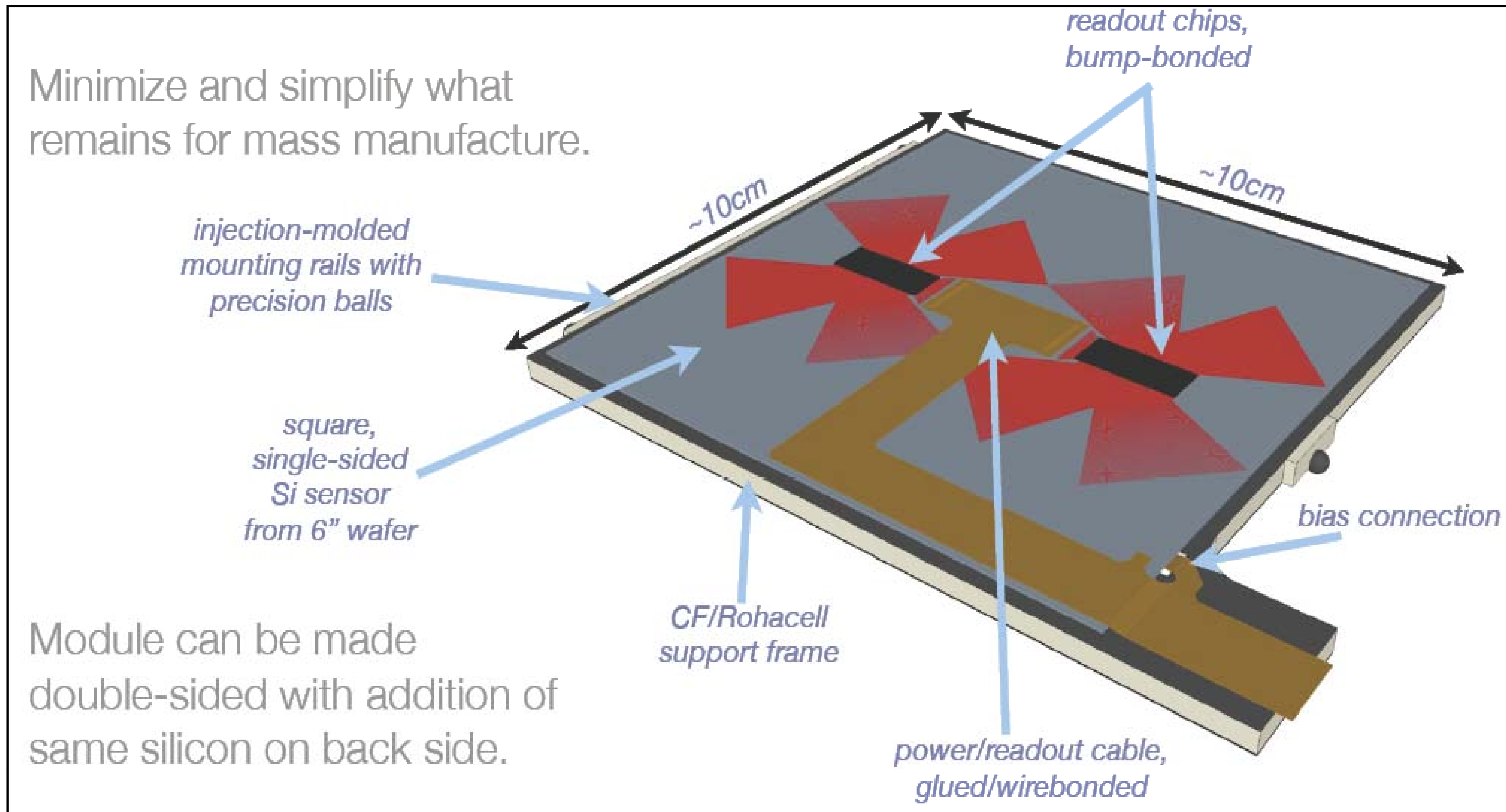
- **Integrate pitch adapter into sensor**
  - Connectivity of strips to readout chip made by an additional oxide layer plus metal layer for signal routing
  - Readout chip bump-bonded to sensor like for pixels



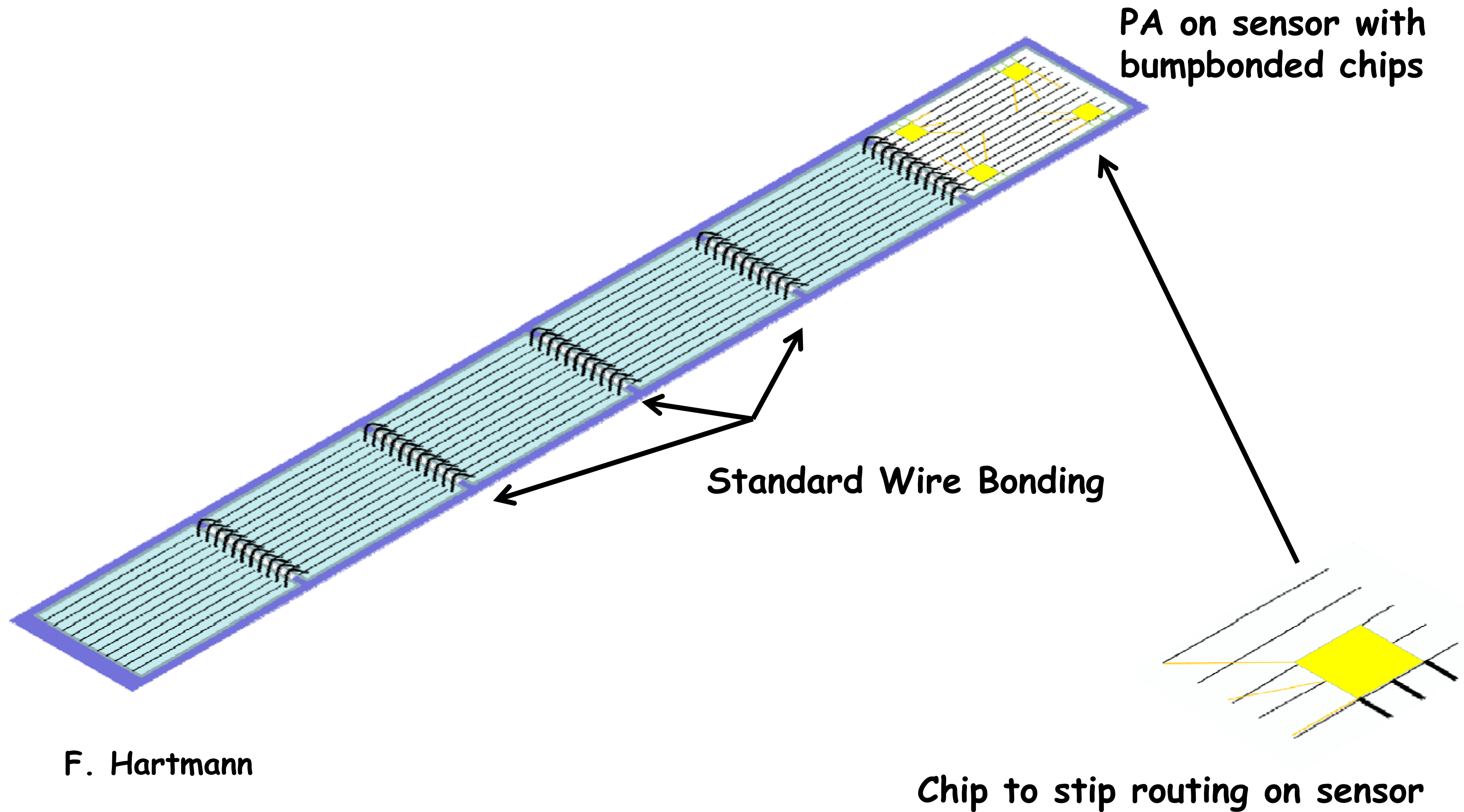


Similar to SiD Concept:

Slide taken from Timothy Nelson‘s Presentation of SiD detector concept at Bejing ILC GDE Meeting (Feb 6, 2007) **…..very elegant!**



Long ladder with 2 sensor types



F. Hartmann

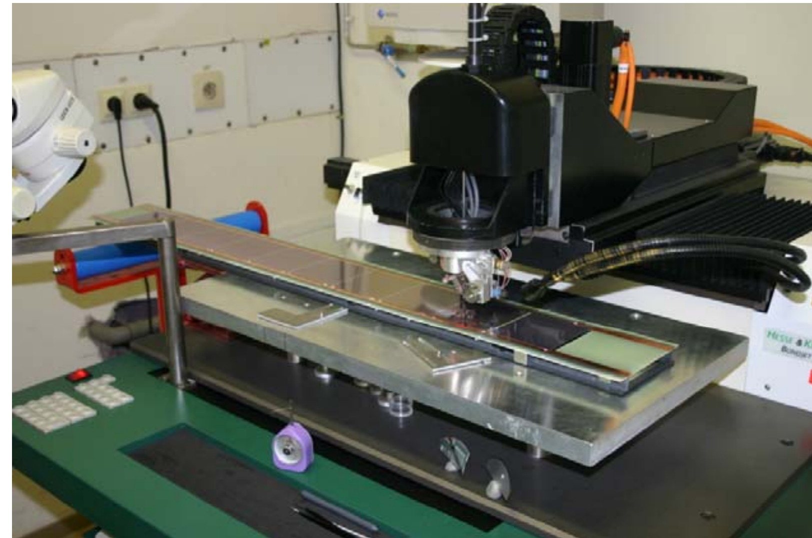
SiLC
Silicon for the Linear Collider

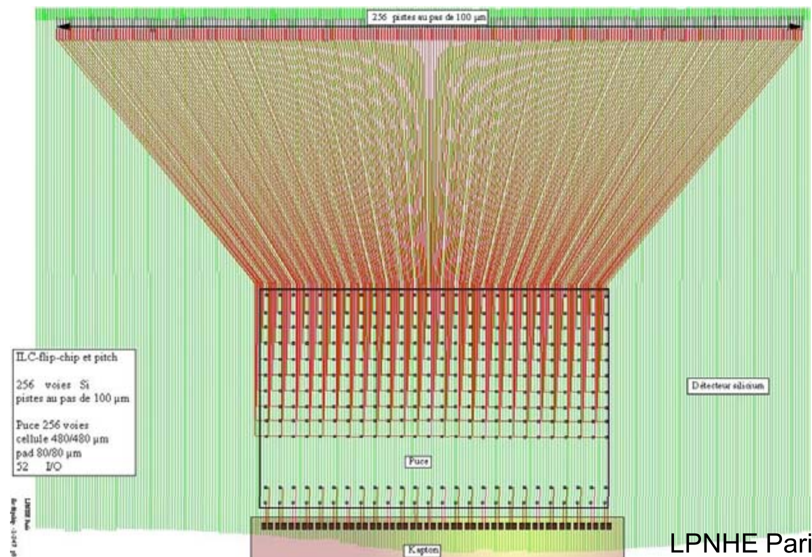
"Inline pitch adapter" for SiLC UMC Chip

- SiLC 130nm chip successfully tested with long ladder out of 10 HPK GLAST sensors
  - ***Wire bonding***

- Next SiLC chip version
  - 128 channels
  - ***Bump-bonding***

IEKP Karsruhe





LPNHE Paris

SiIC work program for sensor R&D

- Step 1 (2007-2008)
  - Use long strips (50 µm pitch)
  - Wafer thinning (100, 200, 300µm)
  - Test new readout chips (DC coupling, power cycling)
  - Improve standardized test structures and test setups
- Step 2a (2009-)
  - Move from pitch adapter to in-sensor-routing
  - Test crosstalk, capacitive load of those sensors
- Step 2b (2009-)
  - Test 6” double sided sensors
- Step 2c (2009-)
  - 8” (12”) single sided DC wafer

Step 1 and 2a:

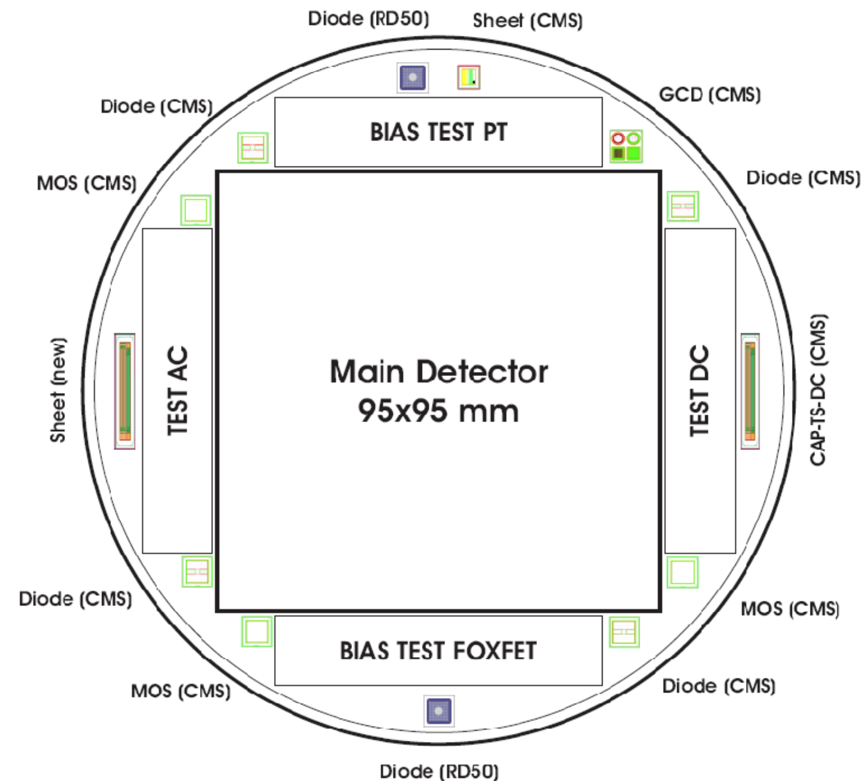
- Bump-bondable 128-channel chip available 2008
- HPK agreed to provide a sensor design
- SiLC adapts strip to pad area
- HPK will process the sensor
- SiLC (LPNHE Paris) provides chip
- HPK bump bonds chip to sensor
  - HPK is very interested to strengthen inhouse bumpbonding
    - In Bump
    - Flipchip
  - Stud-bonding
- Testing begins 2008

Status of the sensor producers

HPK Sensor Order

- Single-sided AC coupled SSD
- **Sensor size:** 91,5 x 91,5 mm² (± 0,04 mm)
- **Wafer thickness**: approx. 320 µm
- **Resistivity**: such that depletion voltage: 50 V < Vdepl < 100 Volt
- **Leakage current**: < 10 µA per sensor
- **Biasing scheme**: poly-Silicon Resistor with 20 MΩ (± 5 MΩ)
- **Number of strips:** 1792 (= 14 x 128)
- **Strip pitch:** 50 um pitch, without intermediate strips
- **Strip width:** 12.5 um
- **Dielectric Structure:** Oxide (SiO_2) + Nitride (Si_3N_4) between p+ and aluminium strips.
- 2 **bond pads** on each side of the strip
- 1 **probe pad** on each side of the strip (contact to p+)

- **We ordered 35 HPK Sensors**
  - 30 “normal sensors”
  - 5 “alignment sensors”
- **Have been delivered last week**



SiLC Silicon for the Linear Collider

HPK Sensor Order

- Main detector will be used to
  - Build prototype modules to test new readout chip (Testbeam takes place this week at SPS@CERN)
  - Build modules for LC-TPC project
  - Build long ladder
- Test structures
  - TESTAC and TESTDC
    - 256 strips with pitch=50um
    - Multi-geometry test structures with different strip widths and different intermediate strips
    - Will be used to test coupling, C_int, resolution (eventually in a testbeam)
  - BIASTEST FOXFET and punch-through
    - 128 channels with pitch=50um
    - with different biasing schemes

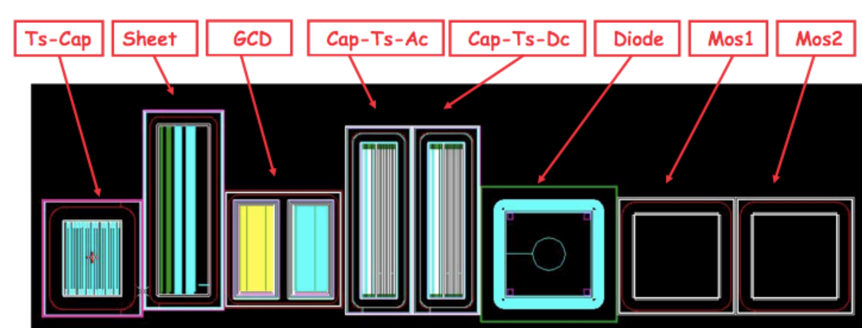
TESTAC:

strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

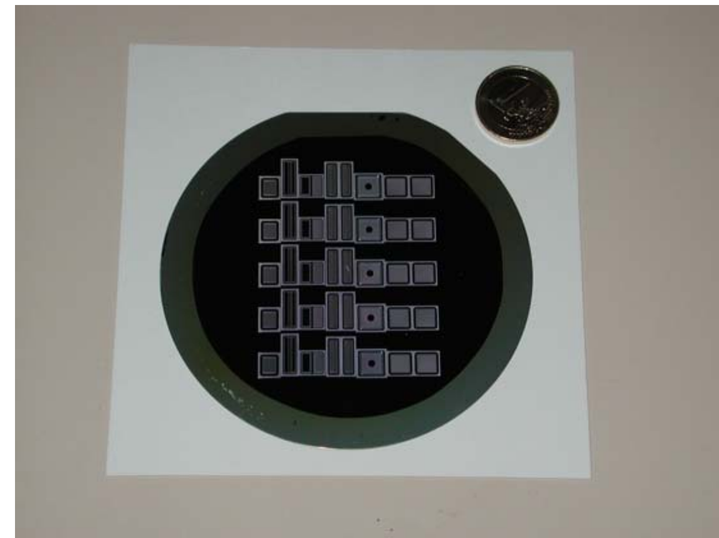
SiLC Silicon for the Linear Collider

IET Warsaw

- Contact established with *Institute for Electron Technology* already three years ago
- They have experience with SOI and chip production, but not with fully depleted devices yet.
- Goal: develop test structures based on CMS 'half-moon', but improved

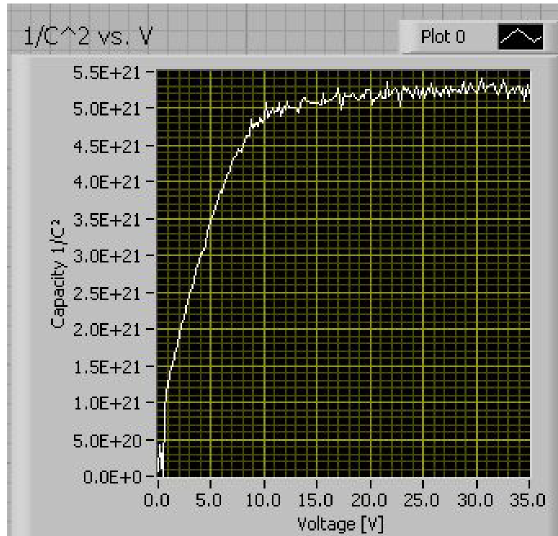


- **Three 4" wafers received from first processing batch**
- **Results look promising**

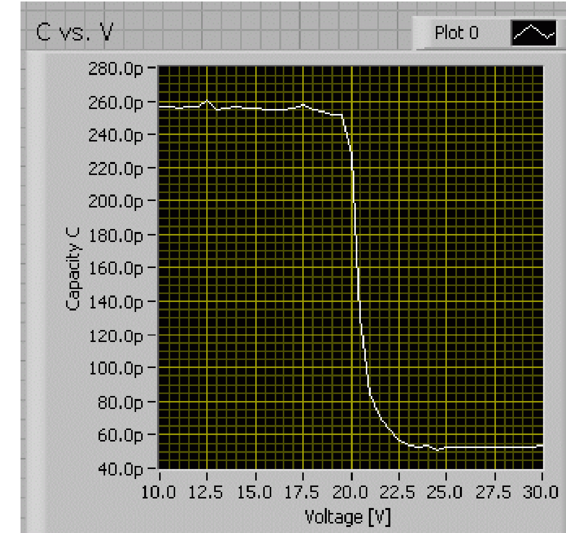


IET Warsaw Results

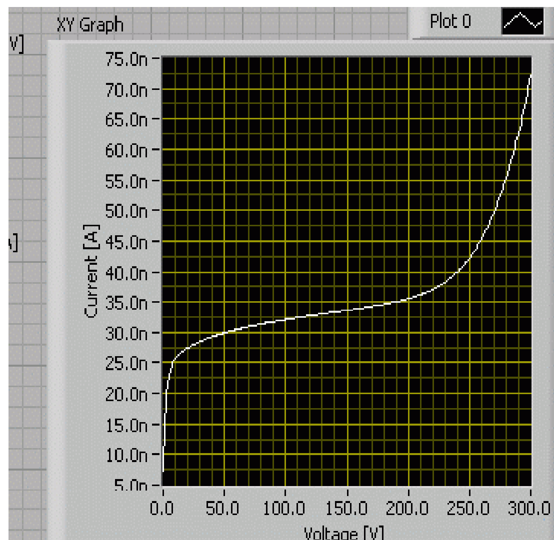
CV Diode:



CV MOS:



IV:



- CV Diode: $V_{depletion}$=8 V
- CV MOS: $V_{flatband}$=21V
- IV: I_{dark}@200V=35nA

Next step:

- Design and production of test structures for dual metal layer

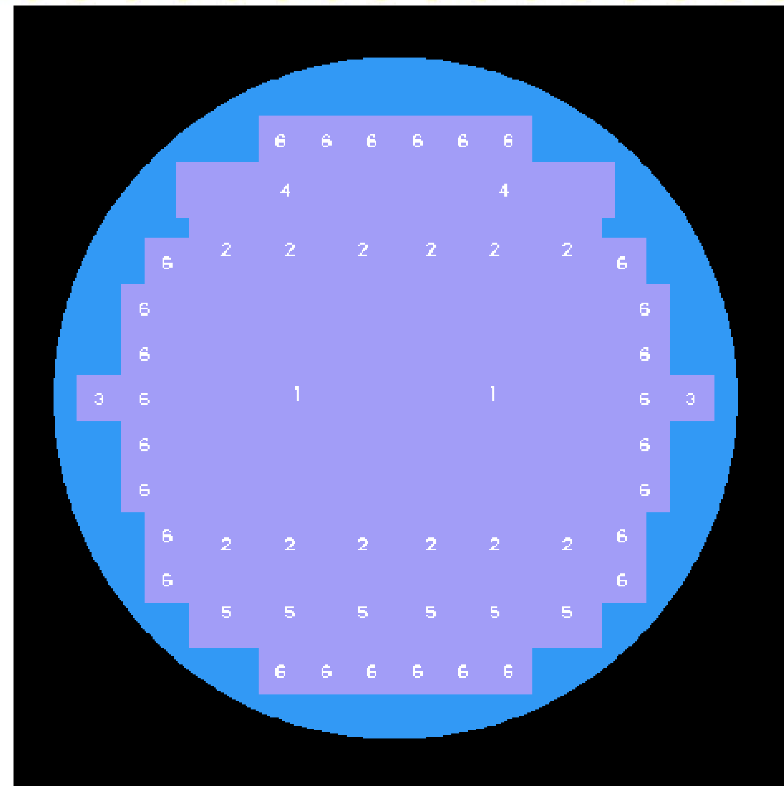
SiLC Silicon for the Linear Collider

VTT (Finland)

- VTT is a large Finnish national research center
- Start of collaboration in December 2007 with goal to develop detectors

Status:

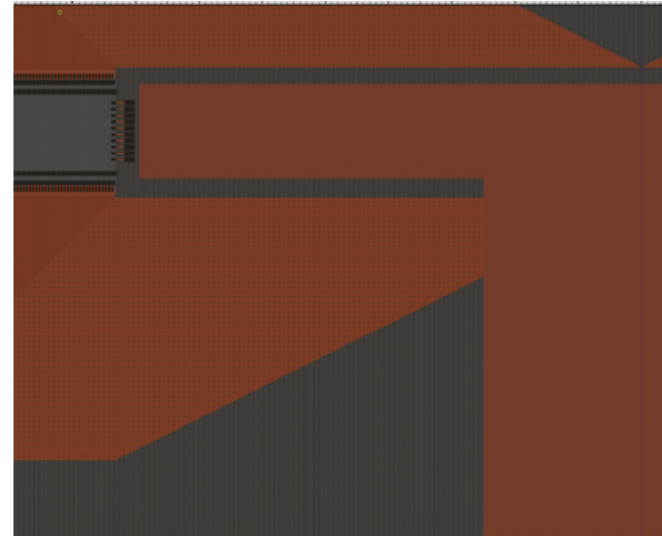
- Design ready
- Two main sensors on 4” wafer
  - One sensor DC coupled
  - Other AC coupled with FOXFET biasing
  - Vienna provided CMS-like test structures
- Processing ongoing
- We are waiting for the first wafers by end of the year

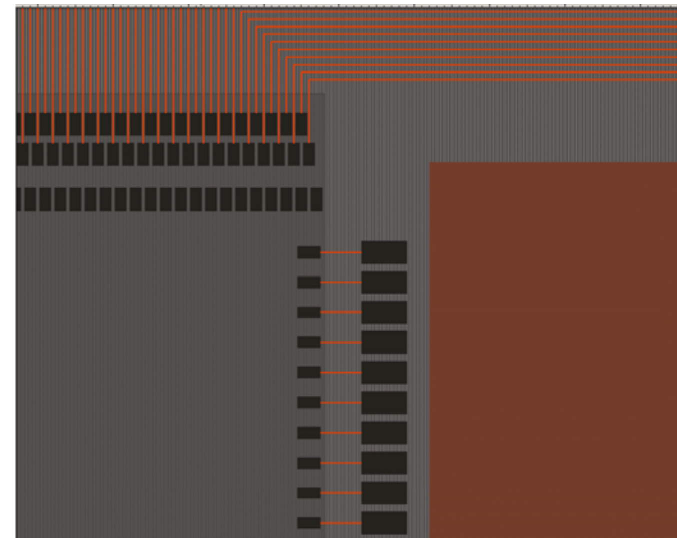


1. **MAIN DETECTOR, 5 X 5 SQCM**
2. *MEDIPIX2, 1.5 X 1.5 SQCM*
3. ALIGNMENT MARKS, 1 X 1 SQCM
4. **HALF MOON TEST STRUCTURE**
5. EDGELESS TEST STRUCTURES, 1.5 X 1.5 SQCM
6. BABY DETECTORS, 1 X 1 SQCM

ON Semiconductor

- Company located in Czech republic, former name “Tesla”
- High wafer throughput
  - 4” and 6” production line running
- Experience already with Delphi and Atlas Pixel detectors
- First contact established
- Agreement to design and build **dual-metal-layer test structures detectors** with them





SiLC
Silicon for the Linear Collider

Summary/Outlook

- Sensor baseline established:
  - FZ, p-on-n, high resistivity, 100-300um thick, 50um pitch
  - preferably DC coupled, otherwise biasing via PolySi, PT or FOXFET
- SiLC/SITRA Goals:
  - Establish companies to deliver silicon detectors for future HEP experiments
  - First contact with sensor producers (e.g. HPK, VTT, ONSemi,..) established
- Outlook / Future plan
  - Develop design, build and test detectors with fine pitch for ILC
  - Dual metal layer structure for in-sensor routing
  - Develop cheap, industrial bump-bonding technology
  - Detector thinning
  - 6” Double sided sensors
  - 8” (12”?) single sided DC sensors

The end.