EUDRB: the data reduction board of the EUDET pixel telescope

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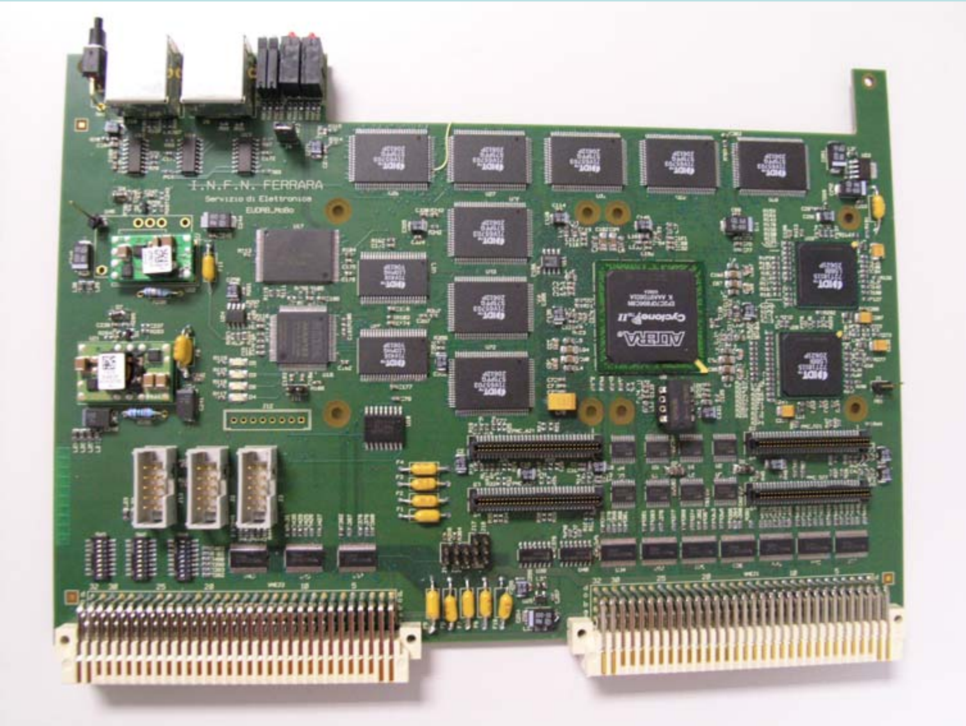
Context

- The EUDET JRA1 project: a pixel-based beam telescope to test pixel sensors suitable for the ILC
- In 2007: build and operate a “demostrator” telescope
  - Beam test campaign at DESY (June, August) and CERN (September)
- MAPS sensor for demonstrator: MimoTEL, 256x256, 30μm x 30μm pitch

- For the final telescope (2008), aim at a ***sensor*** which has sparsification ON THE CHIP to reduce, with the bulk of data, also its readout time.
- To test such sensors, we have designed a DAQ electronics which
  - can support all VMEBus transfer modes up to the 2e-sst
  - …AND can implement real-time sparsification on the readout board..

A VME64x/USB2.0-based DAQ card for MAPS sensors



mother board built around an ALTERA CycloneII FPGA (clock rate: 80MHz) and hosting the core resources and Interfaces (VME64X slave, USB2.0, EUDET trigger bus)

NIOS II, 32 bit "soft" microcontroller (clock rate: 40MHz) implemented in the FPGA for

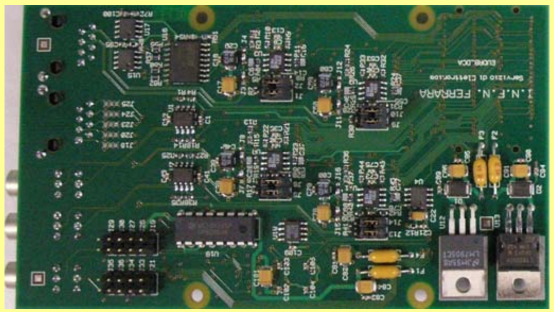
- on board diagnostics
- on-line calculation of pixel pedestal and noise
- remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

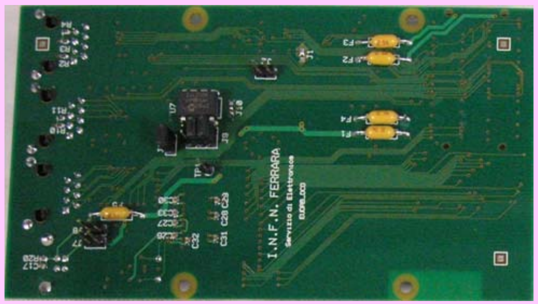
Zero Suppressed readout to minimize the readout dead-time while in normal data taking.

Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations

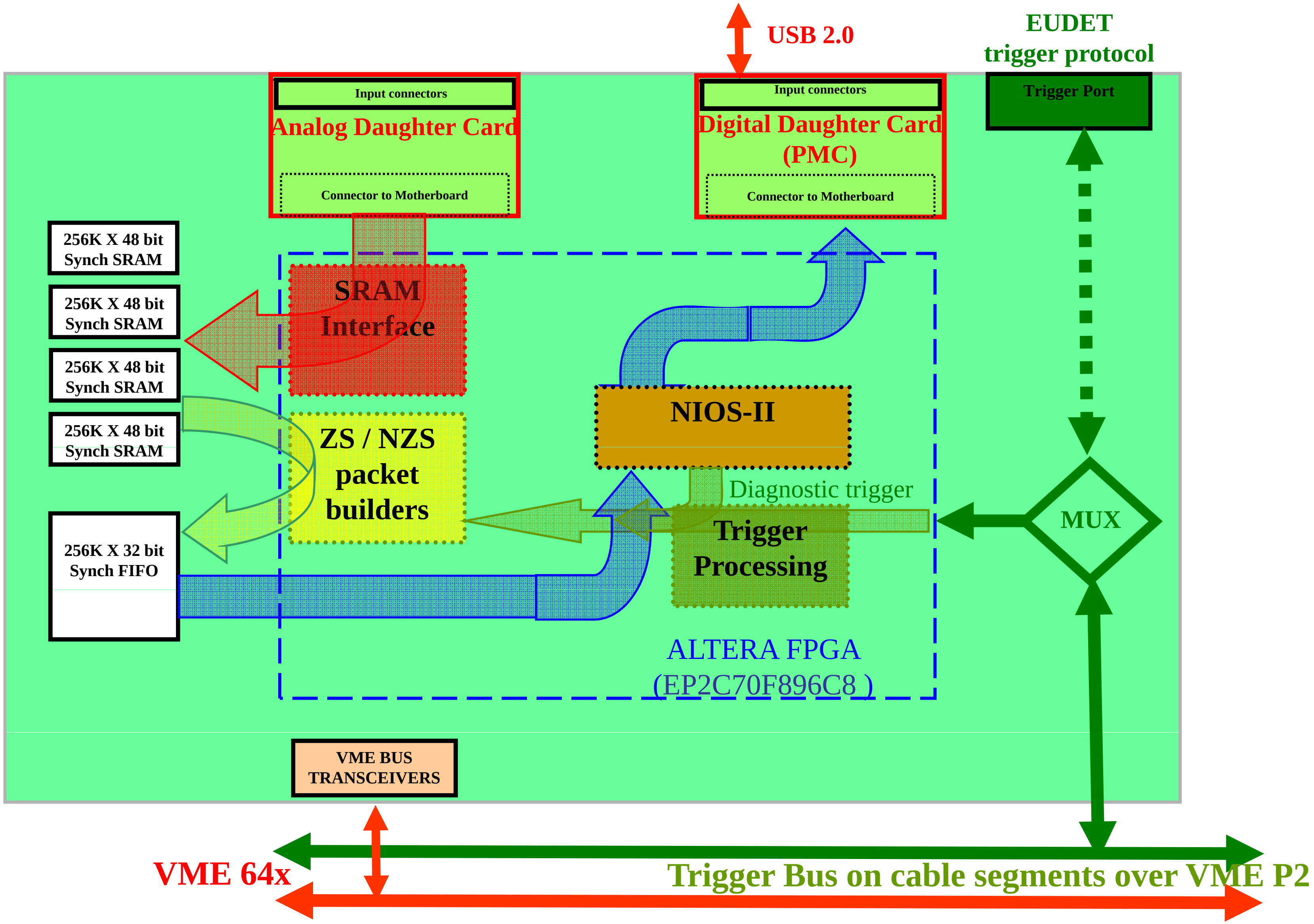
analog daughter card based on the successful LEPSI and SUCIMA designs



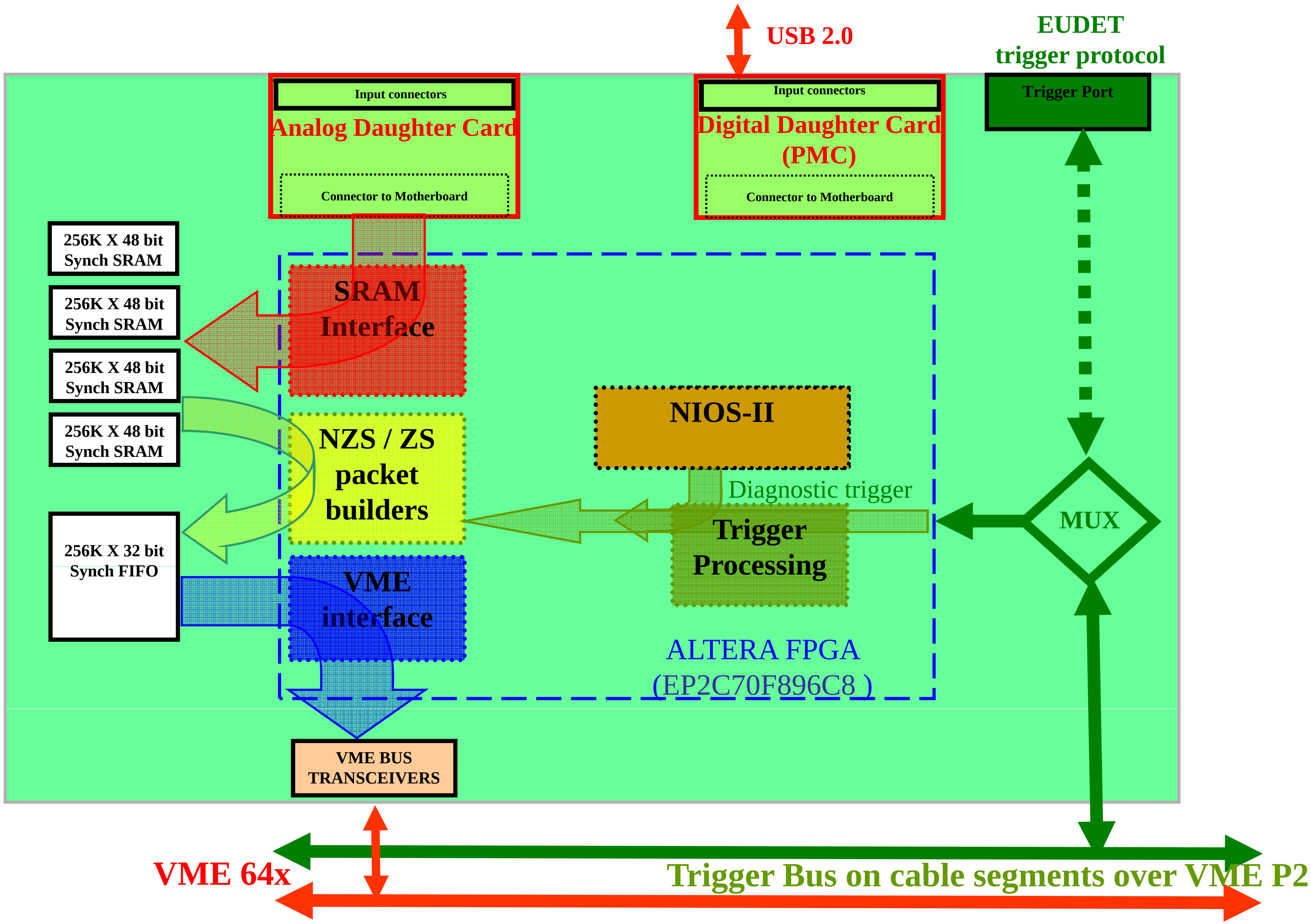
digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link



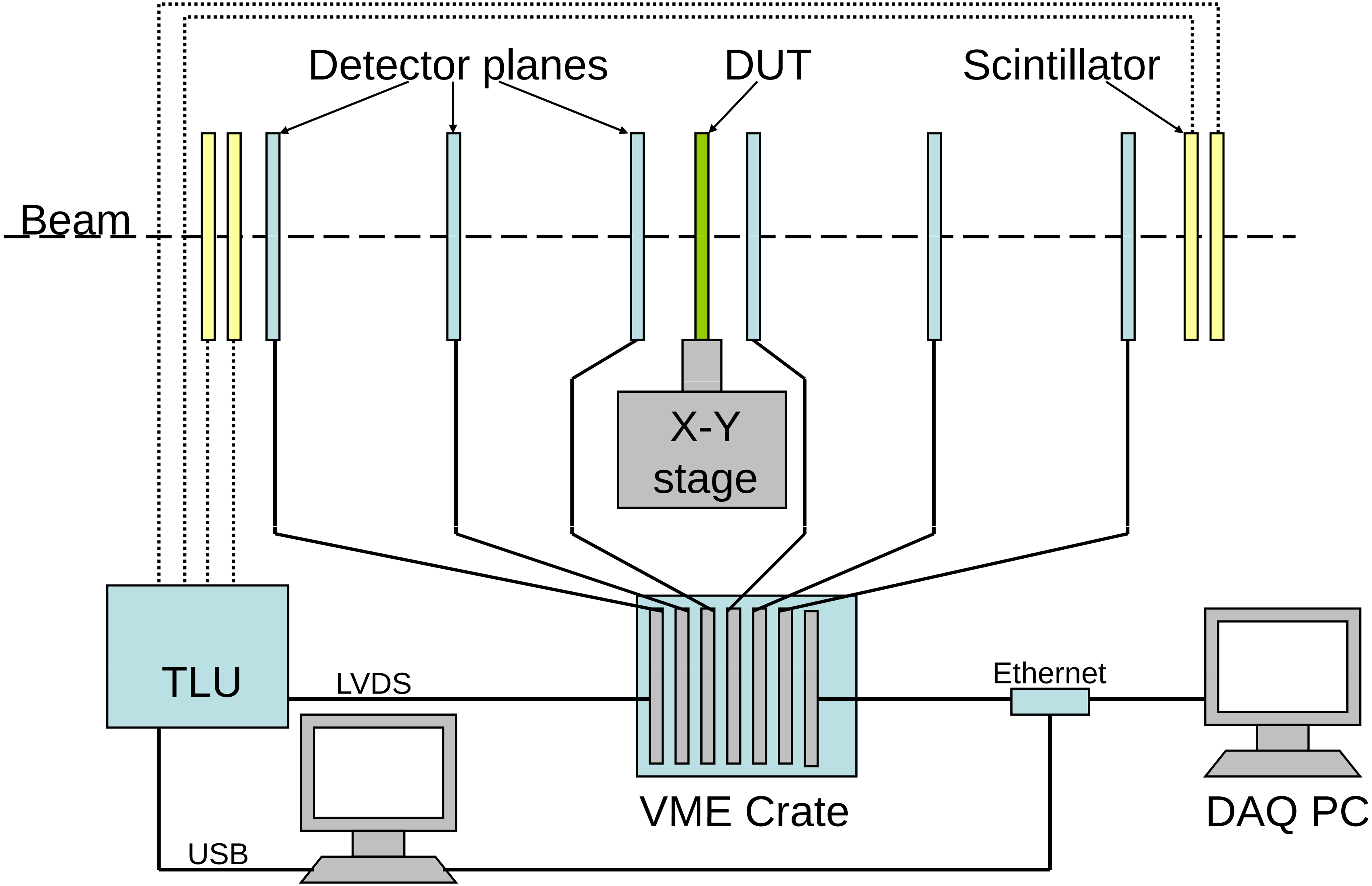
Data Flow for benchtop DAQ (slow) via USB2.0



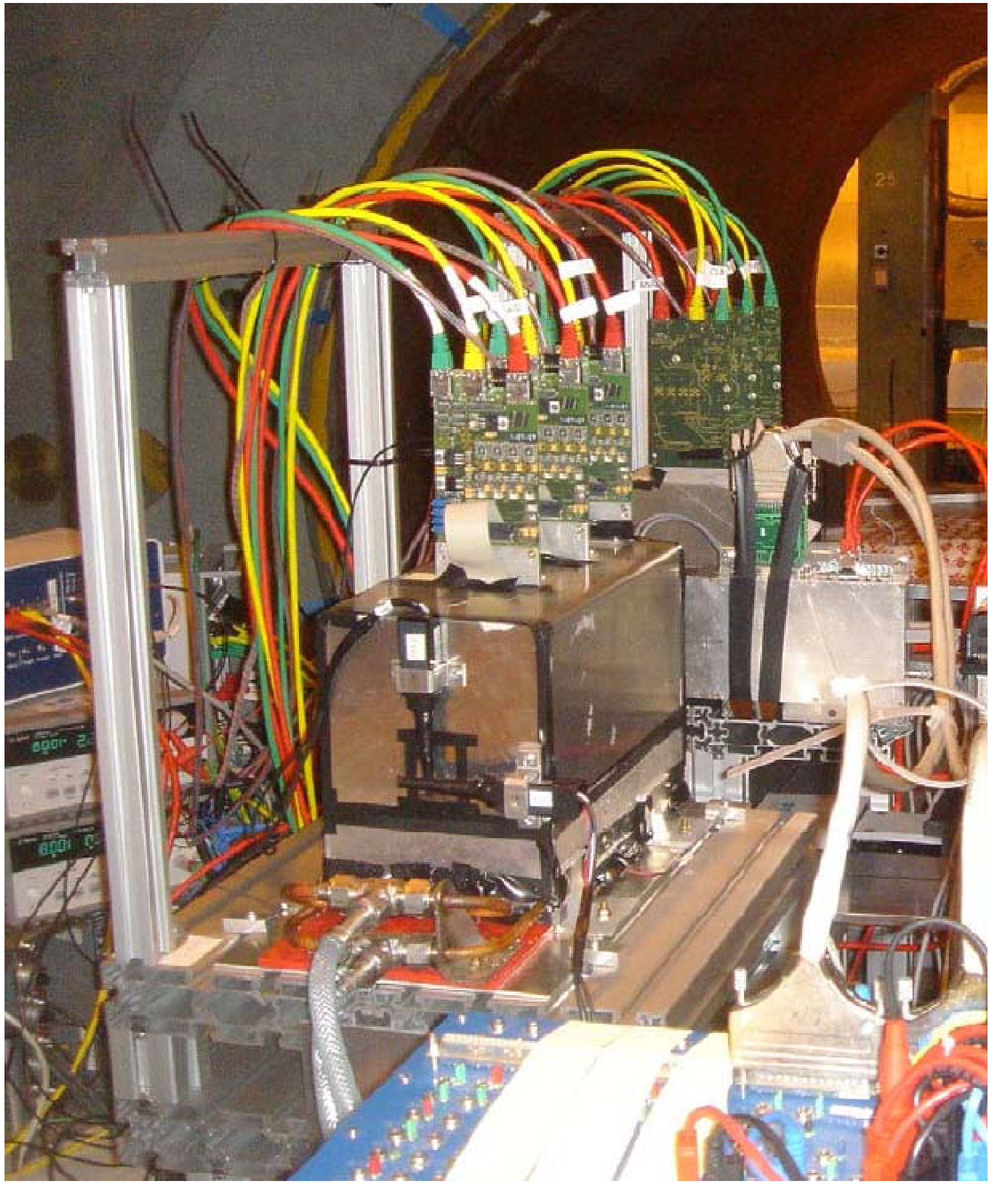
Data Flow for data taking via VMEBus

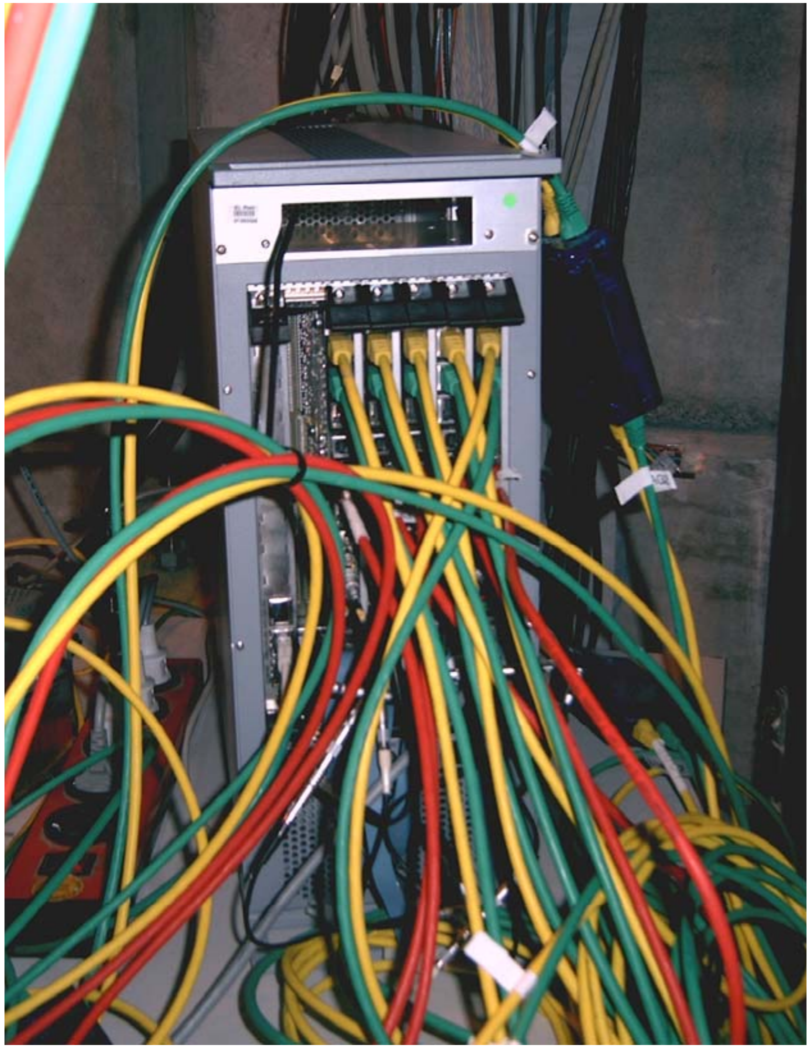


Beam test overview



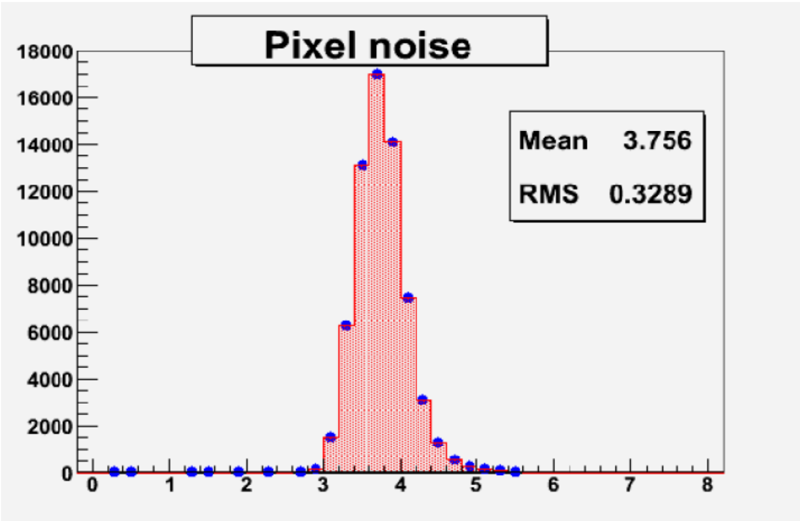
Beam test (CERN)

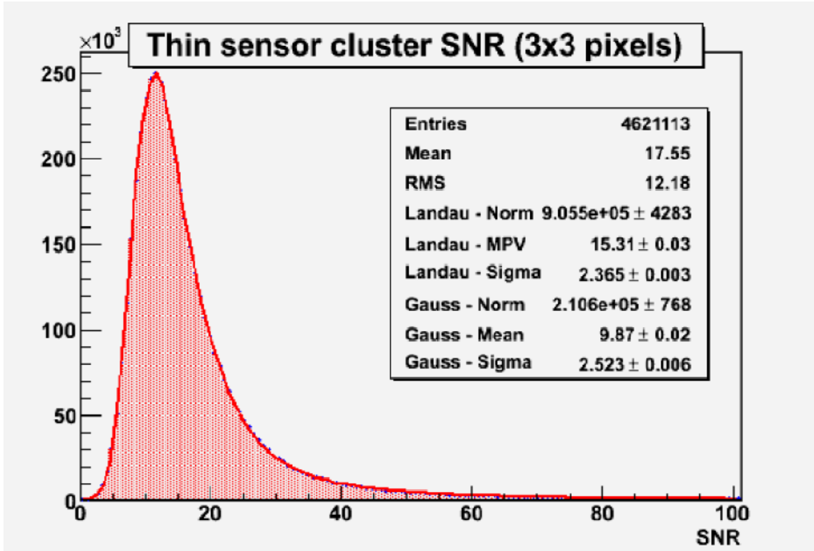


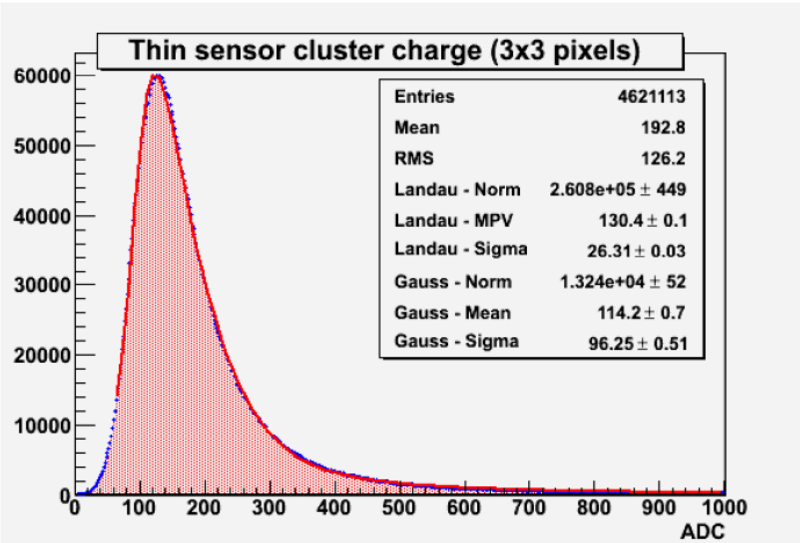


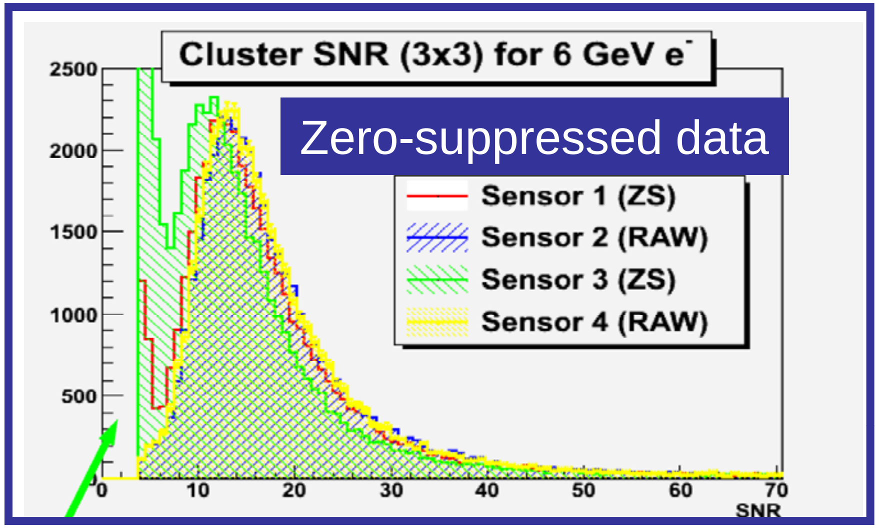
VME crate with 5 EUDRBs

Preliminary results (P. Roloff, A. Bulgheroni)









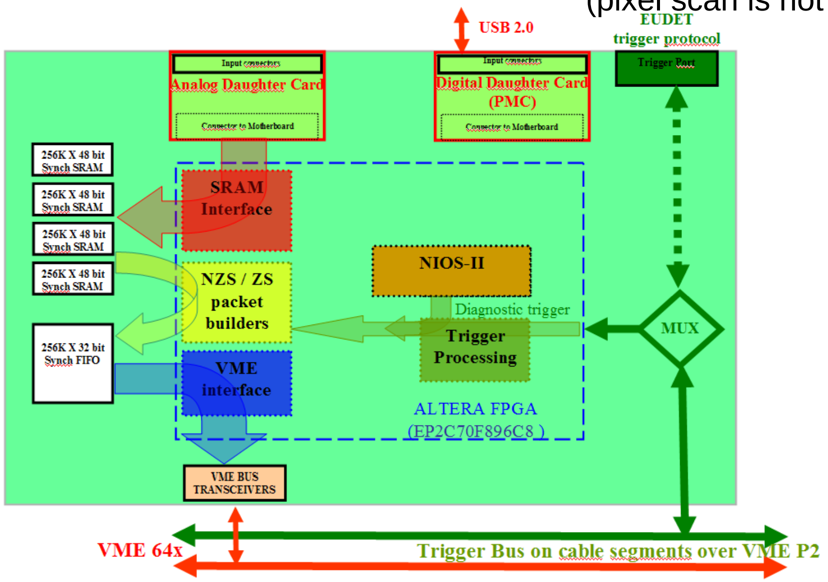
Trigger response times

Trigger response time = Time from trigger to event data packet ready in the output FIFO = Time_TtoDRdy

Time_TtoDRdy = time to extract data from sensor (Time_X) + time to transfer event data into output FIFO (Time_ToFIFO)

Time_X =
- NZS mode = between 1 and 2 frame times = between 3.2ms and 6.4ms for MIMOTEL @ 10MHz
- ZS mode = 1 frame time = 3.2 ms for MIMOTEL @ 10MHz

Time_ToFIFO =
- NZS mode = about 7ms for 3 complete frames (pixel scan is stopped while transfer occurs)
- ZS mode = 0 (the "hit" information is stored in the output FIFO as it is fetched from the sensor): (pixel scan is not stopped while extraction and transfer occur)

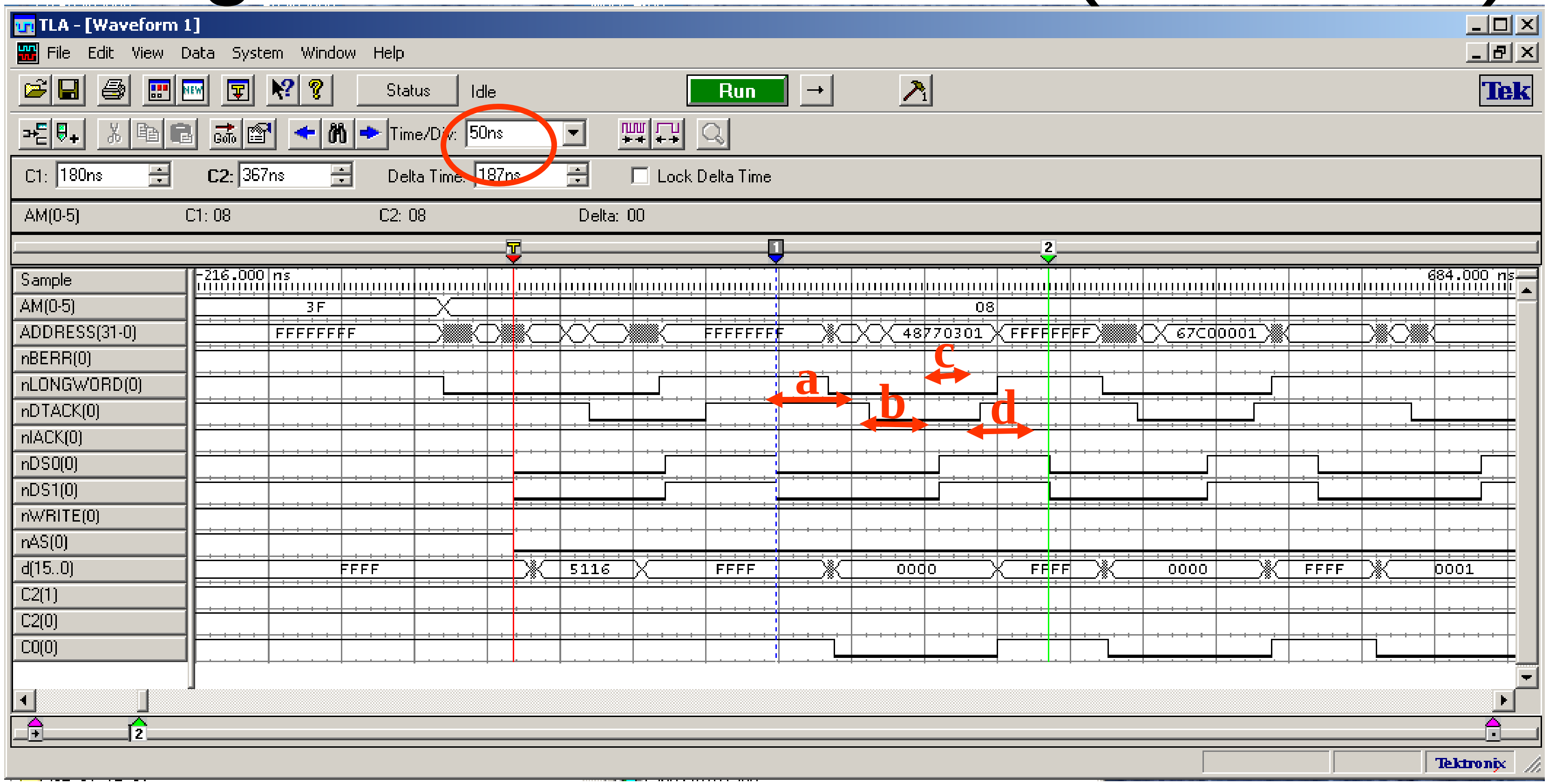


response time: 100-300 Hz

DAQ rate @ beam tests ~3Hz (RAW)
10-15 Hz (ZS)

…Why?!?

Single MBLT transfers (8B/block)

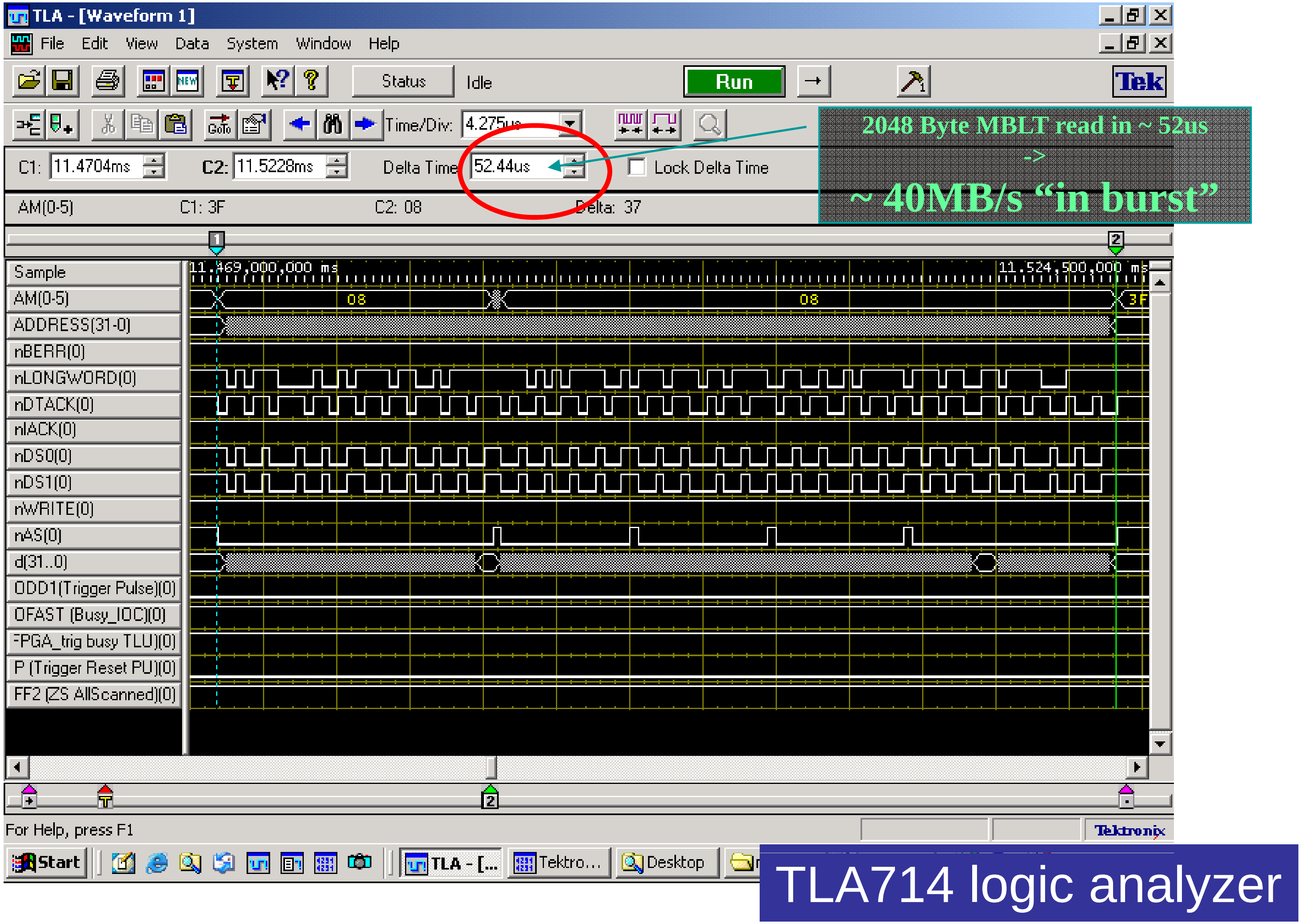


Detail of the MBLT block read.

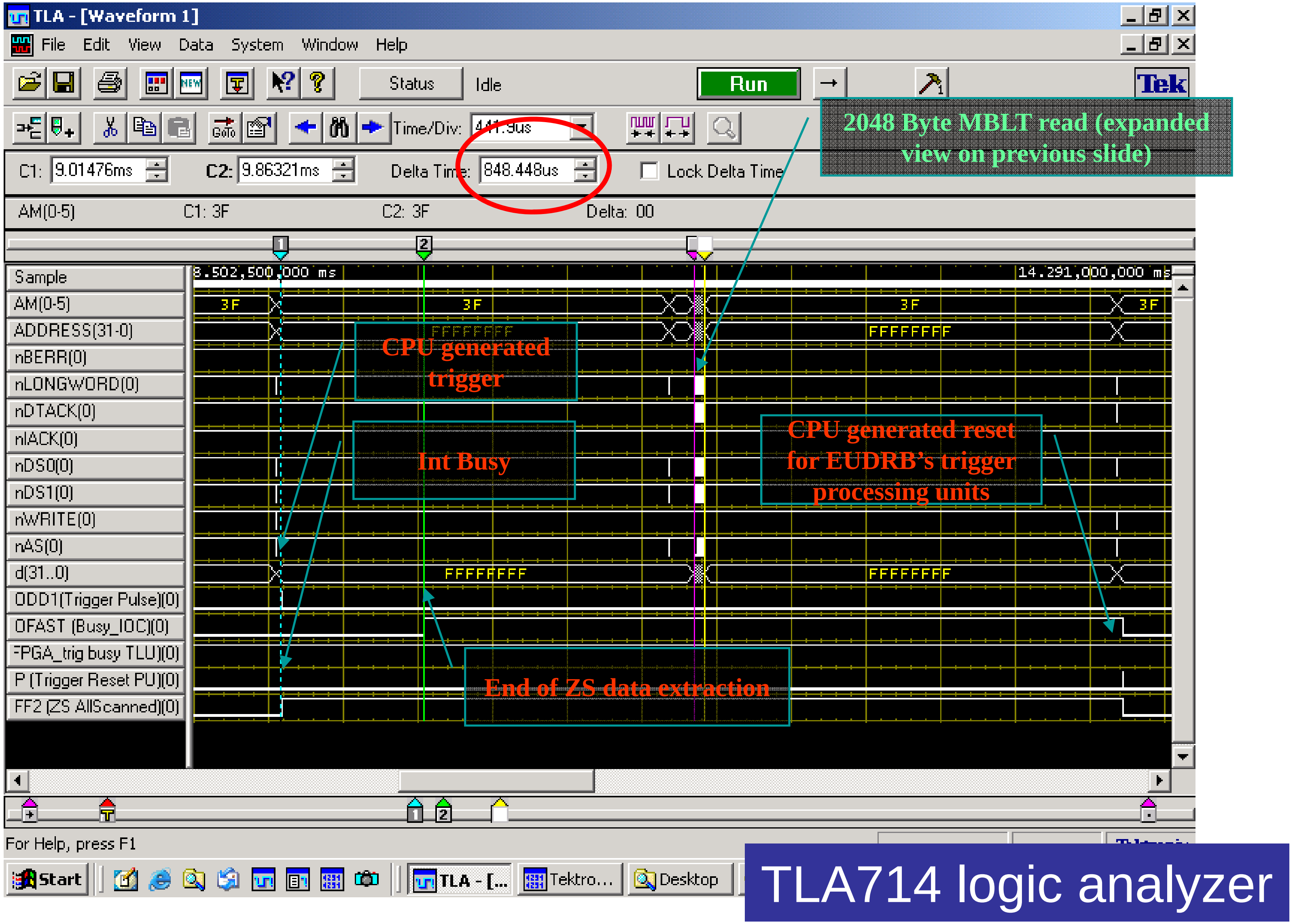
The cycle time between two successive transfers is 187ns (-> 42 MB/s peak transfer rate, compared to the maximum theoretical rate of 80MB/s claimed by the standard). This time is made up of

- (a) Delay from nDS0,nDS1 active to nDTACK active: about 60ns. It is determined by the EUDRB.
- (b) Delay from nDTACK active to nDS0,nDS1 unactive : about 50ns. It is determined by the VME CPU
- (c) Delay from nDS0,nDS1 unactive to nDTACK unactive : about 30ns. It is determined by the EUDRB.
- (d) Delay from nDTACK unactive to nDS0,nDS1 active : about 50ns. It is determined by the VME CPU

Reading a 2048 Byte MBLT



Including the VME CPU…



Next steps

- On the VME side:
  - Understand the ~2ms dead time between single transfers (check of "DataReady Flag, Clear of EUDRBs after readout, pedestal/threshold setting etc..) on the VMEBus. This is due to the VME CPU.
  - Implement slave-termination of MBLT transfers data through the VMEBus. Presently we must use zero-padding termination because of a bug in the software driver for the PCI-VME bridge chip (Tsi 148) residing on the VME CPU board.

- On the EUDRB side:
  - implement 2e-VME transfers (up to 320MB/s nominal transfer speed)
  - start thinking configuration for the final sensors

- Items with lower priority (real bottlenecks are above):
  - write several ZS events on the FIFO and extract data only when the FIFO is full (multi-event mode)
  - implement MBLT in write mode (for pedestal and thresholds)
  - write ZS and NZS data for the same event. Is this still needed?

- Status of new production (8 boards)
  - Boards are in Ferrara, tests starting
  - Will send them back to Artel afterwards
  - Artel will ship to Geneva

Conclusion

- EUDRB successfully used in beam tests at DESY (June, August) and CERN (September)
- Hunting for better performance:
  - VME CPU is the real bottleneck at the moment
  - Some improvements on the EUDRB side also possible