Final Sensors for EUDET Telescope: Progress Report

Evolution since June '07

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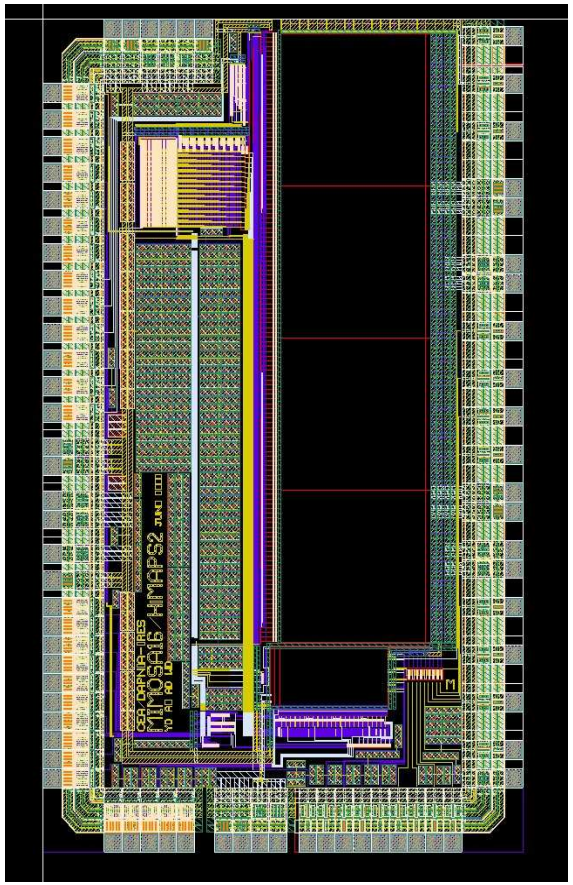
on behalf of DAPNIA-Saclay & IPHC-Strasbourg

OUTLINE

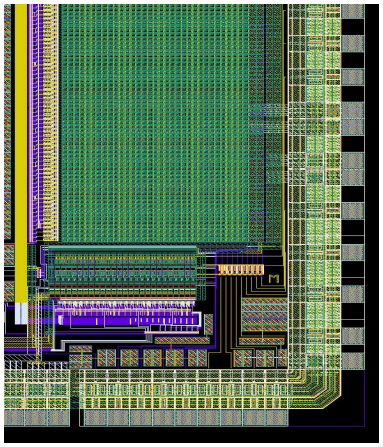
- **MIMOSA-16: preliminary test results of data collected at CERN-SPS**
- **MIMOSA-22: status of design**
- **∅ micro-circuit : status of 1st prototype fabrication**
- **Towards the final sensor**
- **Summary**

Tests of MIMOSA-16

- **MIMOSA-16 design features :**
  - **AMS-0.35 OPTO translation of MIMOSA-8**
    $\hookrightarrow \sim$ **11–15** μm **epitaxy instead of** $\lesssim$ **7** μm
  - **32 // columns of 128 pixels (pitch: 25** μm**)**
  - **on-pixel CDS (DS at end of each column)**
  - **24 columns ended with discriminator**
  - **4 sub-arrays :**
    - **S1 : like MIMOSA-8 (1.7x1.7** μm^2 **diode)**
    - **S2 : like MIMOSA-8 (2.4x2.4** μm^2 **diode)**
    - **S3 : S2 with ionising radiation tol. pixels**
    - **S4 : with enhanced in-pixel amplification**
      (against noise of read-out chain)



$\Rightarrow$



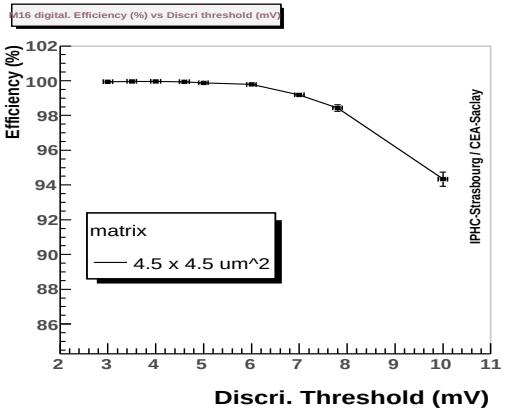
- **Preliminary tests of analog part (”20” & ”14”** μm **epitaxy) performed in Saclay (shown previously):**
  - **sensors illuminated with** ^{55}**Fe source and** $F_{r.o.}$ **varied up to** $\gtrsim$ **150 MHz**
  - **measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs** $F_{r.o.}$
- **Since last JRA-1 coll. meeting: m.i.p. detection with Si-stip telescope studied at CERN in Sept. ’07**

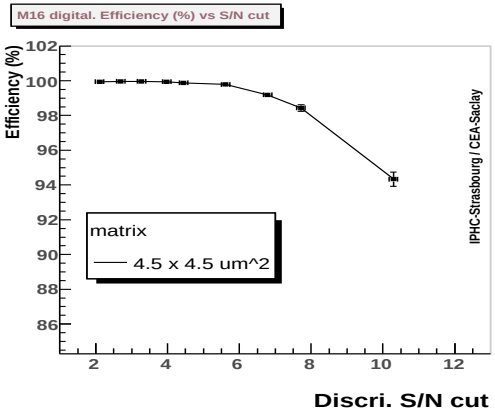
MIMOSA-16 : Tests at CERN-SPS

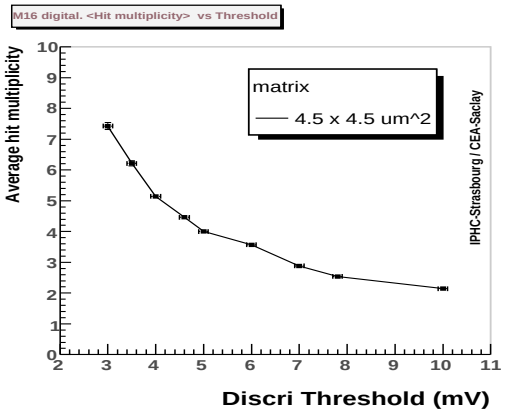
- *CERN-SPS: T4 - H6 (180 GeV "π^-")*
- *1 week of run early Septembre with MIMOSA-16 chips mounted on Si-strip telescope*
- *Read-out time: 51 μs (20 MHz for each group of 8 columns))*
- *6 individual sensors tested:*
  - 3 MIMOSA-16 with "14" μm epitaxy thickness
  - 1 MIMOSA-16 with "20" μm epitaxy thickness
  - 2 MIMOSA-16bis with "14" μm epitaxy thickness
- *Data still being analysed $\rightarrowtail$ results shown are* PRELIMINARY

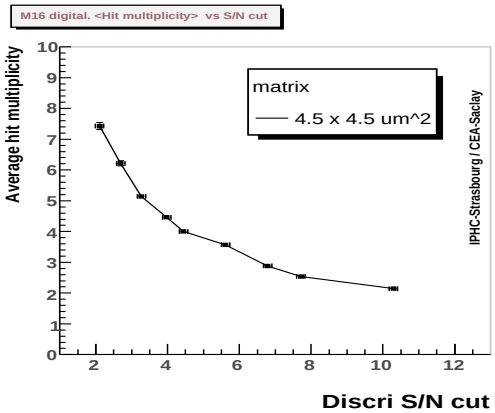
MIMOSA-16: preliminary test results

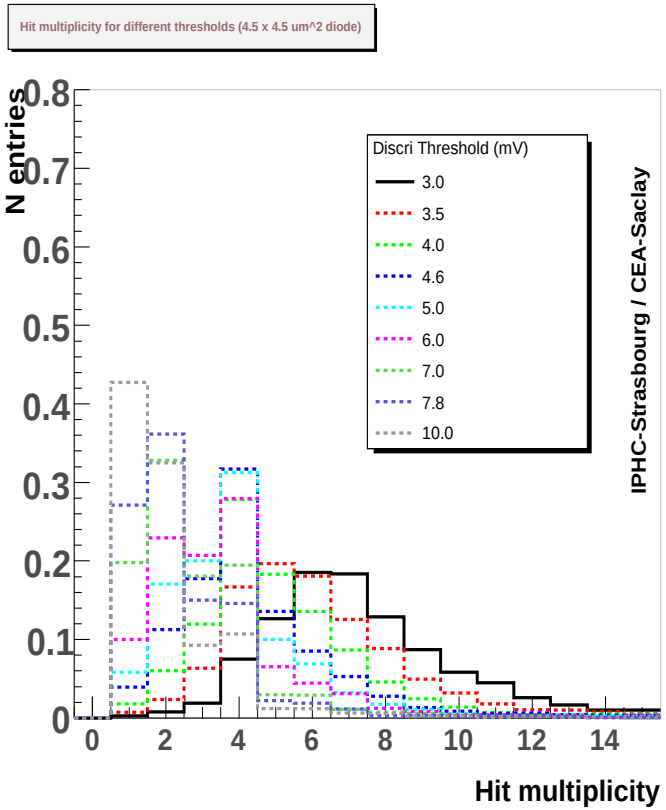
Preliminary analysis results of data collected with sub-array S4 (epi-14) $\longmapsto$ SNR $\sim$ 16









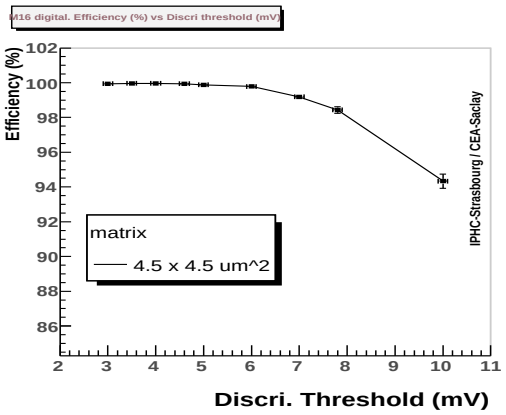


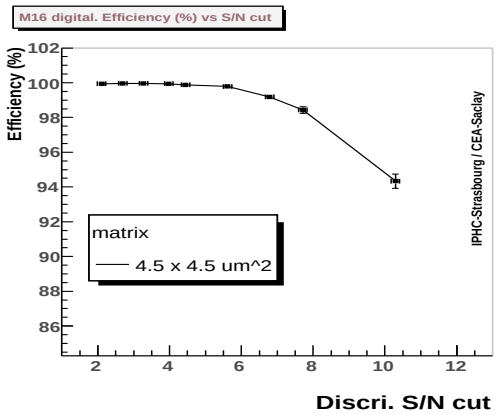
Detection efficiency (includes contributions from single pixel clusters):

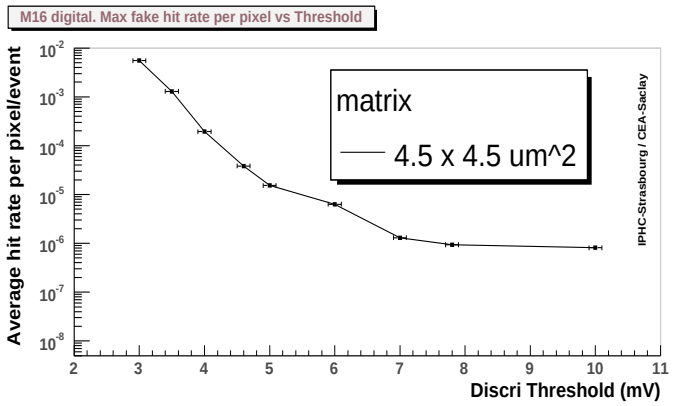
- ▷ **Discri. threshold:** ※ 4 mV $\longmapsto \epsilon_{det}$ = 99.96 $\pm$ 0.03 (stat) % ※ 6 mV $\longmapsto \epsilon_{det}$ = 99.88 $\pm$ 0.05 (stat) %
- ▷ **Discri. threshold:** ※ 4 mV $\longmapsto \lesssim$ 2 % of clusters with 1 pixel ※ 6 mV $\longmapsto \sim$ 10 % of clusters with 1 pixel

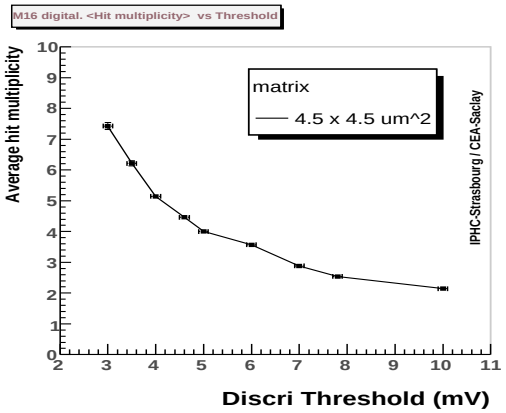
MIMOSA-16: preliminary test results

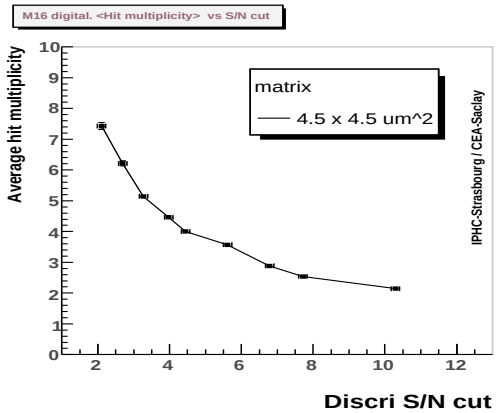
Preliminary analysis results of data collected with sub-array S4 (epi-14) $\longmapsto$ SNR $\sim$ 16

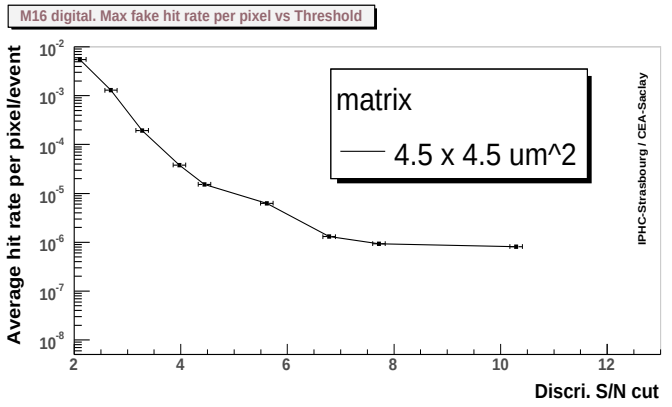










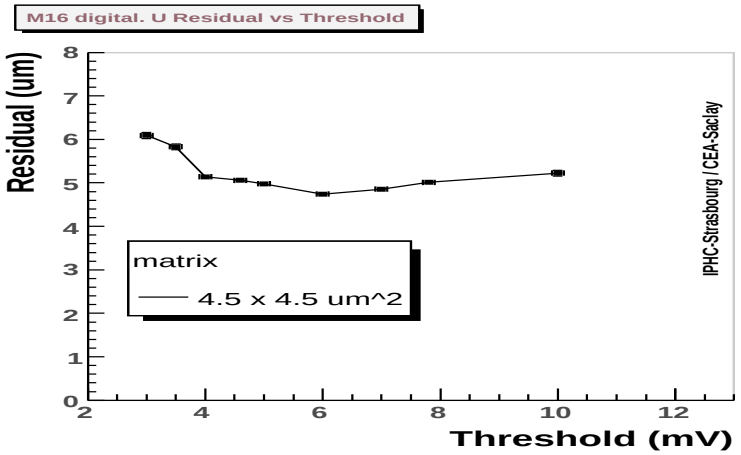


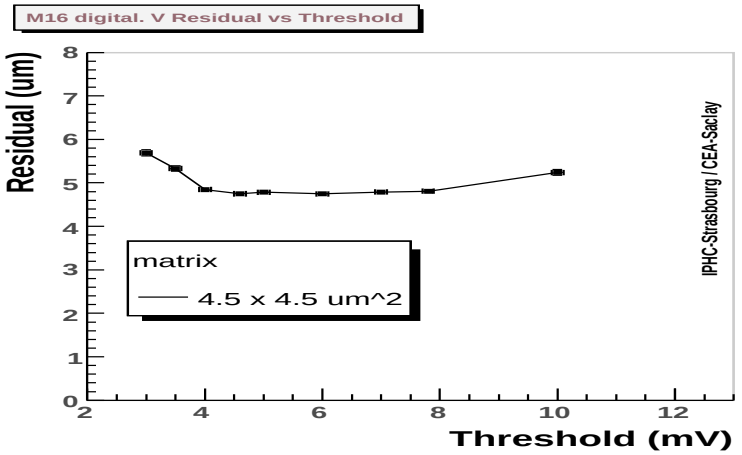
Fake hit rate (dominated by contributions from single pixel clusters):

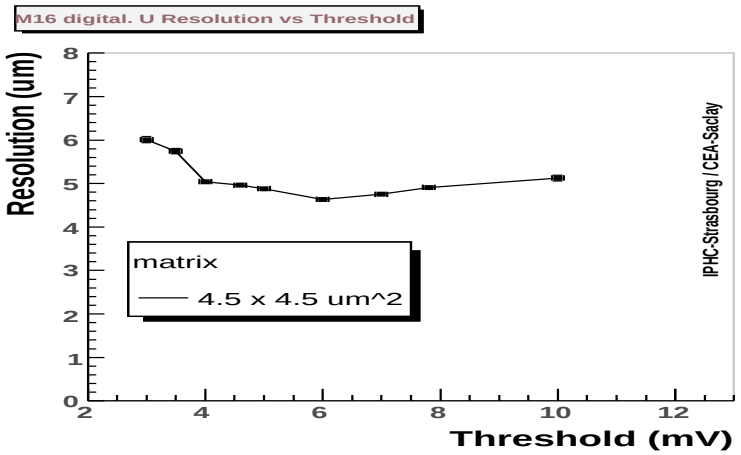
▷ **Discri. threshold:** ※ 4 mV $\longmapsto$ fake rate $\sim 2{\cdot}10^{-4}$ ※ 6 mV $\longmapsto$ fake rate $<10^{-5}$

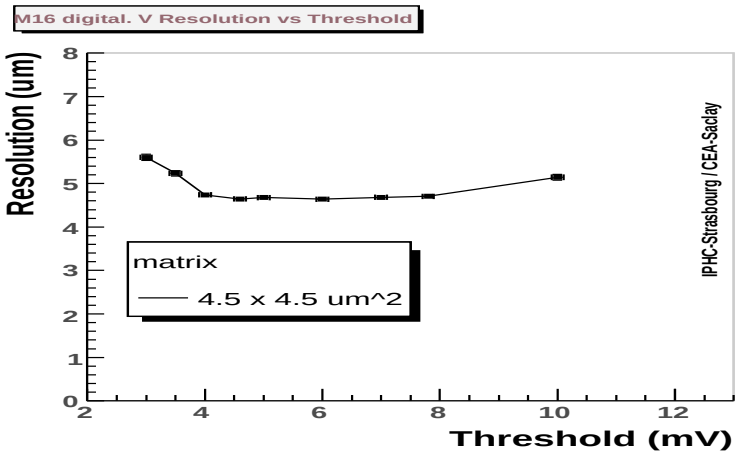
MIMOSA-16: preliminary test results

- **Preliminary analysis results of data collected with S4 sub-array (epi-14)**







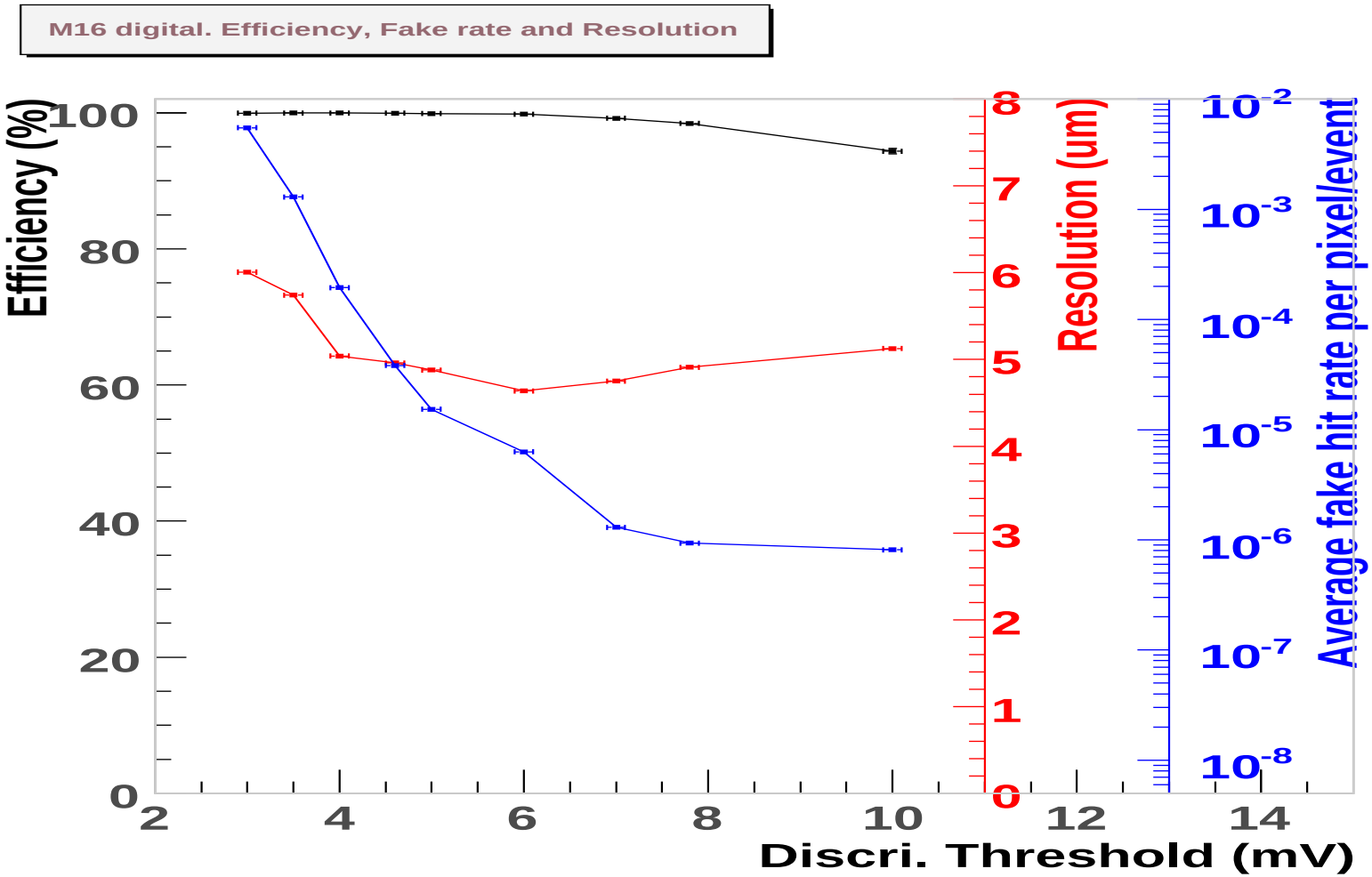


- **Single point resolution is well below the binary resolution reflecting the 25 μm pitch (7.2 μm) :**

  ▷ **Discri. threshold:** ※ 4 mV $\longmapsto \sigma_{sp} \sim$ 4.8–5.0 μm ※ 6 mV $\longmapsto \sigma_{sp} \sim$ 4.6 μm

MIMOSA-16: preliminary test results

Summary of results obtained with S4 sub-array (epi-14) :

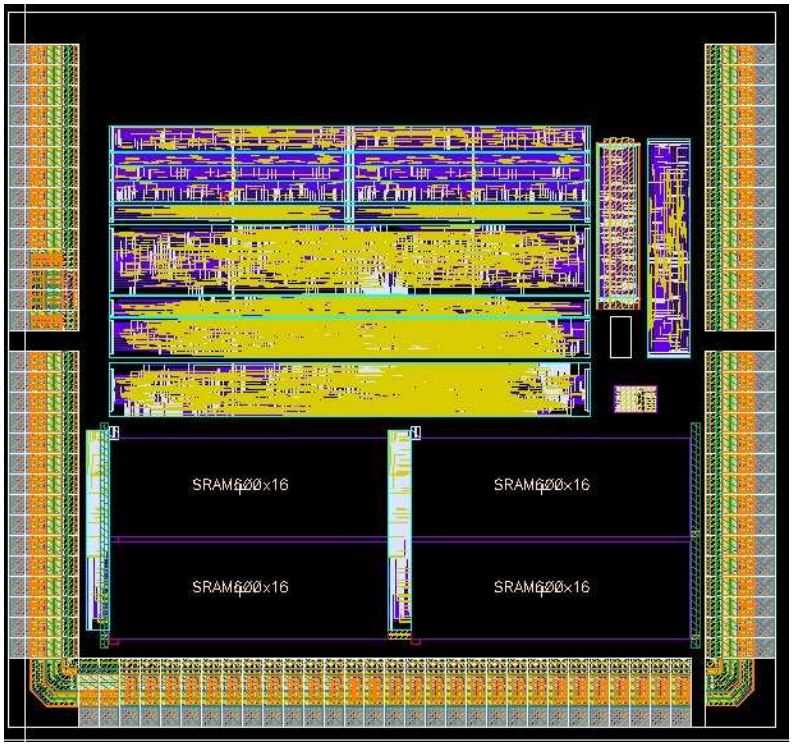


Main outcome of the tests: At least one pixel ⊕ discri. architecture validated for the final sensor

Zero Suppression Micro-Circuit : SUZE-01 Fabrication

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - ◇ step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - ◇ step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim$ (3.9 + 0.24) $\times$ (3.6 + 0.24) mm^2
  $\longrightarrow$ 10.3 keuros (EUDET budget)

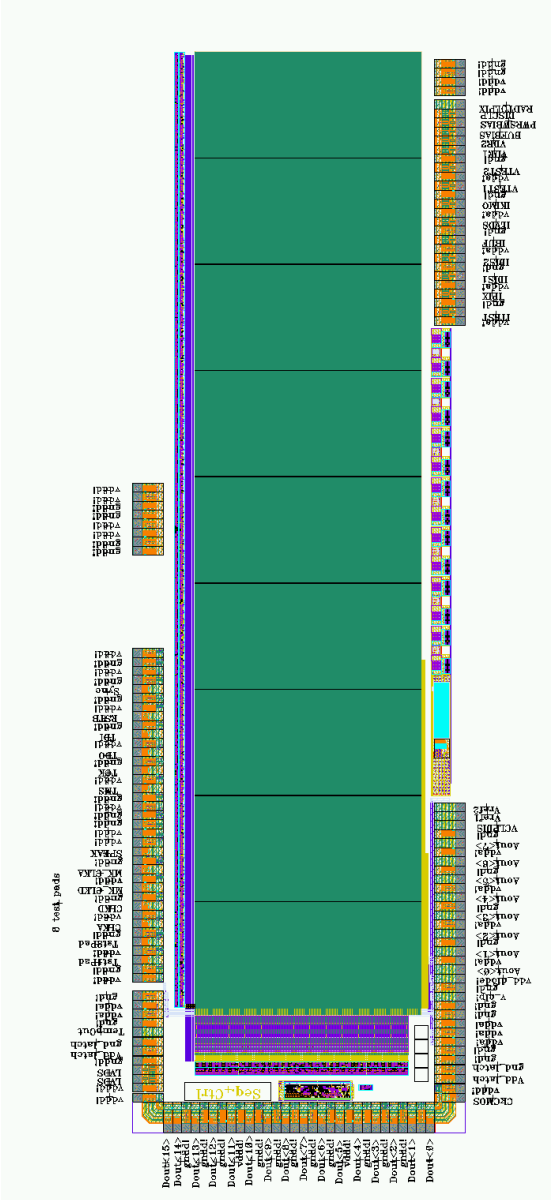


Status :

- sent for fabrication end of July
- back from foundry end of Sept. $\longrightarrow$ tests are still getting prepared $\Rightarrow$ test completion expected by end of year

- Final prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 $\rightarrowtail$ larger surface, smaller pitch, optimised pixel, JTAG, more testability**



Pixel characteristics (optimal charge coll. diode size ?) :

- ⁕ pitch : 18.4 μm (compromise resolution/pixel layout)
- ⁕ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ⁕ 128 columns ended with discriminator
- ⁕ 8 columns with analog output for test purposes
- ⁕ 9 sub-matrices of 64 rows : various pixel designs w/o ionising rad. tol. diode

  $\Rrightarrow$ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)

Testability :

- ⁕ JTAG + bias DAC $\rightarrowtail$ programmable chip steering
- ⁕ 2 additionnal DC voltages to emulate pixel's output

  for independent discriminator performance assessment
- ⁕ output frequency $\leq$ 40 MHz

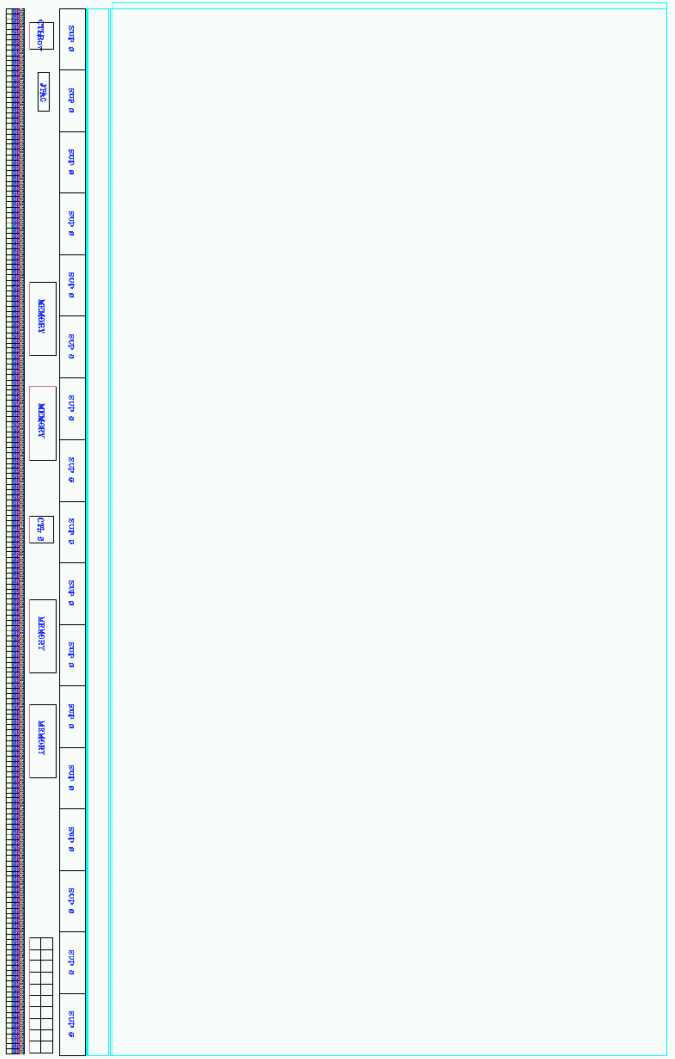
Status :

- ⁕ Design close to completion $\rightarrowtail$ submission by end of Oct. '07
- ⁕ Funding ($\sim$ 50 mm^2): $\sim$ 40 keuros $\rightarrowtail$ EUDET (27 keuros) & DAPNIA resources
- ⁕ Question: sharing/organisation of tests (digital output !) ? use (no integ. $\emptyset$) ?

Roadmap towards the Final Chip

Autumn 2008 : MIMOSA-22+ = Final Sensor

- MIMOSA-22 complemented with $\emptyset$ (SUZE-01)
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm^2)
- Read-out time $\sim$ 100 μs
- Chip dimensions : $\sim$ 20 x 12 mm^2
- Engineering run : $\sim$ 120 keuros for 6 diced and thinned wafers
  - $\hookrightarrow$ funding : EUDET (70 keuros) & IPHC/DAPNIA (50 keuros)



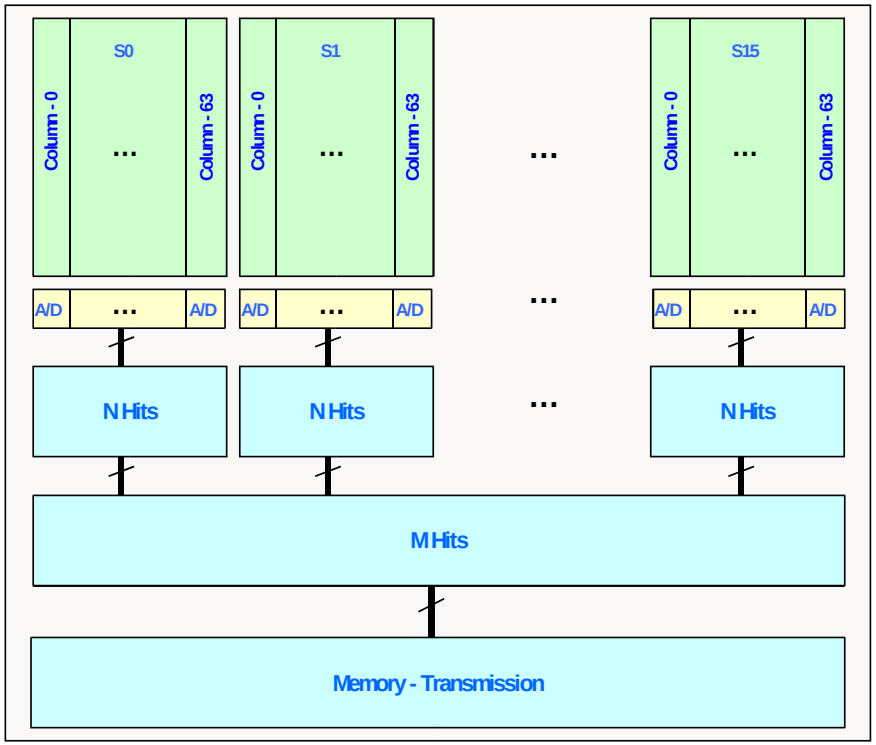
2009 : commissionning $\rightarrowtail$ organisation ?

SUMMARY

- **MIMOSA-16 tests at the SPS $\longmapsto$ preliminary, partial, analysis results:**
  - *The column architecture works very well*
  - *There is at least one pixel architecture which works fine : SNR $\sim$ 16, $\epsilon \sim$ 99.9 %, $\sigma_{sp} \lesssim 5\ \mu m$*
  - *Complementary info expected from the analysis of the other pixel architectures*
- **MIMOSA-22:**
  - *Has become final prototype $\longmapsto$ more features and surface than foreseen originally*
  - *Design well advanced, based on M-16 pixel and column architectures (still some technical difficulties ...)*
    $\longmapsto$ submission to foundry by end of this month !
  - *Funding ($\sim$ 40 keuros) via EUDET and DAPNIA resources*
- **$\emptyset$ suppression micro-circuit :**
  - *Back from foundry a few days ago*
  - *Tests will start soon $\longmapsto$ completed this year*
- **Final sensor combining MIMOSA-22 architecture and $\emptyset$ micro-circuit : MIMOSA-22+**
  - *1088$\times$544/576 pixels (1$\times$2 cm^2)*
  - *Design starting early 2008 (?) $\longmapsto$ will integrate feed-back from MIMOSA-22 and SUZE-01 tests*
  - *Expected to be submitted for fabrication in Autumn 2008*
  - *... prepare its commissionning ....*

Zero Suppression : SUZE-01 Block Diagram

Chip readout architecture including digitization and zero suppression



Block diagram of readout architecture

- Pixel array : 1024x1024 pixels Readout row by row The row is divided into 16 groups
- Analog to digital conversion at the bottom of each column (Discriminator or ADC)

Zero suppression algorithm :

- Find N Hits for each group
  Find M Hits for each row
  (With N and M determined by pixel array occupancy rate)
- Memory wich stores M hits and serial transmission

- Submission of a small size fully digital prototype in AMS 0.35 µm in June 2007