VFCAL Report

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Infrastructure for sensor diagnostics

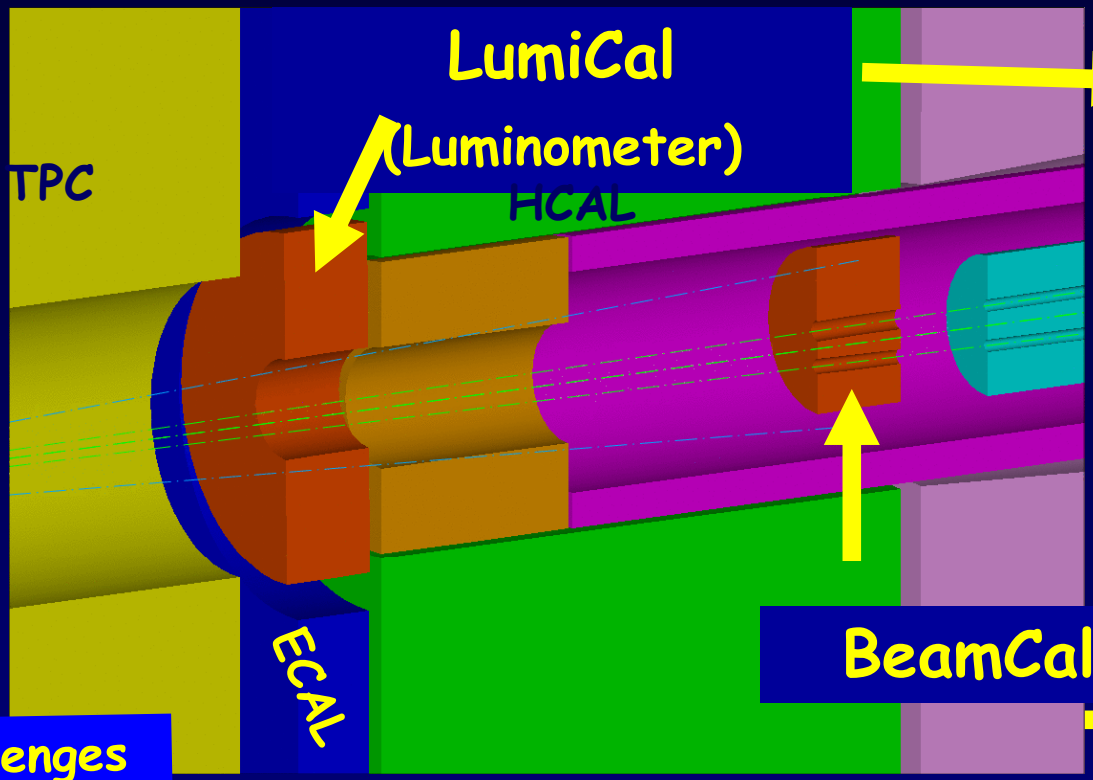
FE Electronics Development

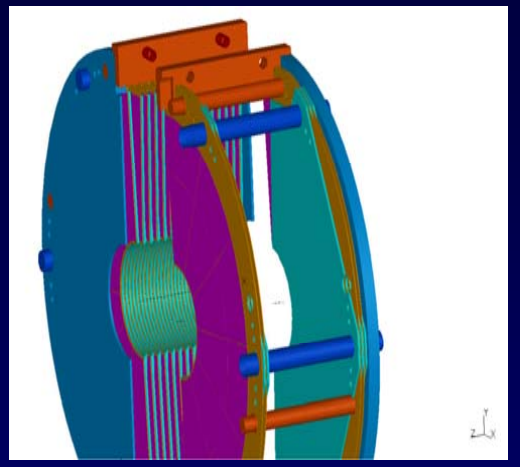
Sensor test facilities and testbeam

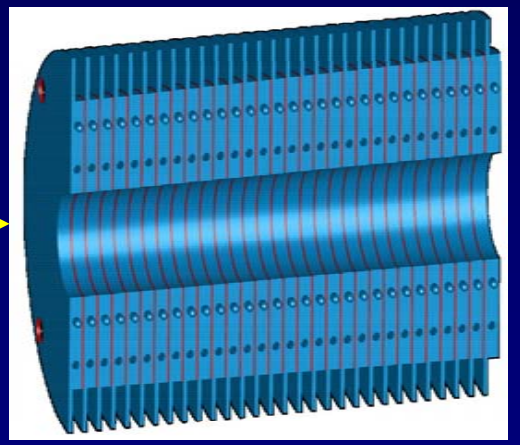
Laser Alignment

Labs involved: Cracow UST, Cracow INP,
Prague (AS), Tel Aviv Univ.
DESY (Z.)

Current design (Example LDC, 14 mrad):







Challenges

LumiCal: -control of position on ~100 μm level
-control of the inner acceptance radius on ~μm level

BeamCal: -radiation hard sensors (~10 MGy/year)

Both: -compact (smallest possible Moliere radius)
-readout after each BX

Infrastructure for Sensor and FE Tests

Clean Rooms (Cracow, DESY, Tel Aviv)

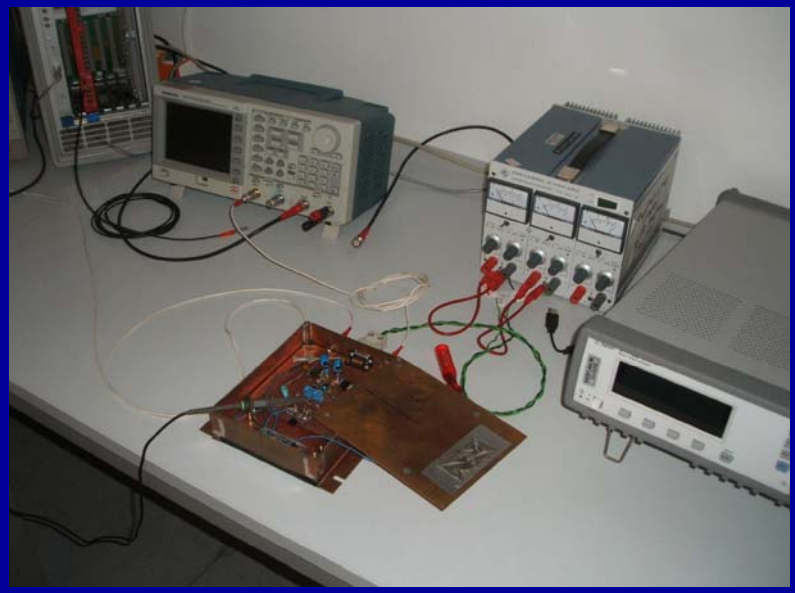
e.g. DESY

two rooms with filtered air (10k), stabilized temperature

- room 1: bonding and assembly
- room 2: all measurements without radioactive source

Upgrade of the probe station at DESY

- New voltage- current devices (Keithley 6487)
- Control software
- Amplifier test bench



Infrastructure for Sensor and FE Tests

Design Flow for IC readout chip tests with the custom sequencer V1495

Quartus II
Electronics Design Tool

- edit functional description (VHDL)
- compile to binary

VME Crate Controller
custom LINUX handler
USB to VME bridge

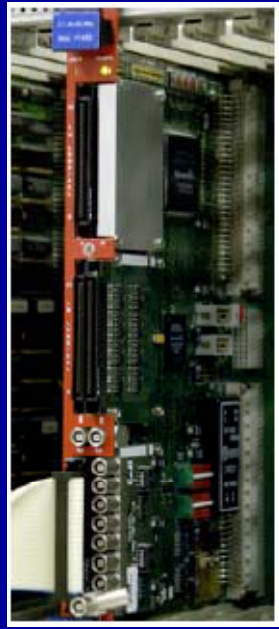
- flash V1495 firmware with user functionality

VME Test Stand
any VME controller

- operate sequencer in stand-alone mode using custom parameter registers

PHY3 Prototype Board
plus Power Supplies, Puls Generators

- operate PHY3 chip with different modes and frequencies



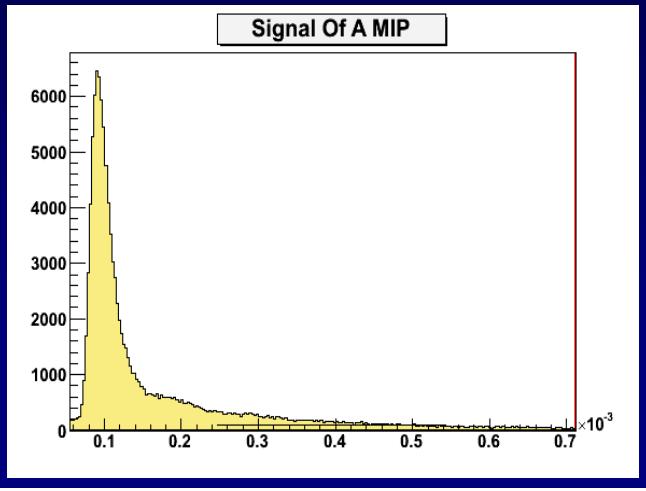
C.A.E.N. V1495 general purpose I/O module

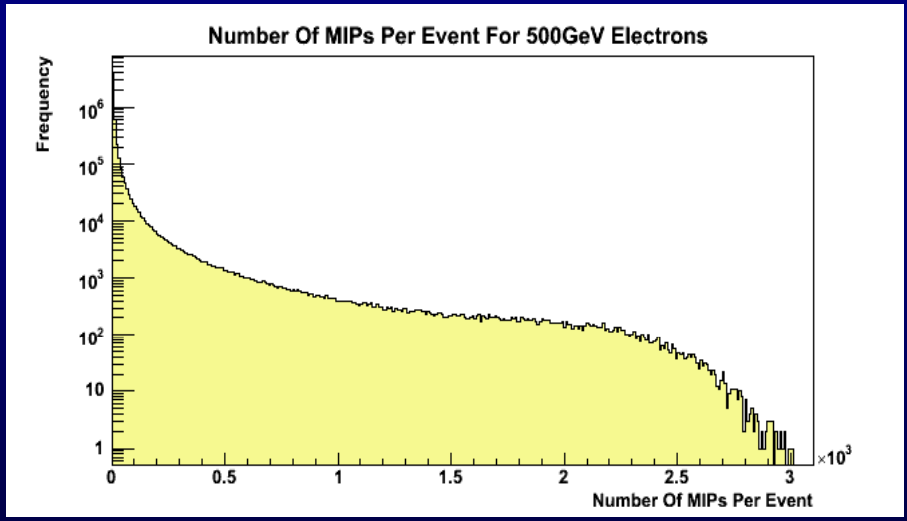
w/ LVDS and NIM In/Out channels

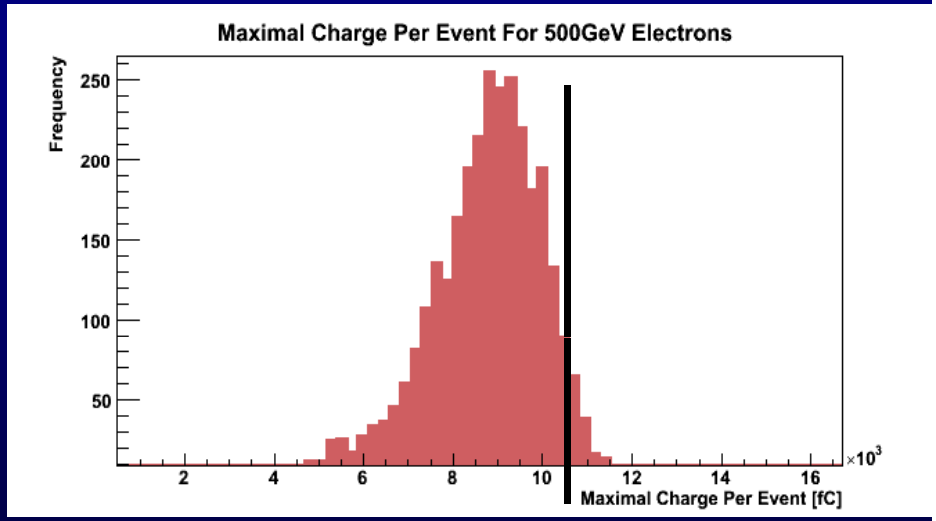
Test Example: PHY3

Simulation Studies for the FE design

1. 500 GeV electrons for 8-Bit & 10-Bit schemes.
2. Energy MPV of a MIP in 0.3 mm thick silicon is 93.8 KeV.
3. The maximal number of MIPs in a single cell is 3,010.
4. 95% of the signal is below 10,575 pC = 2,586 MIPs.



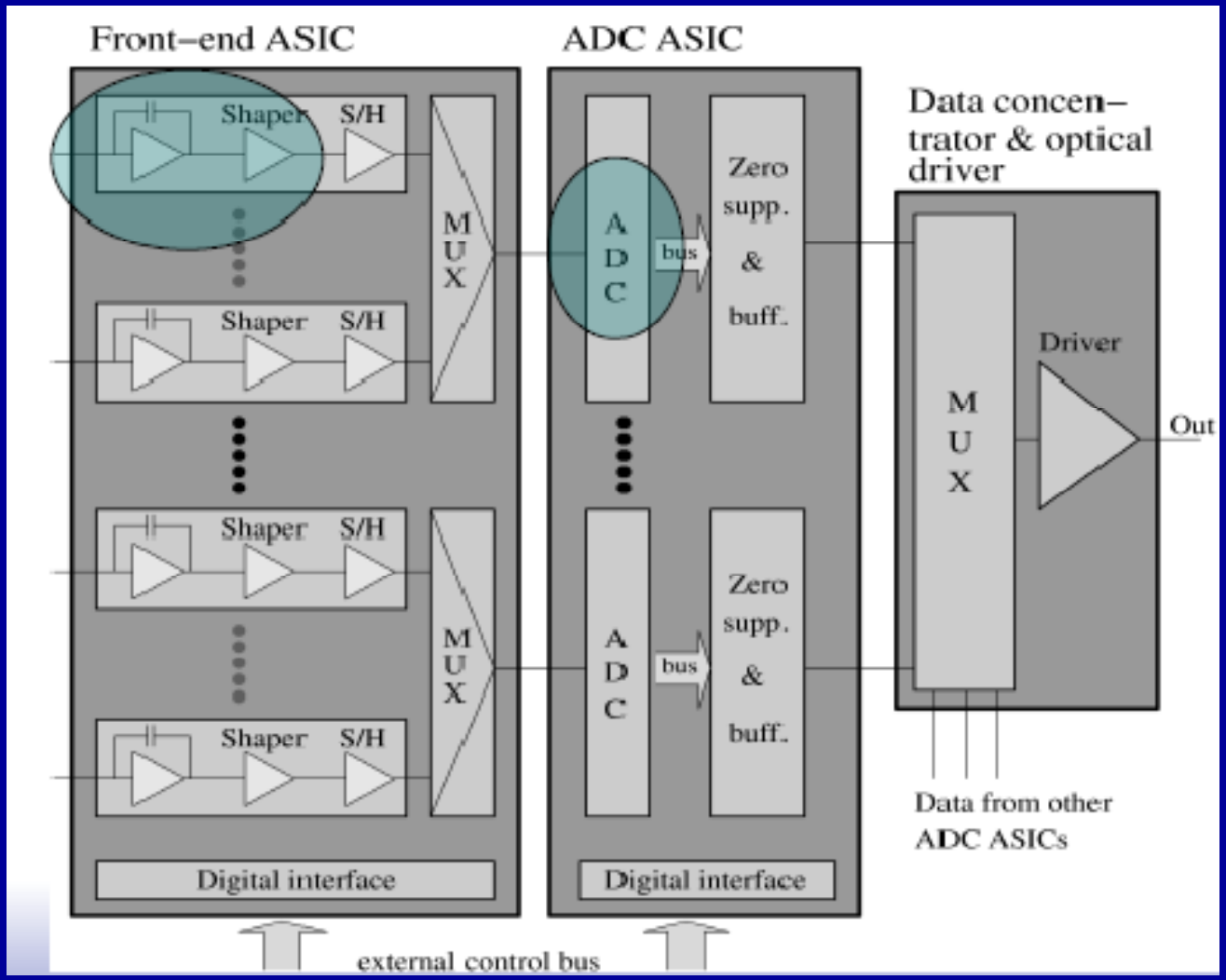




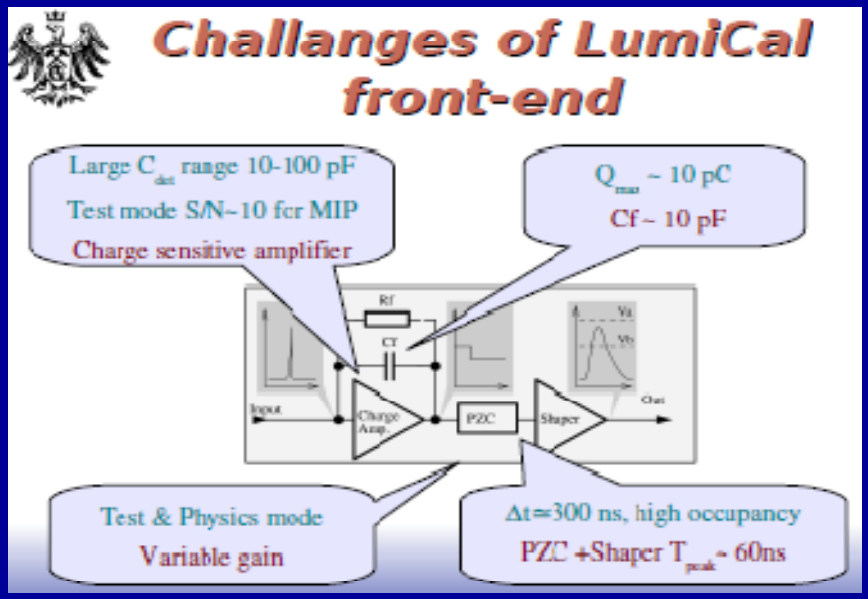
FE Electronics Development

One FE ASIC will contain 32 – 64 channels

One ADC will serve several channels (MC simulations Still not finished)

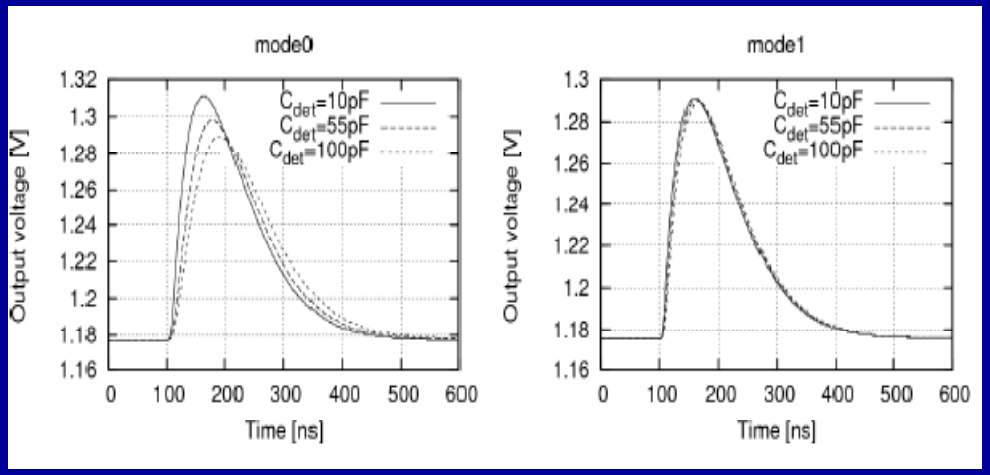


FE Electronics Development

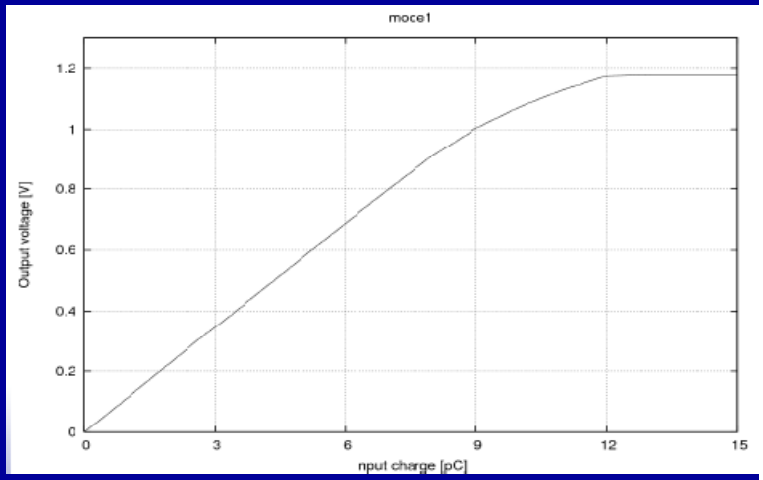


Estimates of signal range and occupancy from MC simulations, translated into design requirements

Response in test- and physics mode for different C_{det}

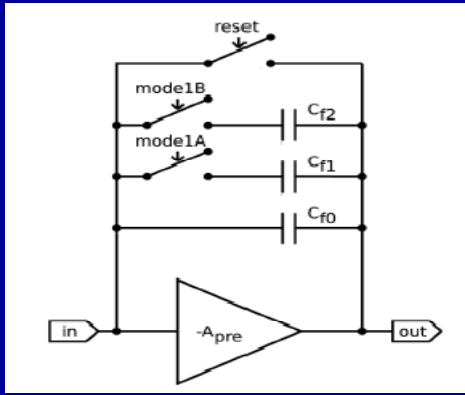


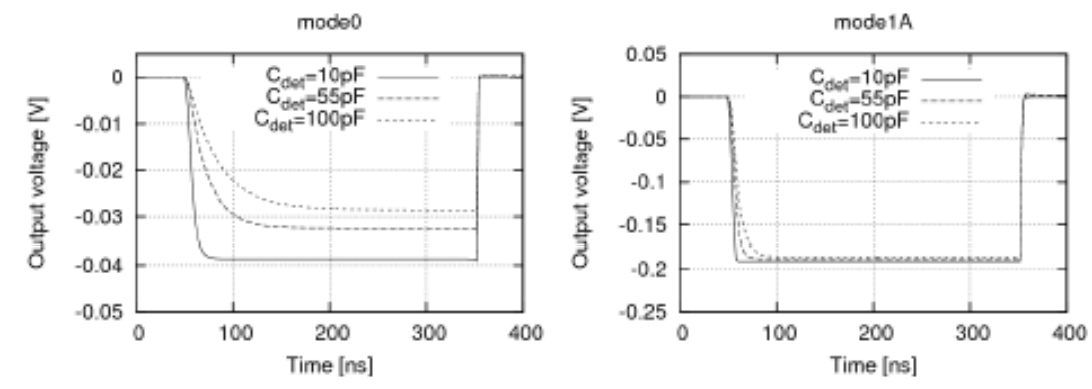
Linearity over the signal size range



FE Electronics Development

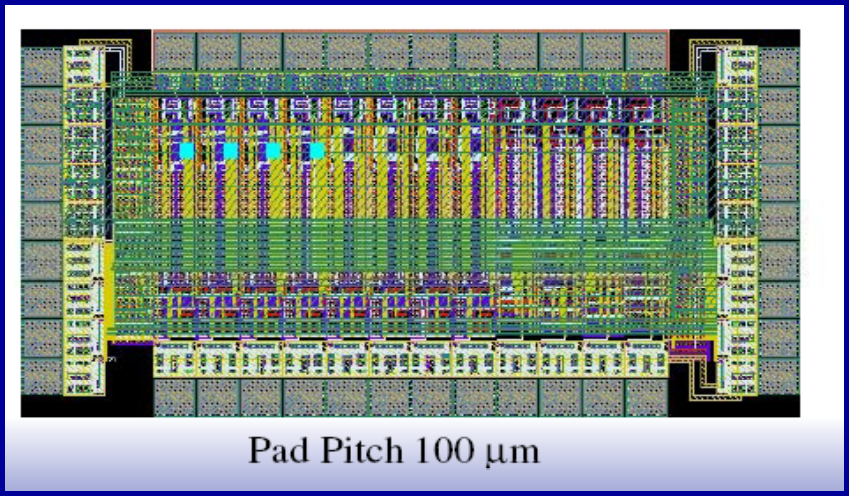
Alternative: Switched reset configuration





Prototype ASIC with 12 channels
Submitted in June 2007

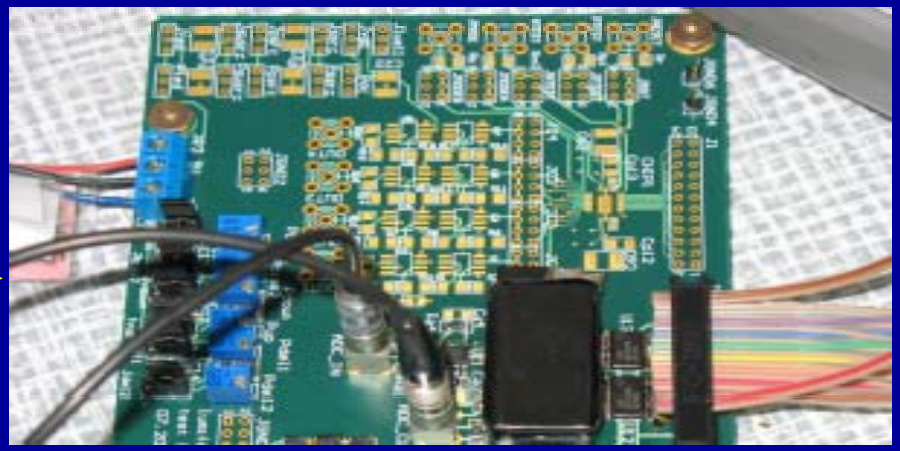
4 channels preamp+PZC+CR-RC
4 channels preamp+PZC+CfRf
4 channels switched reset



FE Electronics Development

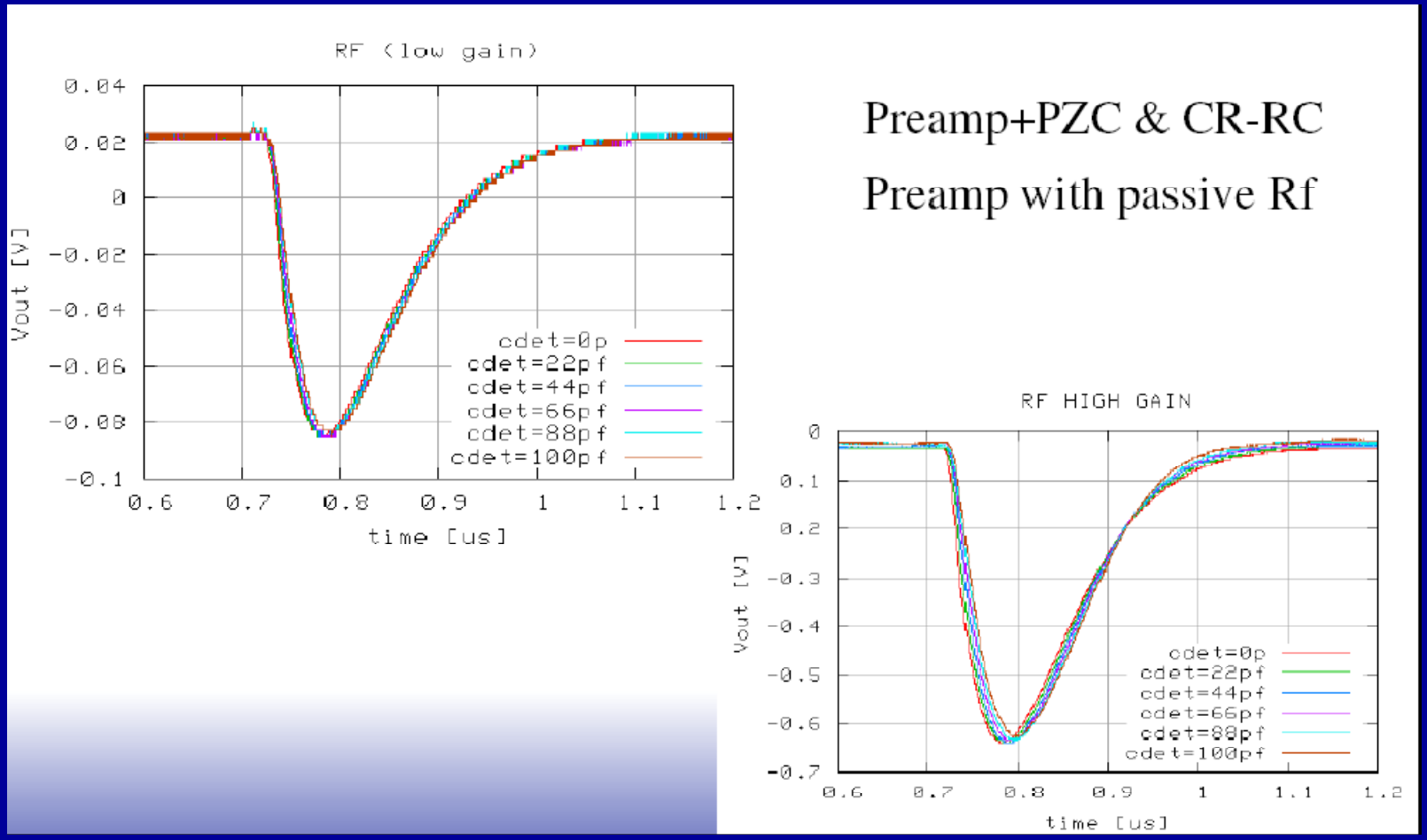
End of Septembre 2007:

- 40 ASICS received
- test PCB designed and produced
- test bench setup under construction
- first results using a generator and an external capacitance



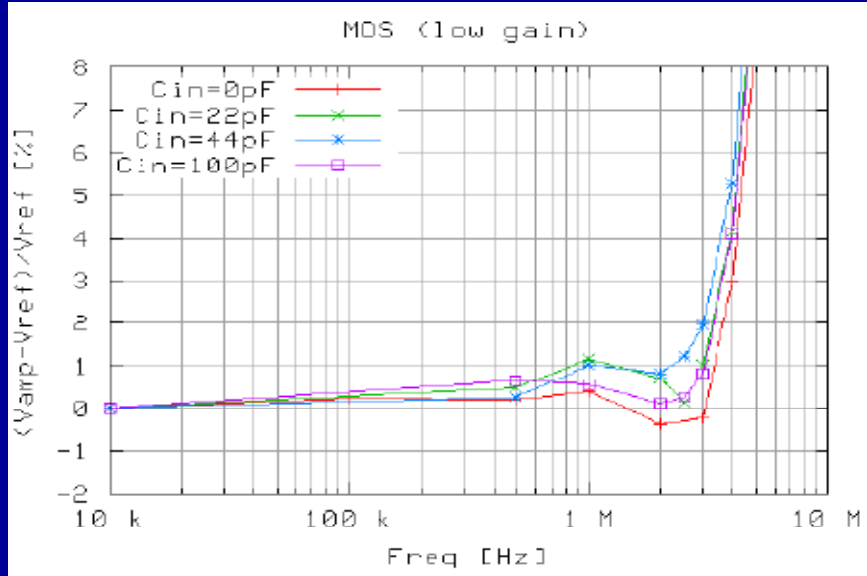
FE Electronics Development

First Results: Output signal shape for different input capacitances



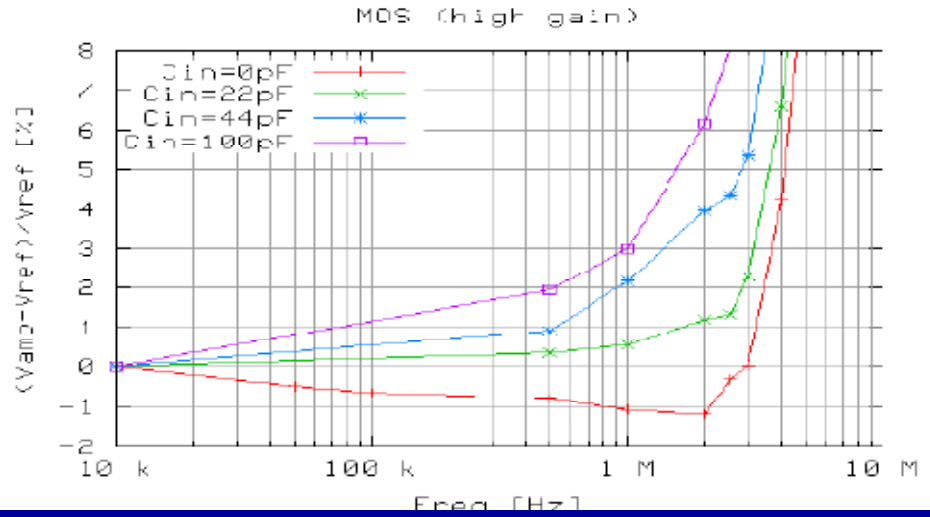
FE Electronics Development

First Results: Output signal vs. input signal frequency



Preamp+PZC & CR-RC

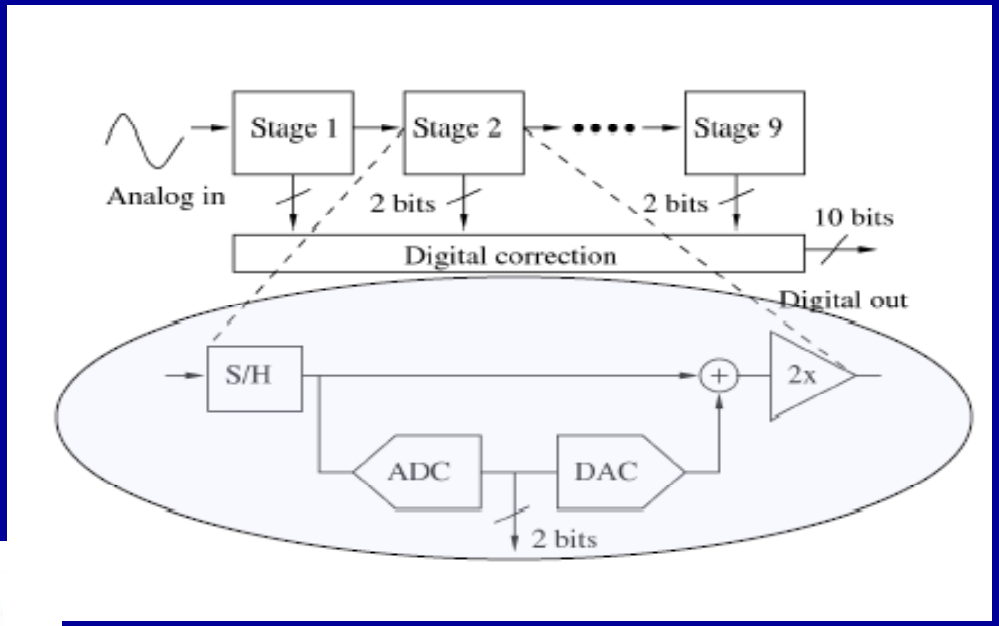
Preamp with active MOS R_f

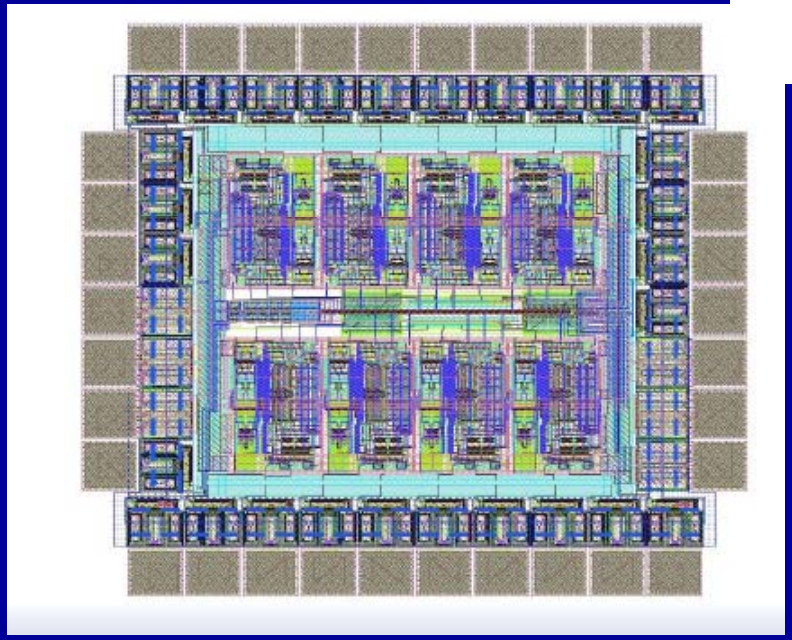


FE Electronics Development

Pipeline ADC concept:

- High throughput
- High robustness
- Power efficient
- Reasonable area





-Prototype ASIC containing 8 pipeline stages submitted in June 2007

- First pieces are alive

- Test Results in December 2007

FE Electronics Development

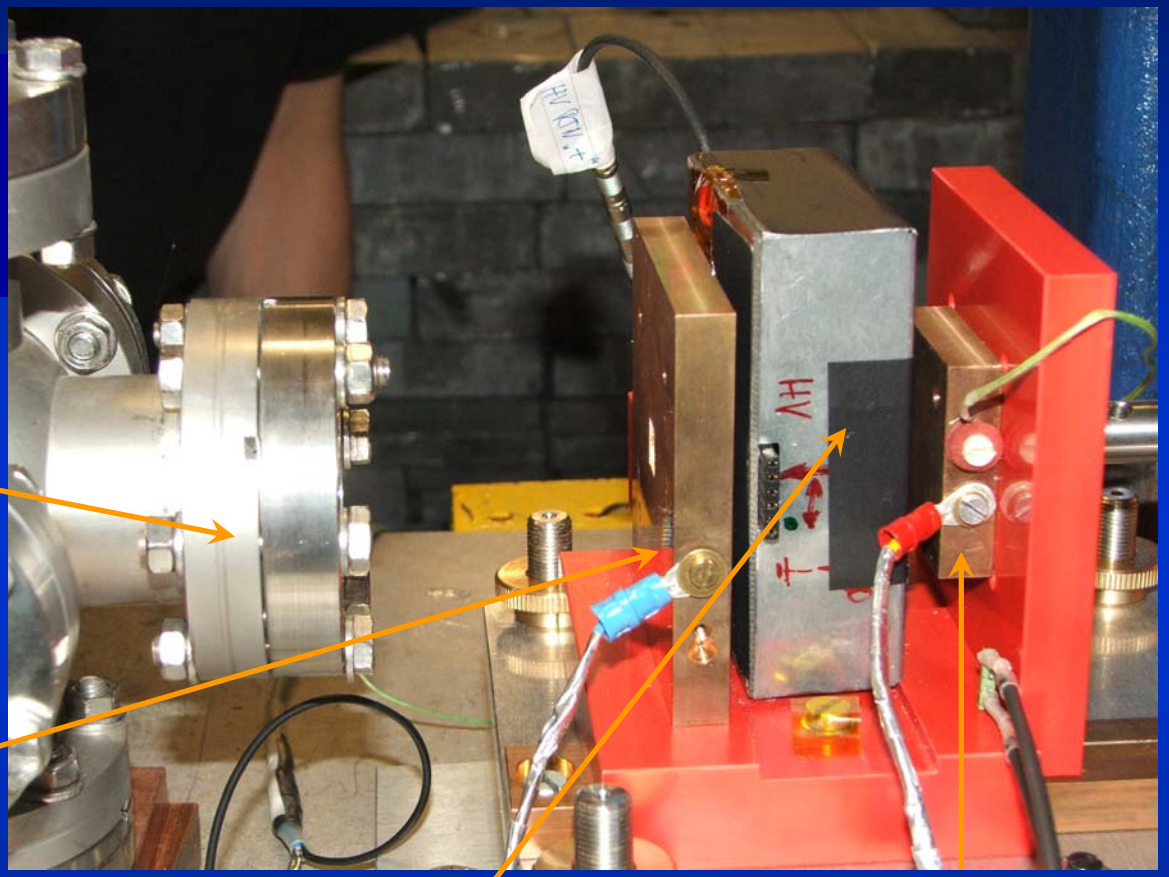
- Design description will be ready in December (EUDET Note)
- Performance results supporting the design
- Improved design beginning 2008

Everything is well on schedule

Test Beam Equipment and sensor tests

Setup used for radiation hardness tests at the SDALINAC accelerator

TU Darmstadt

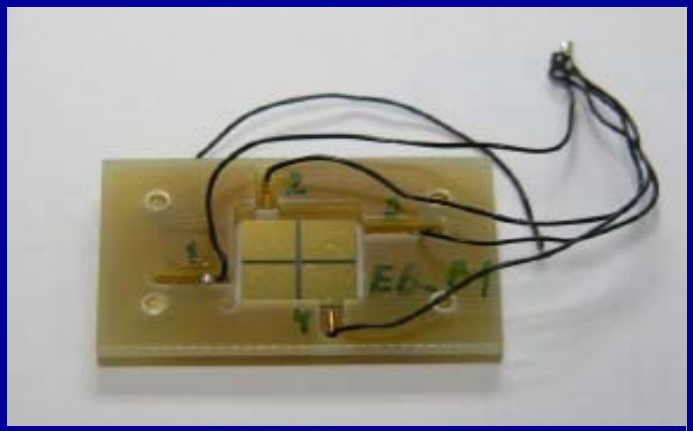


Completed and more comfortable: more efficient use of the beam

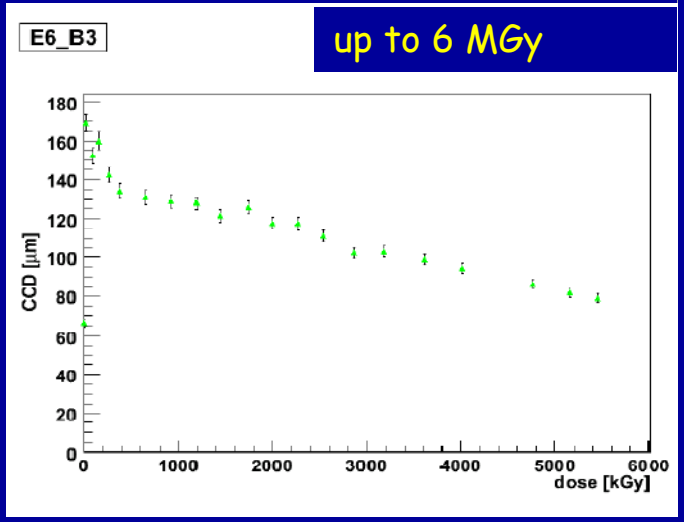
Testbeam

Test Beam 2007

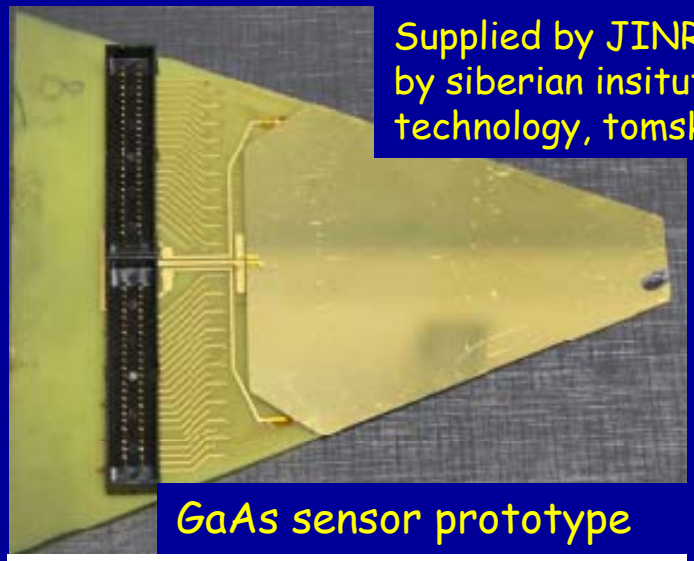
- Completion of Diamond sensor tests
- Test of GaAs sensors
- Test of rad. Hard Si sensors, delivered by BNL and Prague



diamond sensor prototype

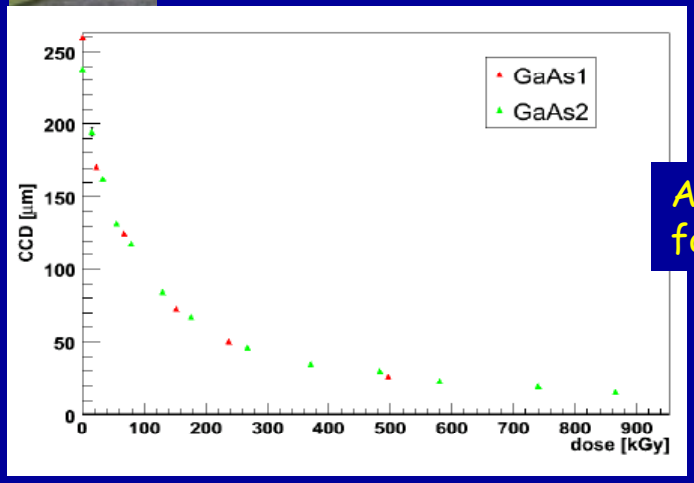


up to 6 MGy



Supplied by JINR, produced by siberian insitute of technology, tomsk

GaAs sensor prototype



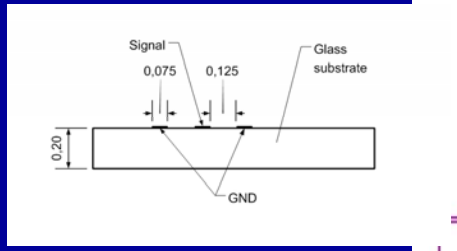
About factor 10

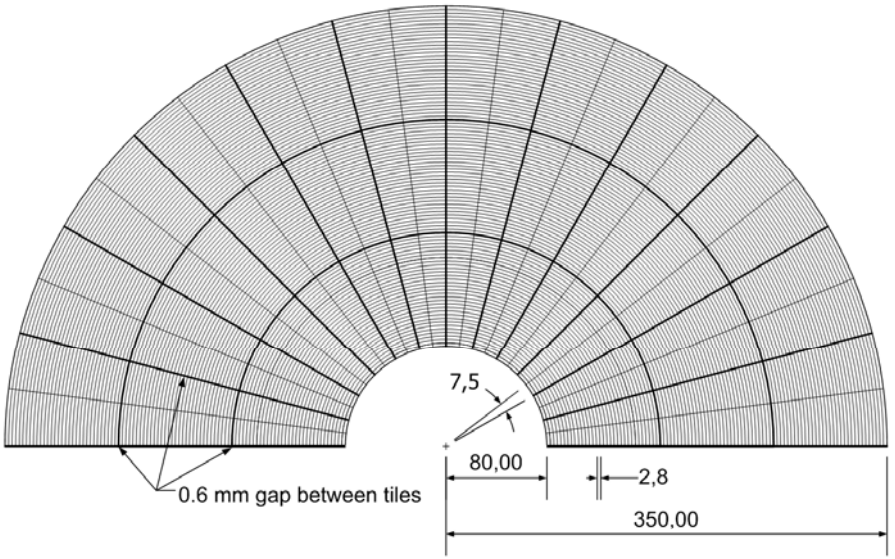
Silicon Sensors for LumiCal

- Sensor prototypes designed
- Contacts to several manufacturers

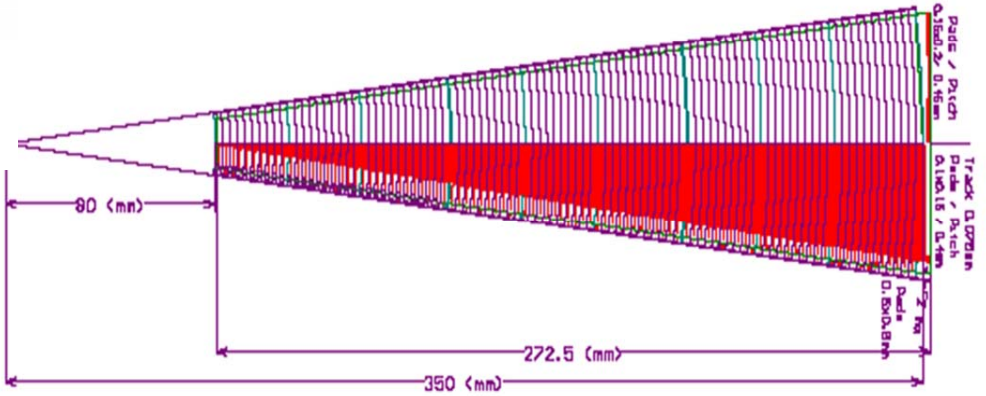
  Tower Semiconductors Israel
  Hamamatsu
  Canbera
  Sintef

- Fan-out design



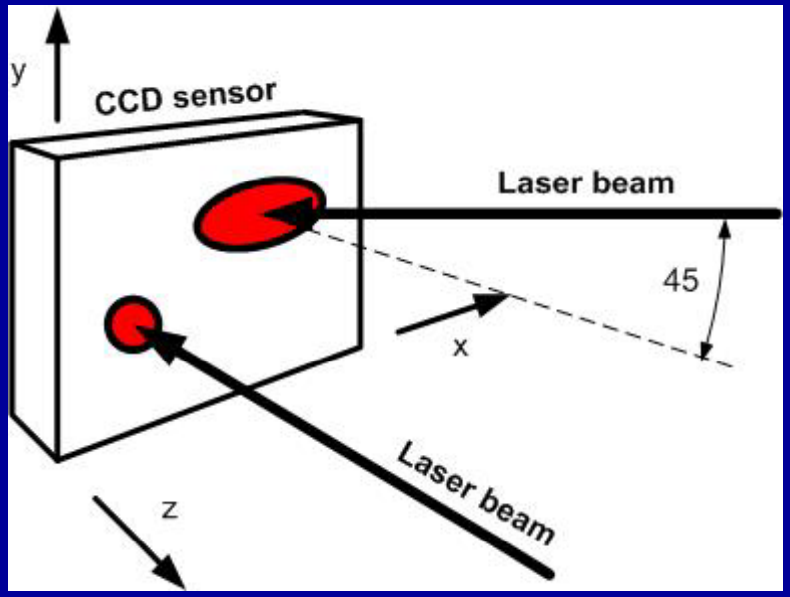


Half plane - 24 sectors, 96 cylinders (36 silicon tiles, 2304 pads)



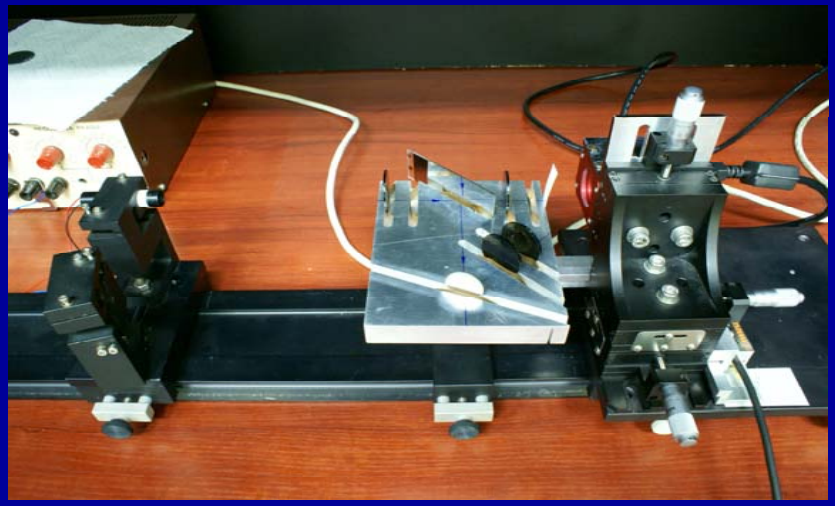
- Sensor Prototypes for tests expected in 2008

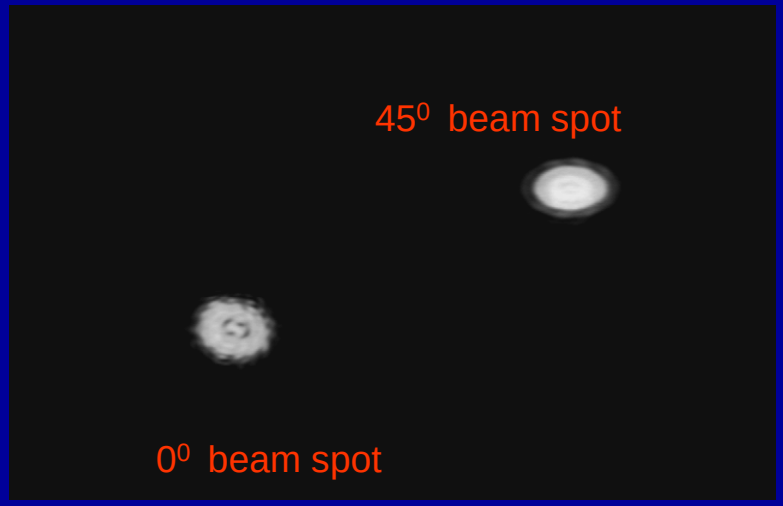
Laser alignment system



Two laser beams (one perpendicular, second with 45˚ angle to the
sensor plane) allows to measure XYZ translation in one sensor

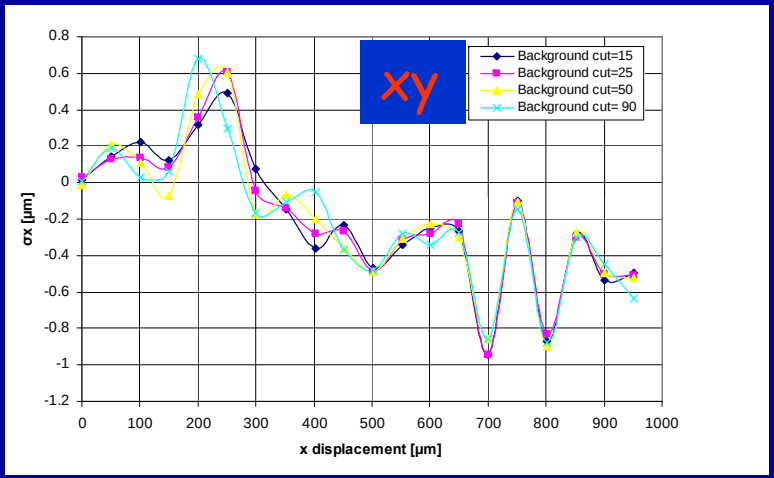
Laser beam spots on the surface of CCD camera (640 x 480 pixels)



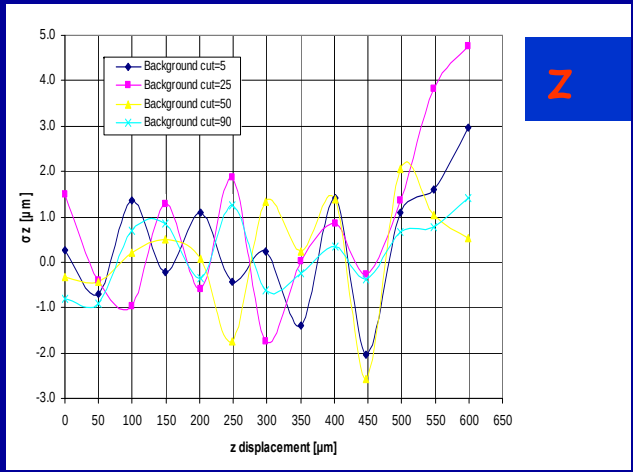


Results and Status

+- 0.5 µm



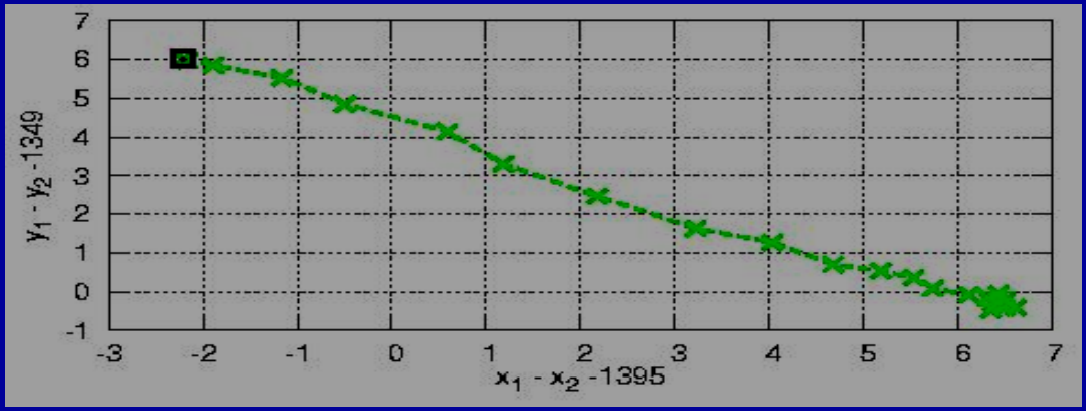
+- 2 µm



Camera has been moved in steps of 50 µm. The distance have been measured with Renishaw RG-24 optical head with the resolution of ±0.1 µm

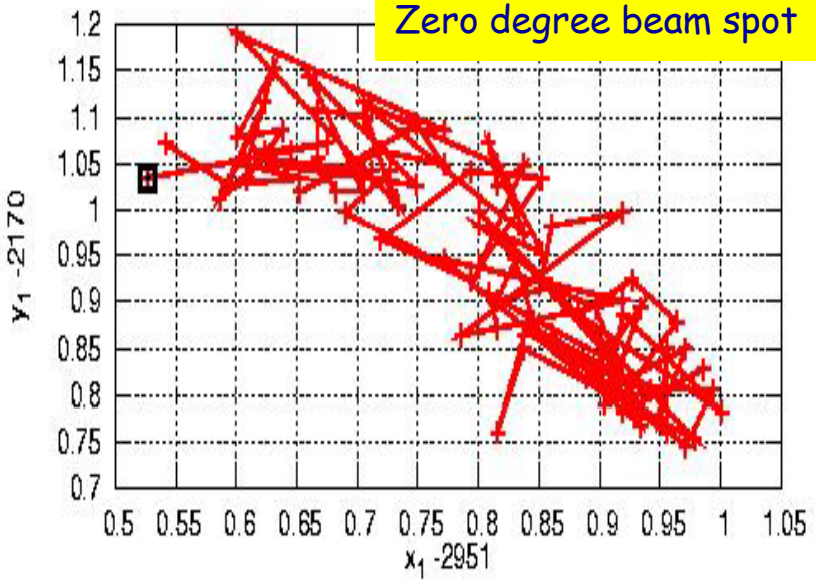
Study of the temperature dependence:

The observed changes are on the level ~ 1 µm/1 ^{0}C

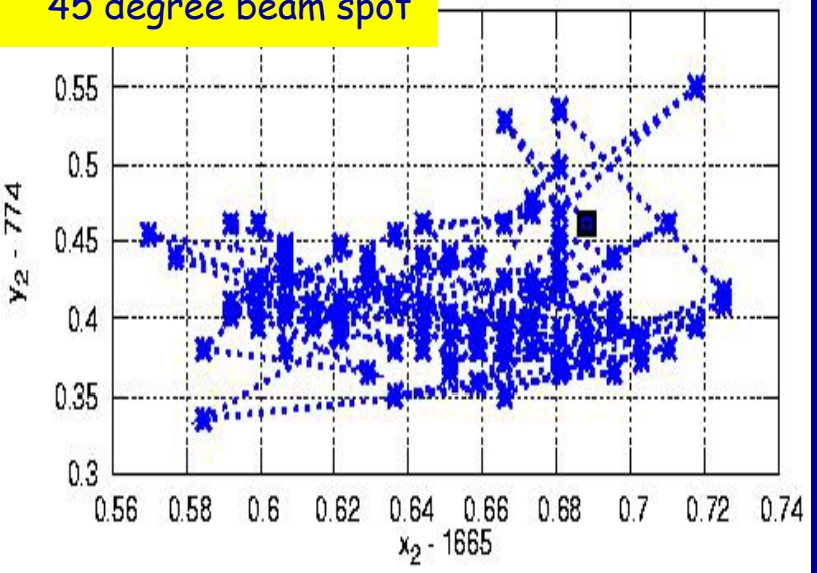


Long-term measurements (~day)

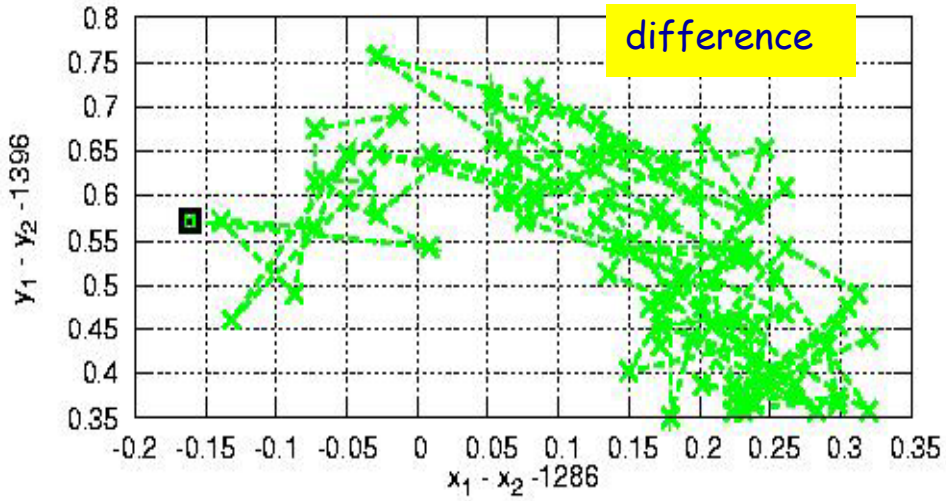
Zero degree beam spot



45 degree beam spot



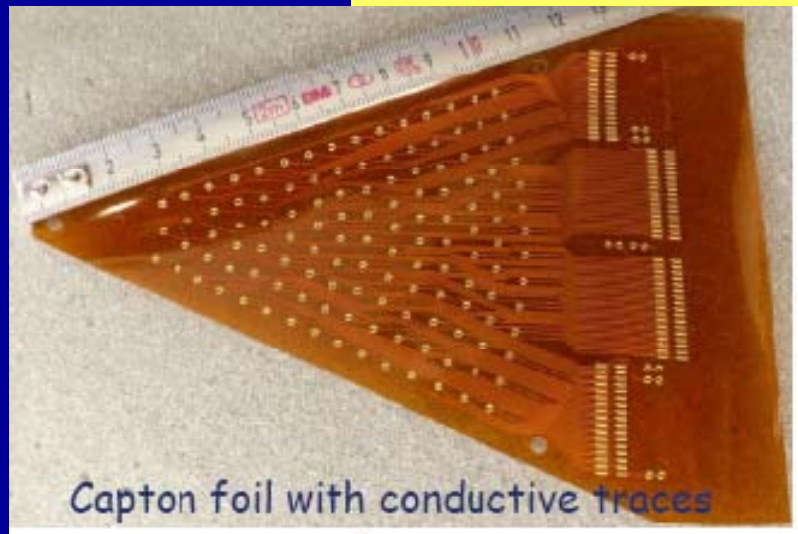
difference



Intrinsic stability
on the level of 0.5 μm

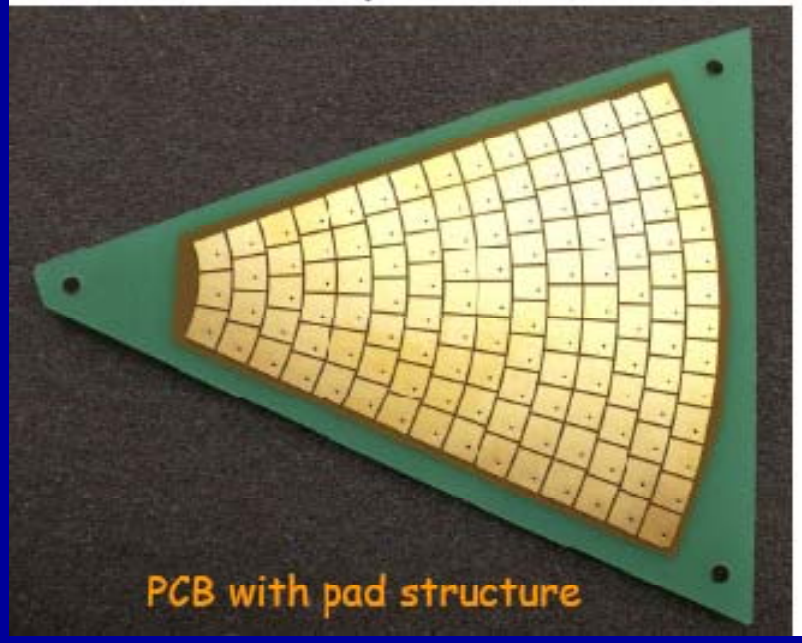
Plan:
-mineaturised laser and sensor heads, dedicated electronics
-more realistic and larger scale setup

Fan-out for a sensor plane



Capton foil with conductive traces

+



PCB with pad structure

Readout structure prototype with metal pads bonded to capton readout

Plans and Summary

- Laboratory infrastructure is created/improved/completed
- Testbenches for FE ASICS prepared
- First FE ASICS are produced, tests started
- Testbeam equipment for rad. hard tests completed and used
- Laser positioning system studies are ongoing
- fist steps towardss a fully instrumented 'ultrathin' sensor plane

VFCAL is 'on schedule'