IN2P3

Omega

LAL LURE IPN Orsay

FEE TASK STATUS REPORT

EUDET annual meeting

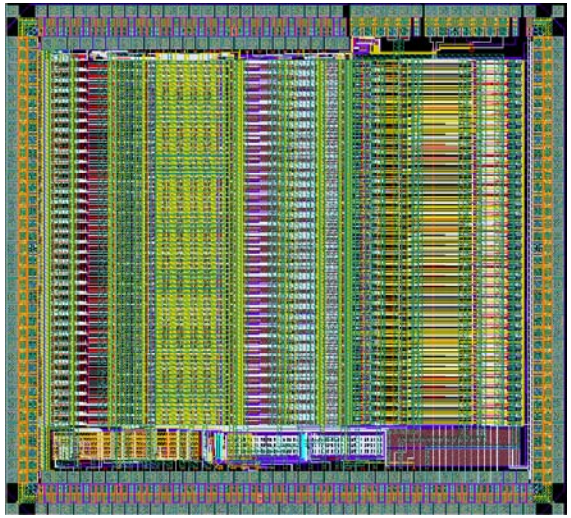
EUDET Calorimeter for ILC

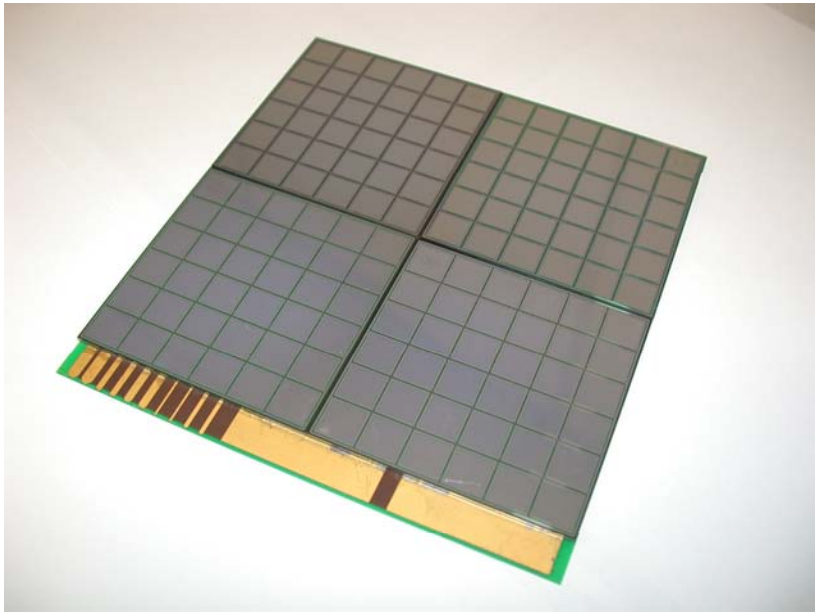
16 October, 2007

Orsay MicroElectronic Group Associated

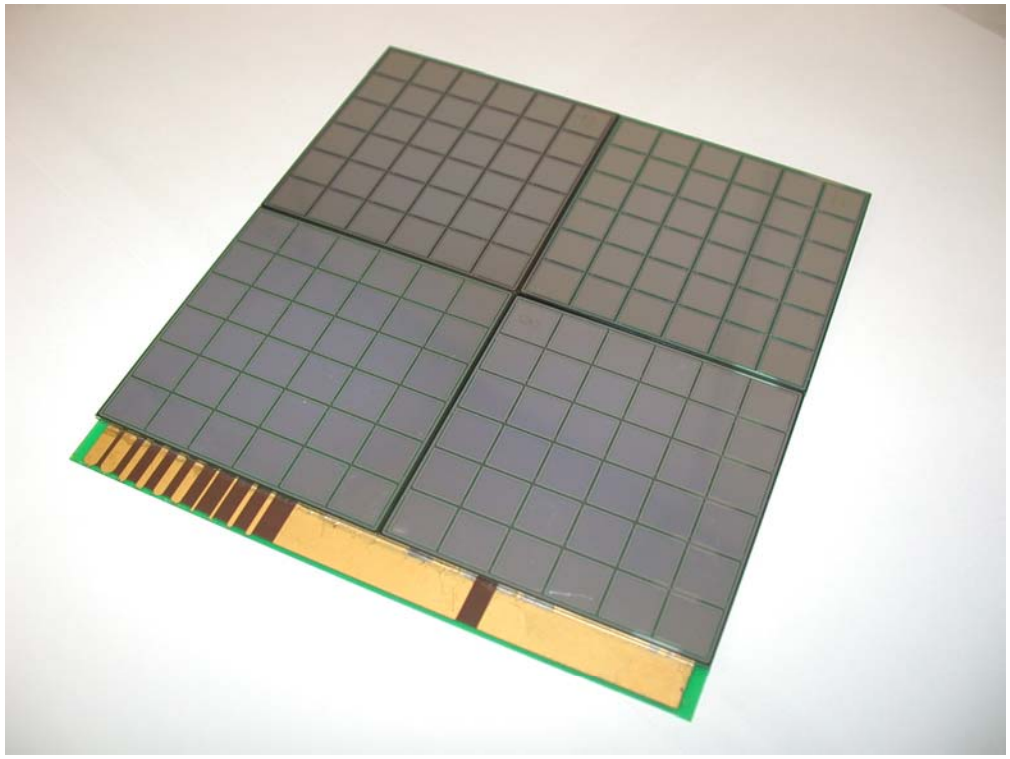
Plan

- PROBLEMATIC AND GOALS
- CHIP PRESENTATION
- SOME RESULTS

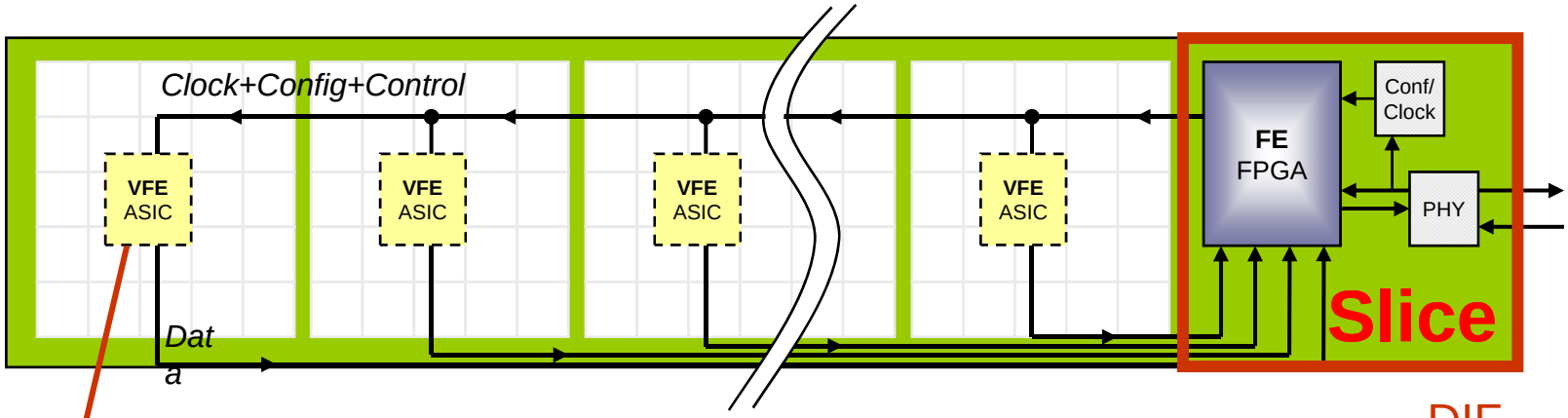




PROBLEMATIC AND GOALS



Common DAQ

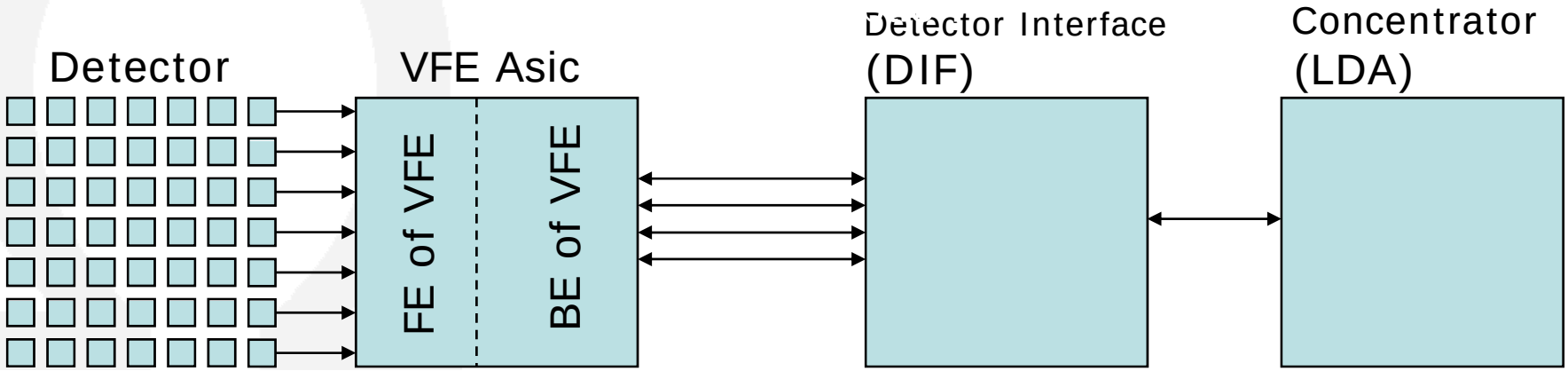


DIF

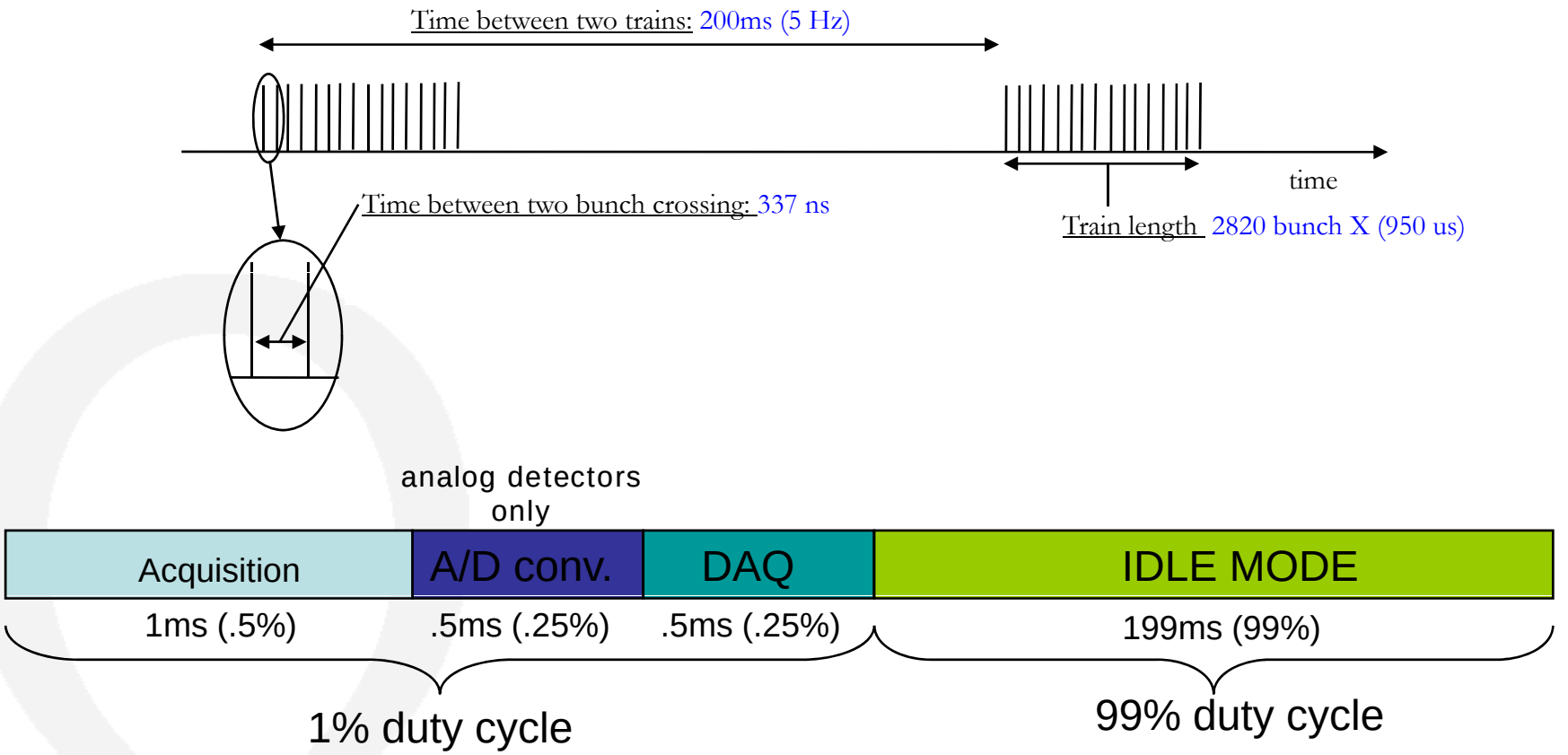
- Timing is the same for all detectors
- Nu
-Ou
→ E

tors

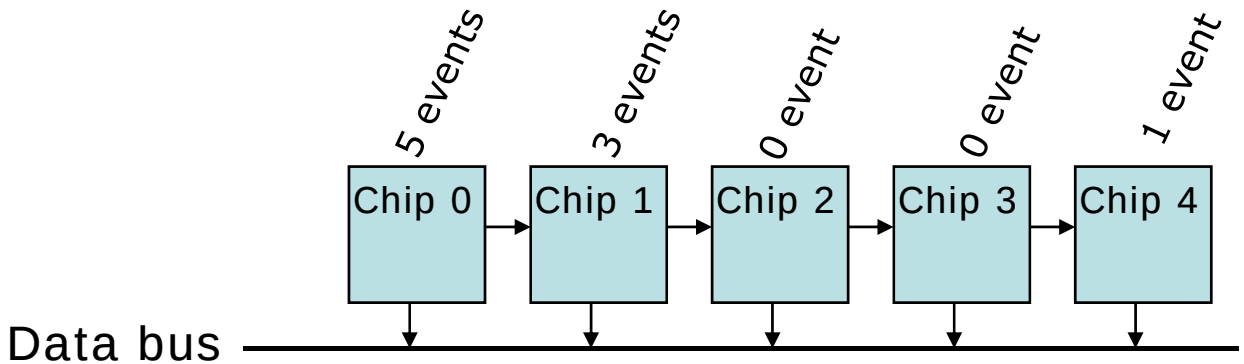
Very high integration
No external components → system on chip
No active cooling → power pulsing for ultra low

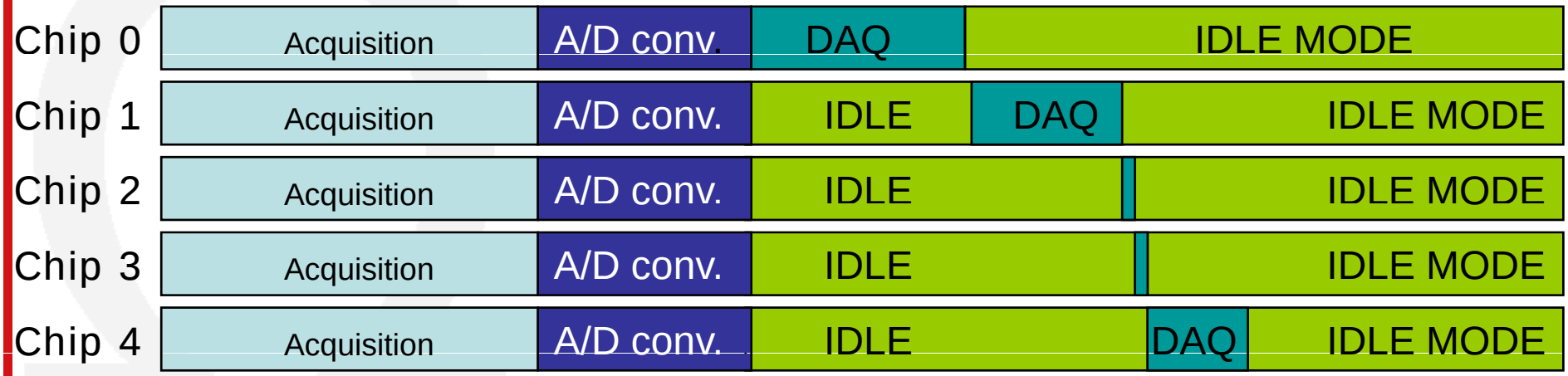


Time considerations

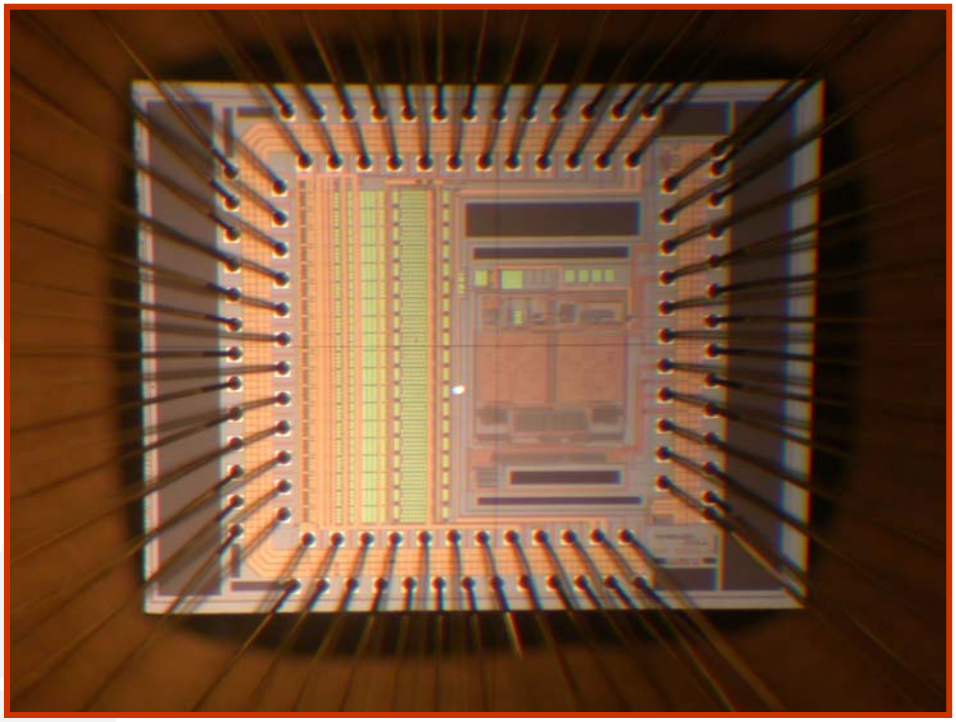


Read out : token ring

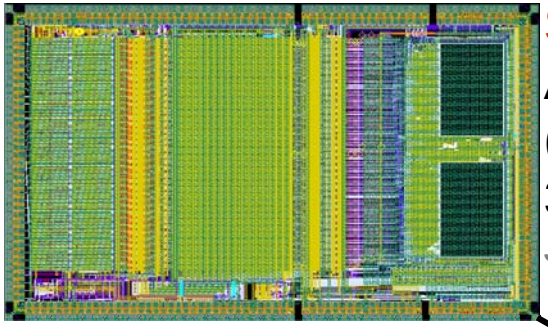




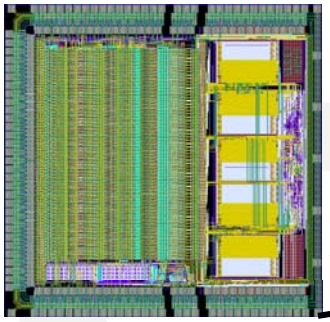
CHIP PRESENTATIONS



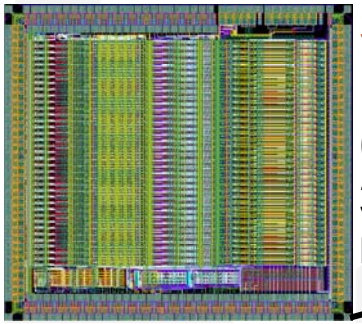
The front-end ASICs : the ROC chips



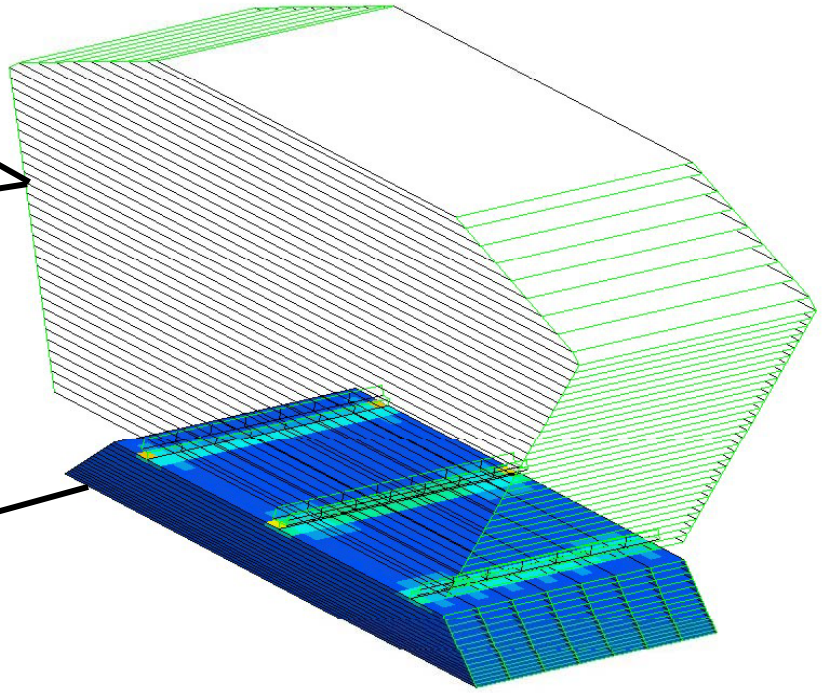
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07



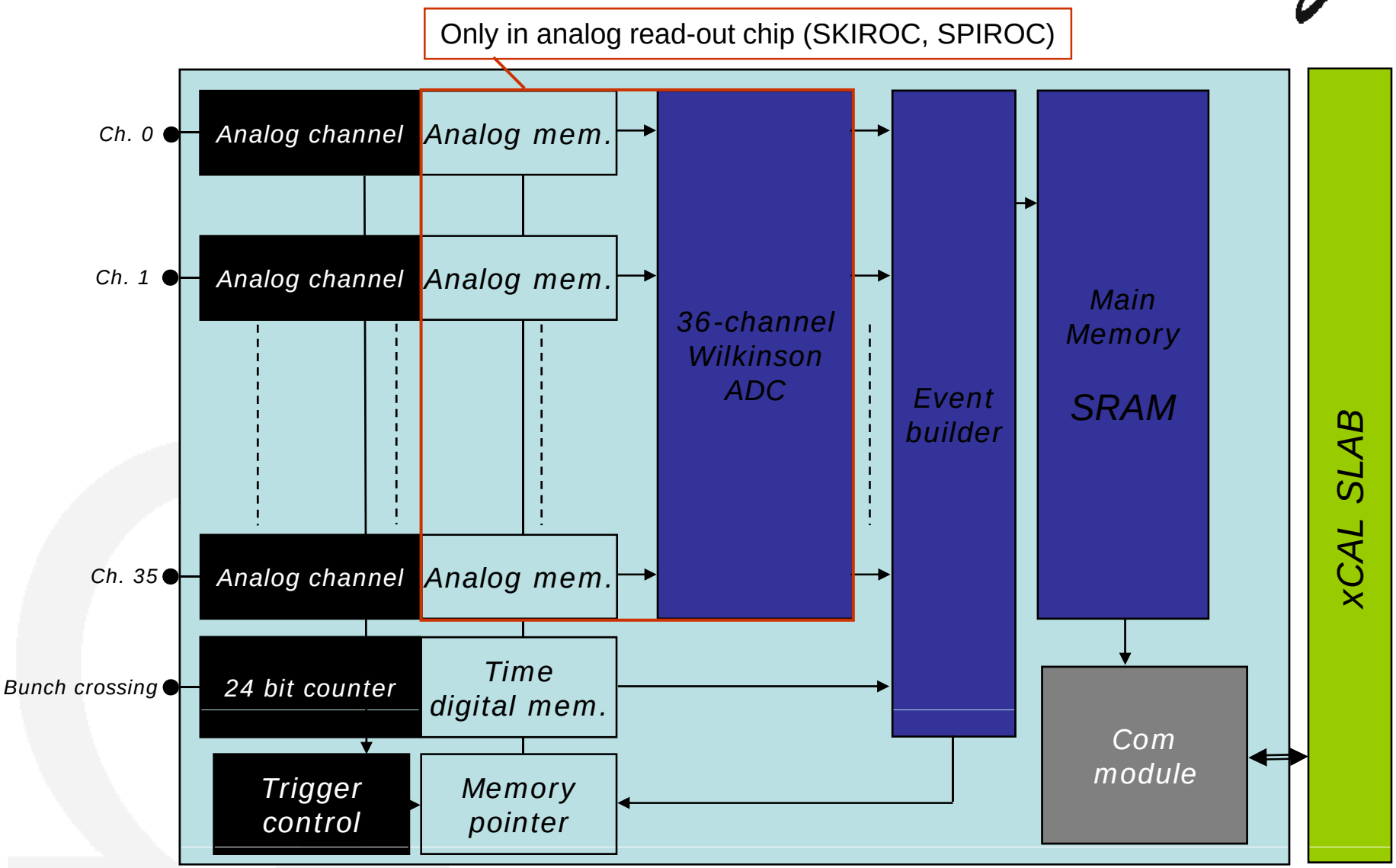
HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



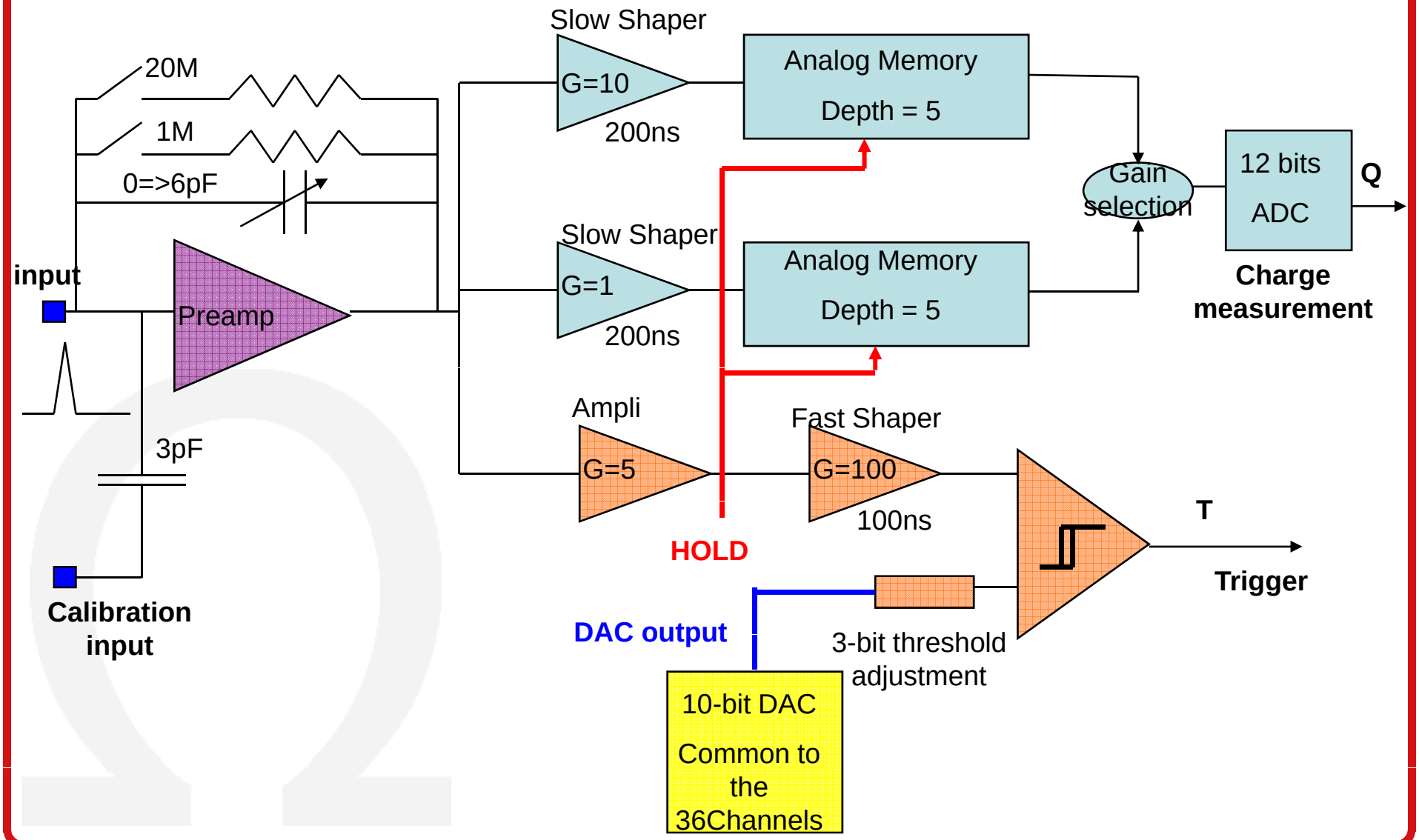
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06



Block scheme of a ROC chip



One analogue channel (SKIROC)

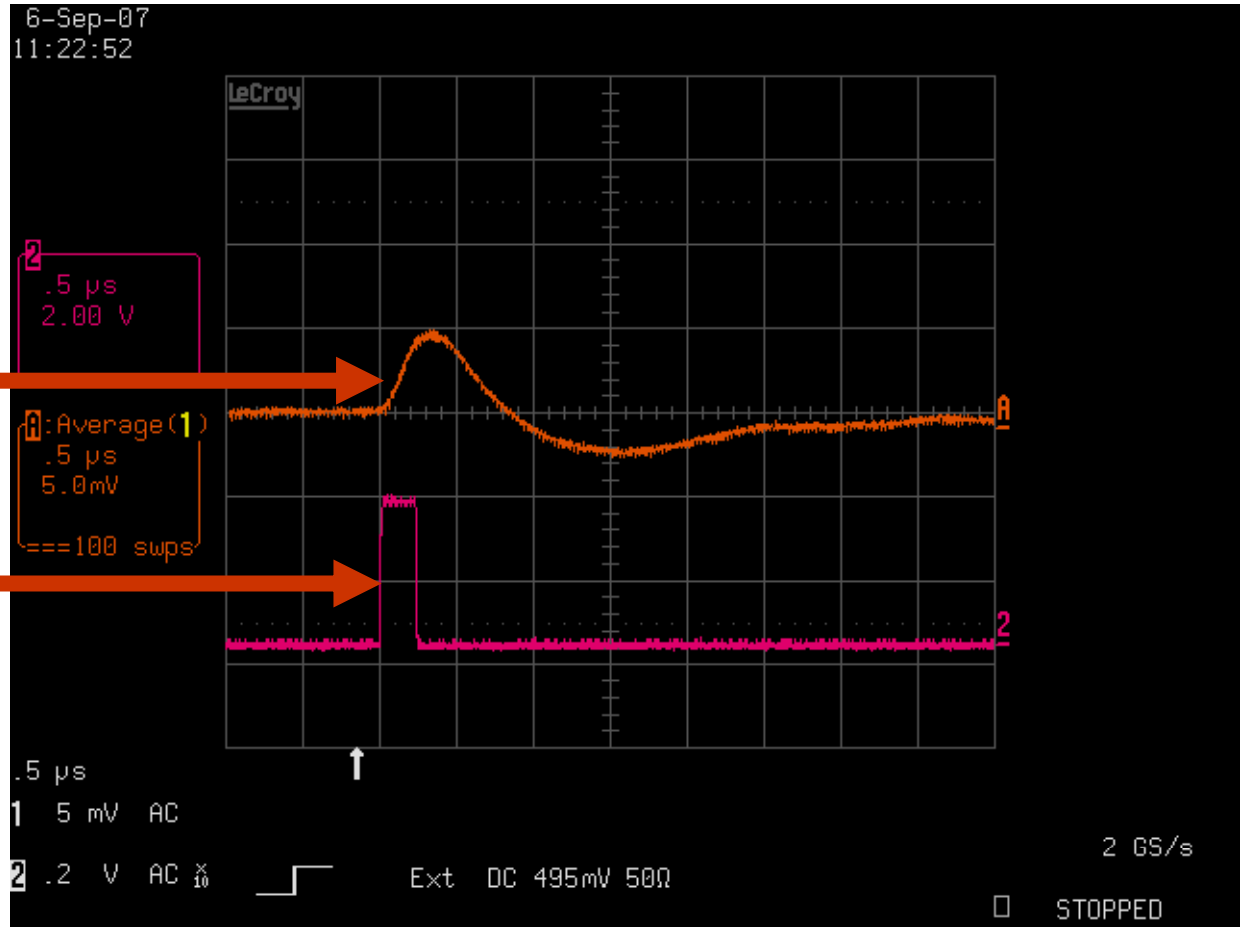


SOME RESULTS

Charge measurement and self-trigger

One MIP measurement (injected charge) in SKIROC

1 MIP in SKIROC



Charge measurement

Self trigger

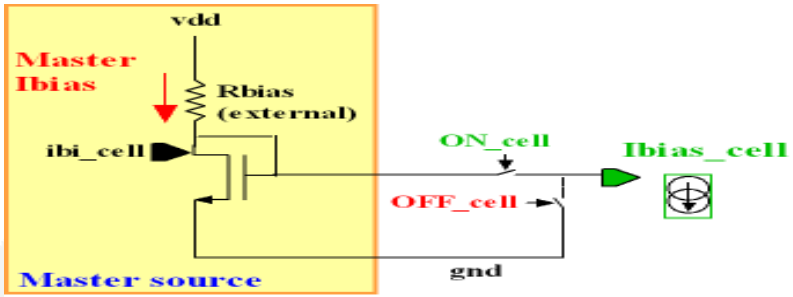
POWER PULSING: Hardroc results

Maximum power available:

- 10 µW/ channel with 0.5% duty cycle

=> 640µW/3.5V=**180 µA** for the entire chip

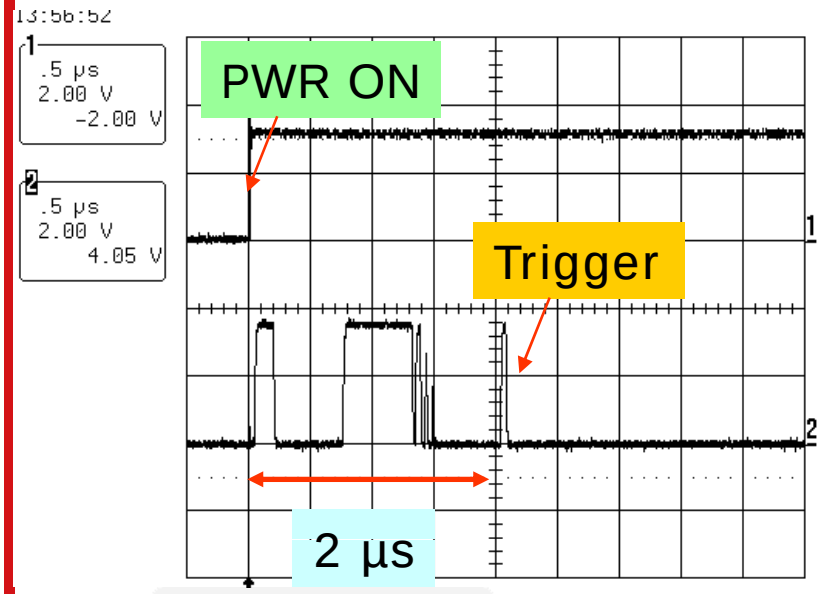
- **OFF**= Ibias _cell switched off during interbunch:

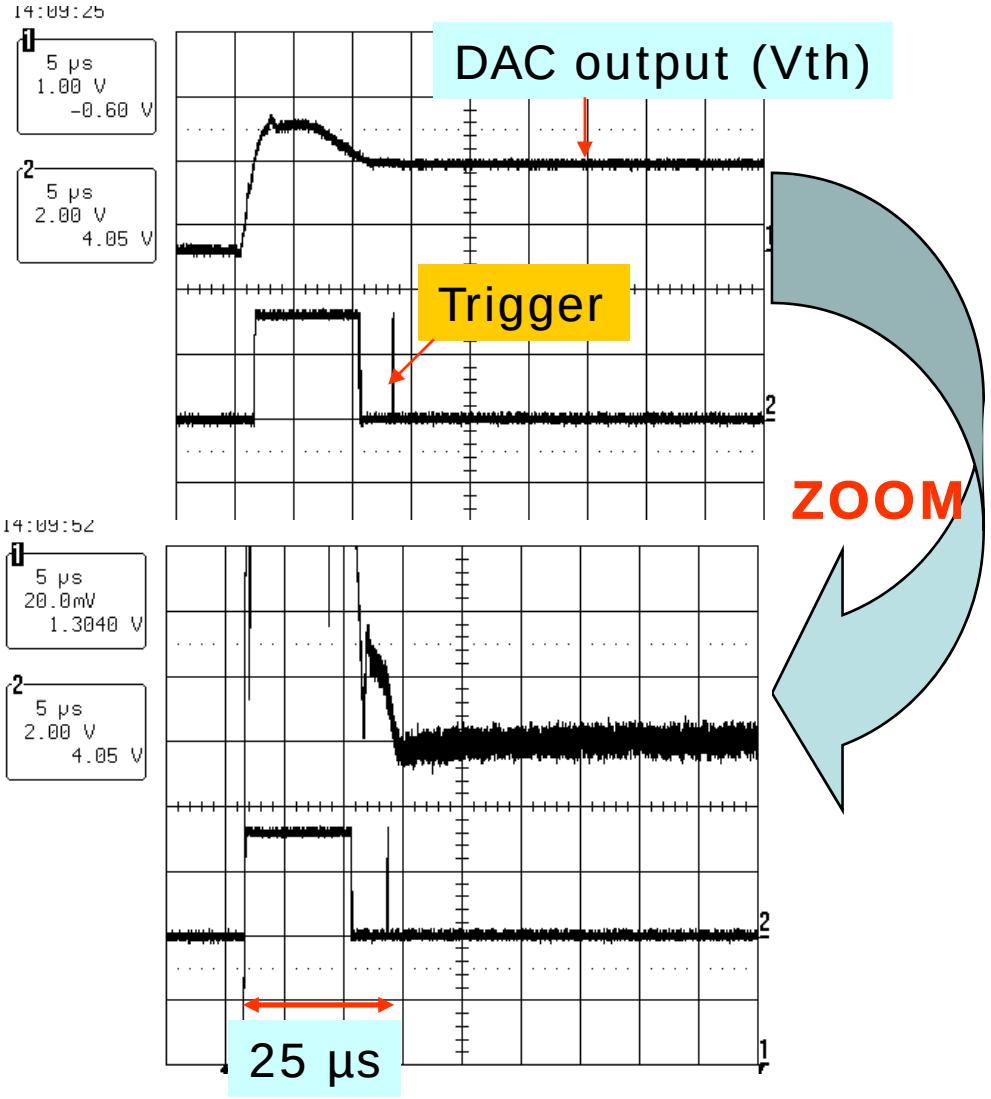


- BUT a few forgotten switches…
  - Bandgap, some reference voltages not power pulsed
- **Easy to fix in the production version**

	ON	OFF
Vdd_pad	0	
Vdd_pa	5.8 mA	5.6 µA
Vdd_fsb	4.9 mA	65 µA
Vdd_d0	2.8 mA	78 µA
Vdd_d1	2.7 mA	0
Vddd+ vddd2	3.3mA	200µA + 0 (Clk OFF)
Vdd_dac	0.77 mA	218 µA
Vdd_bandgap	5.05 mA	2.73 mA
Total (noPP)	25.3 mA	3.2mA
Total with 0.5% PP	125 µA	0 hopefully

Power pulsing: HARDROC settling time

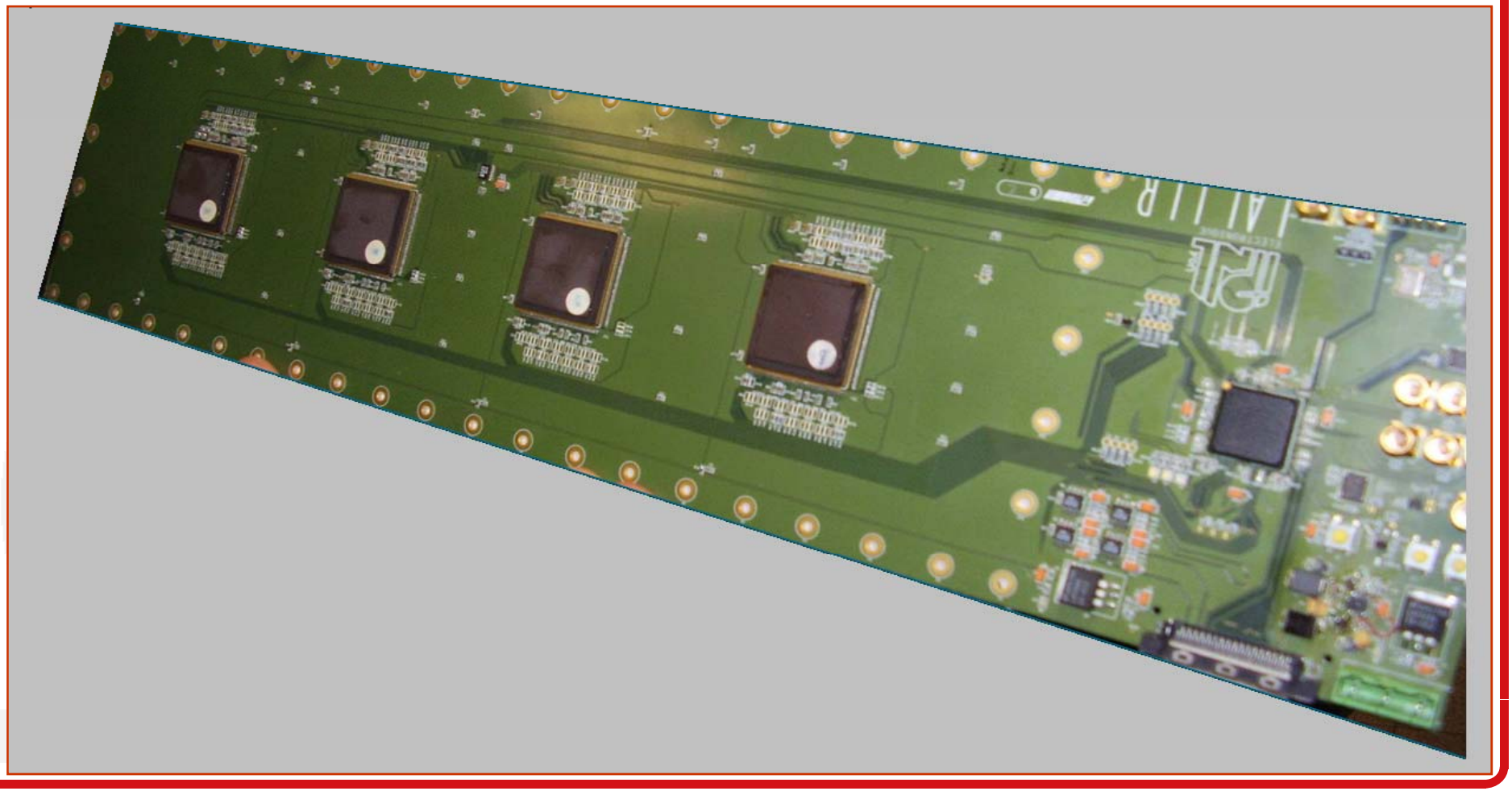




- PWR ON: ILC like (1ms,199ms)
- All decoupling capacitors removed
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - Injection of 100fC, Threshold= 30fC
  - => **Awake time= 2 µs**
- Power pulsing of the DAC:
  - **25 µs (slew rate limited)**

Daisy chain measurement

- First measurement of four chips on the DHCAL prototype PCB (IPNL, LLR, LAL)



Conclusion

- The three calorimeters have a FE ASIC
  - HARDROC for the DHCAL
  - SPIROC for the AHCAL
  - SKIROC for the ECAL
- Some crucial points have been validated
  - Digital daisy-chain
  - Power Pulsing
  - Stand-alone capability (ne external component)
- The production is foreseen mid'08
  - Very agressive schedule
  - Still in the EUDET milestones