

# Front-end electronics for the LPTPC

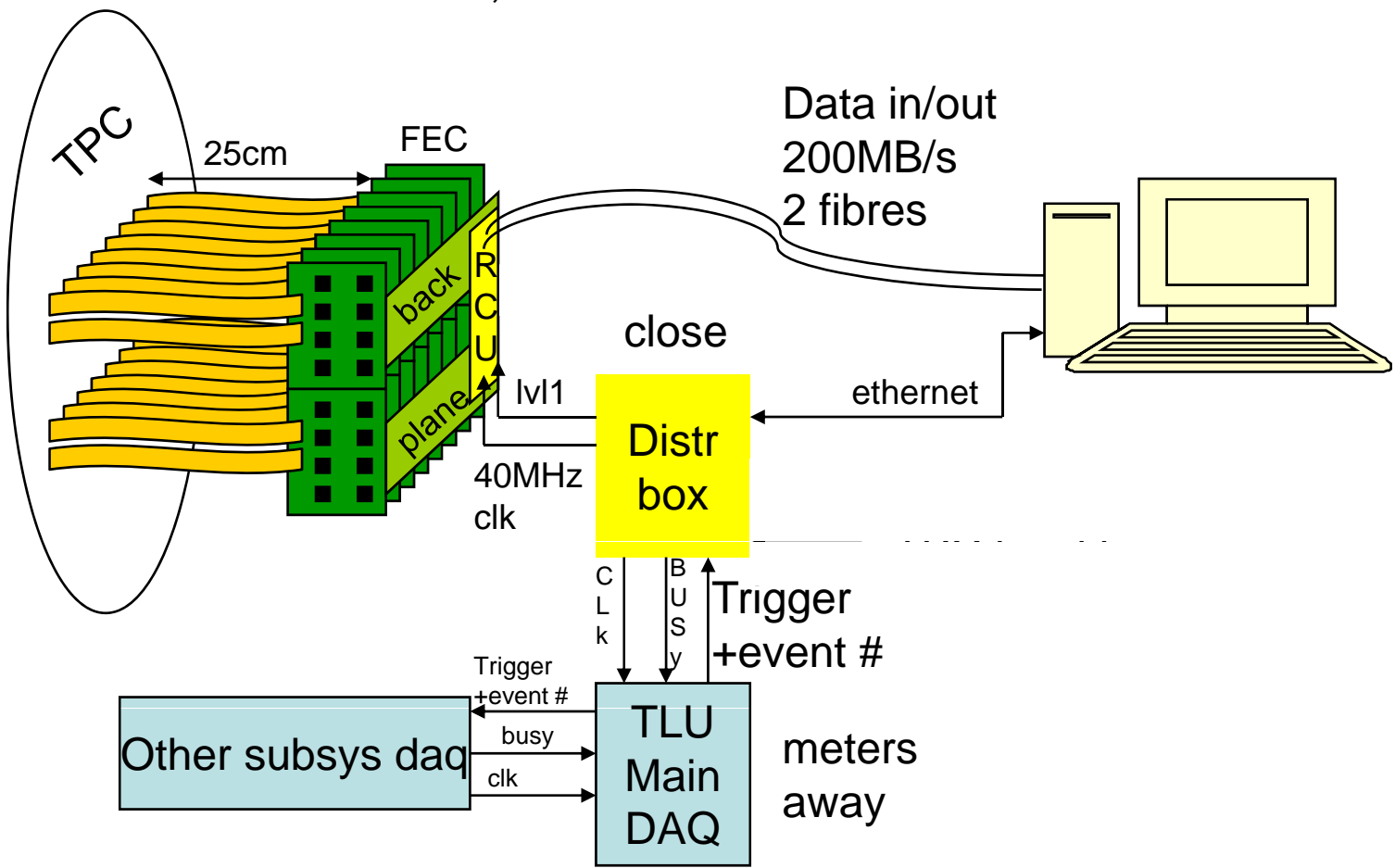
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## Outline of the talk:

- System lay out
- Mechanics for the front-end electronics
- End-cap and panels
- Connectors and cables
- Front-end card; modifications
- Preamplifier (PCA16); specification and status
- Control of the PCA16; FPGA/switches
- ALTRO; status

If we run together with other subsystems

2048ch, 16 FEC



# Mechanics for the front-end electronics

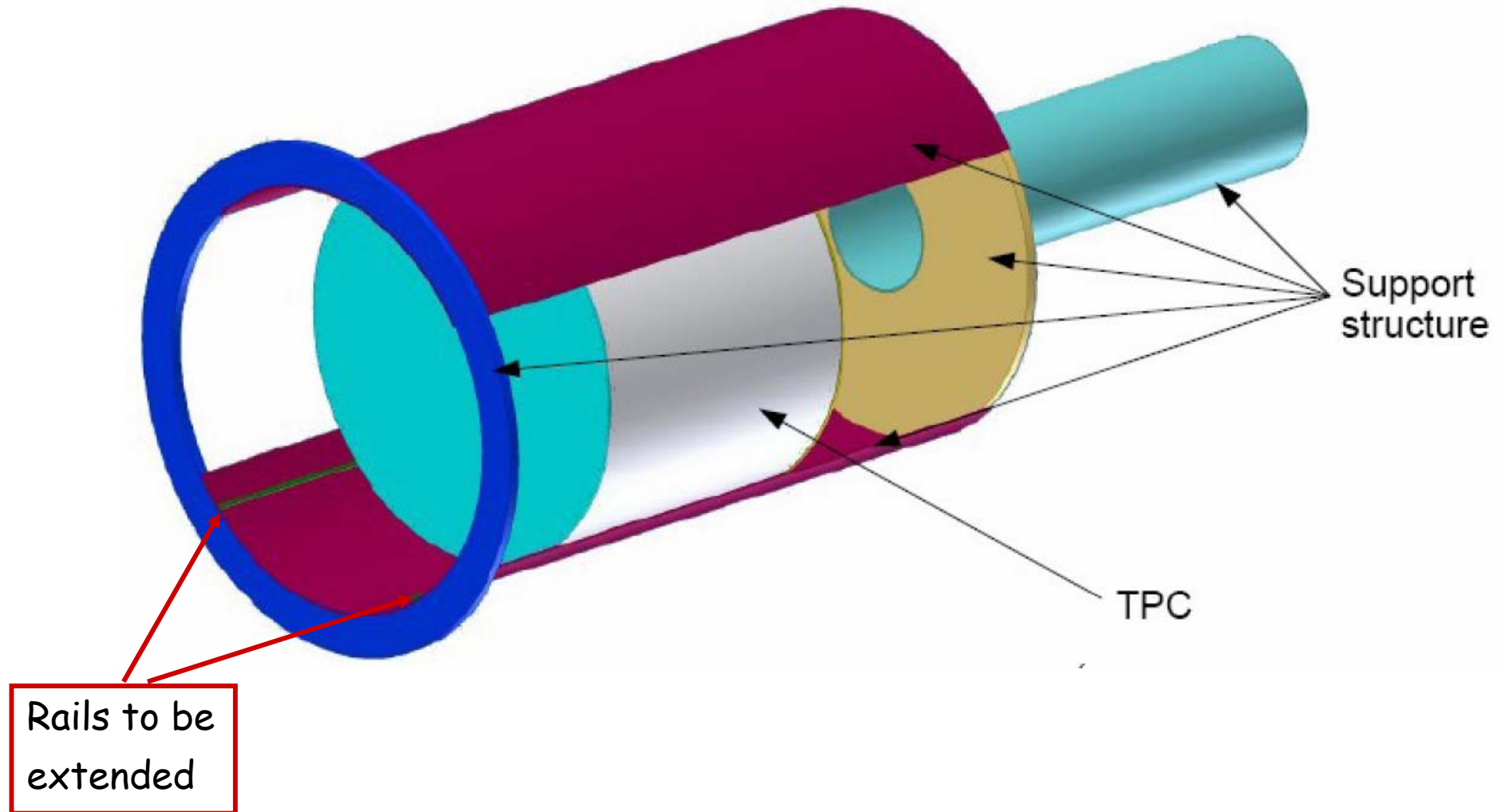
## Constraints:

- The electronics crate has to be fixed to the field cage to avoid that cables are pulled out by accident
- The short length of the cables means that the electronics will stick into the magnet  $\Rightarrow$  the TPC and the electronics have to move as one unit
- The TPC should be rotatable by up to  $90^\circ \Rightarrow$  the electronics must rotate together with the TPC

## Proposal:

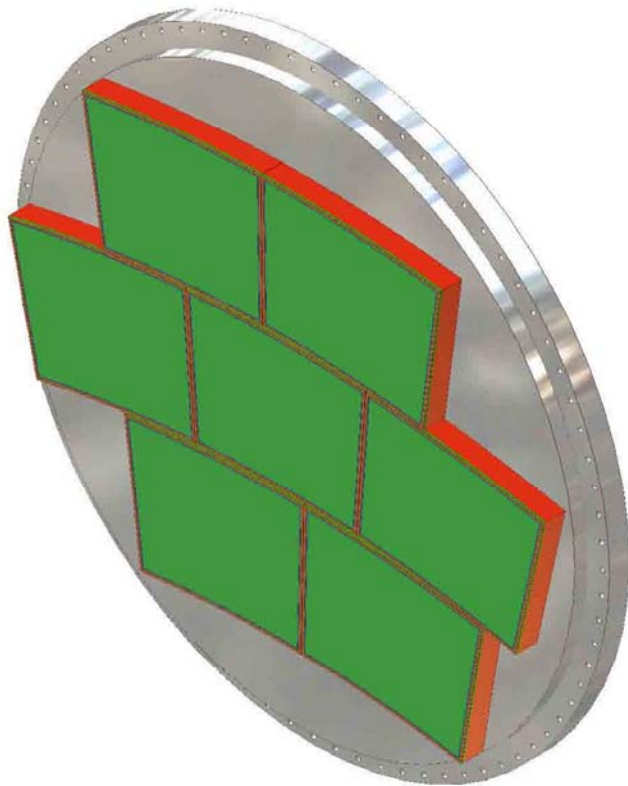
- Extend the rails on which the TPC rests in the magnet such that the TPC and the electronics can rest on the rails outside the magnet during assembly
- Fix the electronics crate to the end flange of the field cage such that it moves and rotates on the rails as one unit

# Mechanics for the front-end electronics

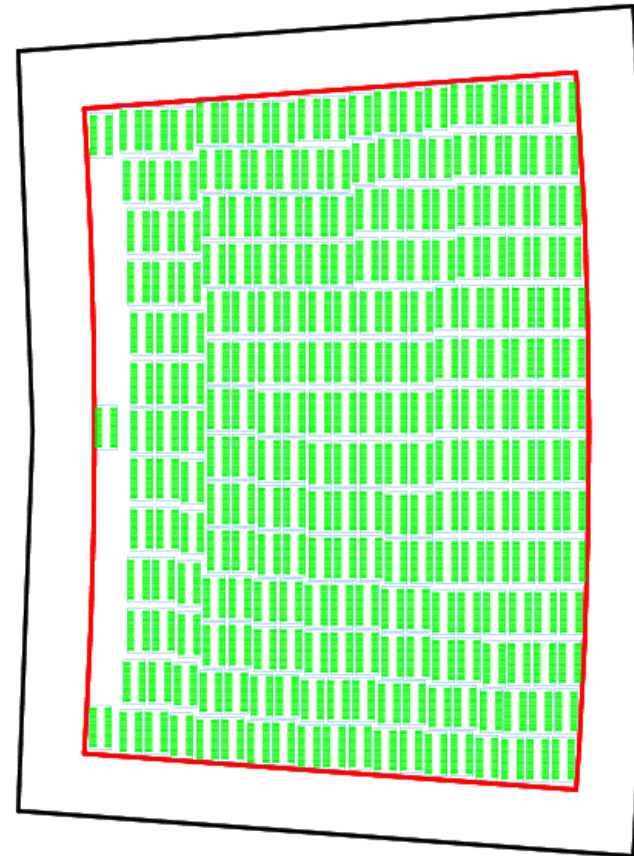


# End-plate and panels

Endplate with panels



Panel with connectors



# Connectors and cables

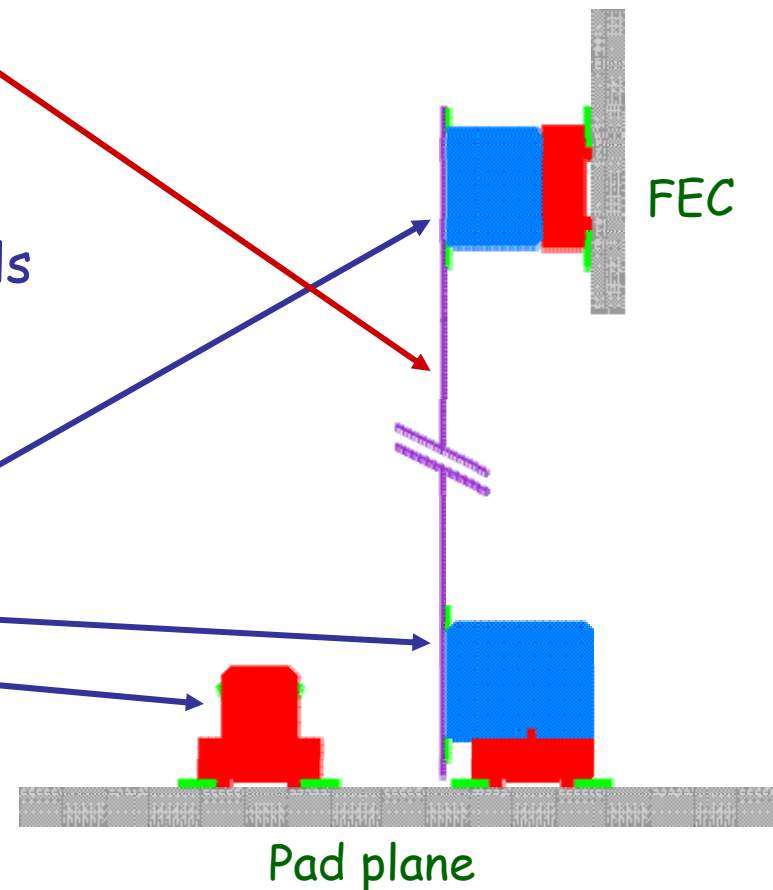


- The front end card is connected to the pad plane via **kapton cables**
- 100 cables have been produced
- 10 have been equipped with contacts
- > 300 cables needed for 10.000 channels
- Will be ordered after tests

## Connectors:

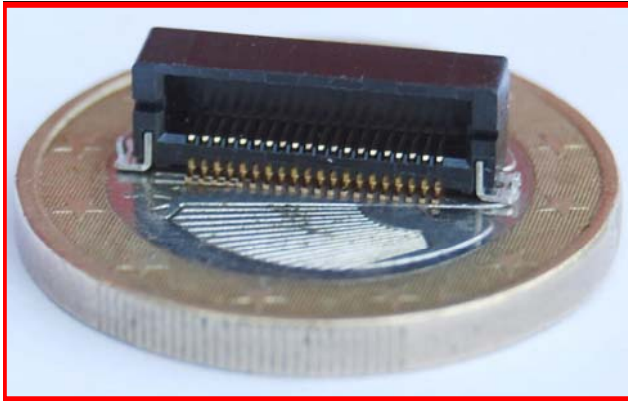
	SE	Japan
WR-40P-VF-N1	100	500
WR-40P-HF-HD-A1E	100	500
WR-40S-VF-N1	200	1000

Delivery middle-end of October



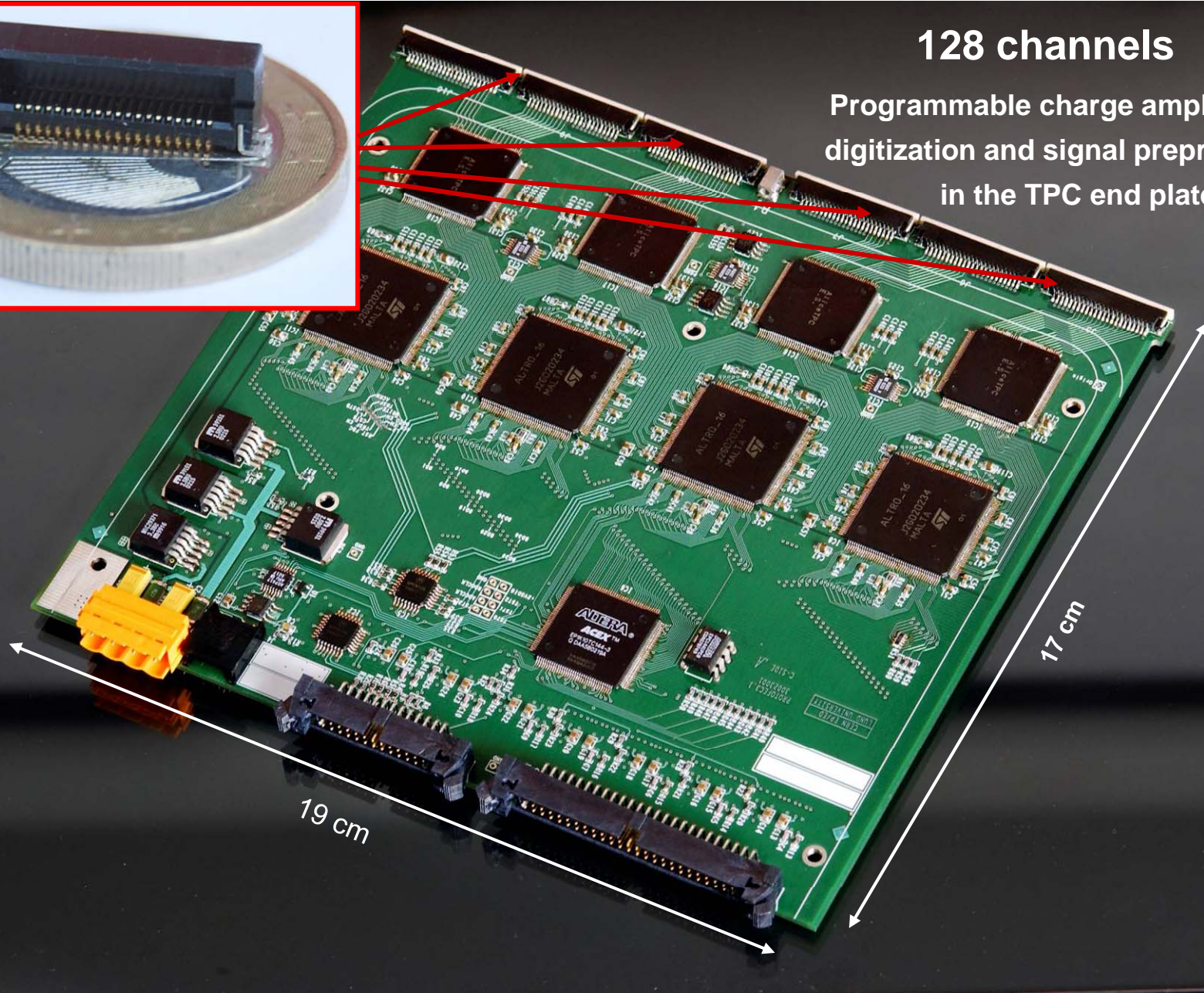


# ALICE TPC Front End Card



128 channels

Programmable charge amplification,  
digitization and signal preprocessing  
in the TPC end plate

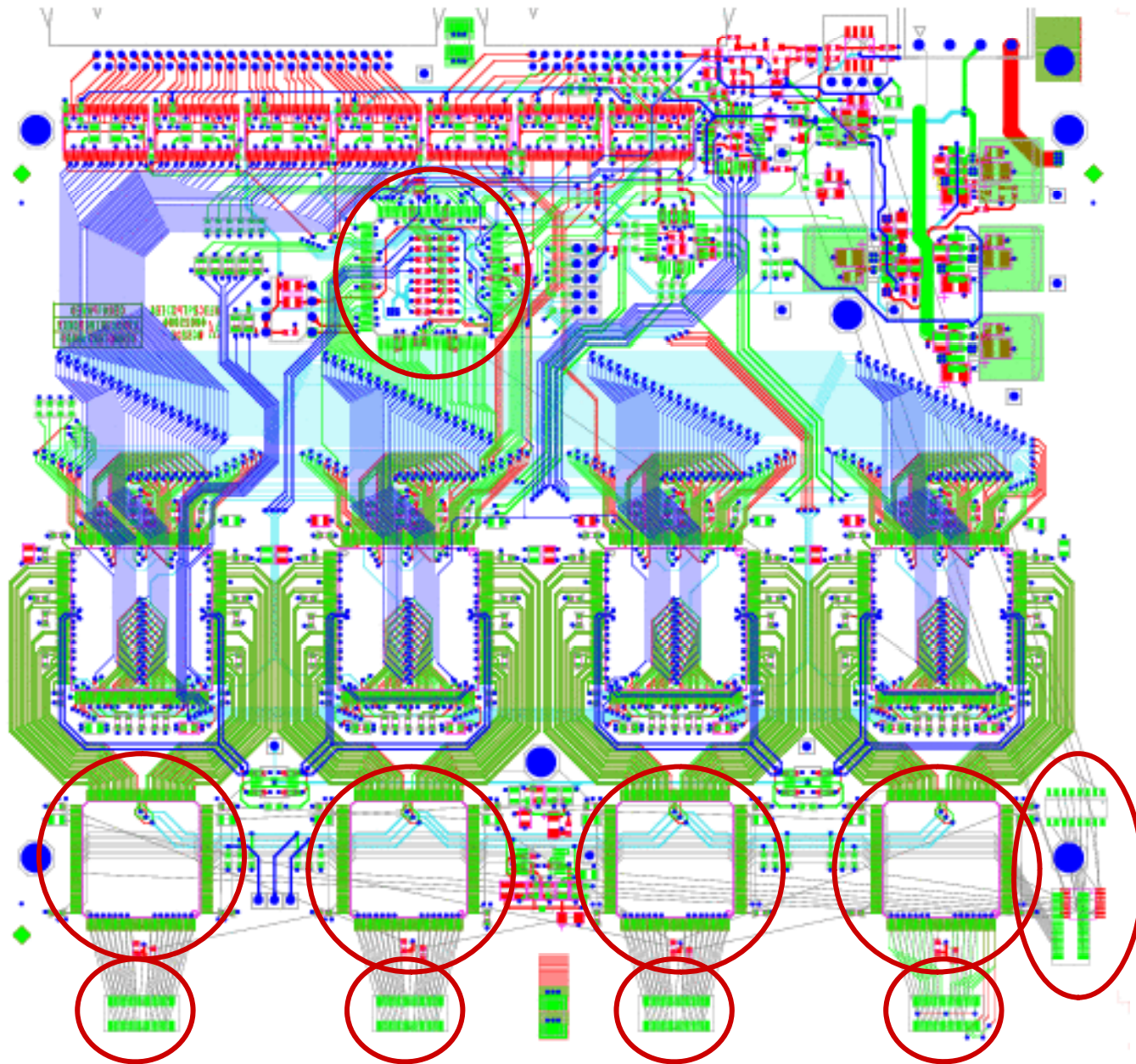


19 cm

17 cm



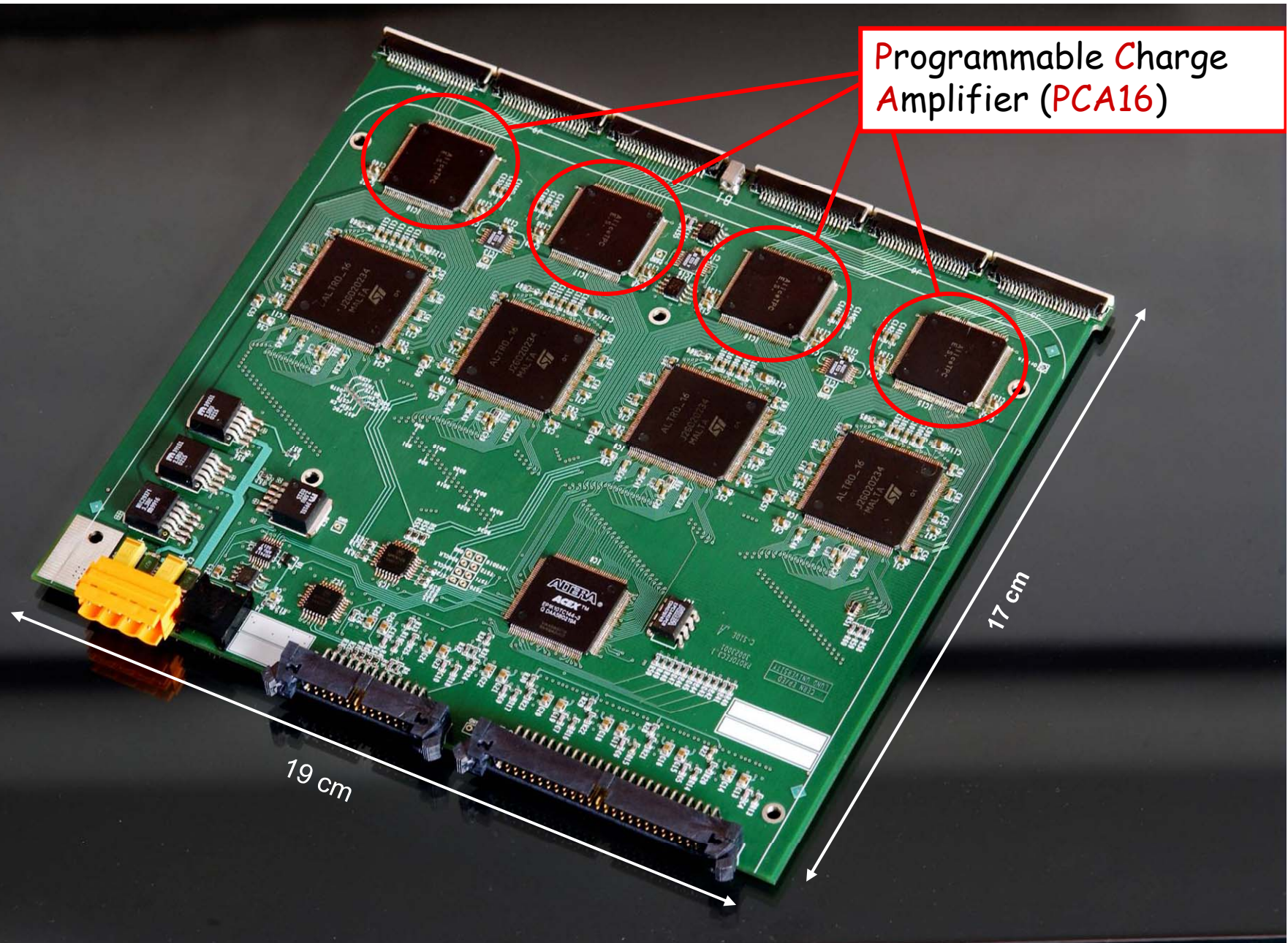
# Preliminary layout of the modified FEC





# ALICE TPC Front End Card

Programmable Charge Amplifier (PCA16)



# Programmable Charge Amplifier (PCA16)

- 1.5 V supply; power consumption <8 mW/channel
- 16 channel charge amplifier + anti-aliasing filter
- Single ended preamplifier
- Fully differential output amplifier
- Both signal polarities
- Power down mode (wake-up time = 1 ms)
- Programmable peaking time (30 - 120 ns)
- Programmable gain in 4 steps (12 - 27 mV/fC)
- Preamp\_out mode
- Tunable time constant of the preamplifier



# Status of PCA16

## Production

- 200 of the 130 nm PCA16 chip were delivered from the foundry in the week 39.
- They have been sent to the packing company and are expected to be returned in 4-5 weeks i.e. end October - middle November

## Tests

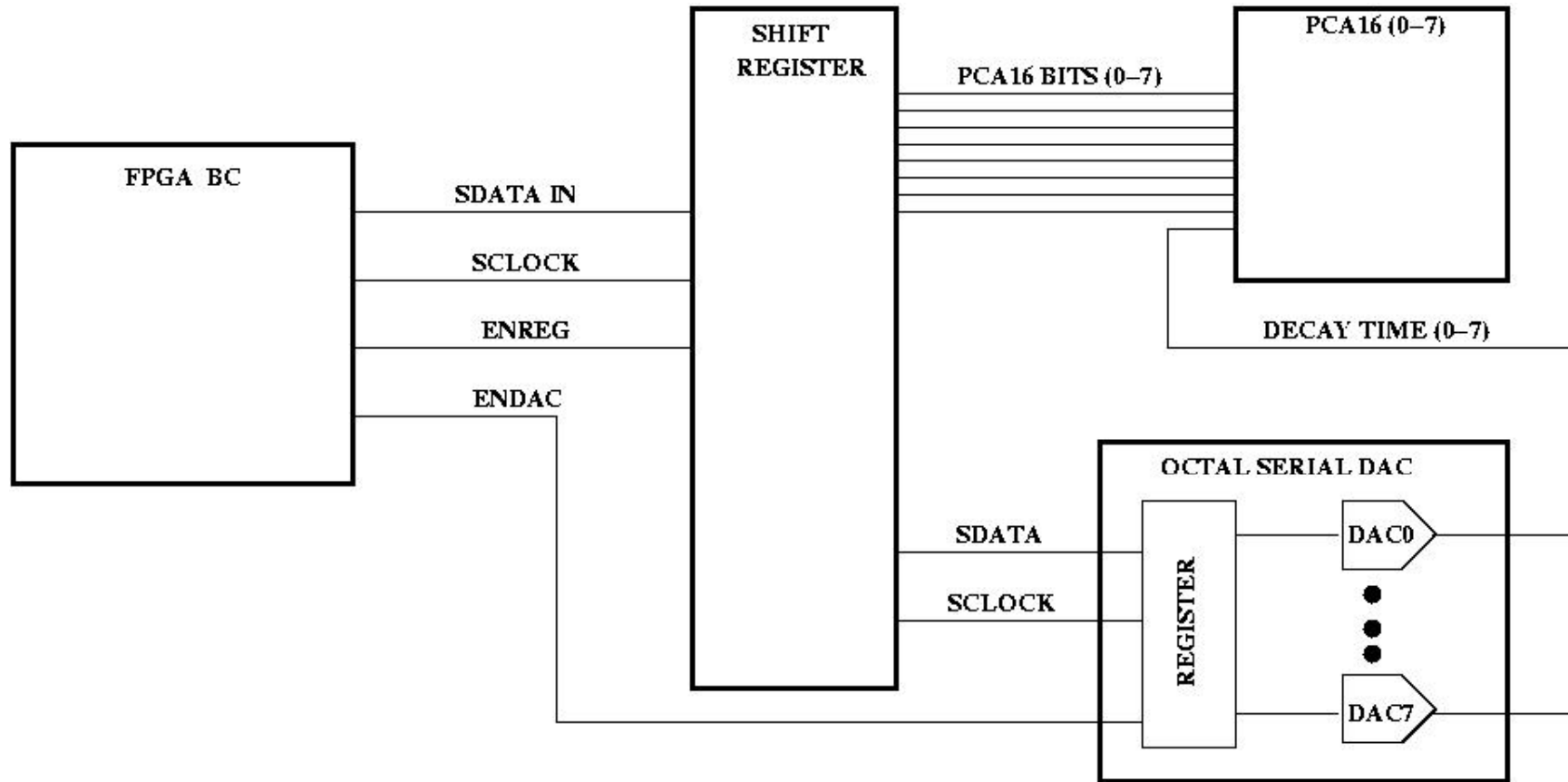
- Verification of the design by manual tests at CERN
- For tests of the larger quantity one might consider to use the robot in Lund, but then it has to be rebuilt and reprogrammed. The mechanical rebuild can be organised by Lund but we need someone to do the reprogramming.
- **Decision has to be taken and preparations have to start soon**



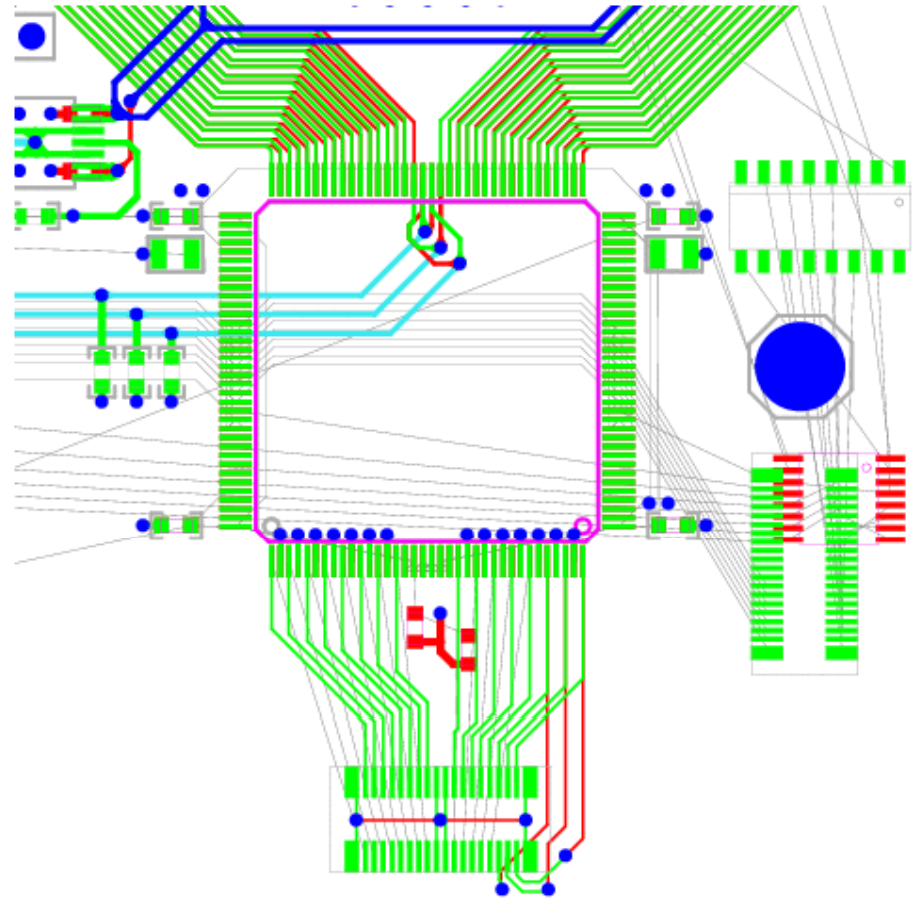
# Control of the PCA16

- Option A (baseline):
  - Use existing serial interface on the board controller (BC) to set an octal DAC (digit to amplitude converter) and an 8-bit shift register (polarity, gain, shaping time, ...) of the PCA16
  - Reprogramming of the BC FPGA with help of CERN people
  - Connection FPGA - PCA16: Analogue and Digital GND decoupled by capacities and by the DAC ➔ Expect no noise on PCA16 inputs (to be tested)
- Option B (fall-back):
  - Jumpers/dip-switches on FEC (analogue) side ➔ modification of cooling plate? Is a cooling plate needed at all?
  - To settle this issue we need to know the distance between FECs. The test can be done at CERN

# Control of the PCA16



# Control of the PCA16



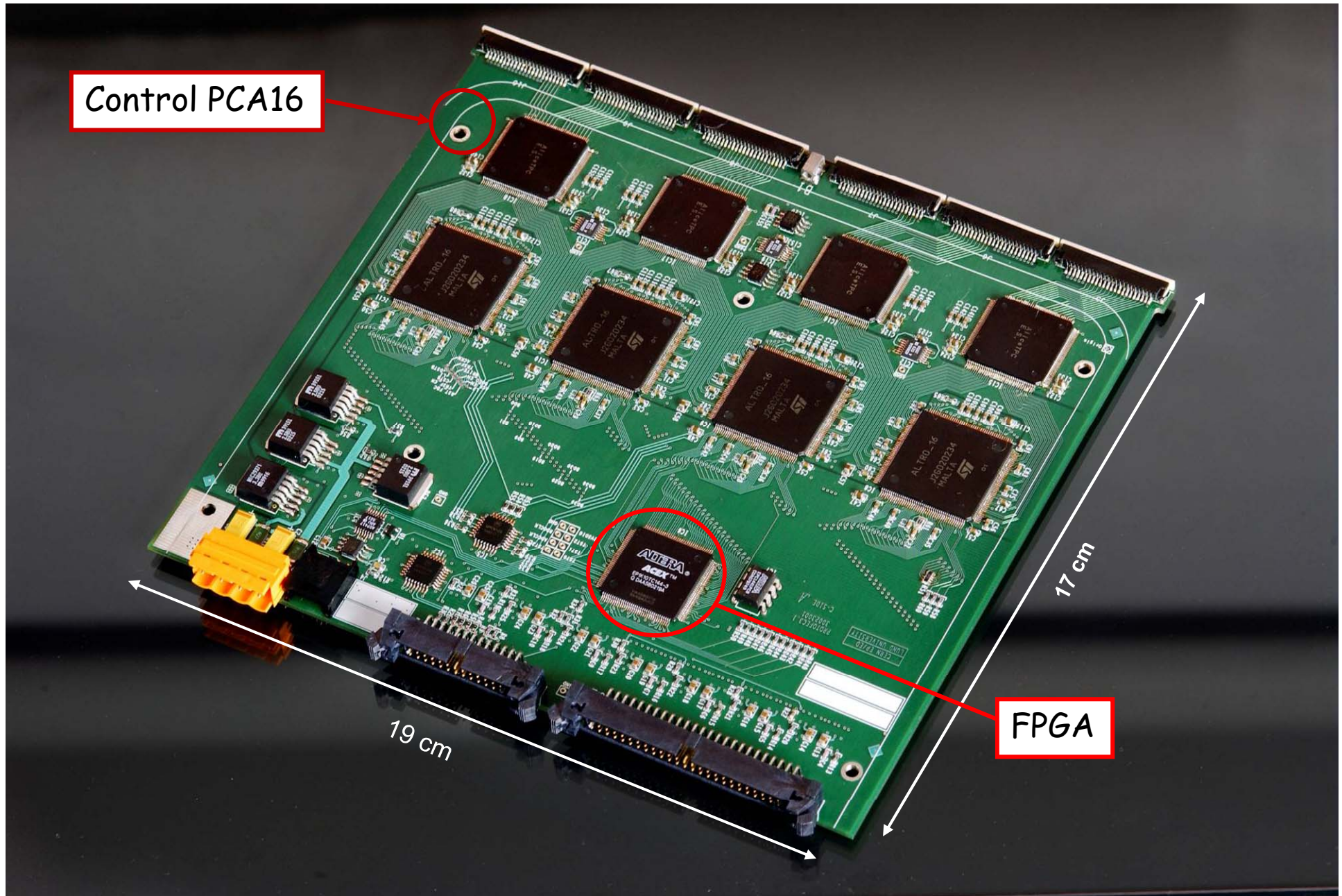
# ALICE TPC Front End Card

Control PCA16

FPGA

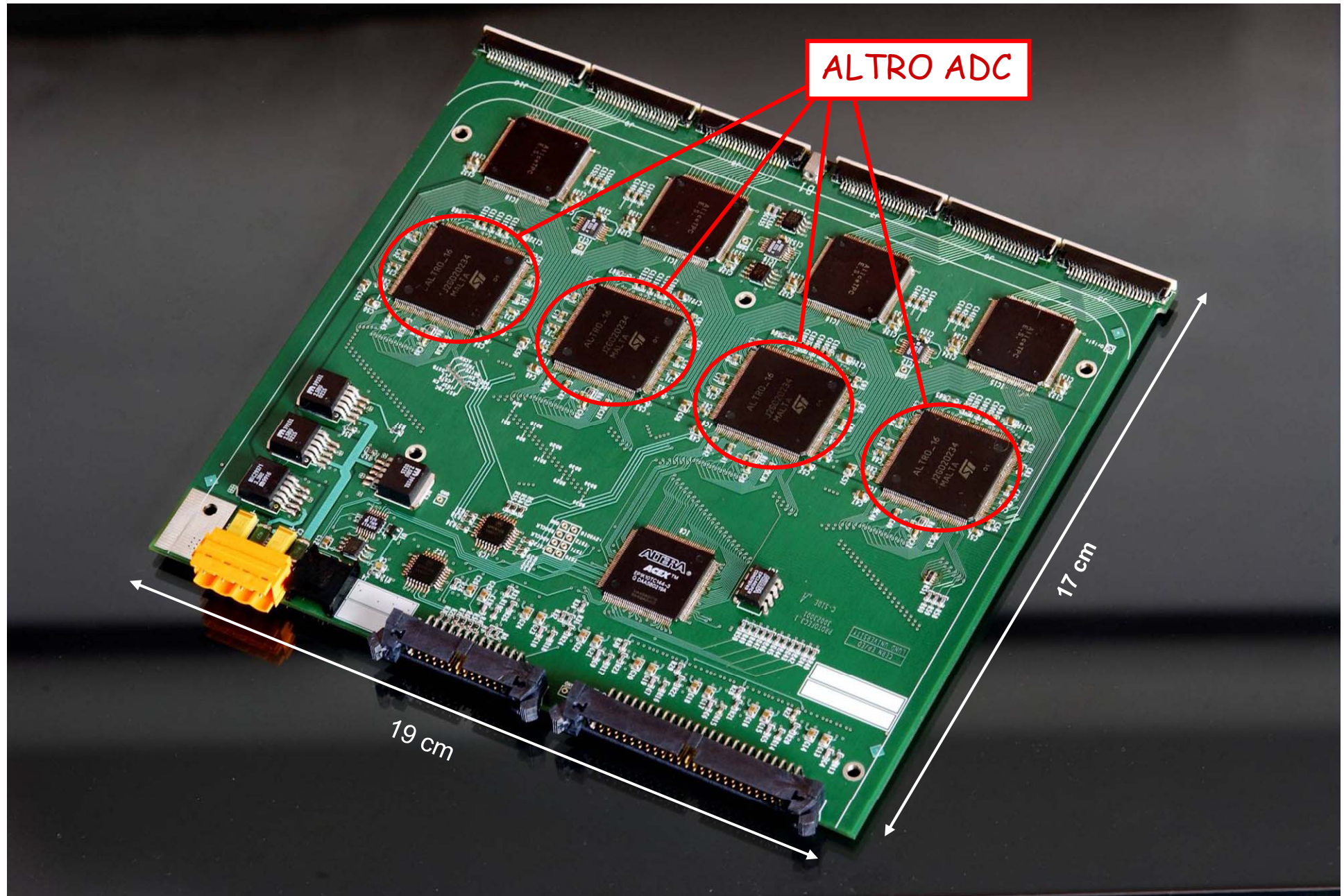
19 cm

17 cm





# ALICE TPC Front End Card



# ALTRO

Number of available 40 MHz ALTRO chips from ALICE (~2000 ch) 125

New production of 25 MHz ALTRO chips for other experiments:

- Number of chips produced 16489
- Number of chips accepted by the test 14273 (86%)
- Number of chips not accepted by the test 2216 (14 %)

- Number of chips ordered by other exp. 13400
- Remaining accepted chips available for ILC-TPC 873

- Out of the chips that failed the test it is expected that 33% may be recuperated 730

- Total number available chips for ILC-TPC ~1600  
This number corresponds to 25600 channels

# 10-bit multi-rate ADC

High speed, high-resolution analogue to digital converter

Resolution: 10 bits

Speed: 40 MHz

Power: 30 mW (0.75 mW per MHz)

Area: 0.6 mm<sup>2</sup> in a 0.13mm CMOS process

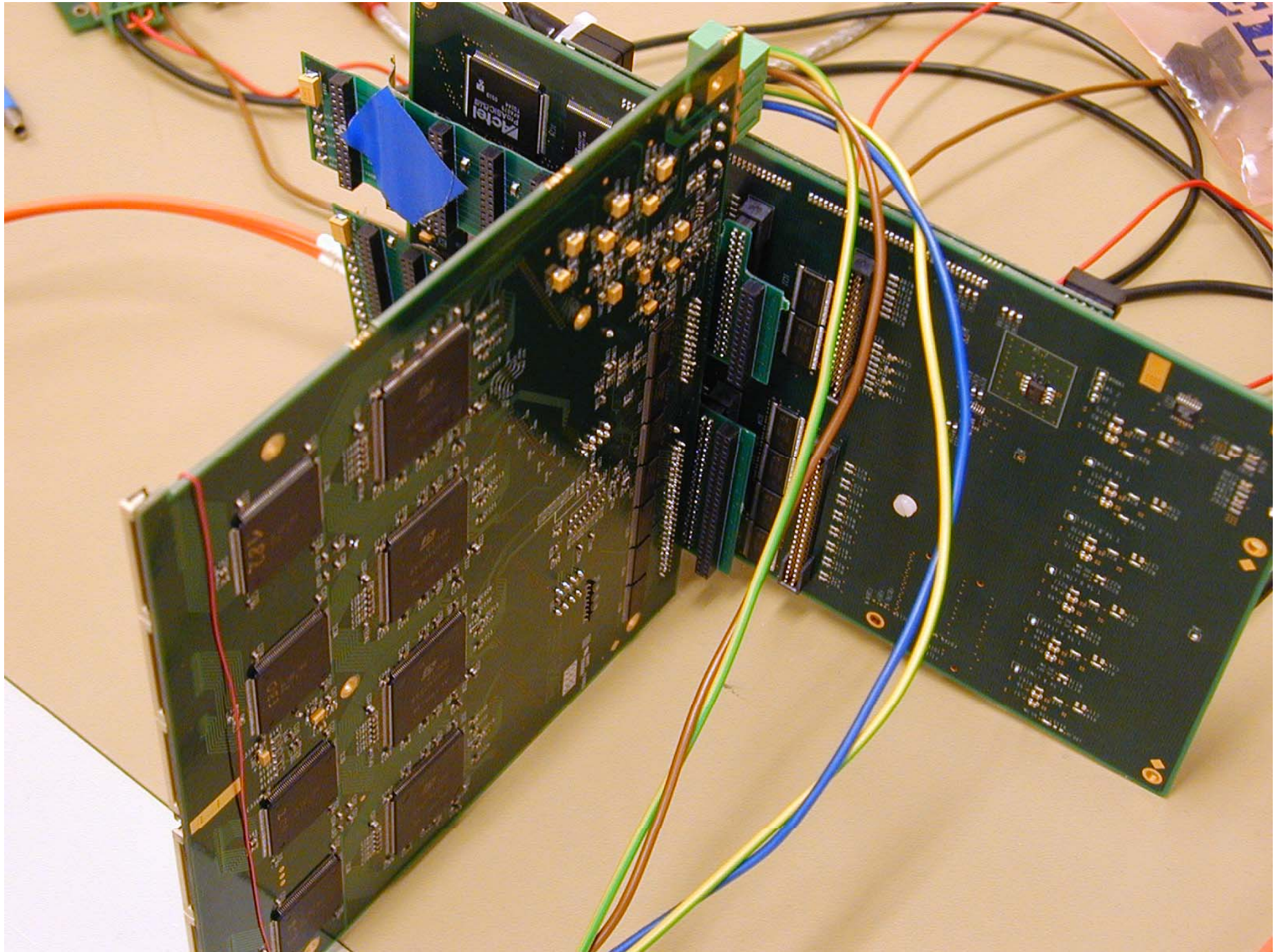
## Project Schedule

December 2007	Schematics design complete
March - April 2008	Layout ready -> Submission to foundry
June - July 2008	Core ready -> Packaging
July - August 2008	Chip ready -> Test at CERN

## Summary: Project Milestones

- Milestone I (Q1 2007)
  - Programmable Charge Amplifier (prototype);  
12 channel non-programmable charge amplifier produced and tested  
16 channel programmable charge amplifier (PCA16) produced; 200 chips  
(Sept. 2007)  
Tests of PCA16 (Nov. - Dec. 2007)
- Milestone II (Q2 2007)
  - 10-bit multi-rate ADC (prototype); 4-channel 10-bit 40-MHz ADC.  
(Dec 2007, schematic design)
    - Available: ~125 ALTRO chips 40 MHz  
~1600 ALTRO chips 25 MHz
  - Modified circuit board (design) (Oct. 2007)
- Milestone III (Q3 2007)
  - Operating DAQ-system (Test system operating Sept. 2007)
  - Production and bench-top tests of modified FEC. (Dec. 2007; provided minimum 8 PCA16 available in Lund)





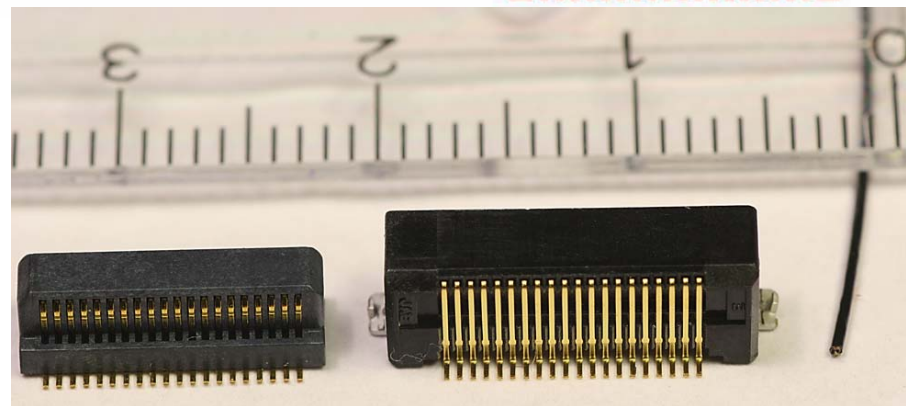
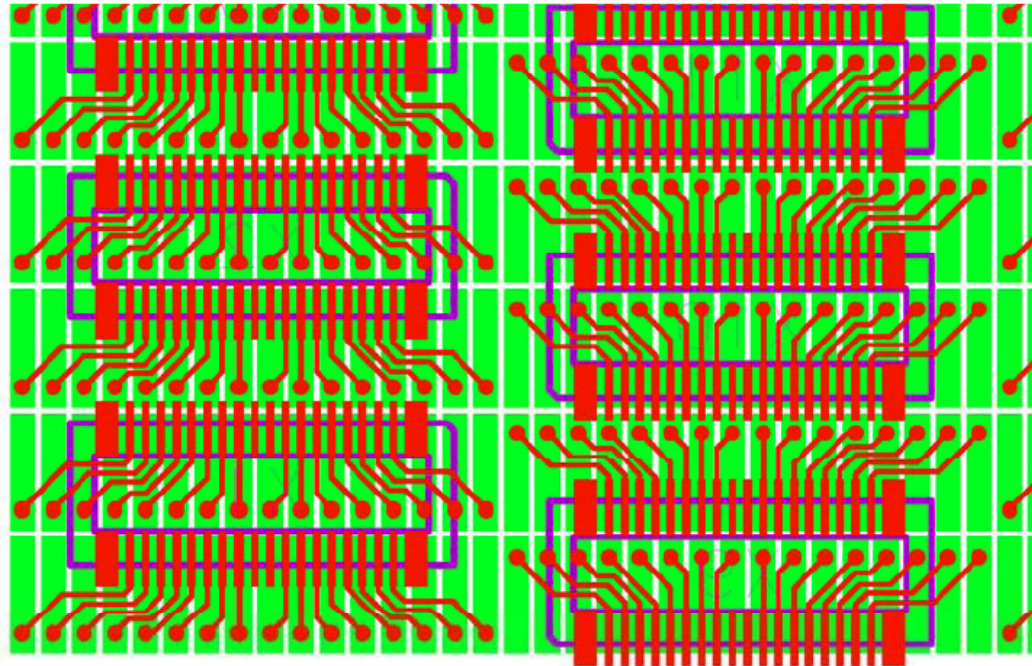
**Starting point:** min pad size  $1 \times 4 \text{ mm}^2$

**Requirements:** highest possible flexibility in terms of pad geometry and shape of pad panels  
⇒ Small modules (i.e. small connectors)

**Proposal:** 32 channels modules, where each channel corresponds to an area of around  $4 \text{ mm}^2$   
- Japan Aviation Electronics offers a 40 pin connector with 0.5 mm pitch and the dimensions  $13.9 \times 4.7 \text{ mm}^2$ . Thus, this connector allows additional 8 pins for grounding.



# Example of signal routing from 1x4 mm<sup>2</sup> pads to the WR-40S connector



## The general test concept (as presented at NIKHEF)

The intention is to build a modular electronic read-out system which offers a flexibility to test various types of avalanche read-out techniques and pad geometries.

- The read-out electronics should be dismountable from the pad board such that it can be easily moved from one panel to the next
- The amplifier board should be directly attached to the pad board via a connector
- The analogue and digital electronics should be mounted on separate cards connected by short ribbon cables
- The DAQ system should be flexible, such that it can be duplicated and distributed to different users performing table-top experiment.

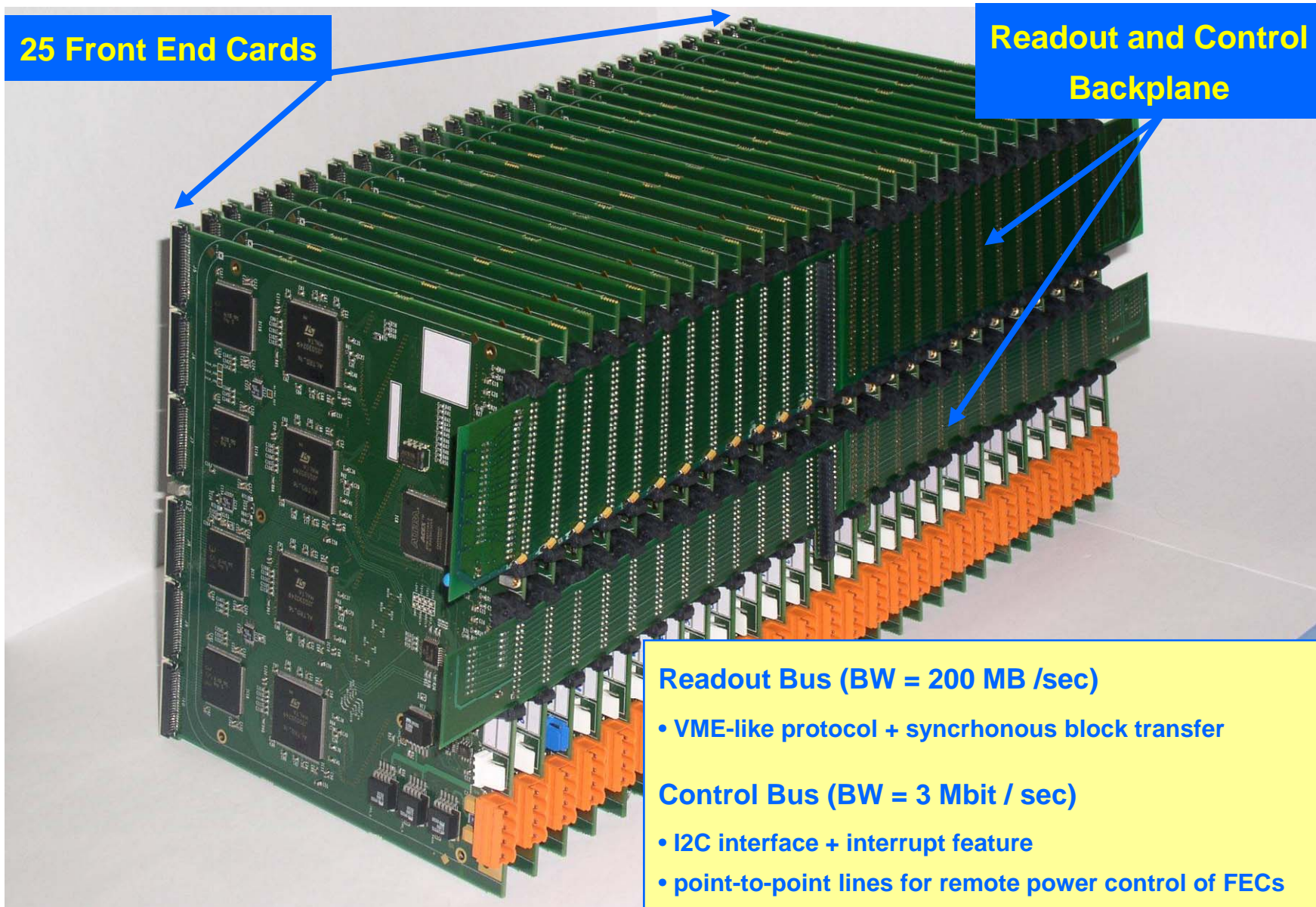
Is this still valid??? ⇒ Option to test different types of amplifiers (shaping, non-shaping....)



# Readout & Control Backplane

25 Front End Cards

Readout and Control Backplane



**Readout Bus (BW = 200 MB / sec)**

- VME-like protocol + synchronous block transfer

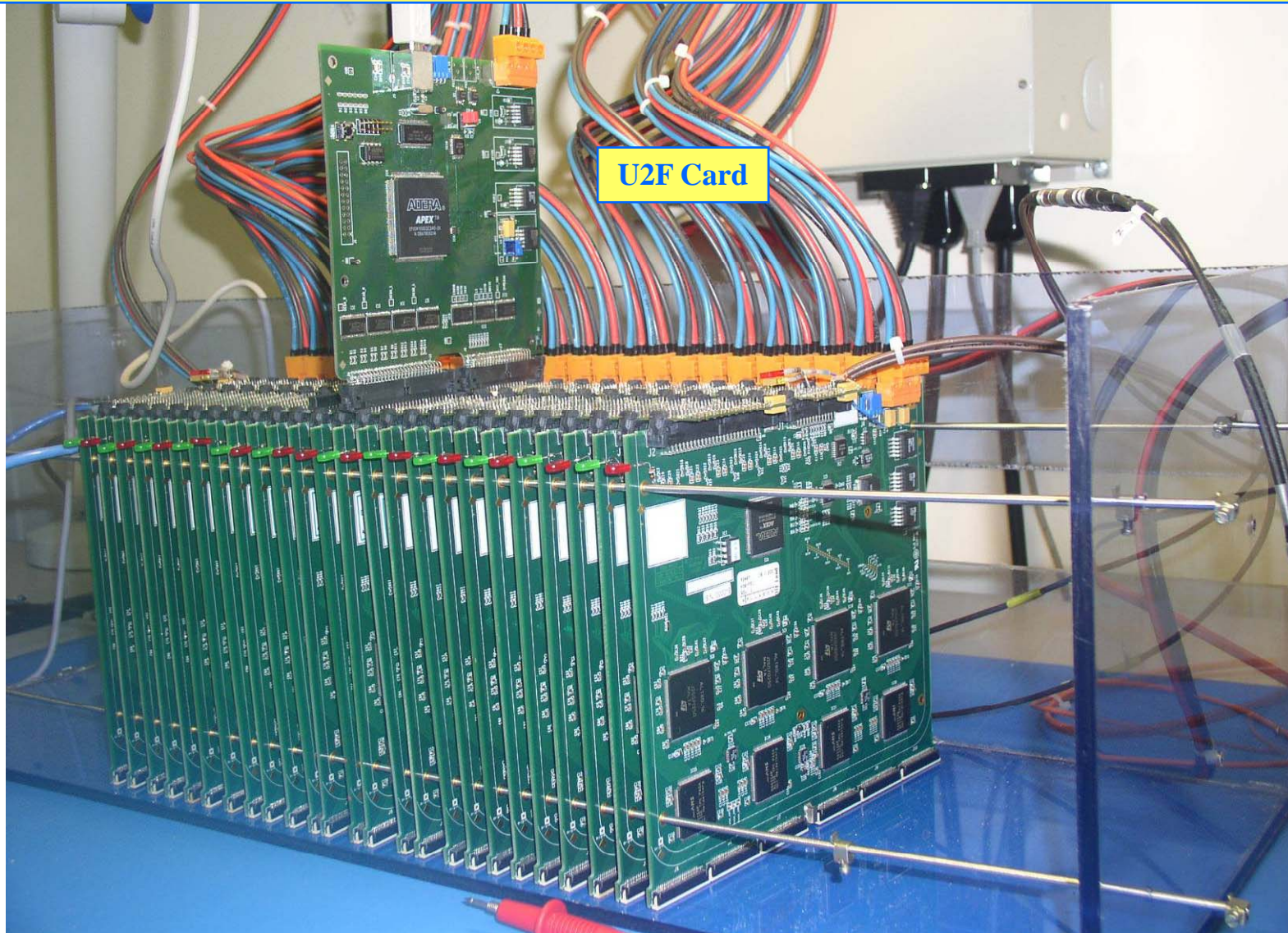
**Control Bus (BW = 3 Mbit / sec)**

- I2C interface + interrupt feature
- point-to-point lines for remote power control of FECs



# USB to FEC Interface Card (U2F)

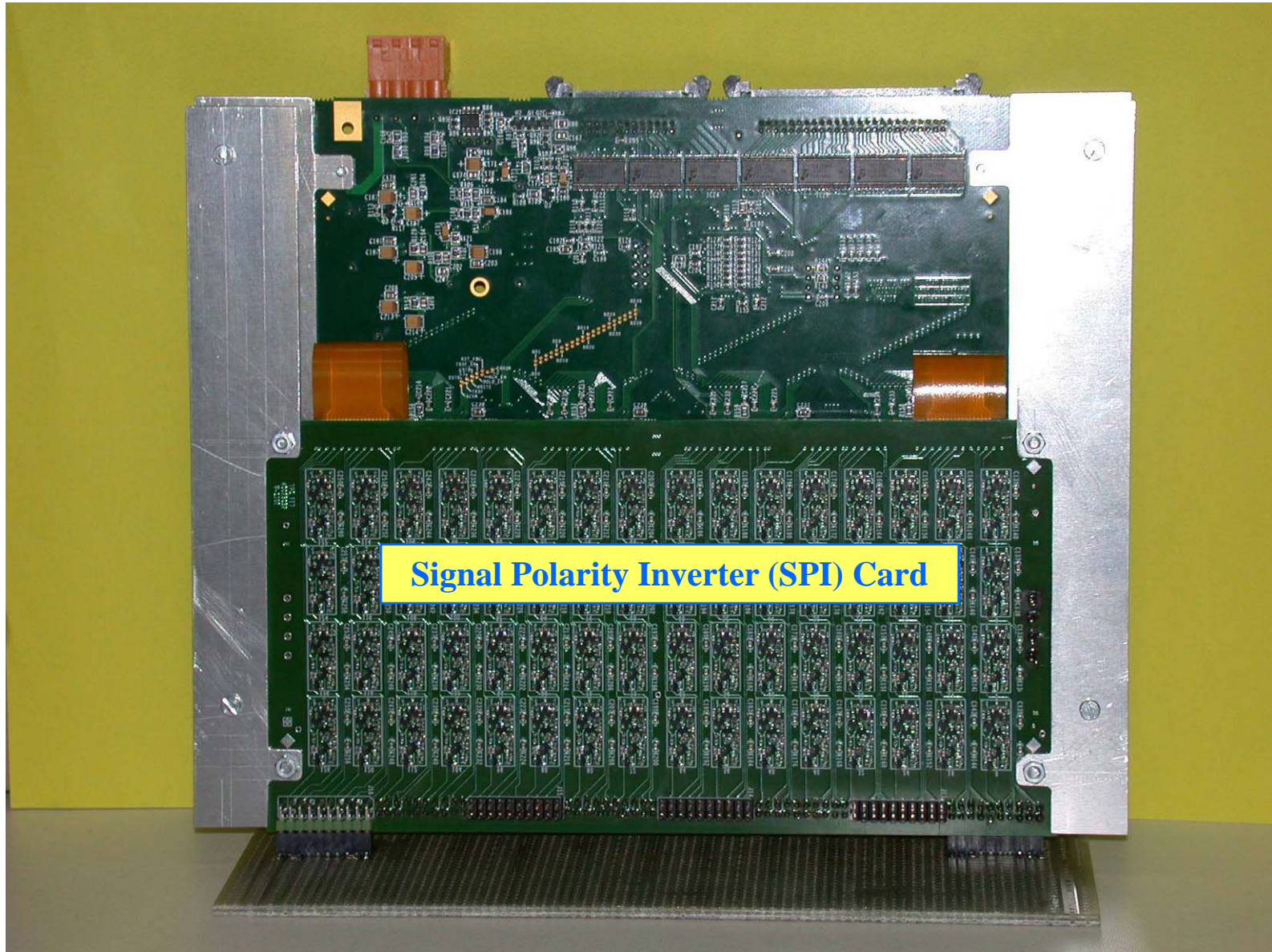
The U2F Card can read up to 16 FECs (2048 channels)





# SPI Card + ALICE TPC FEC

Temporary during the development phase of the new preamplifier

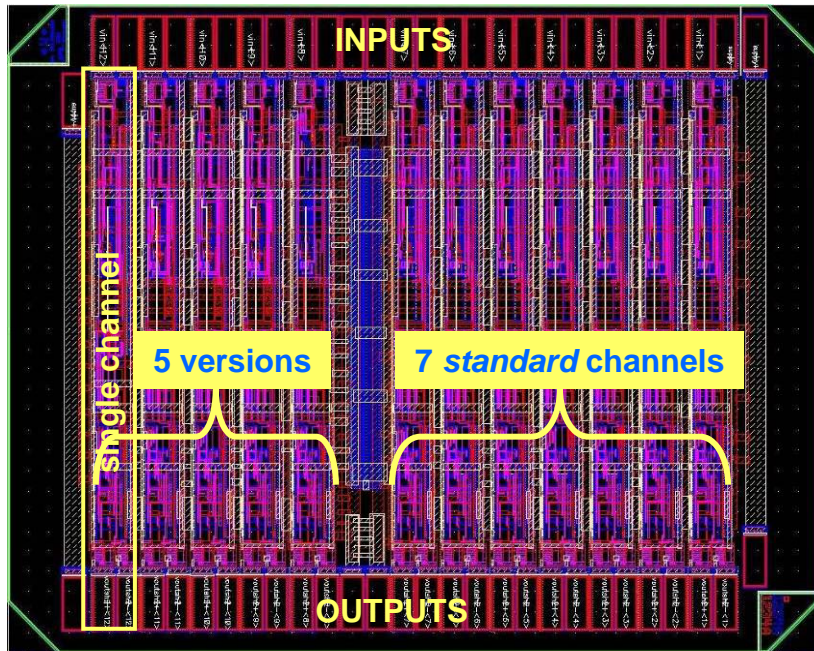


## Readout electronics for the Large Prototype TPC (LPTPC)

- modular with well defined interface for
  - ✓ various amplification technologies (GEM &  $\mu$ Megas)
  - ✓ different module geometries
- easy to use and with a modern DAQ system
- Two strategies pursued in EUDET
  - new TDC (Rostock)
  - FADC-based (Lund, CERN)



# Programmable Charge Amplifier

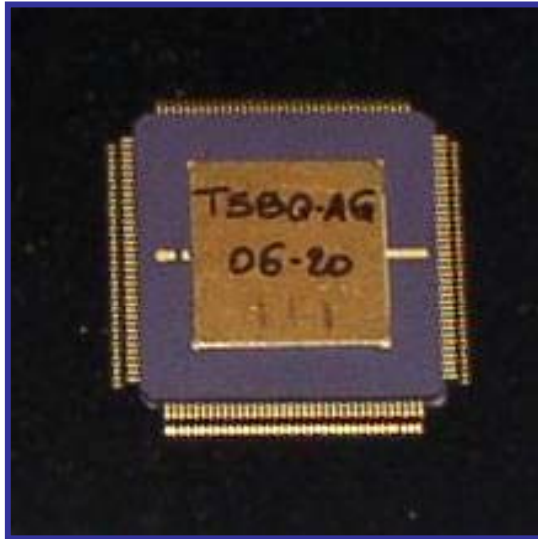


## Production Engineering Data

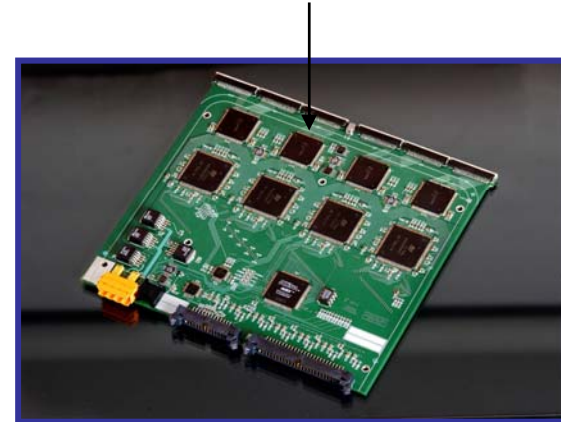
- 12- channel 4th order CSA
- various architectures (classical folded cascode, novel rail-to-rail amplifier)
- process: IBM CMOS 0.13  $\mu\text{m}$
- area: 3  $\text{mm}^2$
- 1.5 V single supply
- Package: CQFP 144
- MPR samples (40): Apr '06

Parameter	Requirement	Simulation	MPR Samples
Noise	< 500e	300e (10pF)	270e (10pF)
Conversion gain	10mV / fC	10mV / fC	9.5mV / fC
Peaking time ( <i>standard</i> )	100ns	100ns	100ns
Non linearity	< 1%	< 0.35%	0.4%
Crosstalk	<0.3%	0.4%	< 0.3%
Dynamic range	> 2000	3300	4600
Power consumption	< 20mW	10mW / ch	10mW / ch (30pF cl)

# Programmable Charge Amplifier



- The CQFP 144 package has the same pin-count and similar pin-out as the ALICE TPC PASA
- In the near future the new chip will be tested on a ALICE TPC FEC

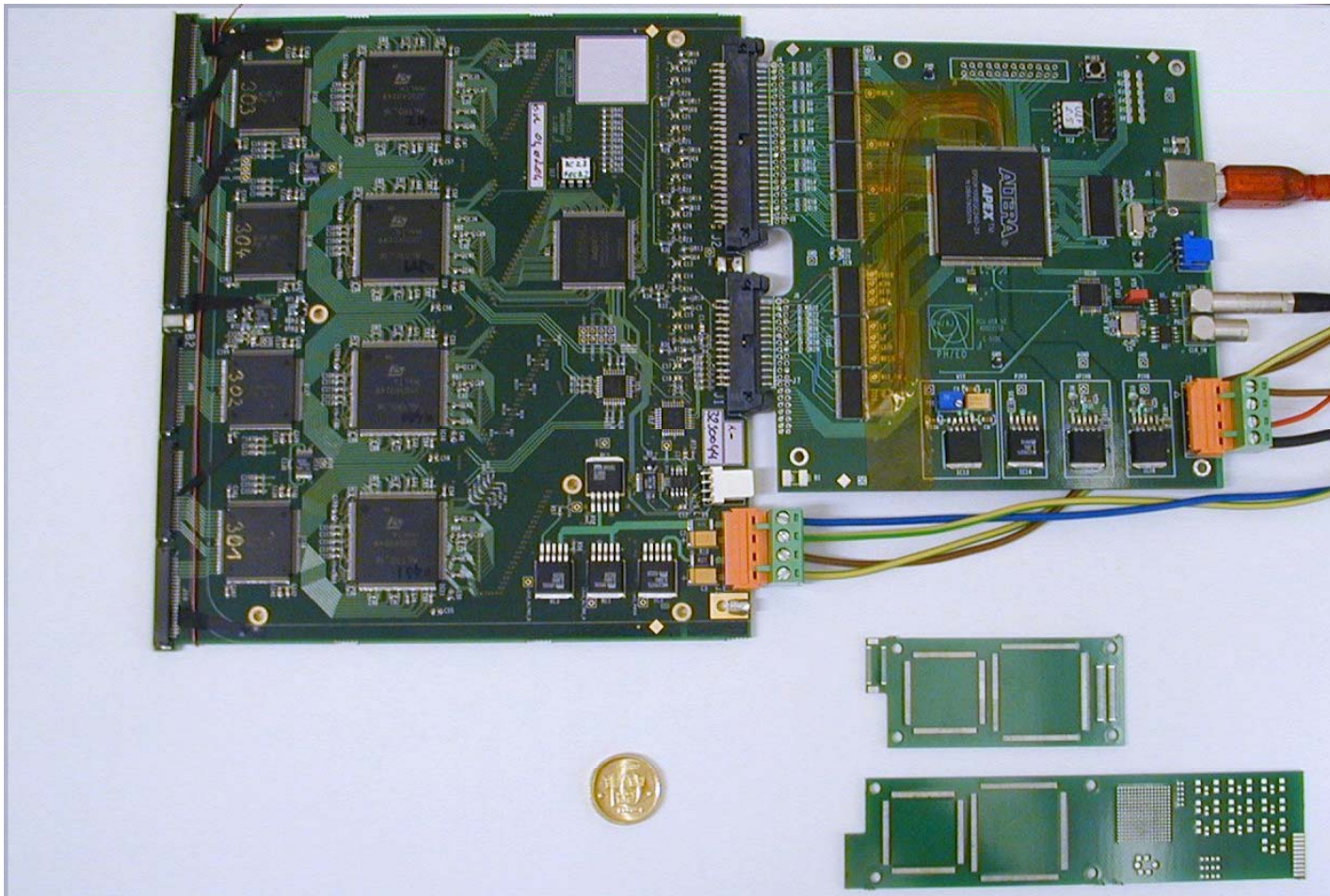


## Next Step

- Programmable Charge Amplifier (prototype)
  - 16 channel charge amplifier + anti-aliasing filter
  - Programmable peaking time (20ns - 140ns) and gain

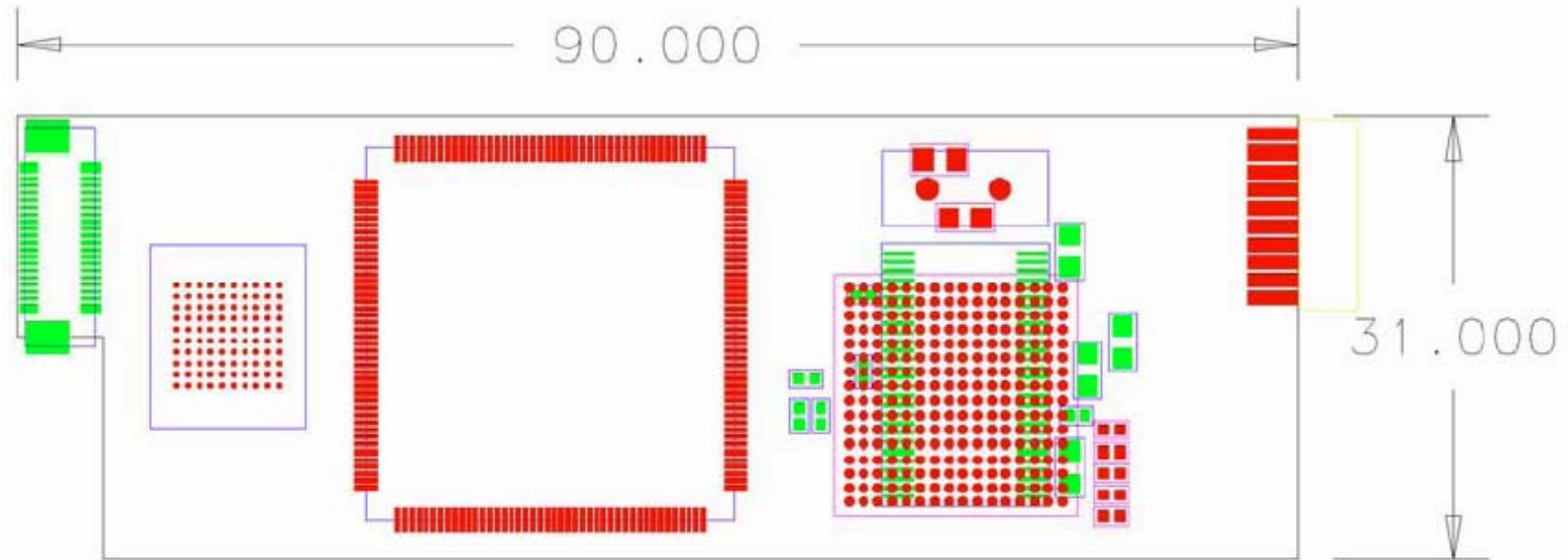
# The mini-FEC new design

**Motivation:** should be compatible with the available area such that it can be mounted directly onto the connectors at the plane  
⇒ the number of equipped pads can be increased without getting space problems.



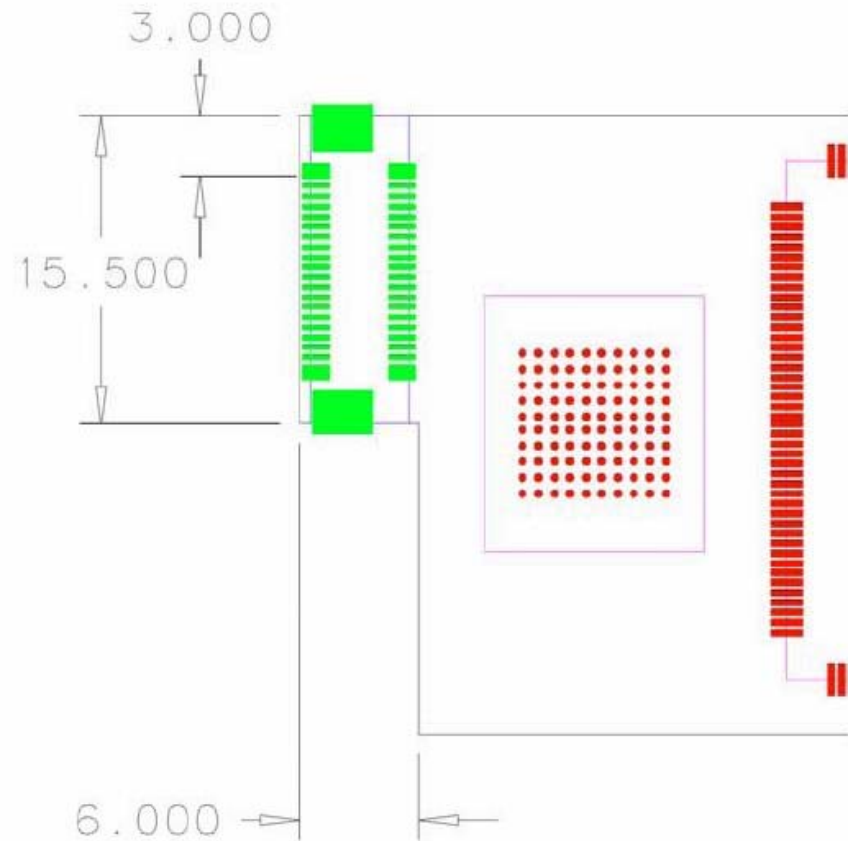
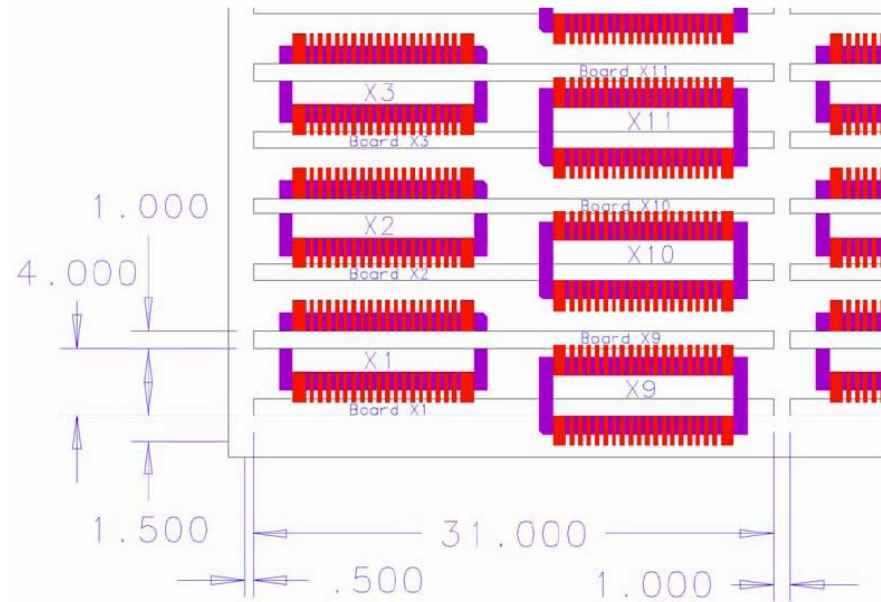


# The mini-FEC new design (based on the ALTRO chip)



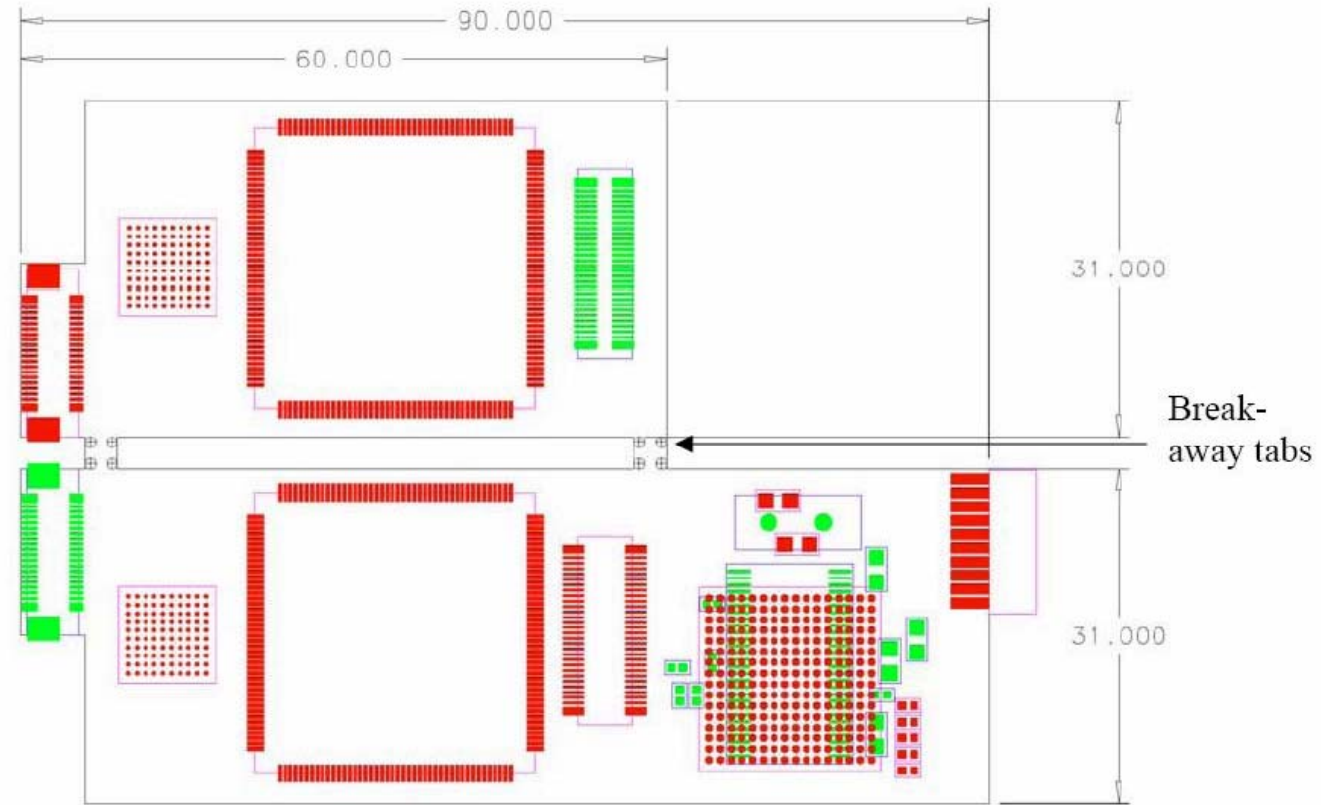


# Connector arrangement



# Dual mini-FEC

(based on the ALTRO chip)



## Mini-FEC based on commercial components

- In telecommunication a completely new approach of handling signals has been developed (digitizing baseband + digital signal processing, DSP).
- Recent development in density and complexity of FPGA's (field programmable gate array) and lower prices.
- Completely reprogrammable DSP in contrary to ASIC.
- A new generation of multi-channel, high-speed and high resolution FADC's with low noise and serial digital output has been developed, offered to a reasonable cost.

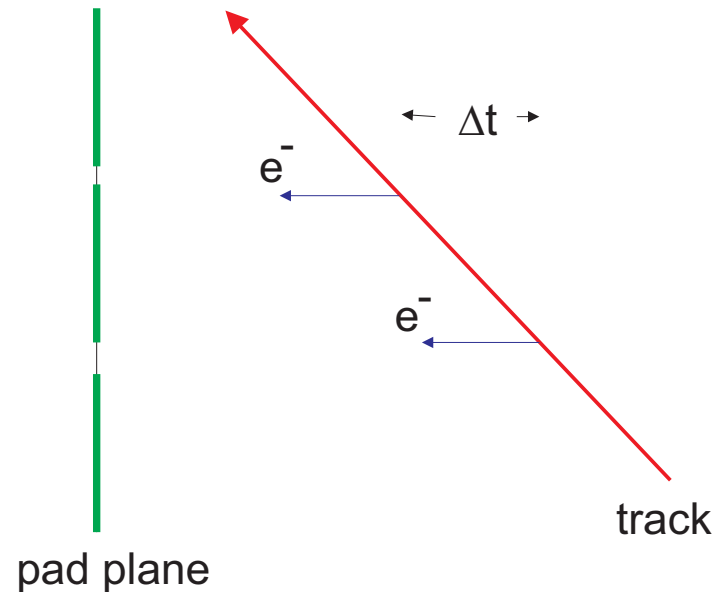


# Pulse characteristics

- For tracks traversing the chamber parallel to the pad plane i.e perpendicular to the beam axis, the pulse length is determined by the longitudinal diffusion.

- For inclined tracks the pulse length is given by the difference in arrival time of the electrons emitted at the ends of the track segment covered by the length of a pad.

⇒ Pulses will be of different length



Options:

- Charge preamp,  $\tau_{\text{rise}} \sim 40 \text{ ns}$ ,  $\tau_{\text{decay}} \sim 2 \mu\text{s}$  and shaper integrator 200-500 ns  
10 MHz sampling

- Charge preamp,  $\tau_{\text{rise}} \sim 40 \text{ ns}$ ,  $\tau_{\text{decay}} \sim 2 \mu\text{s}$ , no shaping, 25 MHz sampling

Available: Charge preamp,  $\tau_{\text{rise}} \sim 20\text{-}140 \text{ ns}$ , shaping, 40 MHz sampling

Dispute: The characteristics of the intrinsic GEM-pulse



# Summary: Project Milestones

- Milestone I (Q1 2007)

- Programmable Charge Amplifier (prototype);

- 12 channel non-programmable charge amplifier produced and tested

- 16 channel programmable charge amplifier (PCA16) produced; 200 chips (Sept. 2007)

- Tests of PCA16 Nov. - Dec. 2007

- Milestone II (Q2 2007)

- 10-bit multi-rate ADC (prototype); 4-channel 10-bit 40-MHz ADC. The circuit can be operated as a 4-channel 40-MHz ADC or single-channel 160-MHz ADC.

- (?????)

- Available: ~125 ALTRO chips 40 MHz

- 1600 ALTRO chips 25 MHz

- Modified circuit board (design) (Oct. 2007)

- Milestone III (Q3 2007)

- Operating DAQ-system (Test system operating Sept. 2007)

- Production and bench-top tests of modified FEC. (Dec. 2007)