Progress report on LumiCal front-end electronics development

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Outline

- Introduction
- Front-end design & simulations
- First measurements of front-end prototypes
- ADC design & prototype status
- Summary

Challenges of LumiCal front-end

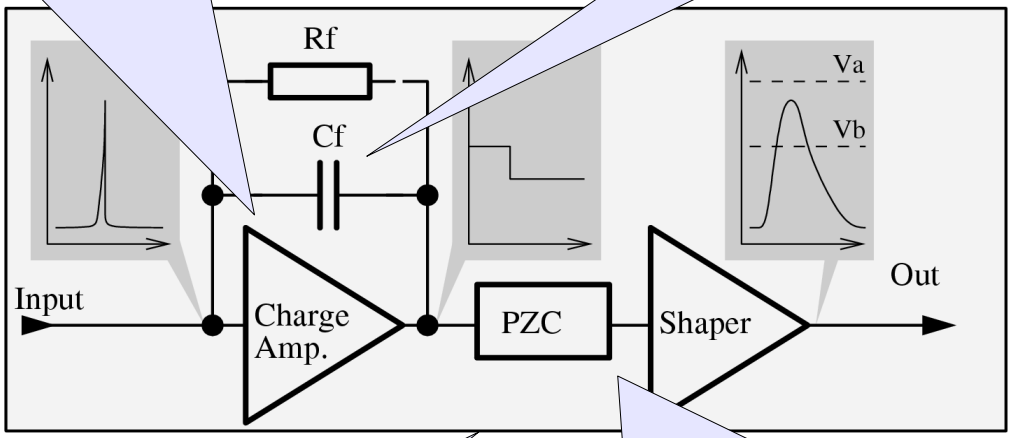
Large C_{det} range 10-100 pF

Test mode S/N~10 for MIP

Charge sensitive amplifier

Q_{max} ~ 10 pC

Cf ~ 10 pF



Test & Physics mode

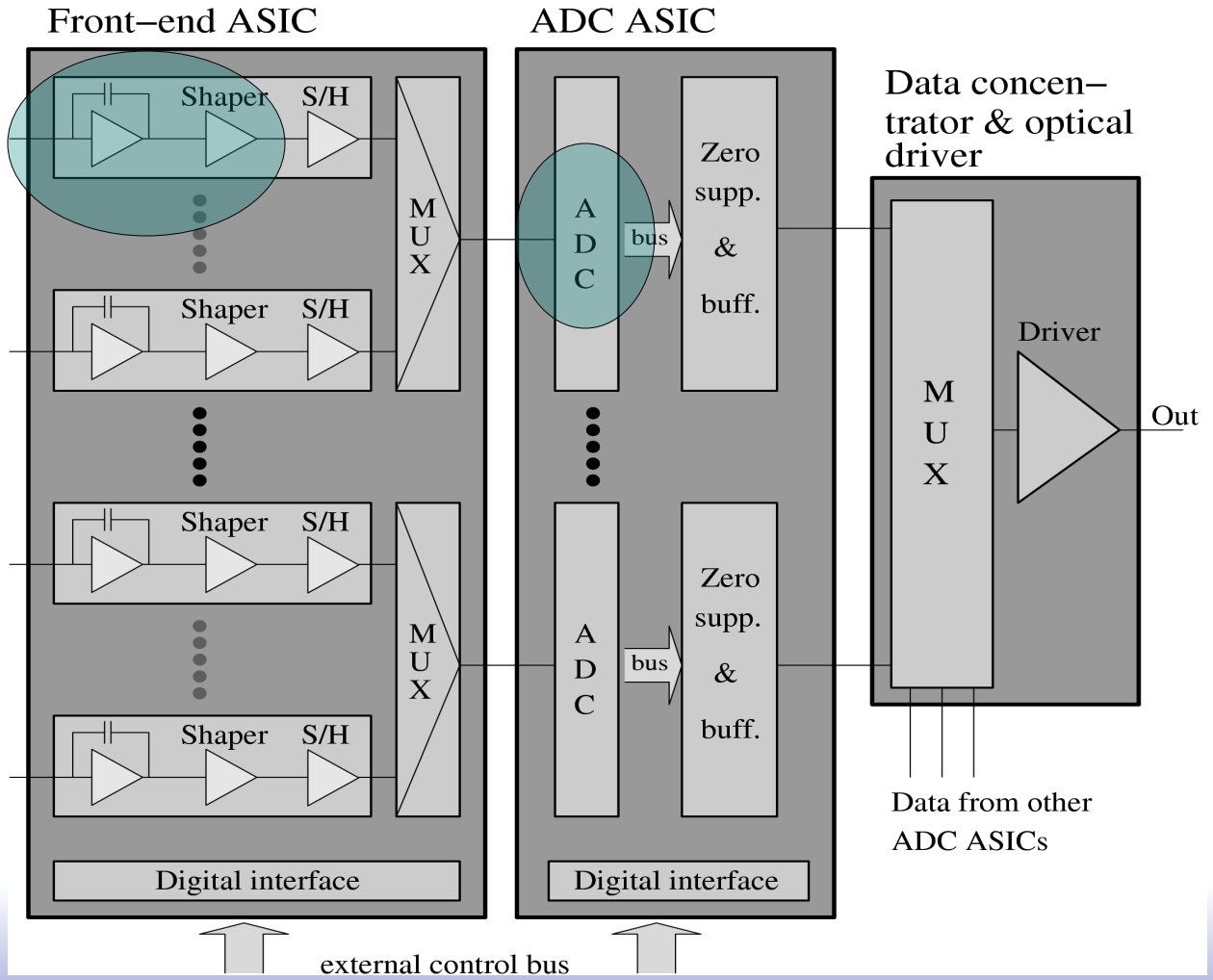
Variable gain

Δt≃300 ns, high occupancy

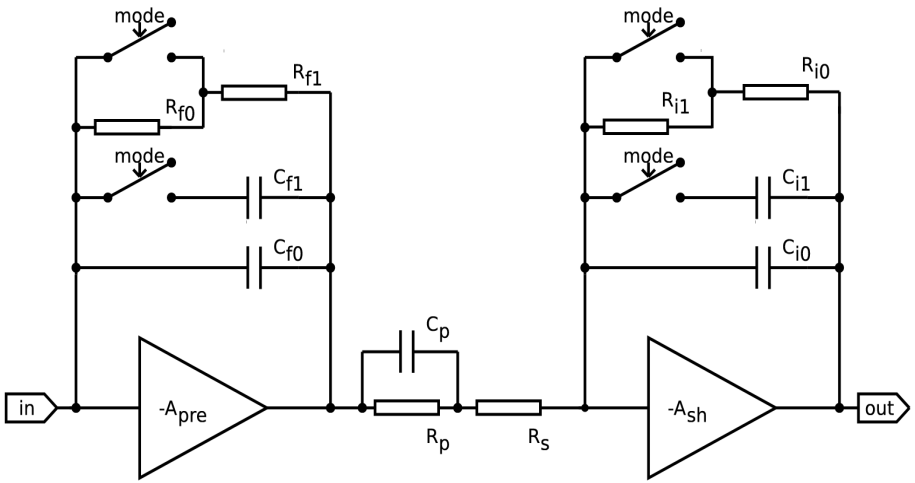
PZC +Shaper T_{peak} ~ 60ns

LumiCal readout architecture

- Front-end ASIC will contain 32-64 channels
- An ADC will serve ~8(1?) front-end channels
- First prototypes in AMS 0.35 µm

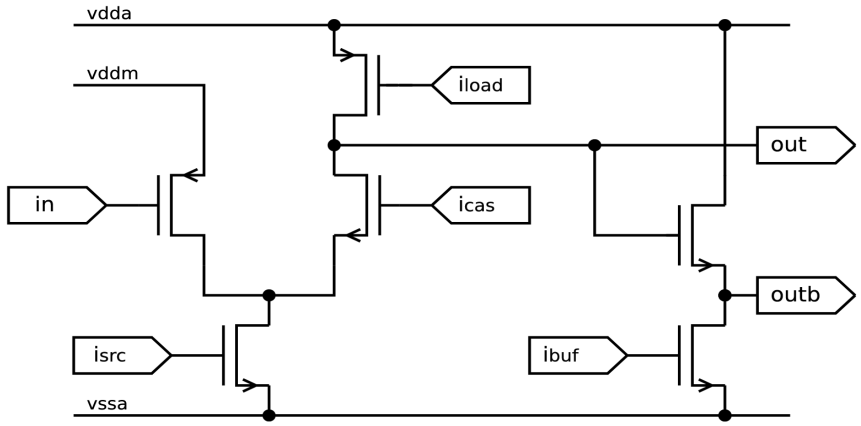


Front-end electronics architecture

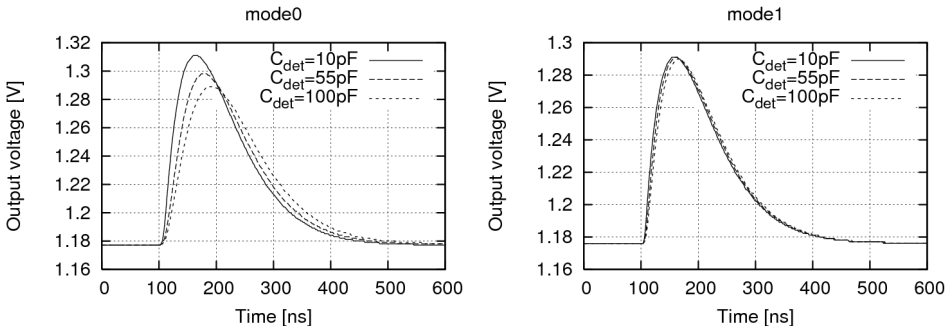


- Preamplifier: I_{pre}~2.5mA, PMOS input, Cf~10pF (physics), Cf~0.5pF (test)
- Shaper: 1st order, T_{peak}~60ns, variable gain, I_{sh}~0.5mA

- Both Preamplifier and Shaper designed as folded cascode plus source follower

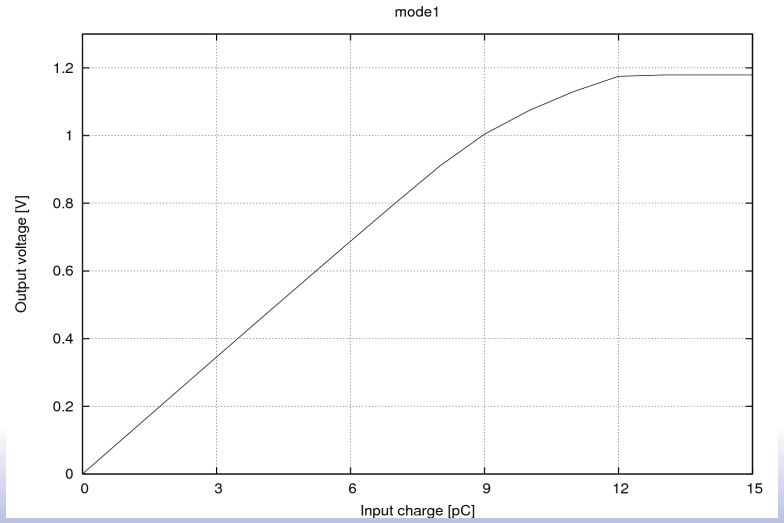


Front-end simulations

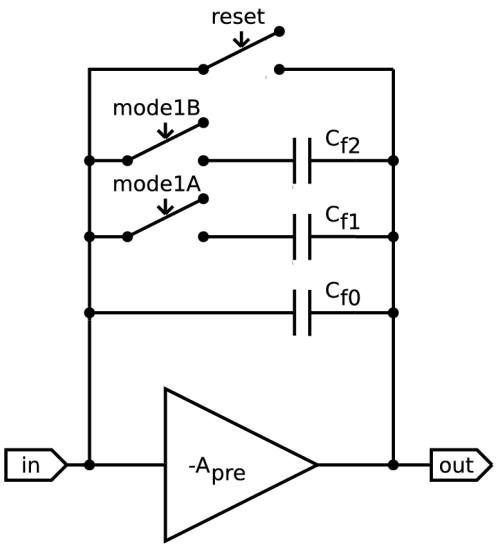


- Front-end response in test (mode0) and physics (mode1) mode for different C_{det}

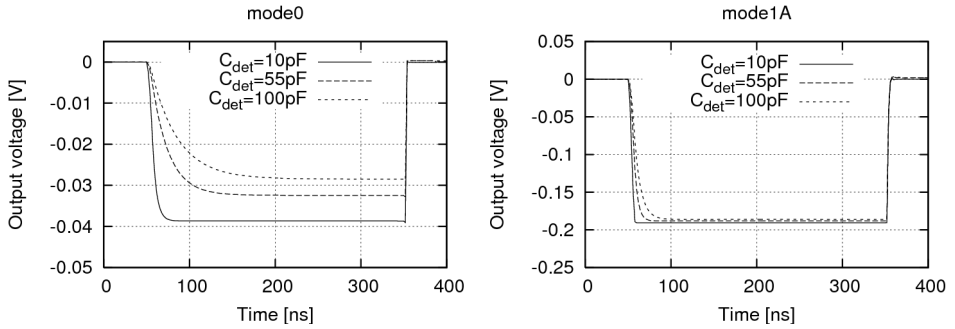
- Output amplitude versus injected charge in physics mode



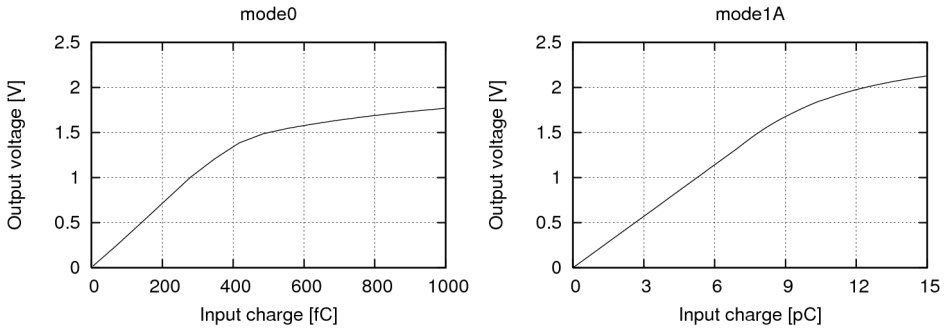
Alternative front-end
Switched-Reset configuration

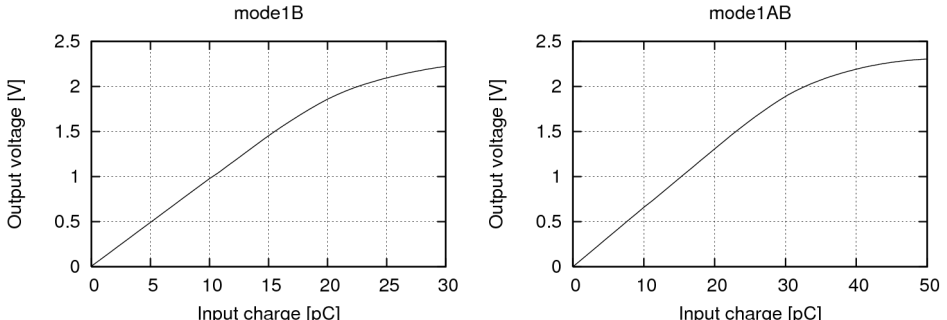


Switched-Reset configuration



Response in test (mode0) and physics (mode1) mode



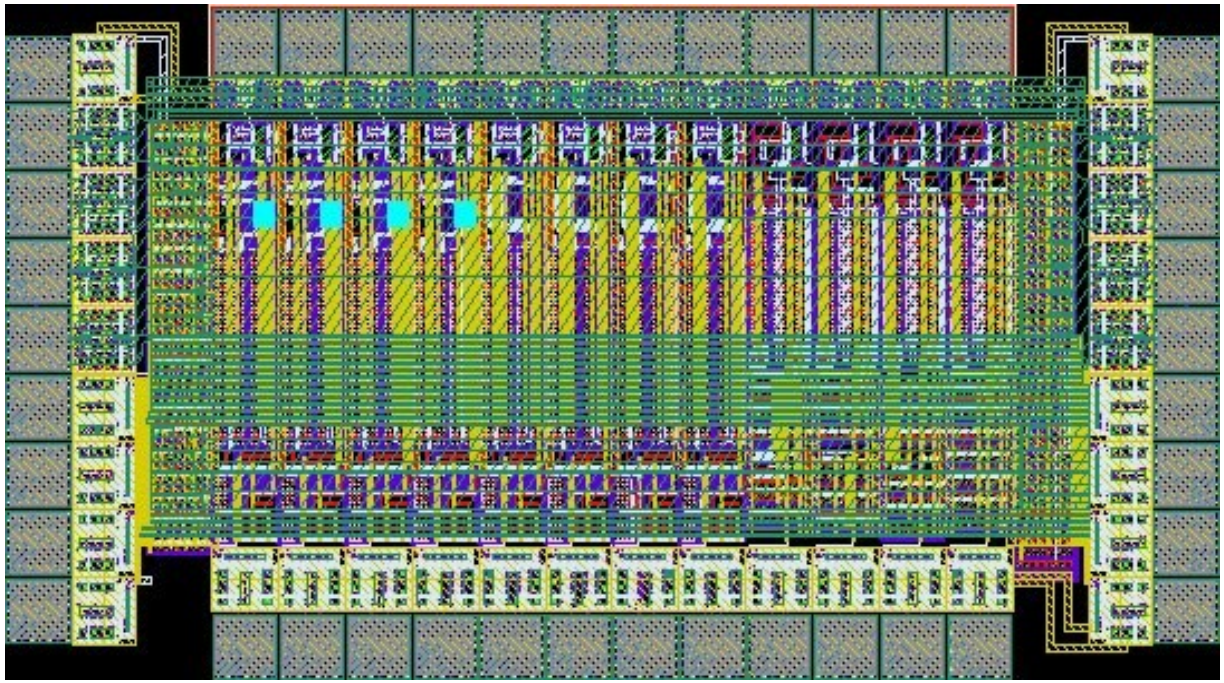


- Output amplitude versus Q_{in} for different gain setting

Layout of LumiCal front-end ASIC

Prototype ASIC containing 12 channels submitted in

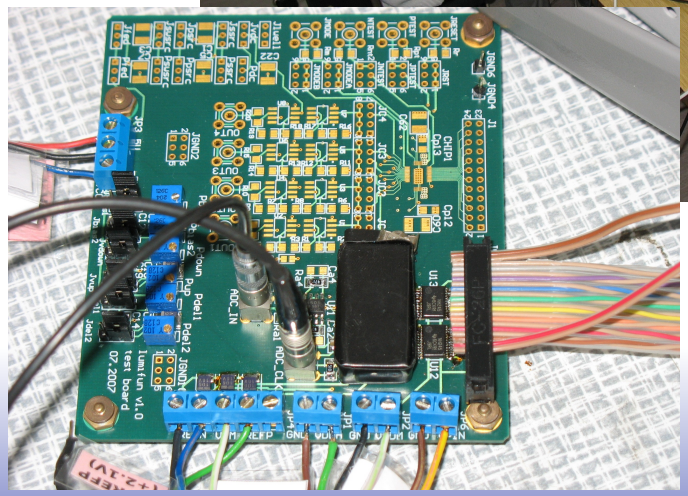
June 2007



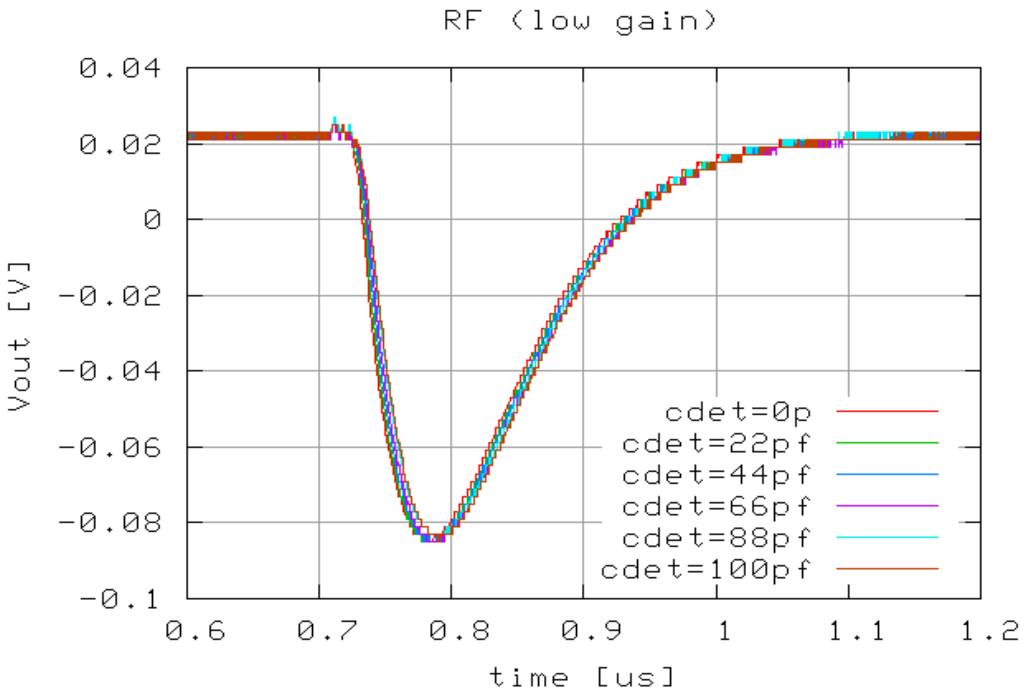
Pad Pitch 100 µm

First measurements

- 40 ASICs received
- PCB designed & produced
- Setup in progress
- Tests with generator and external capacitance started

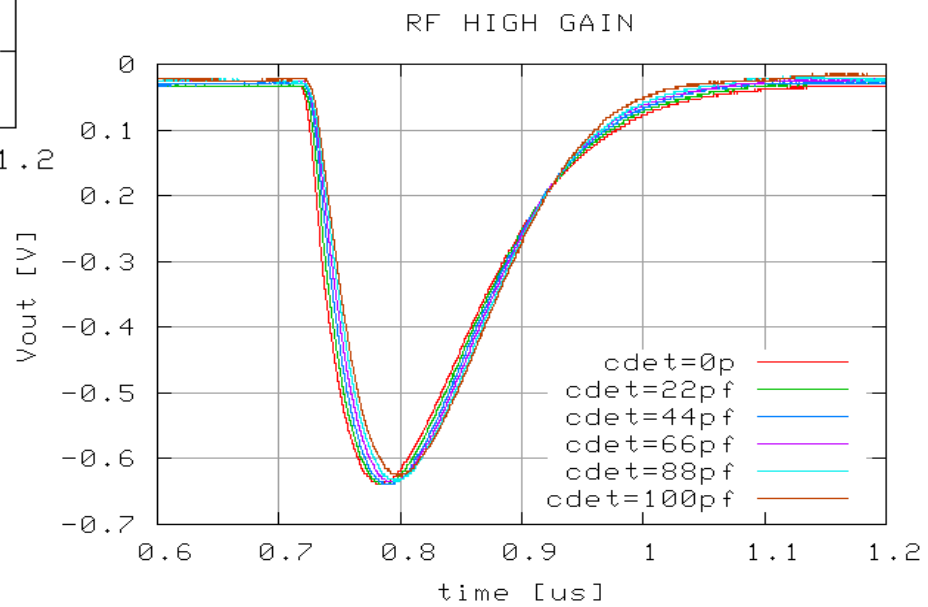


Pulse shape-passive R_f in feedback

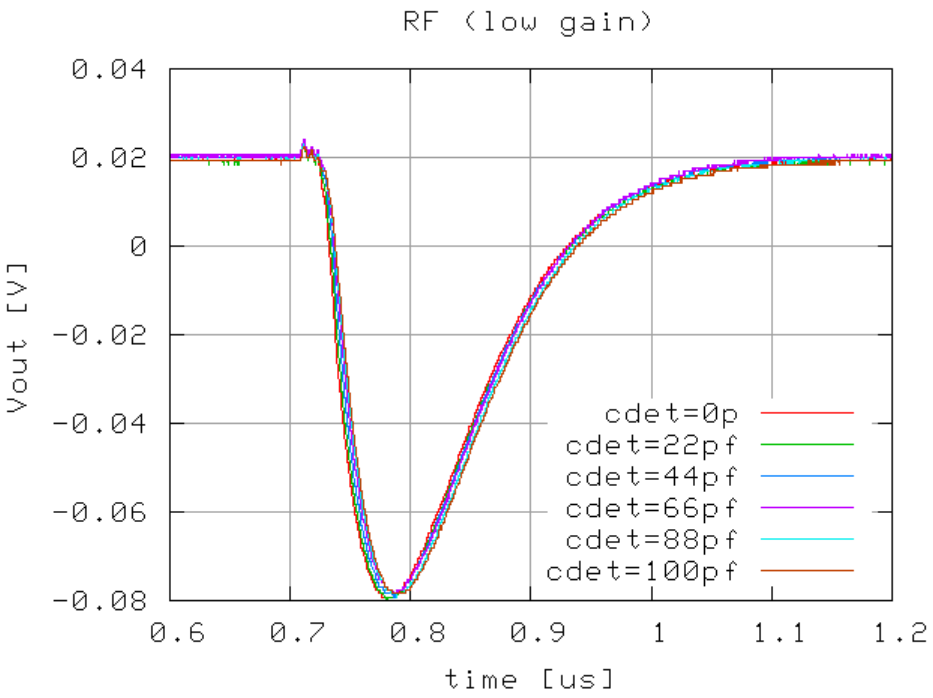


Preamp+PZC & CR-RC

Preamp with passive Rf

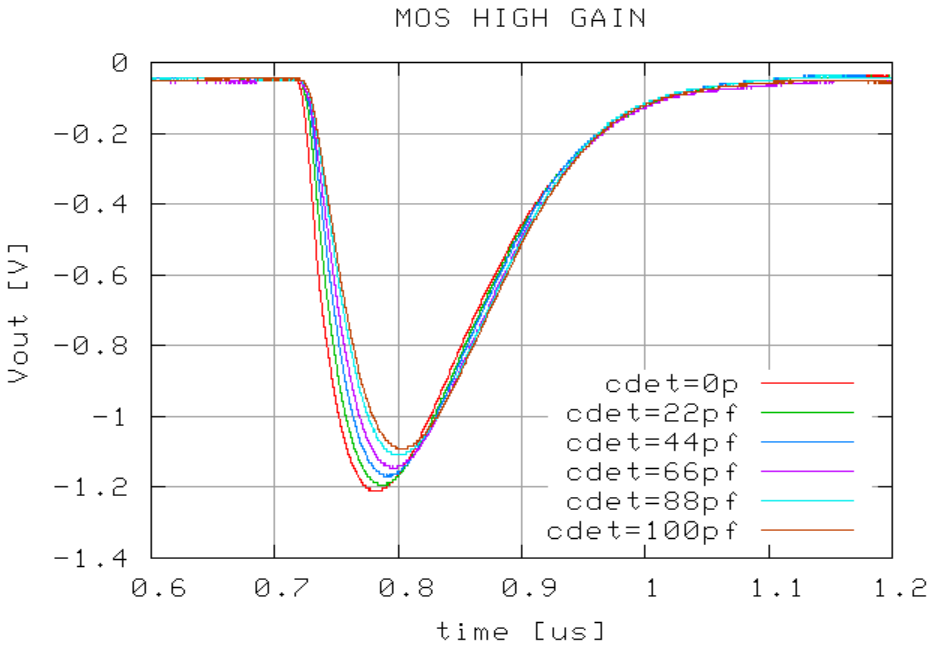


Pulse shape-MOS in feedback

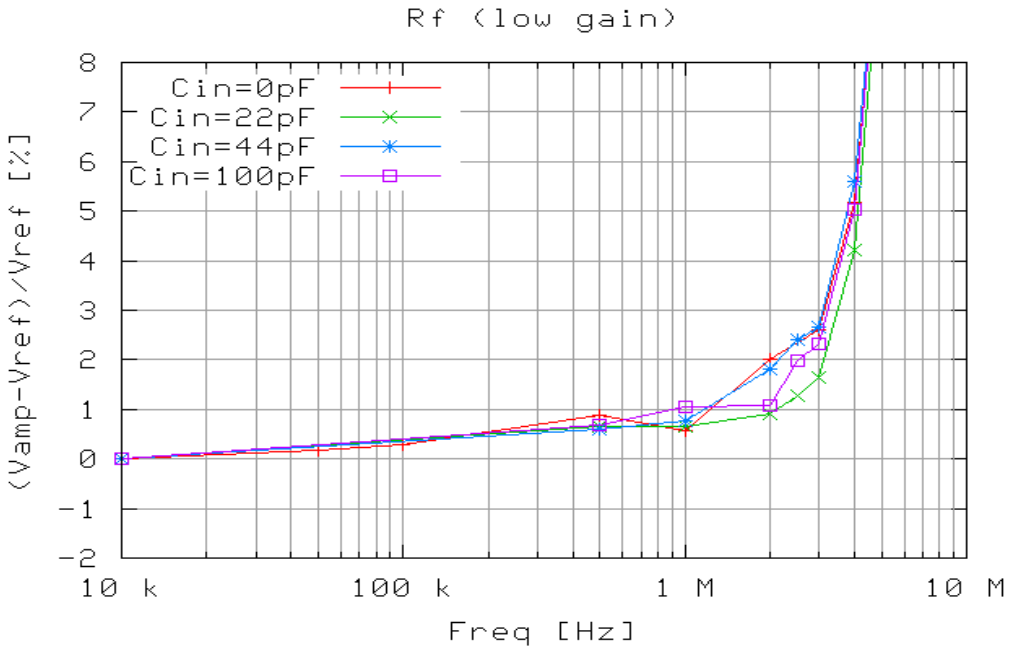


Preamp+PZC & CR-RC

Preamp with active MOS Rf

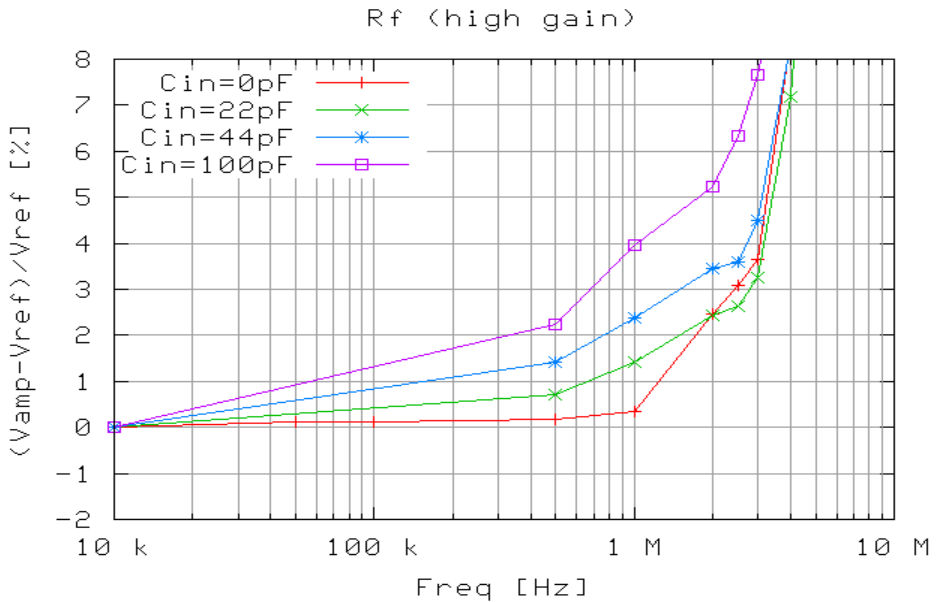


Amplitude vs frequency

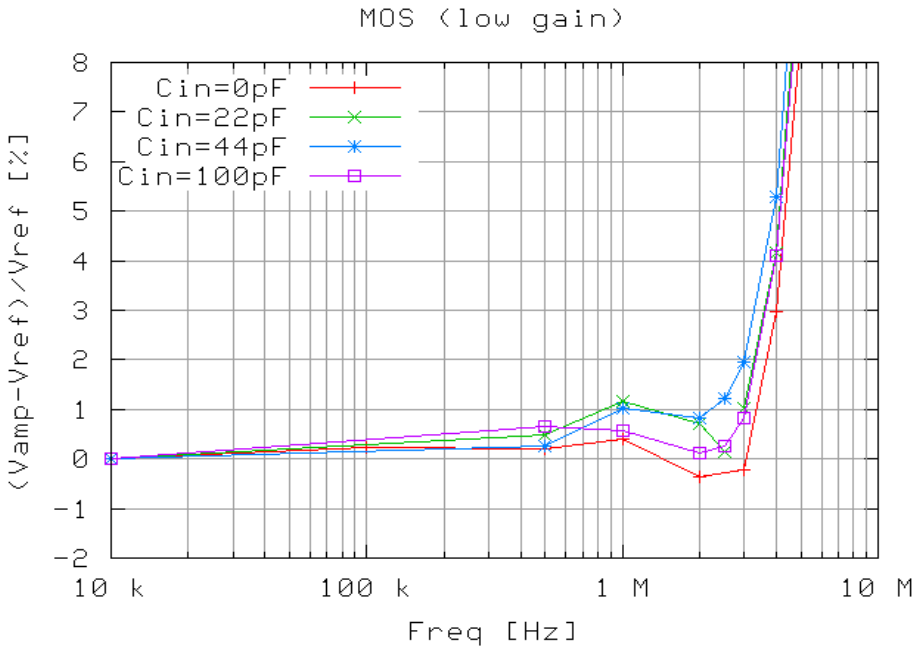


Preamp+PZC & CR-RC

Preamp with passive R_f

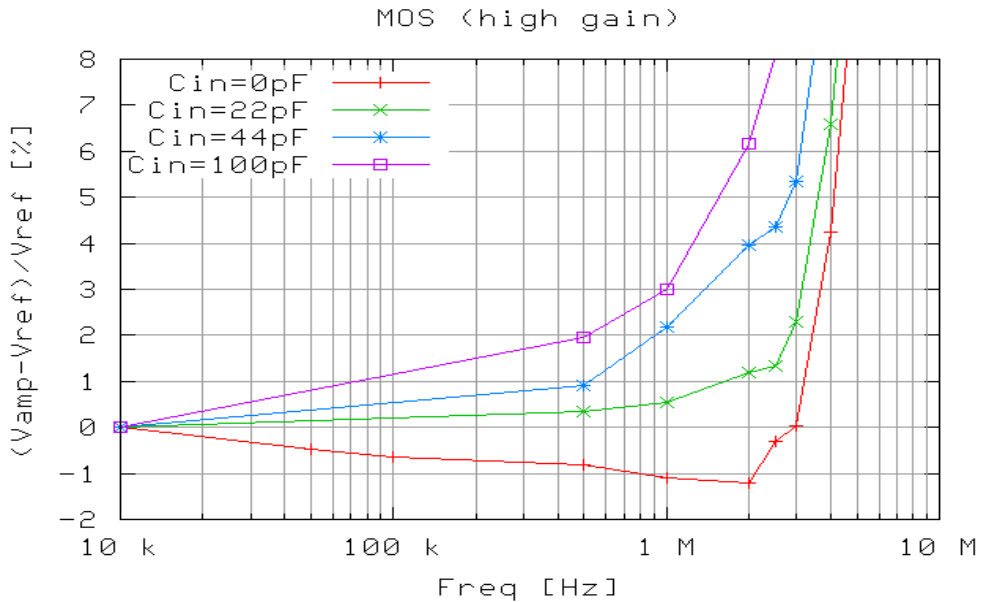


Amplitude vs frequency

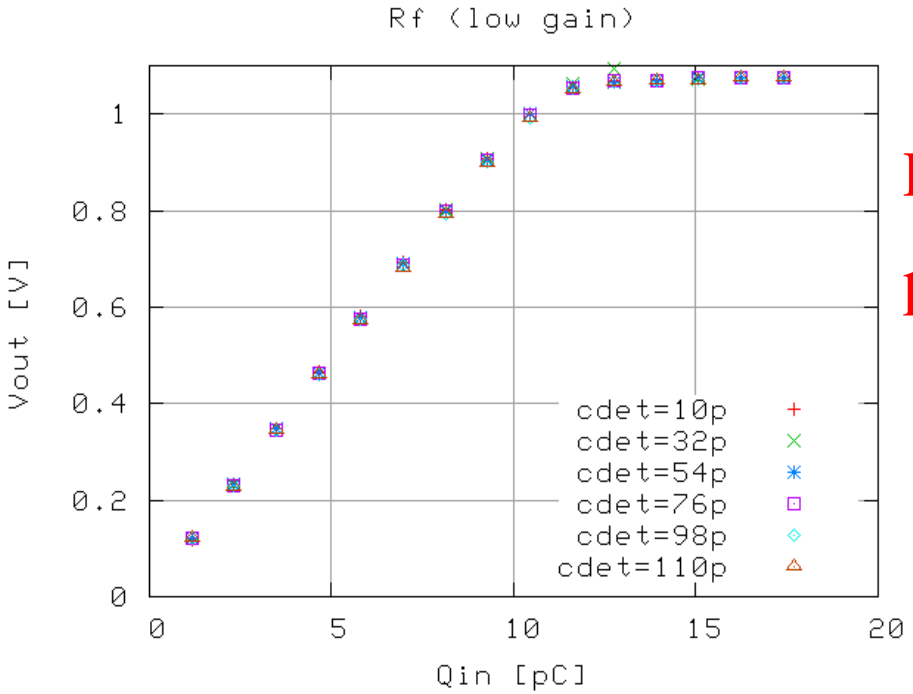


Preamp+PZC & CR-RC

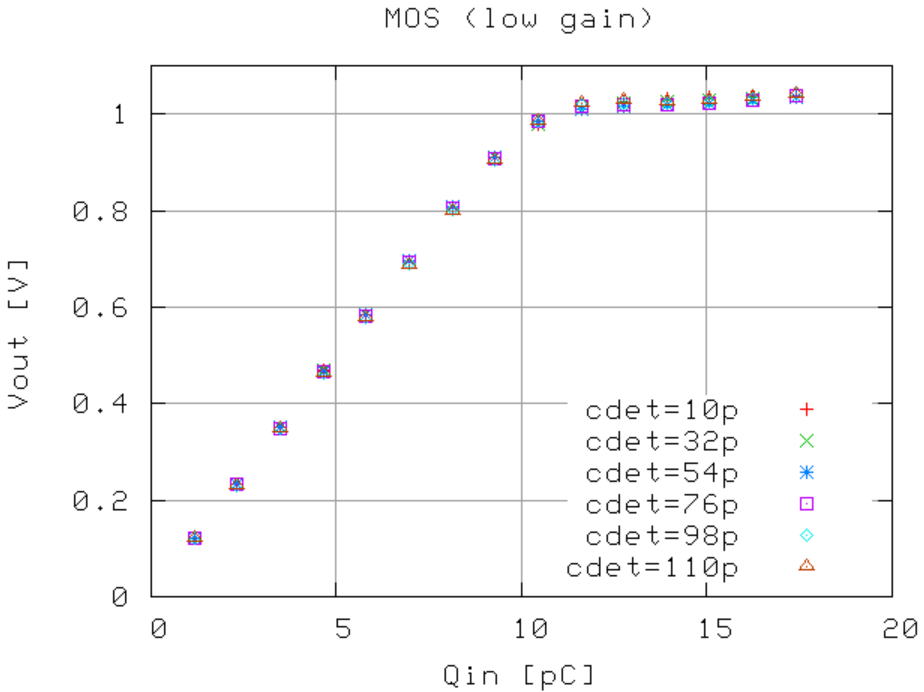
Preamp with active MOS R_f



Amplitude vs Q_{in}

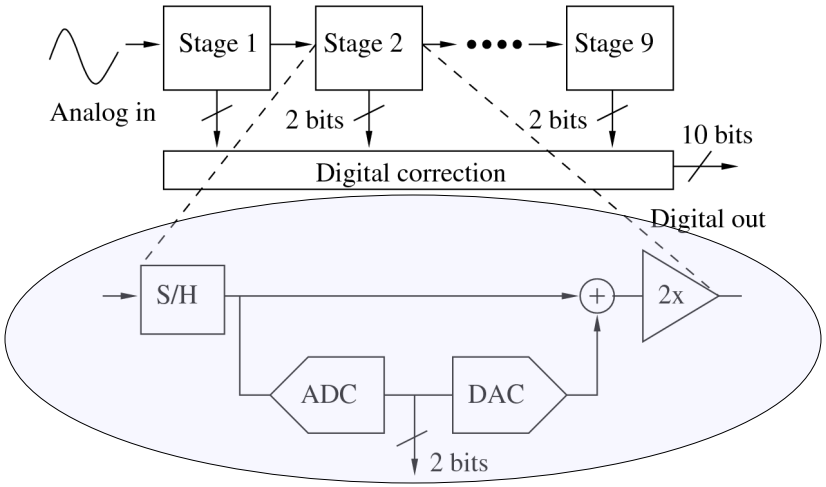


Preamp with passive R_f



Preamp with active MOS R_f

ADC architecture

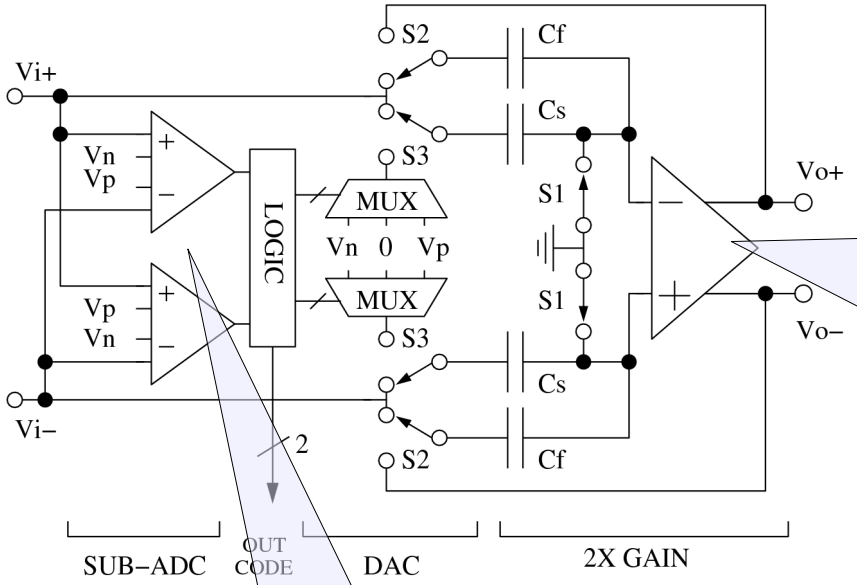


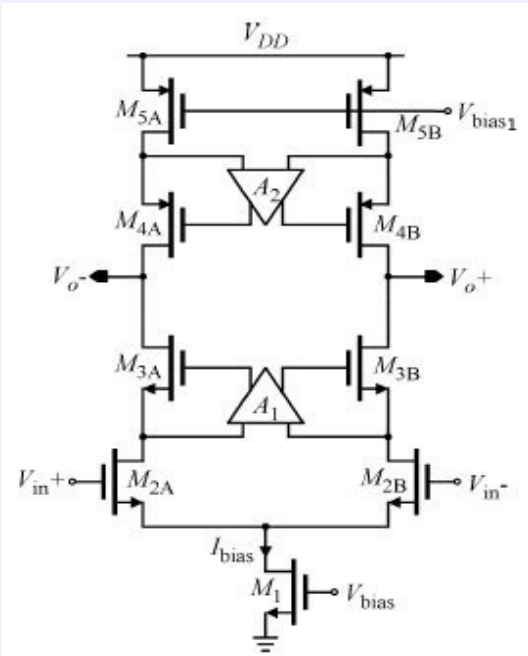
- 10 bit pipeline ADC
- 1.5 bit per stage
- Fully differential architecture

Pipeline advantages

- High throughput
- Robustness
- Power efficient
- Reasonable area

1.5 bit stage architecture

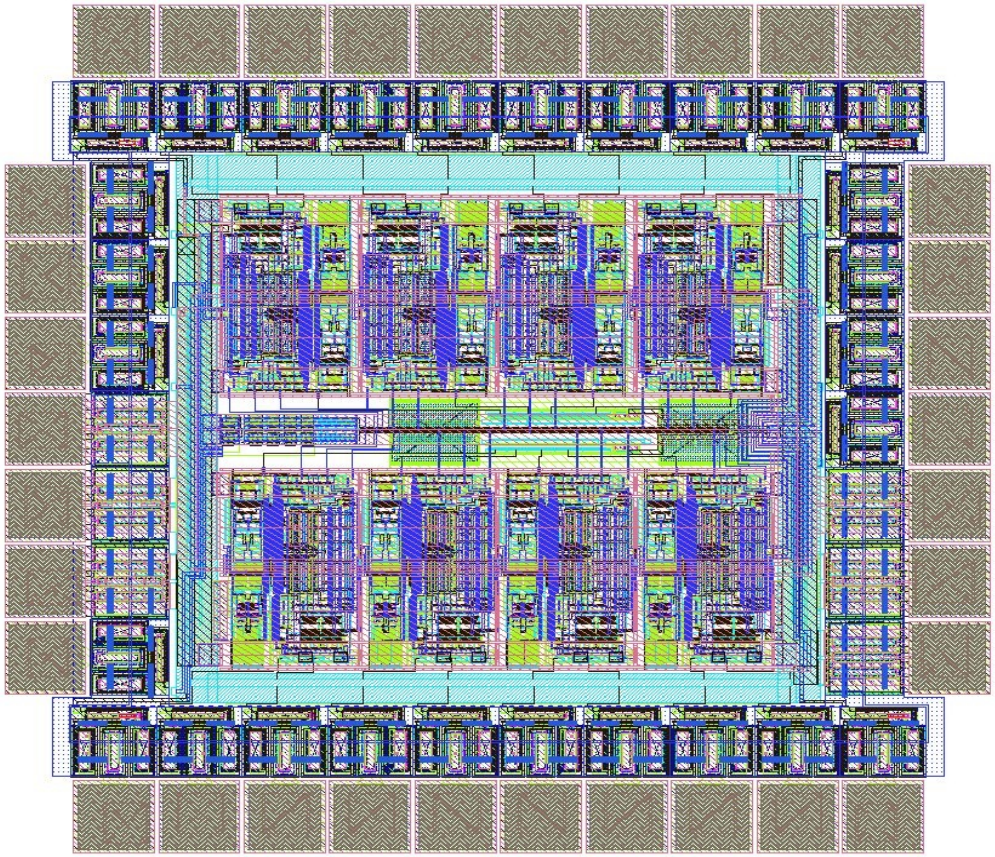




Dynamic latch comparators

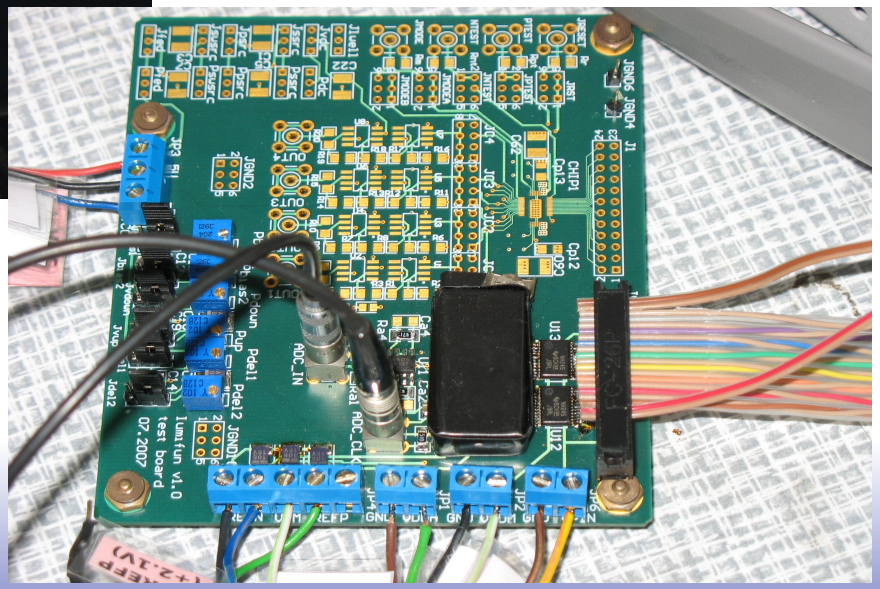
Layout of ADC blocks

Prototype ASIC containing 8 pipeline stages submitted in June

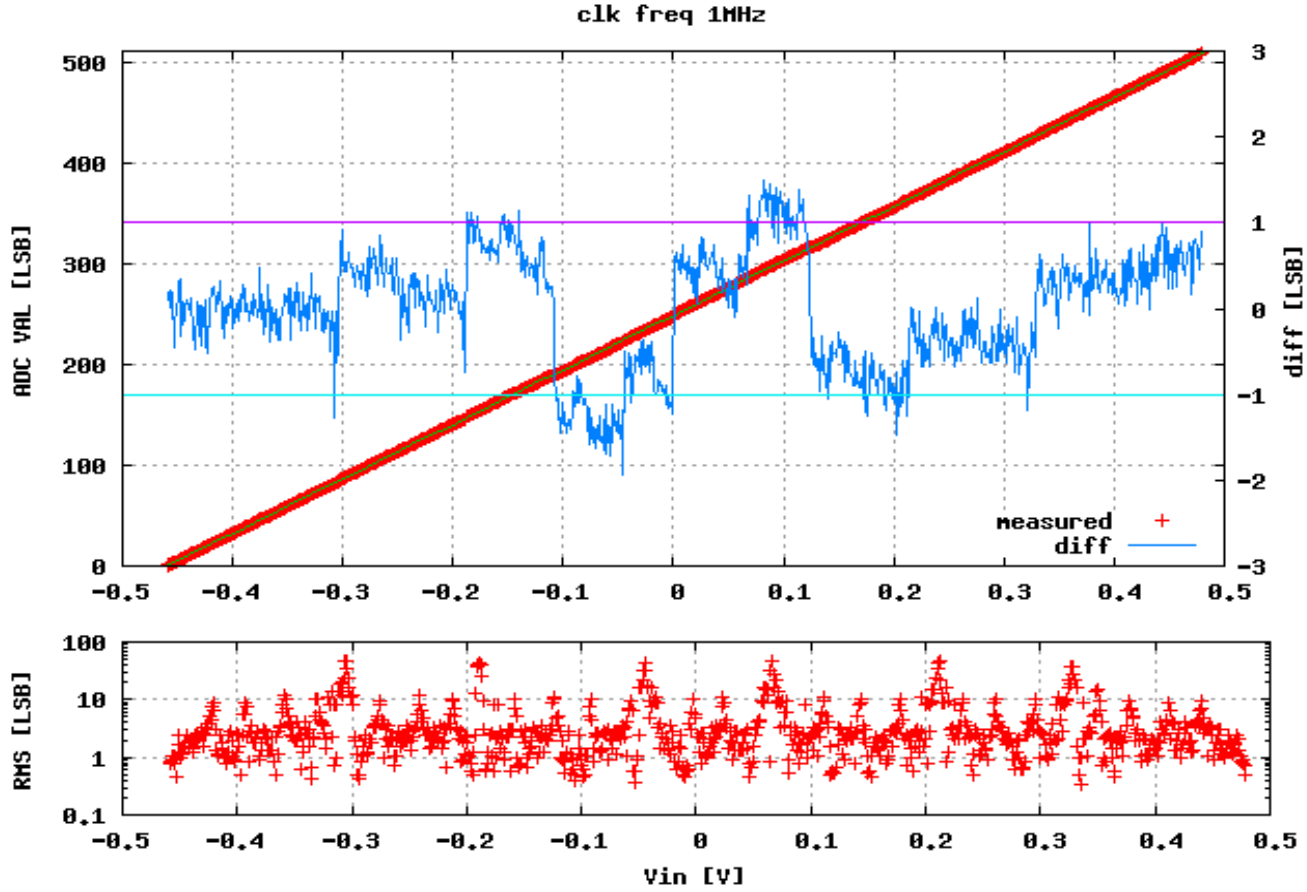


Only pipeline stages. No reference voltages. No digital correction. No ...

Setup in progress...



First test attempts...



Digital correction not applied properly

DC input signal

Other important setup problems (clk phase, etc...)

Development status

- First prototypes alive & ready to be tested!
- Measurements just started, quantitative results not yet available. ~2 months needed to complete tests.
- Some important issues (noise!) not yet touched
- Improvements in ADC setup needed for proper tests
- Discussion and decisions about future directions (i.e. sensor geometry, dynamic threshold?) needed

Summary & milestones

- June 2007 - first prototypes of the front-end and ADC functional blocks are being submitted
- ~December 2007 - tests of prototypes completed
- ~March 2008 – ADC components completed, front-end including S/H completed, prototypes submitted
- ~October 2008 - tests of ADC and front-end completed, design of supporting circuitry (biasing, DACs,...)
- ~December 2008 - submission of complete front-end and ADC prototypes
- ~June 2009 - tests of prototype ASICs completed