Deep submicron readout chip development

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on behalf of

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SiD phone meeting August 3d 2007

Outline

- Goals in CMOS 130nm
- Present results
- Chip 2 and further tests
- Next chip

Status and Goals

	This chip
• Full readout chain integration in a single chip	yes
- Preamp-shaper	yes
- Zero-suppression decision (threshold analog sums)	yes
- Pulse sampling: Analog pipe-lines	yes
- On-chip digitization: ADC	yes
- Buffering and pre-processing: Centroids, least squares fits	no
- Lossless compression and error codes	no
- Calibration and calibration management	no
- Power switching (ILC timing)	no

• CMOS 130nm		2006-7	yes
• CMOS 90nm	128 ch.	2008	-
• 512-1024 channels planned			4 channels

Targeted

- Amplifier: 30 mV/MIP gain
- Shaper: 700ns-3 μs
- Sparsifier: threshold on analog sum
- Sampler: 16-deep
- ADC: 10-bit

- Noise:
  Measured with 180nm CMOS:
  375 + 10.5 e-/pF @ 3 μs shaping, 210μW power

Front-end in 130nm

130nm CMOS:

- Smaller
- Faster
- Lower power
- Will be (is) dominant in industry

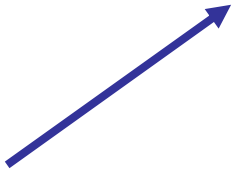
- (More radiation tolerant)

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date
- Crosstalk (digital-analog)

UMC Technology parameters

	180 nm	130nm
• 3.3V transistors	yes	yes
• Logic supply	1.8V	1.2V
• Metals layers	6 Al	8 Cu
• MIM capacitors	1fF/mm²	1.5 fF/mm²
• Transistors	Three Vt options	Low leakage option



Useful for analog storage during < 1 ms

2006-7 Chips Summary

130nm

Under test

Chip #1 (4 channels)

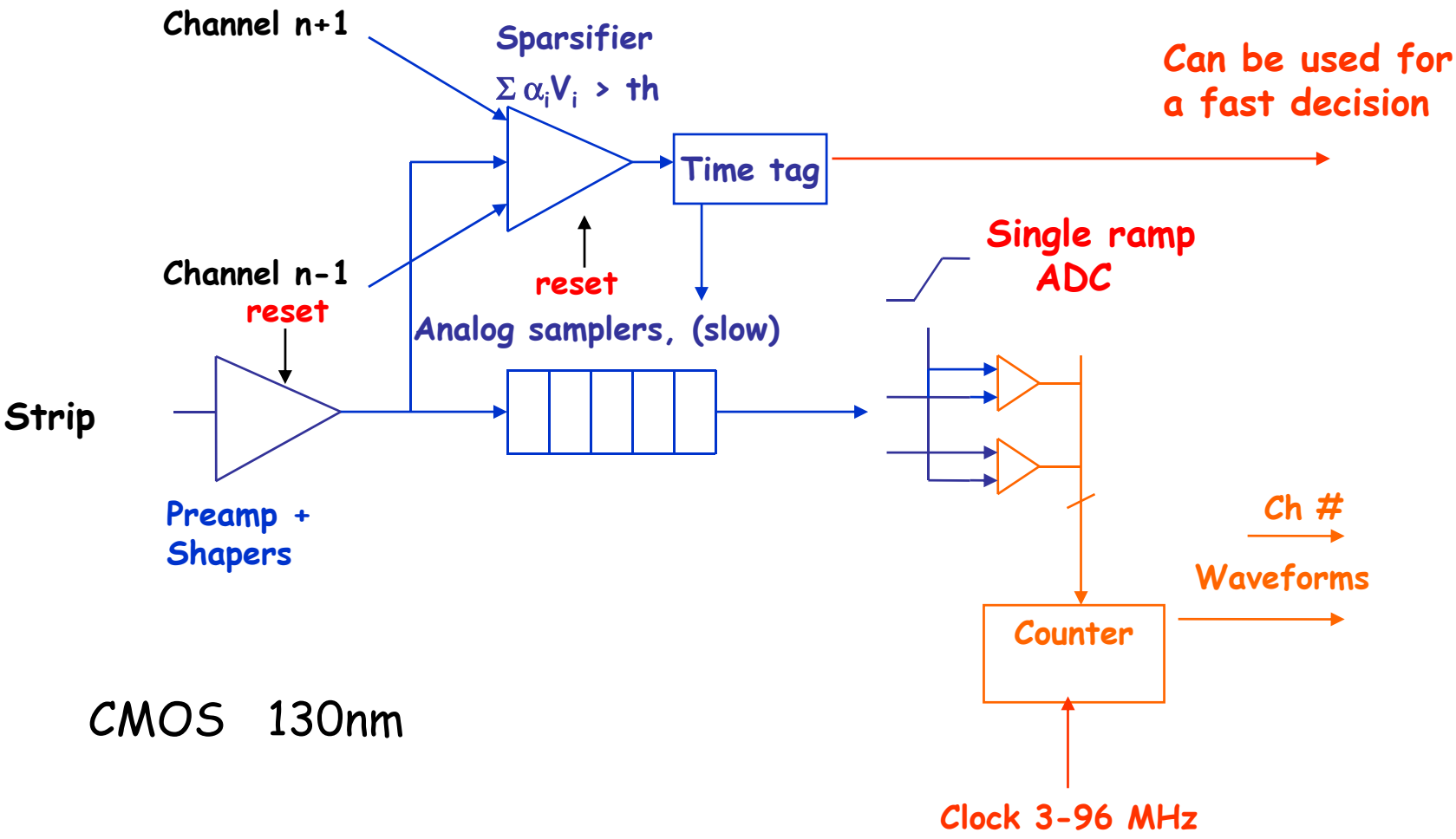
- Preamp-shapers + Sparsifier
- Pipeline 1
- ADC
- Digital

(Almost) Under test

Chip #2 (One channel)

- Preamp-shapers + Sparsifier
- DC servo
- Pipeline 2
- DAC
- Test structures: MOSFETS, passive

4-channel chip



CMOS 130nm

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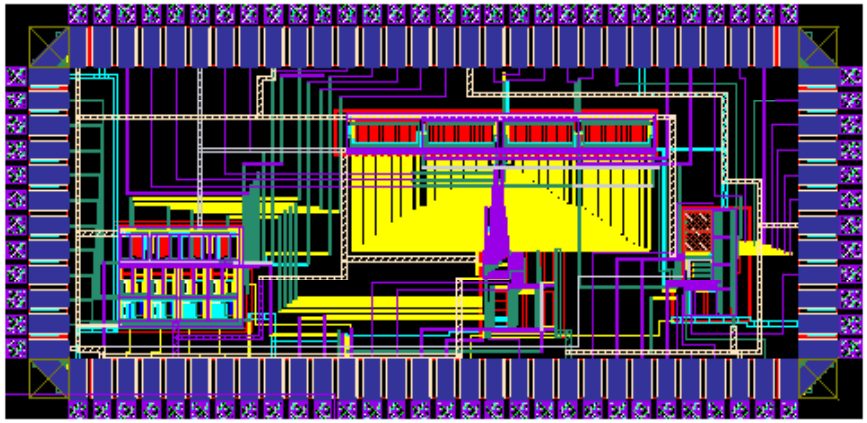
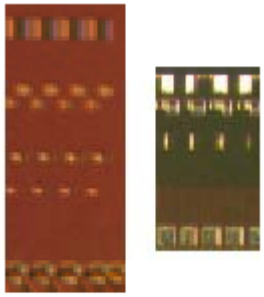
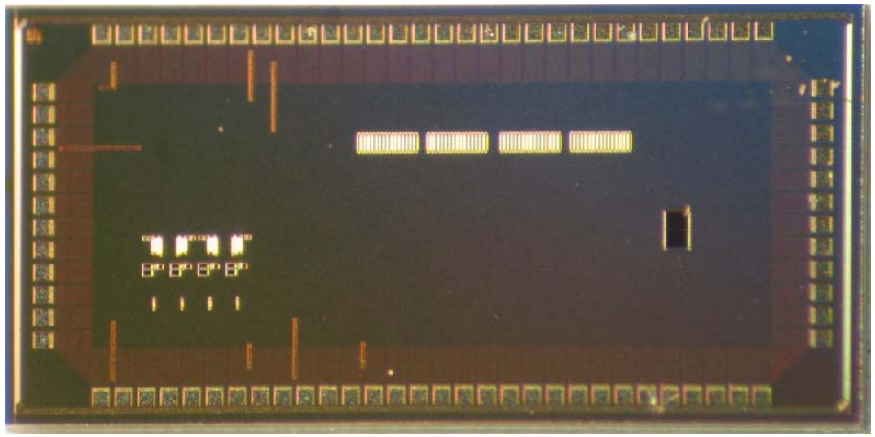
Silicon



Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm



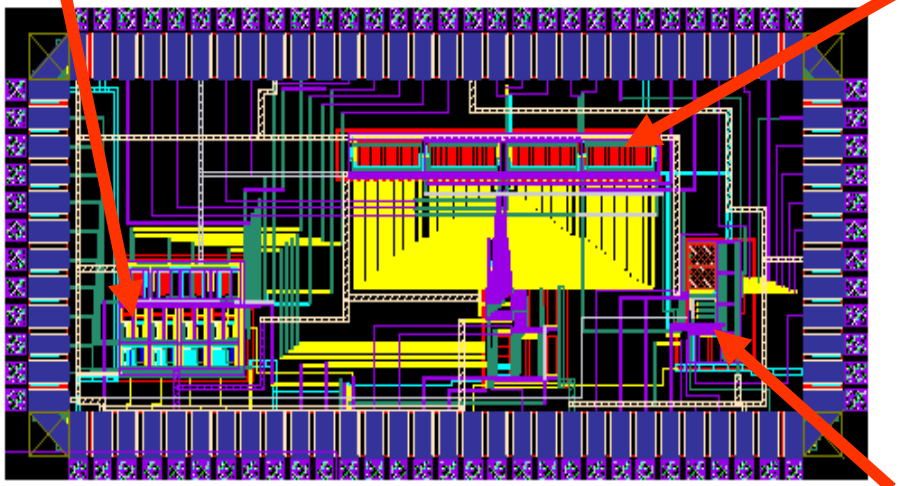
Picture

130nm chip

LAYOUT :

Amplifier, Shaper, Sparsifier 90*350 µm2

Analog sampler 250*100 µm



A/D 90*200 µm

Layout of the 130nm chip including sampling and A/D conversion

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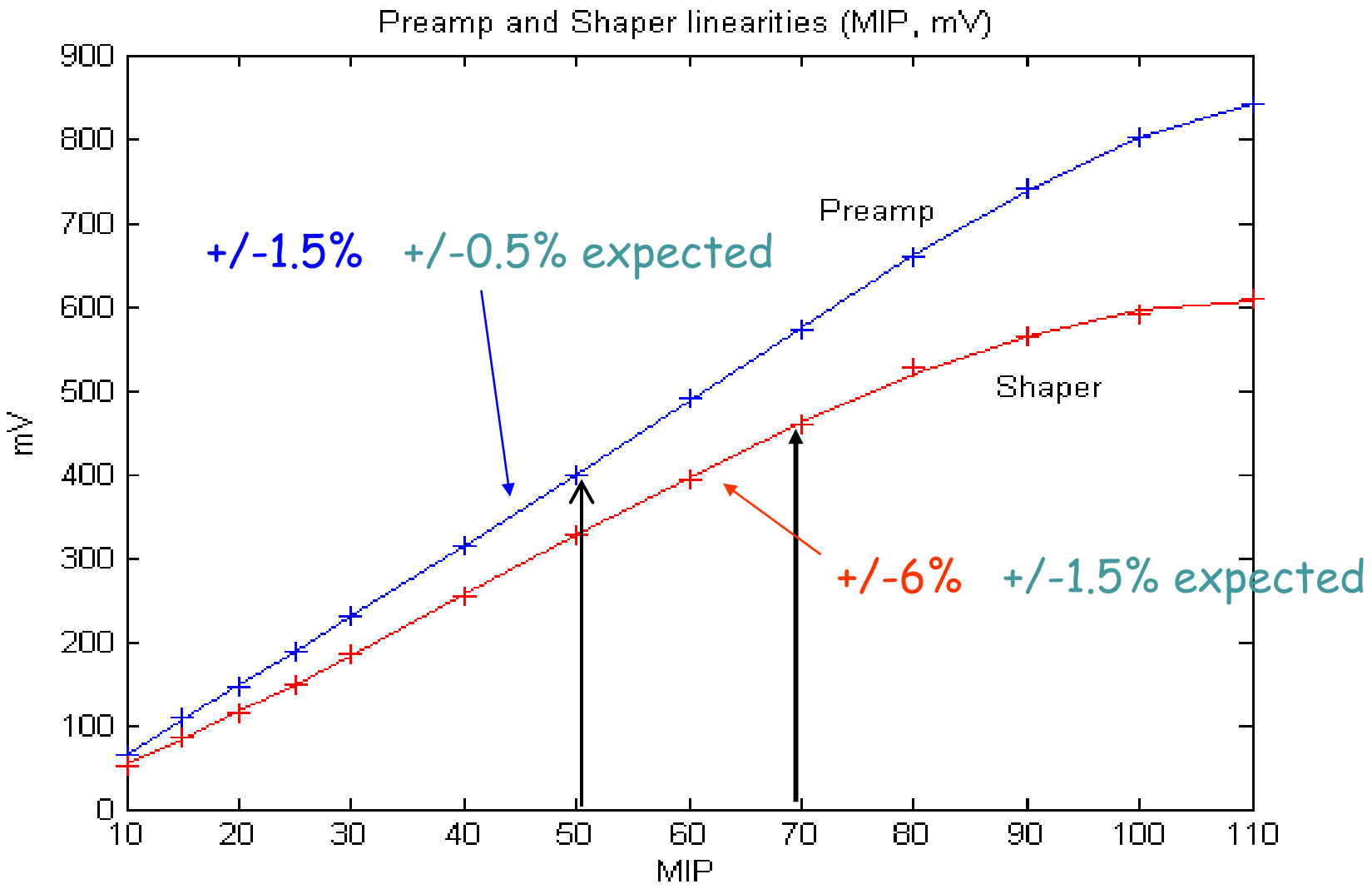
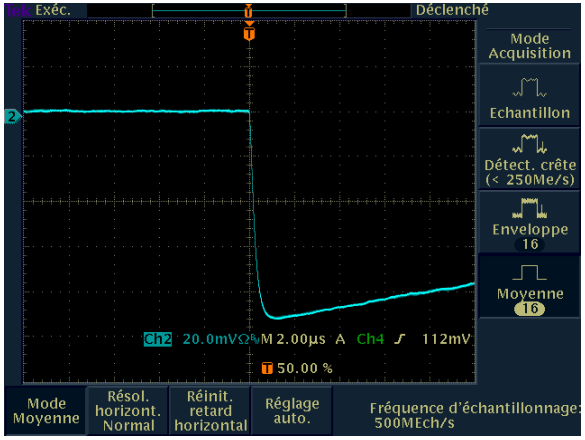
Linearities 180nm chip

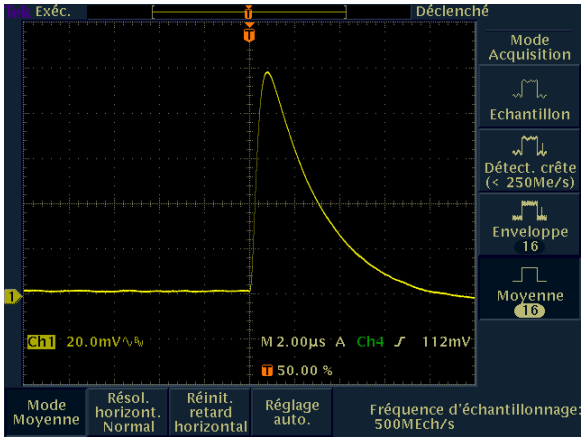


Chip 130nm

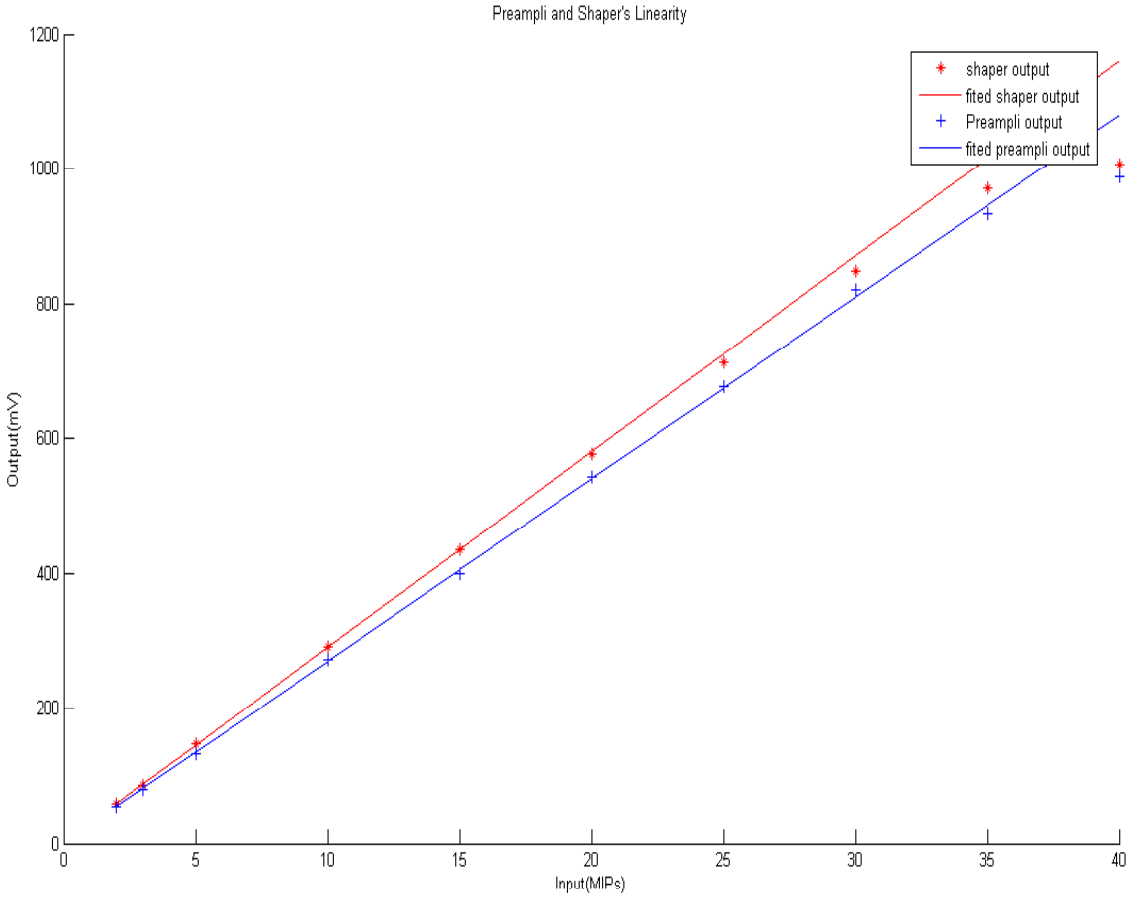
MEASUREMENT : GAIN - LINEARITY

Preamp Output





Shaper output

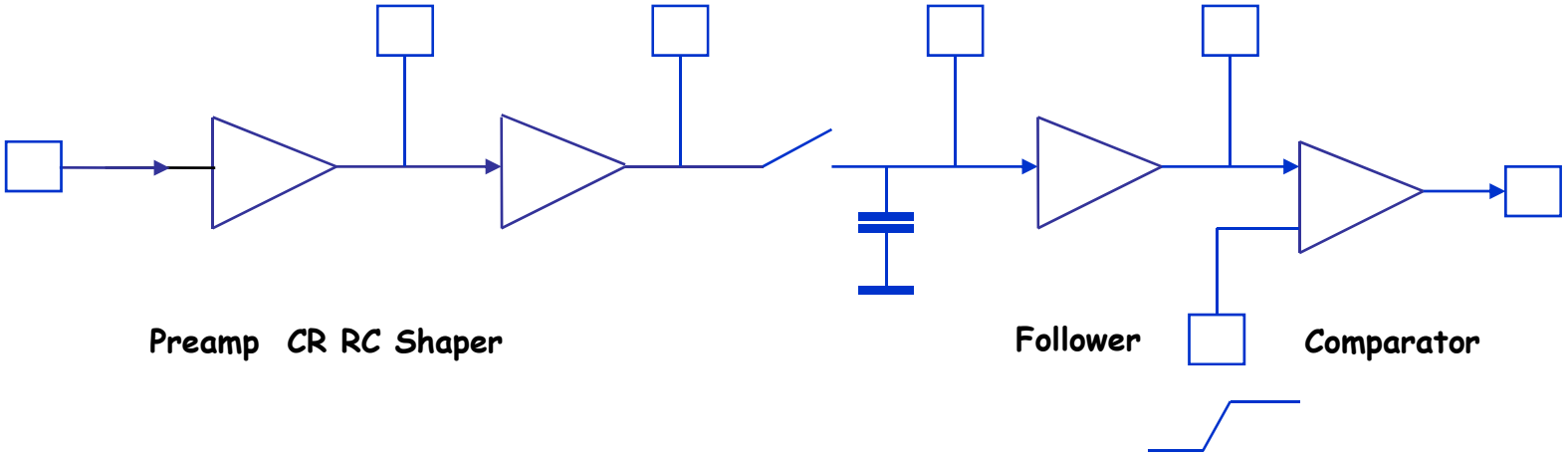


Preamp :

- Gain = 27mV/MIP
- Dynamic = 20MIPs (<1%)

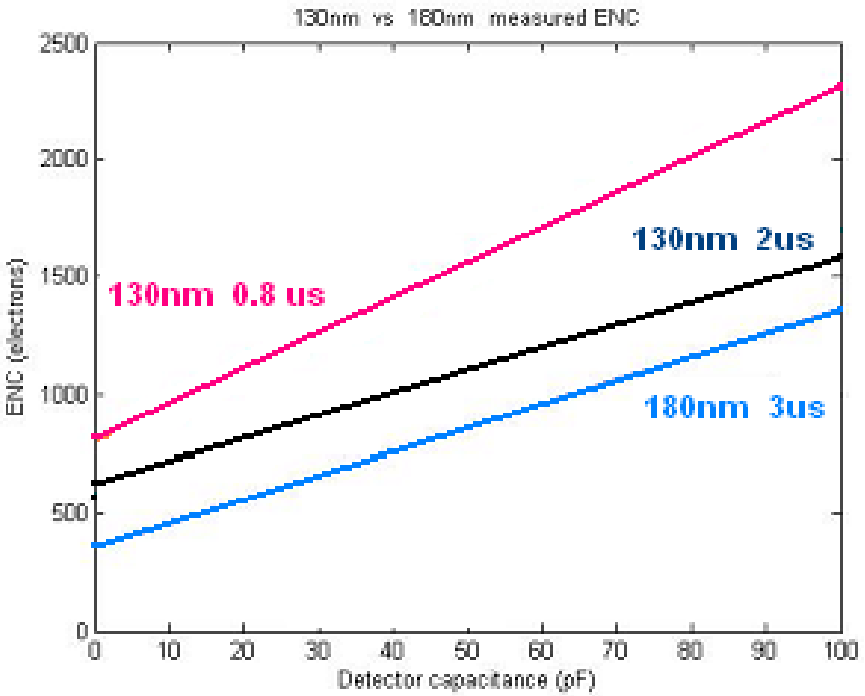
Shaper :

- Gain = 29mV/MIP
- Dynamic = 20MIPs(<1%)


Preamp
CR RC Shaper
Follower
Comparator

130nm chip noise results

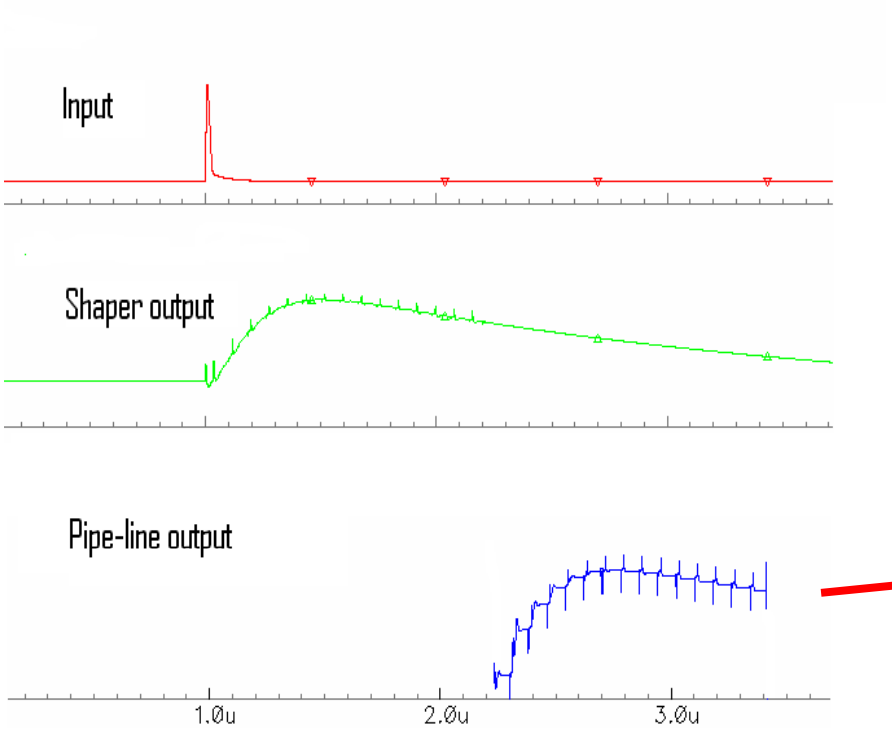
Gain OK: 29 mV/MIP — **OK**
Dynamics: 30 MIPs @ 5%, 20 MIPS 1% — **OK**
Peaking time: .8 – 2.5µs (.7 – 3µs targeted)

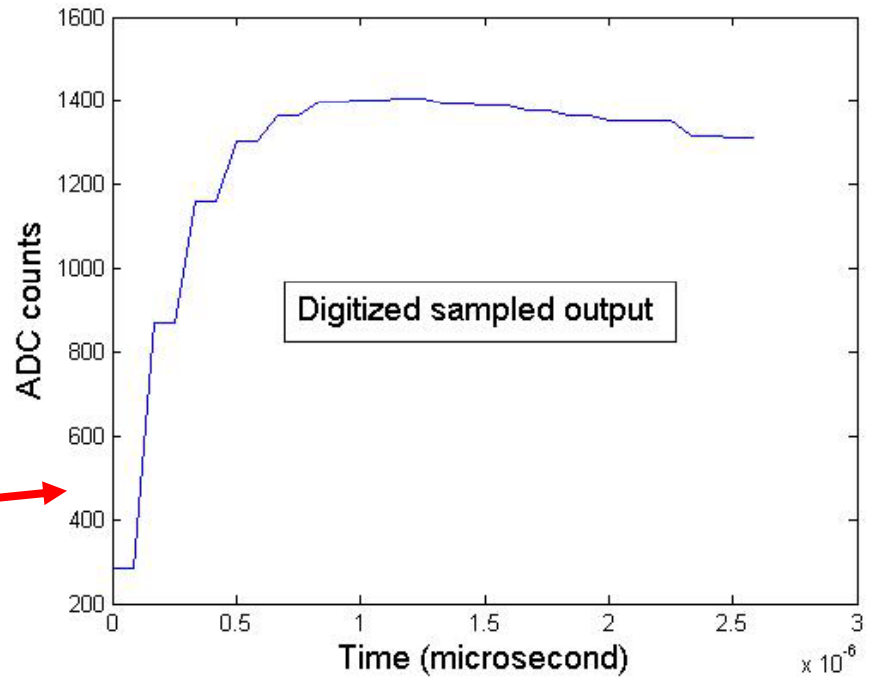


Power (Preamp+ Shaper) = 245 µW

Noise:	130nm @ 0.8 µs :	850 + 14	e-/pF	245 µW	(150+95)
	130nm @ 2 µs :	625 + 9	e-/pF		
	180nm @ 3 µs :	375 + 10.5	e-/pF	210 µW	(70+140)

Analog pipeline output



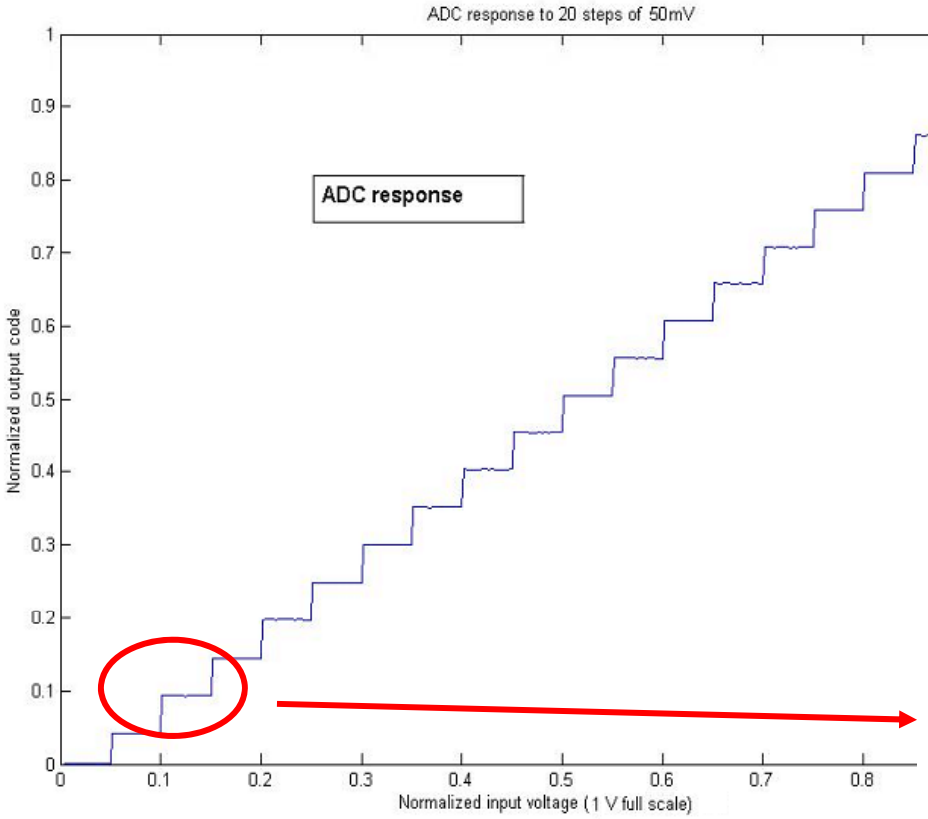


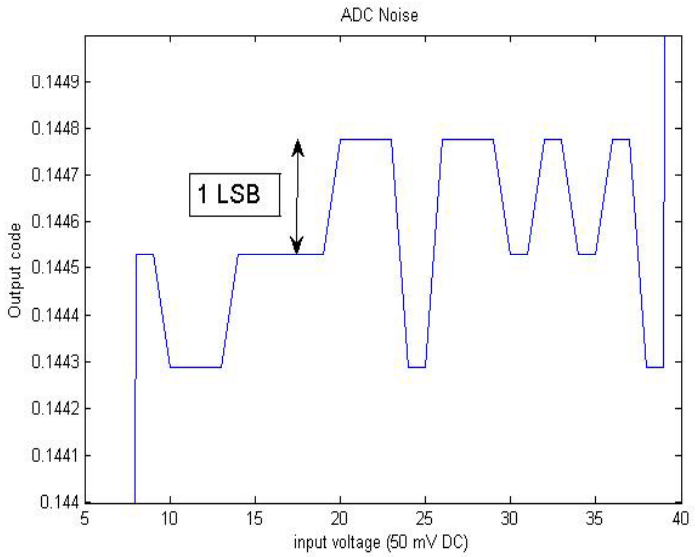
Simulation of the analog pipeline

Measured output of the ADC

1 ADU= 500 µV

ADC noise


ADC response to 20 steps of 50mV
ADC response
Normalized output code
Normalized input voltage (1 V full scale)


ADC Noise
1 LSB
Output code
input voltage (50 mV DC)

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130-1 tests to come

Measure ADC extensively

- Linearities
  Integral, differential
- Noise
  Fixed pattern, random
- Speed: Maximum clock rate
- Effective number of bits

130nm Chip 2

LAPP Annecy le Vieux (D. Fougeron)

One channel test version in 130nm including:

- Preamp + shaper
- Improved pipeline (output buffer)
- Calibration channel (calibration caps)
- Calibration DAC

Chips presently under test

If OK, all analog blocks will be validated for a multi-channel version in 130nm aiming to read a real detector.

130-2 tests to come (LAPP Annecy)

Measure improved pipeline extensively

Denis Fougeron's (LAPP) design

- Linearities
  Integral, differential
- Noise
  Fixed pattern, random
- Speed
  Maximum clock rate
- Droop
  Hold data for 1ms at the ILC

Outline

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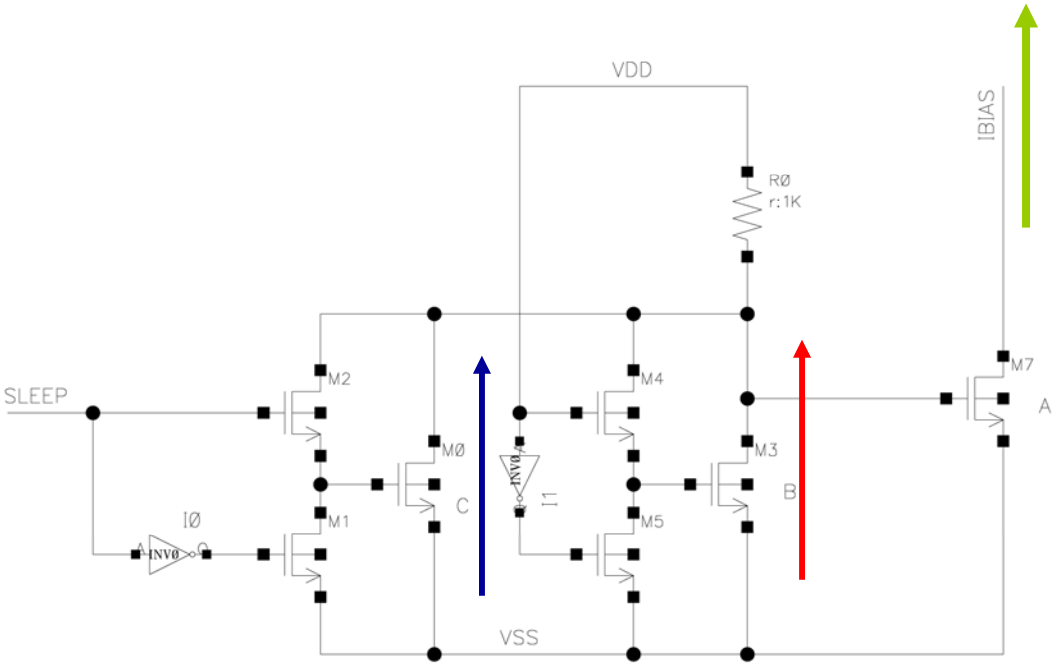
Power cycling

Switch the current sources between zero and a small fraction (10^{-2} to 10^{-3}) of their nominal values



This option switches the current source feeding both the preamplifier & shaper between 2 values to be determined by simulation.
Zero or a small fraction (0.1% - 1%) of biasing current is held during « power off ».

Zero-power option tested on 180nm chip with a 2 ms deadtime under improvement

Chip 130nm-3

Equip a detector

- Experience from lab test bench (laser + source) and 2007 beam-tests
- 130nm chips 1 + 2

- 128 channels with :
  - Preamp-shapers + sparsifier
  - Pipeline
  - ADC
  - Digital
  - Calibration
  - Power cycling

Planned Digital Front-End

- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data lossless compression
- Tools
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs
  - Need for a mixed-mode simulator

Some issues with 130nm design

- Noise likely modeled pessimistic, but measured acceptable

  90nm could be less noisy (Manghisoni, Re, Perugia 2006)
- Lower power supplies voltages reducing dynamic range
- Design rules more constraining
- Some (via densities) not available under Cadence

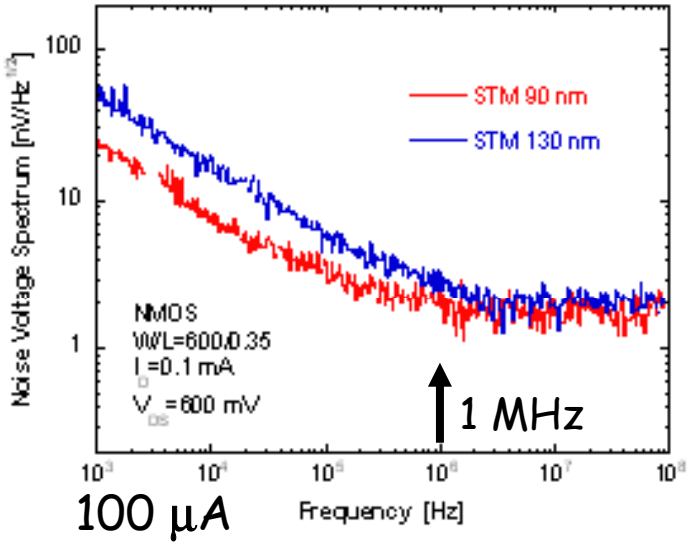
  Calibre (Mentor) required.
- Low Vt transistors leaky (Low leakage option available at regular Vt)

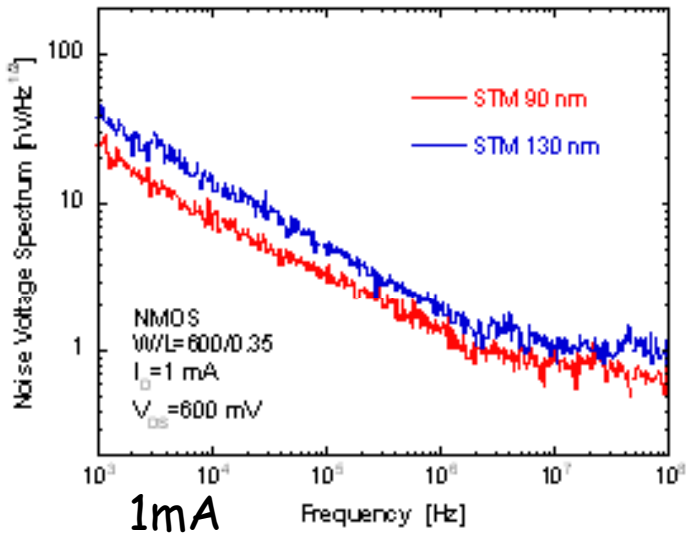
Manageable, UMC design kits are user friendly,
Europractice very helpful.

130-90nm noise evaluation (STM process)

Noise and inversion region

L. Ratti et al *FE2006 Perugia*





- At low drain current both devices work in the weak inversion region → channel thermal noise is roughly the same for both devices
- At high drain current, a significant difference in the channel thermal noise can be detected ← device from the 90 nm technology works closer to weak inversion region
- Better 1/f noise performance provided by the STM 90 nm technology

Conclusion

These CMOS 130 designs and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels), at:

- DC power under 500µW/ch
- Silicon area under 100 x 500 μm^2/ch

The End …