LCFI Testing and Electronics

Andrei Nomerotski (U.Oxford)

ALCPG2007, 25 Oct 2007

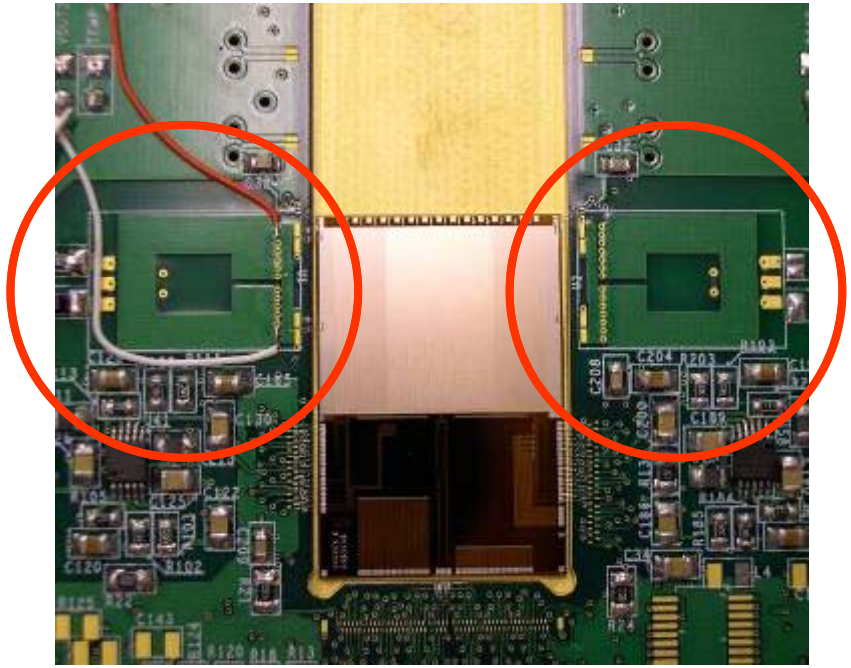
- Clock drive
- External electronics and DAQ
- Radiation damage studies
- Ladder design

Driving Clock

- CPCCD have considerable capacitance and need to run at 50 MHz
- Translates to 20 A clock current to drive 40 nF to 2 V – this is a major challenge for CPCCD
  - 1 mm of bond wire = 1nH = 0.3 Ohm @ 50 MHz → need bump bonding
- Two approaches
  - Transformer Drive
  - **Custom ASIC**, commercial chips not adequate

Transformers as Clock Drive

- Planar air core transformer:
  - High voltage/Low current → Low voltage/High current
- Design of 16:1 transformer ratio in 10 layer PCB
  - Can be driven by commercial RF amplifier through 50 Ohm cable
  - Low cost

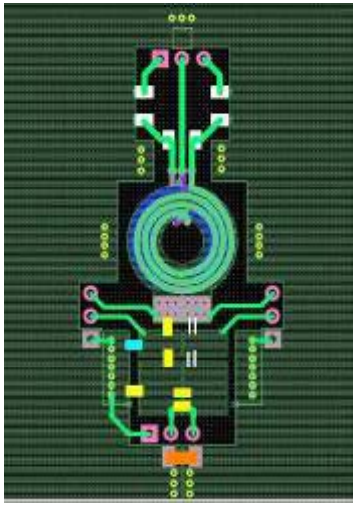


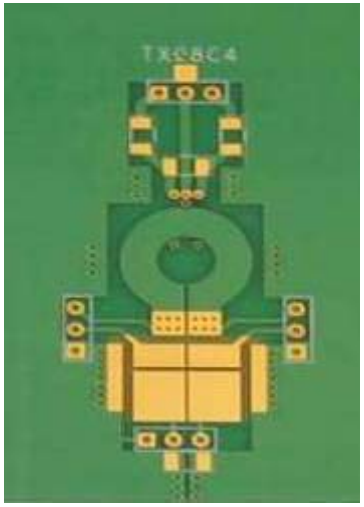
MB4.3 with transformer drive

- Produced and tested in 2006
  - See X-ray hits at 45 MHz
  - Limitations from imbalance between phases and noisy RF generator

New Transformers

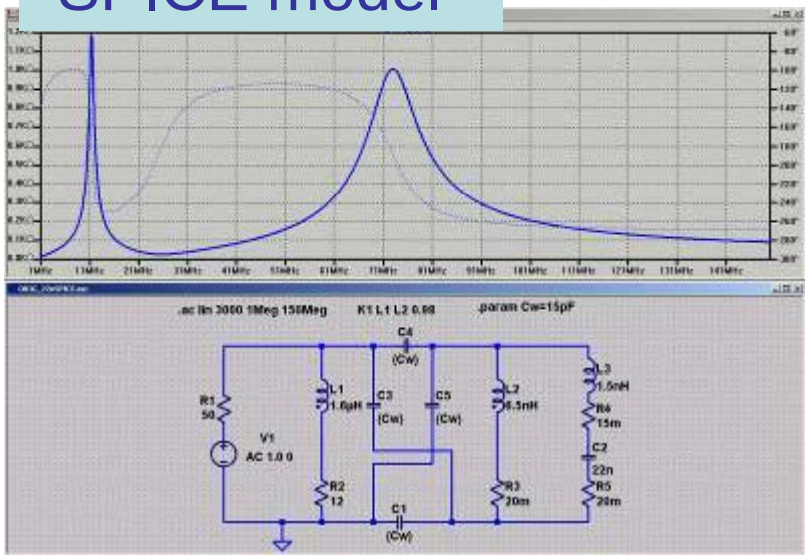
- Phase imbalance caused by parasitics
  - Can be removed by capacitance in series
- New, improved design prepared
  - Different turns ratios and loading schemes
  - Circular spiral winding
- Testing of standalone transformers started
  - Good agreement with simulations: frequency scans



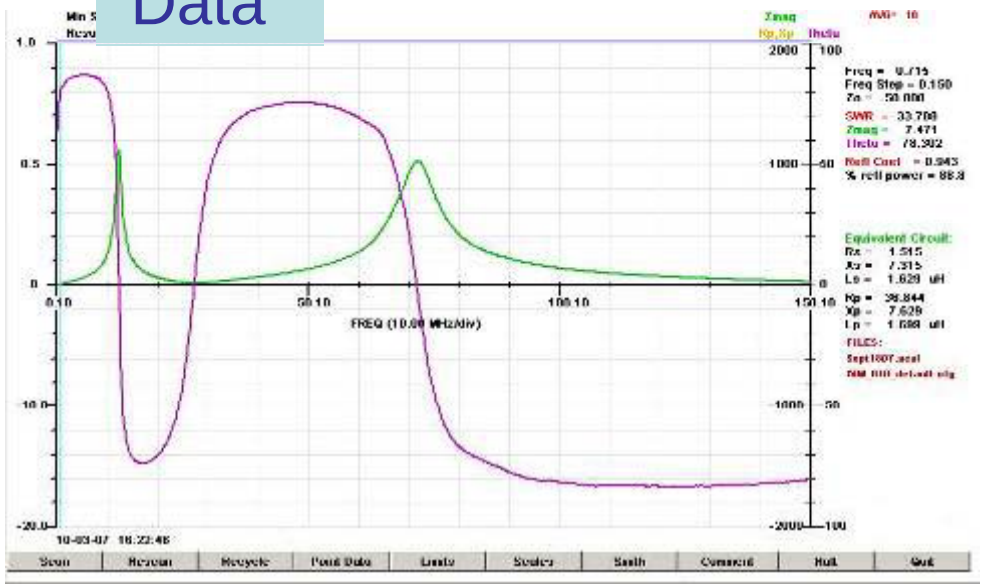


- Transformers are backup after success of CPD1

SPICE model

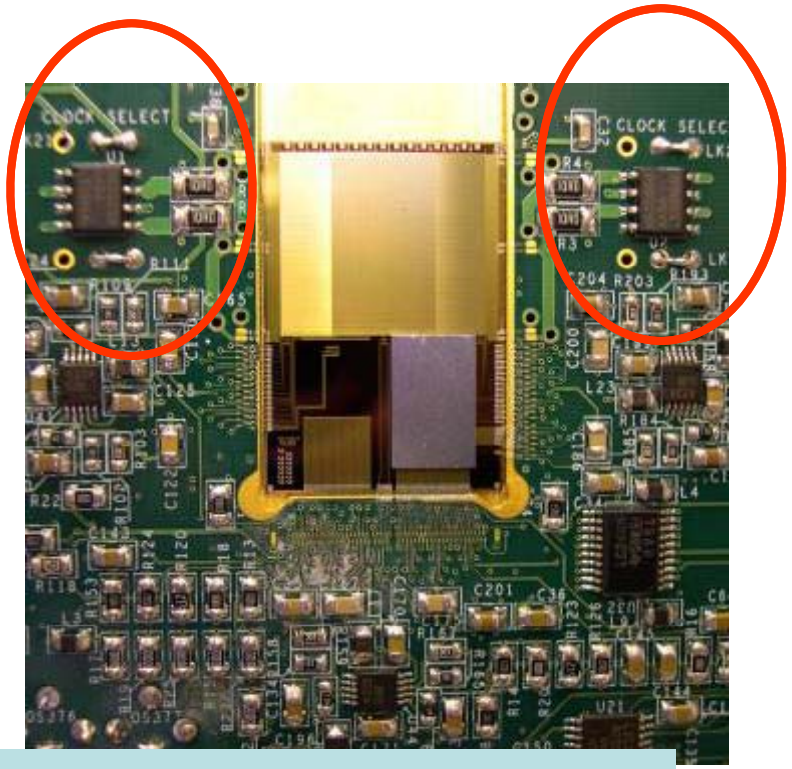


Data



Commercial Clock Drive

- Initial testing performed using MAX5057 commercial chip
- Used for small CPC2
- Limited to 5 MHz
  - Max current 8 Amp

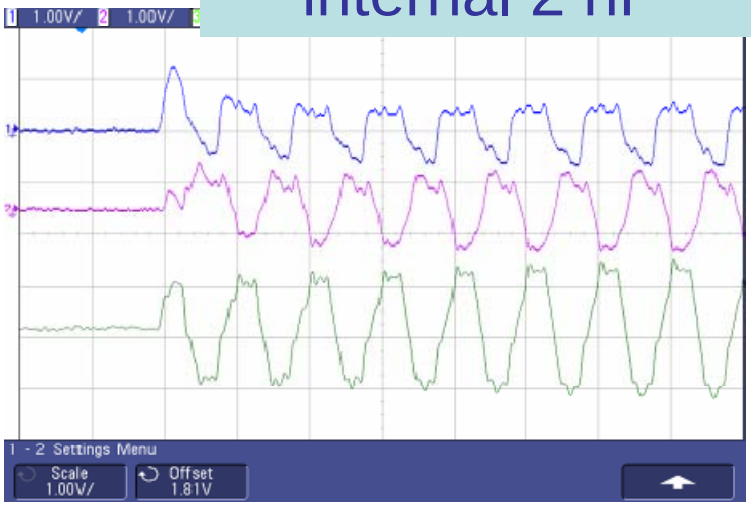


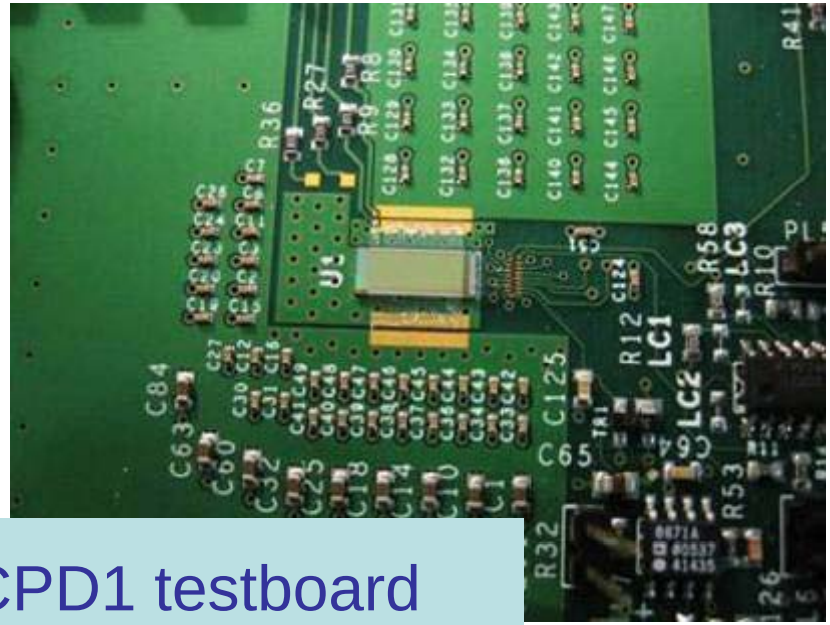
MB4.4 with MAX5057

Clock Drive with CPD1

- CPD1 testboard: careful layout to cancel inductance
- CPD1 tests at 50 MHz
  - 32 nF-equivalent internal load
  - 40 nF external load
- With bump bonding should be similar to internal load

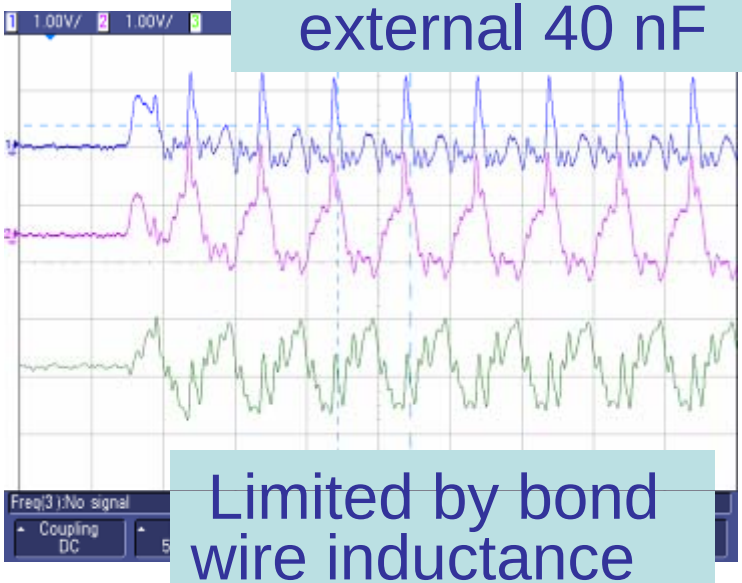
50 MHz, one section internal 2 nF





CPD1 testboard

50 MHz, 8 sections external 40 nF

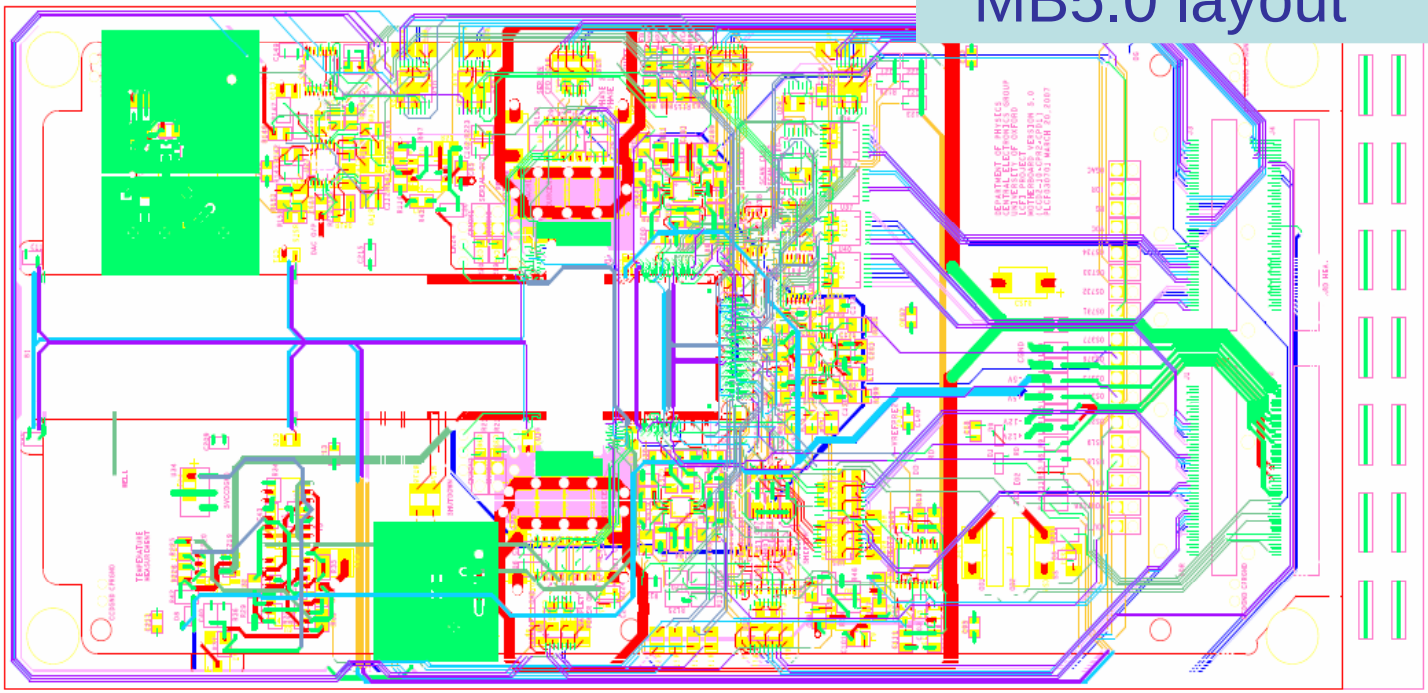


Limited by bond wire inductance

CPC2 MotherBoard

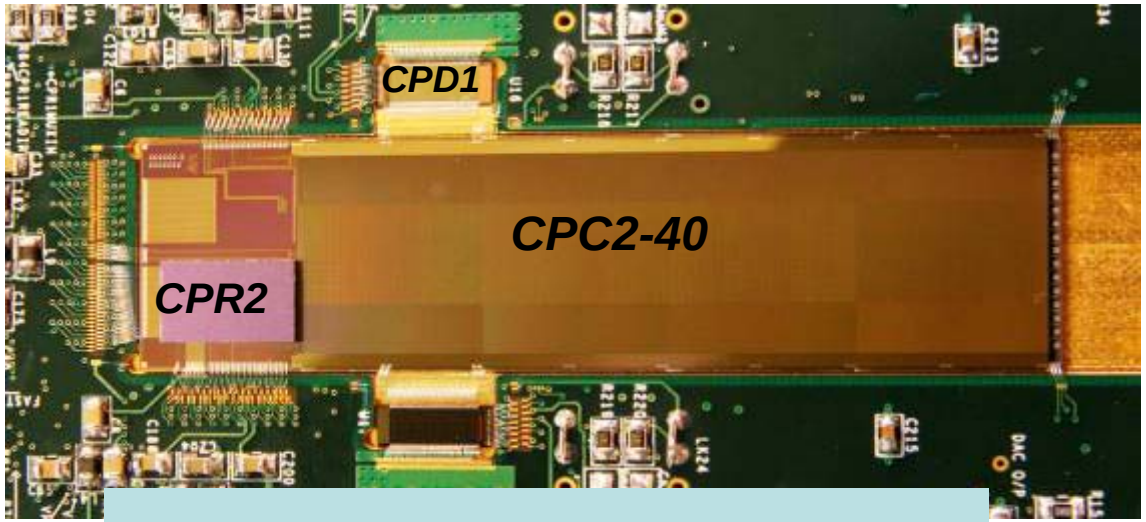
- Interfaces CPC2/CPR2/CPD1 to the outside world, temperature control, monitoring
- Combination of weak analogue, fast digital signals and 20 A clock – challenge!
  - Complicated 14 layer design

MB5.0 layout



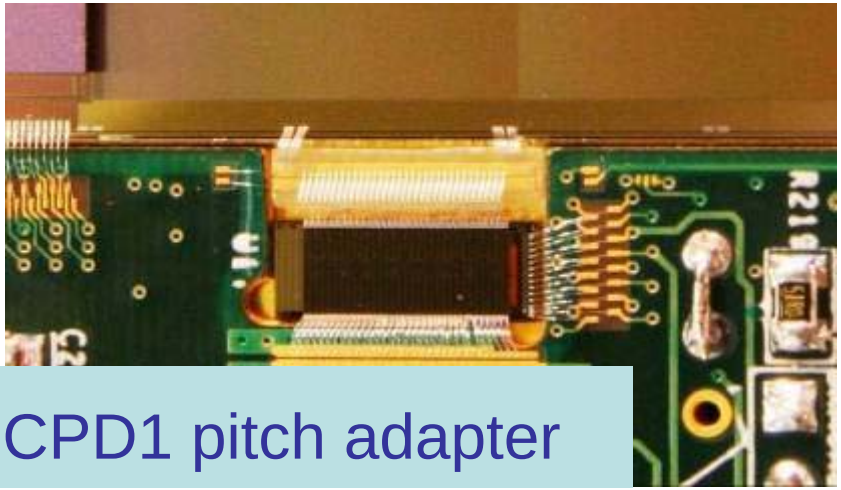
Integration of CPR2/CPR2/CPD1

- Commercial drivers replaced by two custom CPD1 chips
  - Small adapter board to interface CPC2 and CPD1 clock bonding pads



MB5.0 with CPC2/CPR2/CPD1

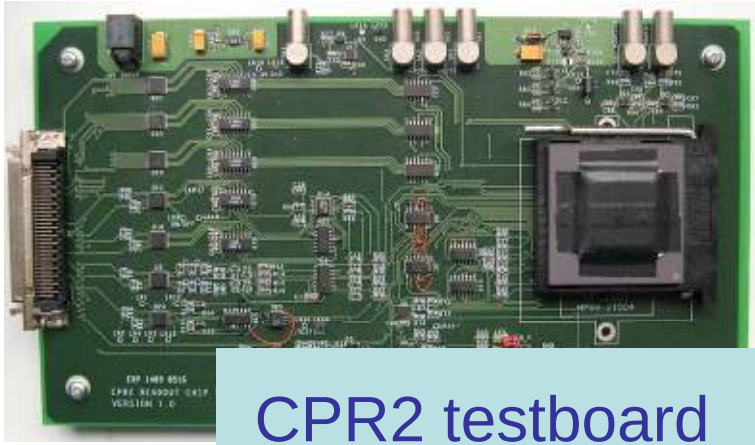
- Low noise (100 e) performance at 20 MHz



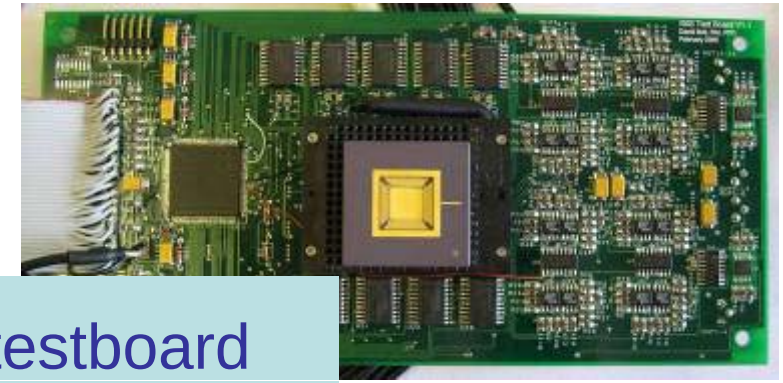
CPC2 – CPD1 pitch adapter

Test Boards

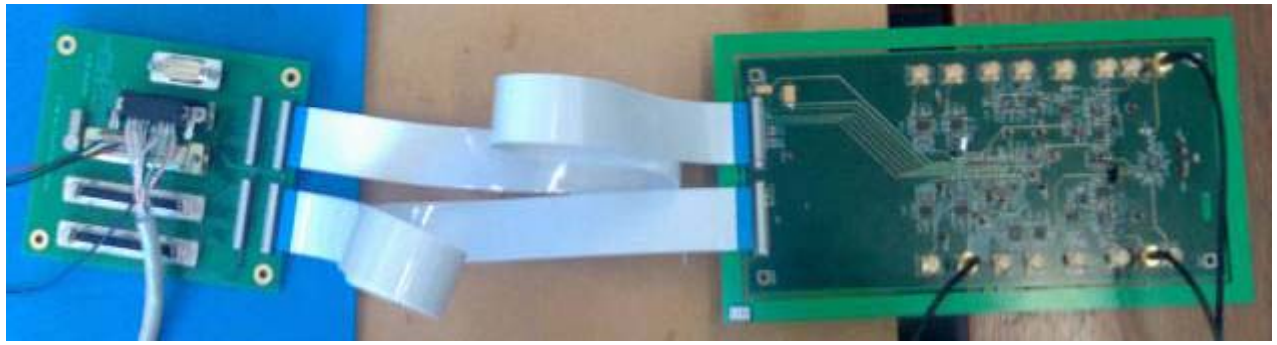
- CPR2 testboard
- ISIS testboard
  - Used for 2007 beam tests
- CPC-T testboard
  - CPC-T are mini-CPCCD with reduced capacitance
  - 50 MHz clock for 4 phase CCD
  - Built-in capacitance measurement



CPR2 testboard



ISIS1 testboard



CPC-T test board with transition board

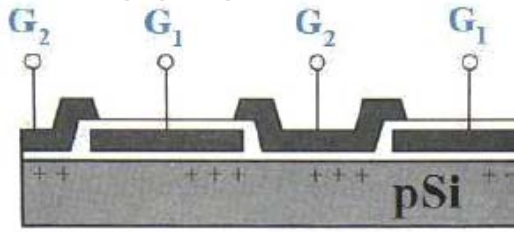
DAQ

- Work horse BVM2 – a VME based module
  - Used in multiple stands in different configurations
- Used to provide all CCD timing sequences and to control all motherboards and testboards
  - Specialized daughter boards
  - SCSI LVDS and TTL configurable outputs
- Successfully used in the ISIS beam tests in October 2007

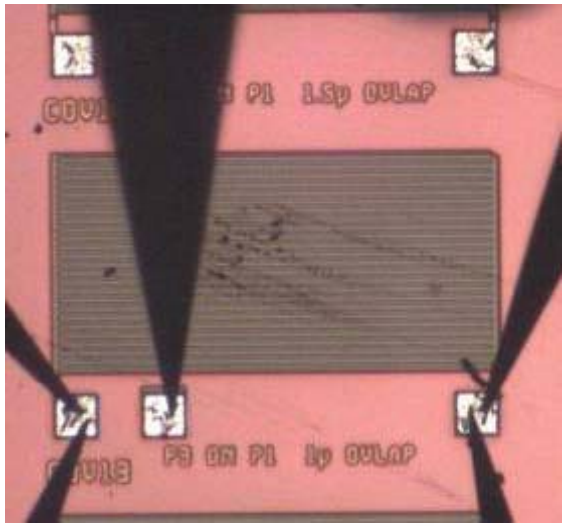
- New, improved version BVM3 under development
  - Software implementation of many hardwired functions
  - Synchronization between several boards

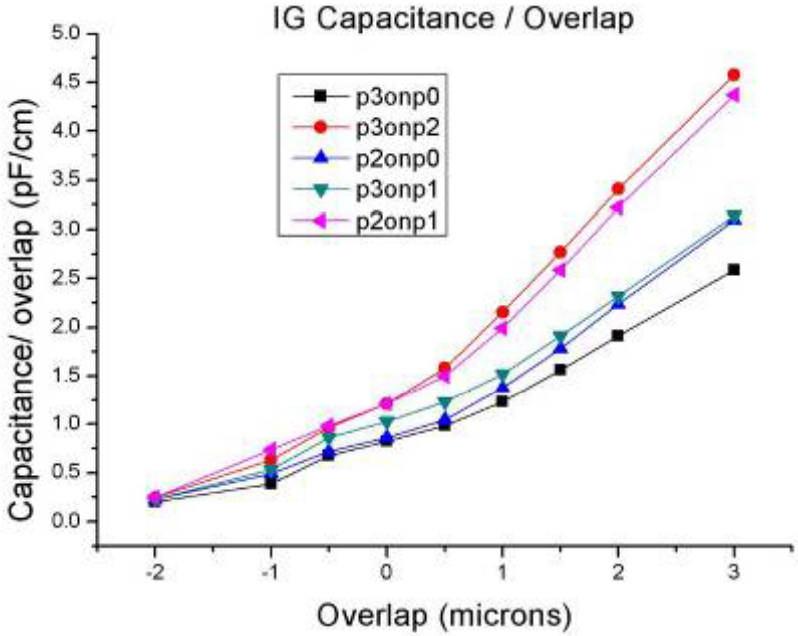
Capacitance Test Structures

- Reduction of CCD capacitance is a major goal
  - Addressed in CPC-T
- Intergate capacitance is the largest contributor



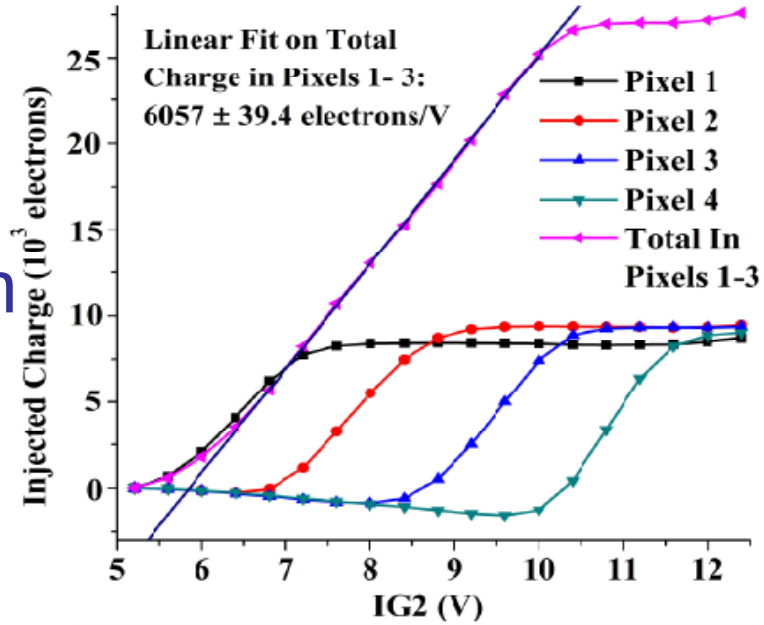
- Tests structures have variable gate overlap [-2 to +3 micron]
  - Good understanding of results
  - Allowed comparison with simulations



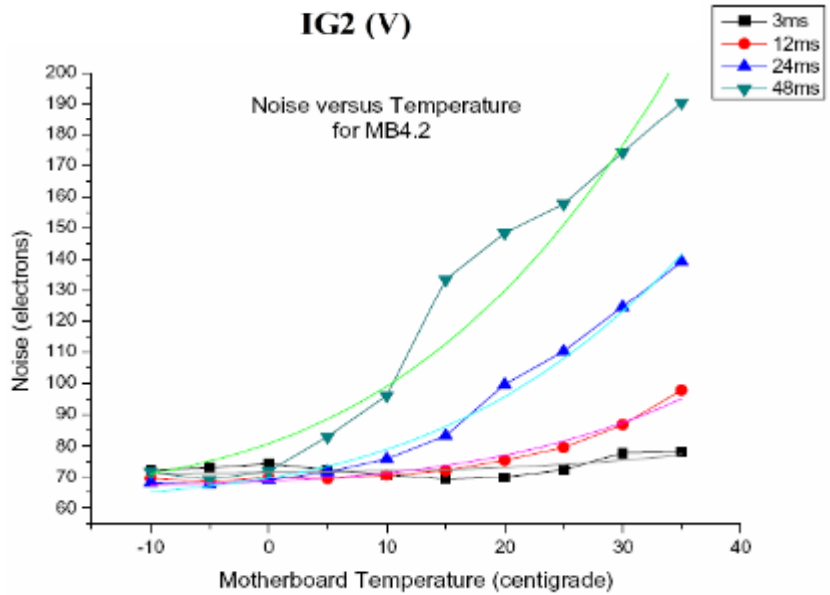


CPC2 Well Capacity and Shot Noise

- Well capacity 6000 electrons
  - Used test charge injection
  - Corresponds to ~4 MIPs



- Shot noise is caused by fluctuations of integrated leakage current
  - Varies with integration time and temperature
  - ~50 fA/pixel at 20ºC



Radiation Damage: What to Expect?

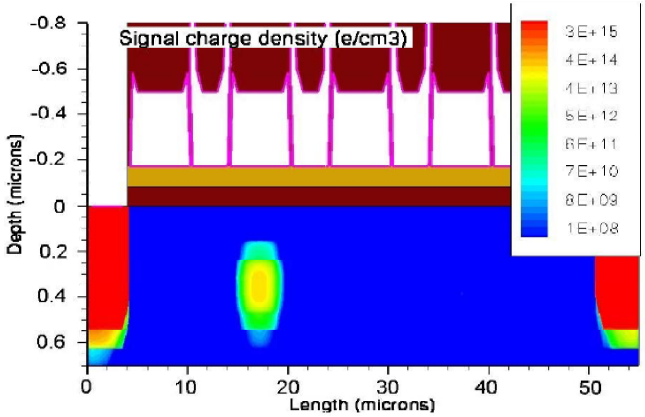
At R=14 mm

- Pair background from Beamstrahlung
  - 10 MeV electrons, 3.5 /bx/cm^2 → 0.5 10^{12} /year/cm^2 (→15 krad/year)
  - Surface damage: accumulation of charge at SiO_2/Si interfaces
  - Bulk damage: traps & leakage current
- Neutrons
  - 1 MeV n; 0.01 /bx/cm^2 → 1.6 10^9 /year/cm^2
  - Bulk damage

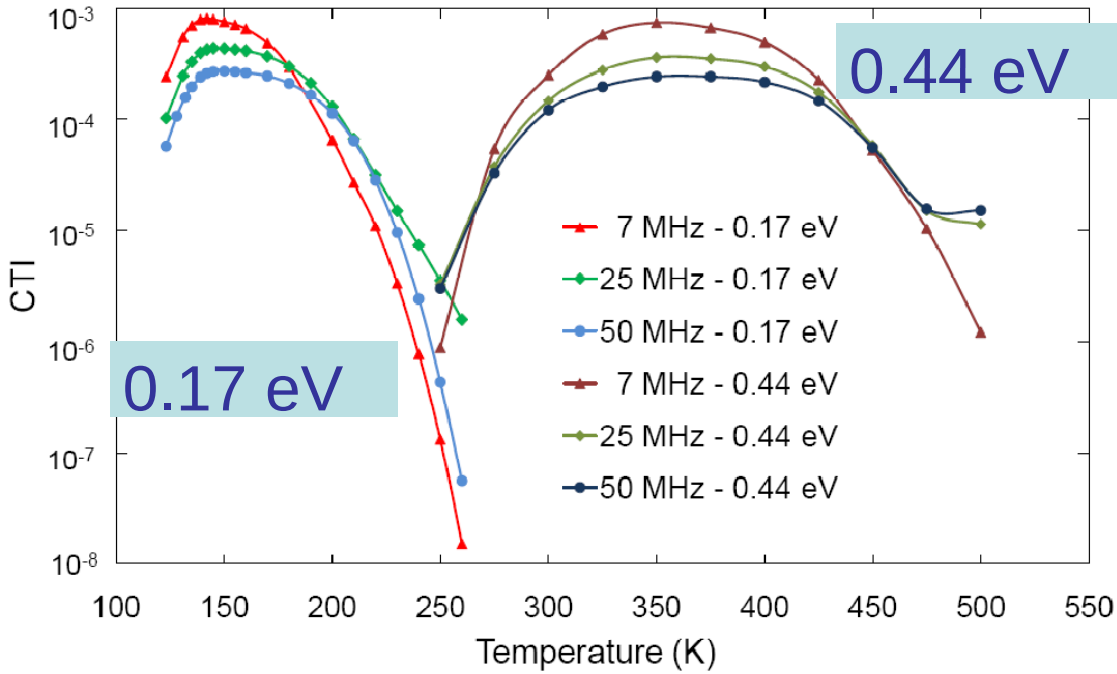
- Surface damage can be accommodated by adjustment of CCD biases
- Bulk damage translates to trap density
  - 0.17 eV trap; 3 10^{11} /year/cm^3; caused by electrons
  - 0.44 eV trap; 4 10^{10} /year/cm^3; caused by electrons and neutrons

Radiation Damage: Simulations

- ISE-TCAD simulations of charge propagation in the presence of traps
  - Charge trapped and later released: function of T and frequency
  - There is an optimum temperature window of low Charge Transfer Inefficiency (CTI) between -50 °C and 0 °C
- This should be confirmed experimentally in CPC2 and CPC-T

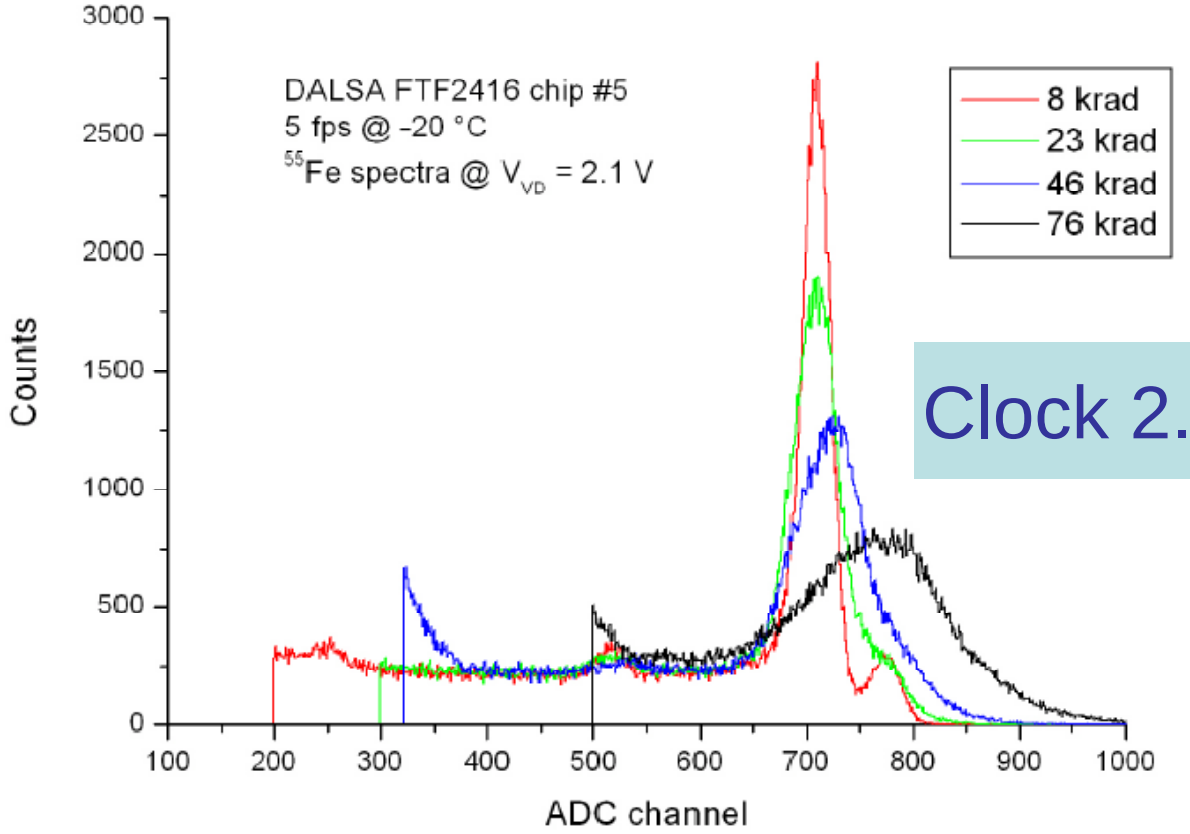


CCD model



Irradiations of DALSA CCDs

- Study to verify rad hardness of non-overlapping polySi gates
  - Charge-up of SiO_2 insulation between gates
  - Relevant for ISIS technologies with small cells
- DALSA CCD survived 70 krad from ^{90}Sr beta source
  - No change in minimal clock amplitude

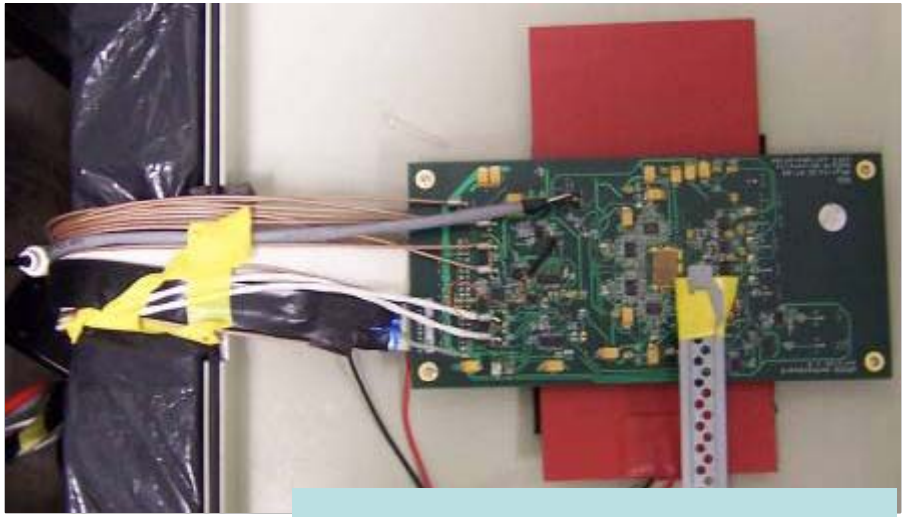


Clock 2.1 V; 5.9 keV ^{55}Fe

Irradiations

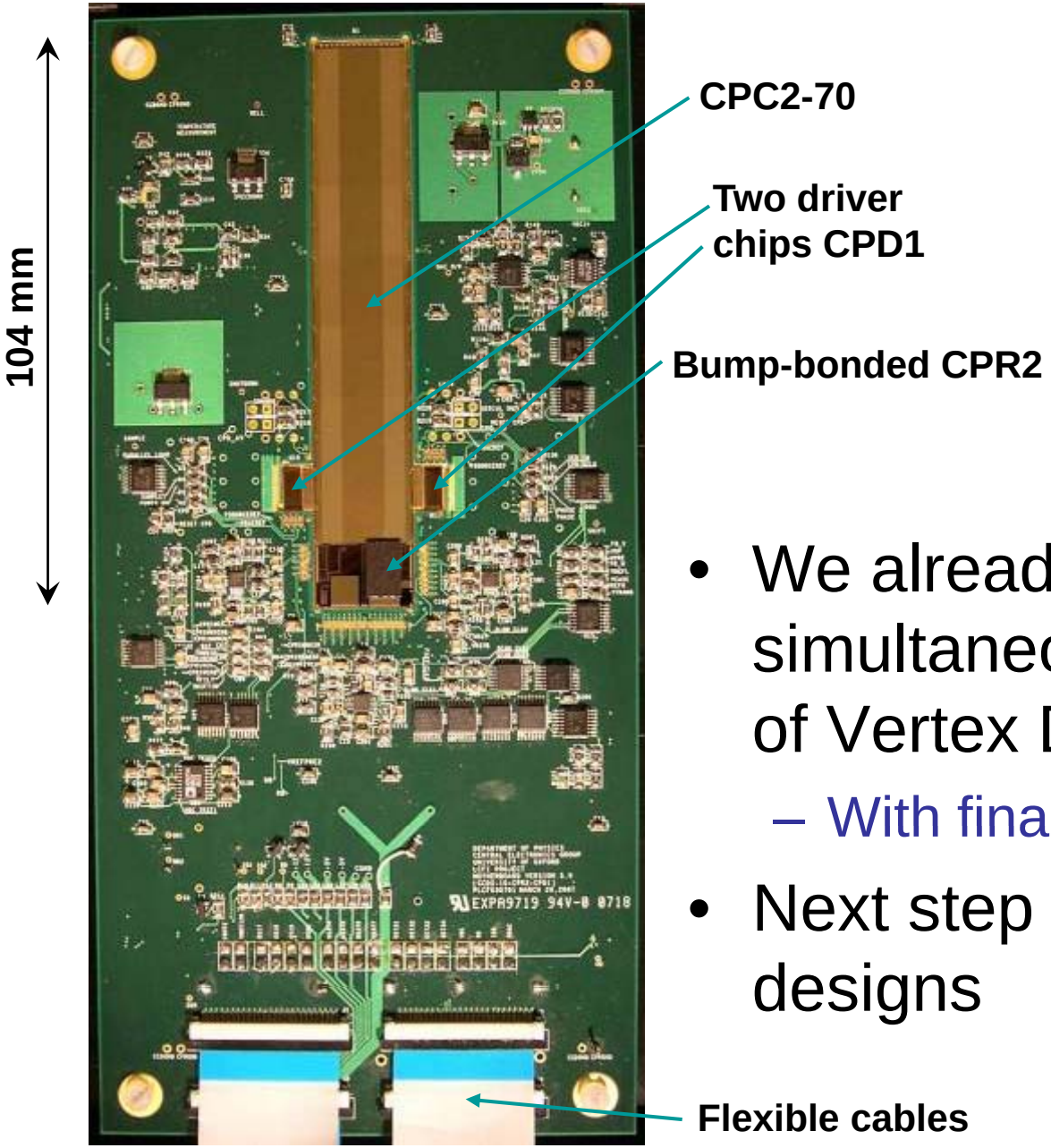
Plan

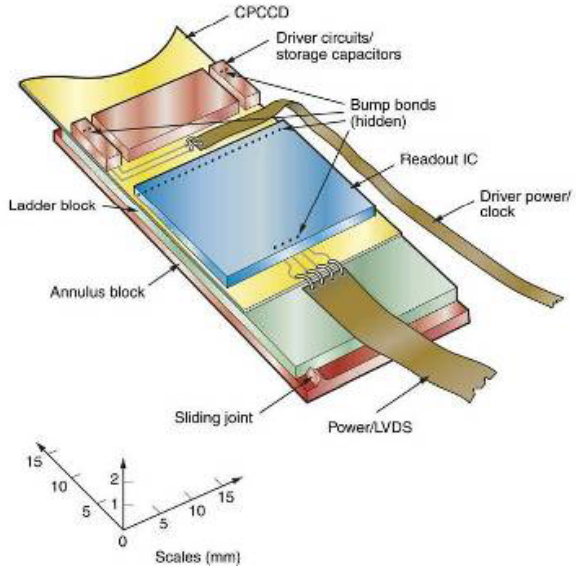
- Characterize CPC1 before irradiation
  - CTI vs temperature
- Irradiate with sources
  - ^{252}Cf, neutrons ~2 MeV
  - ^{90}Sr, electrons ~1 MeV
- Measure CTI after irradiation



CPC1 motherboard

Towards Ladder with CPCCD



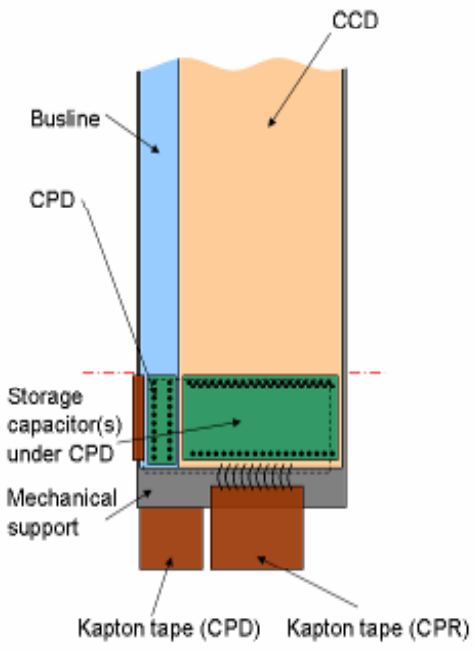


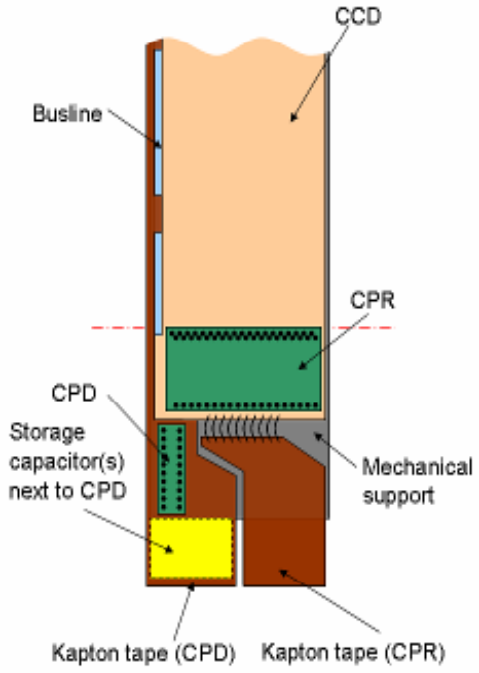
- We already operate simultaneously all components of Vertex Detector ladder
  - With final sensor length 100 mm
- Next step : first realistic ladder designs

Ladder Design

- Considered different configurations how to connect CPR and CPD to CPCCD
  - Low mass flexible kapton cables to bring power and signals
  - Short barrel design allows to place CPR and CPD on different sides of ladder
- Clock distribution and required clock current play key role
  - Clock distribution using double metal layer (DLM) bus. Minimizes amplitude drops but doubles capacitance – needs optimization.
  - How far away need large capacitors?

- Strong influence on CPC3 design and connections to all aspects of the LCFI programme





Summary

- Strong involvement in algorithms and physics studies
  - State of the art vertexing package released
- Column Parallel CCDs perform well at 20 MHz with custom clock driver CPD1
  - Run at 45 MHz with transformer drive
- CPCCD readout chip CPR2 runs at 7 MHz
  - Improved version CPR2A ready soon
- Have proof of principle for ISIS and actively looking for vendors for next generation ISIS2
- Actively exploring various mechanical solutions based on foams and thin silicon

- Ready to demonstrate a full scale ladder prototype in the next funding cycle