Optimising CMOS Pixel Sensors for the ILC Micro-Vertex Detector

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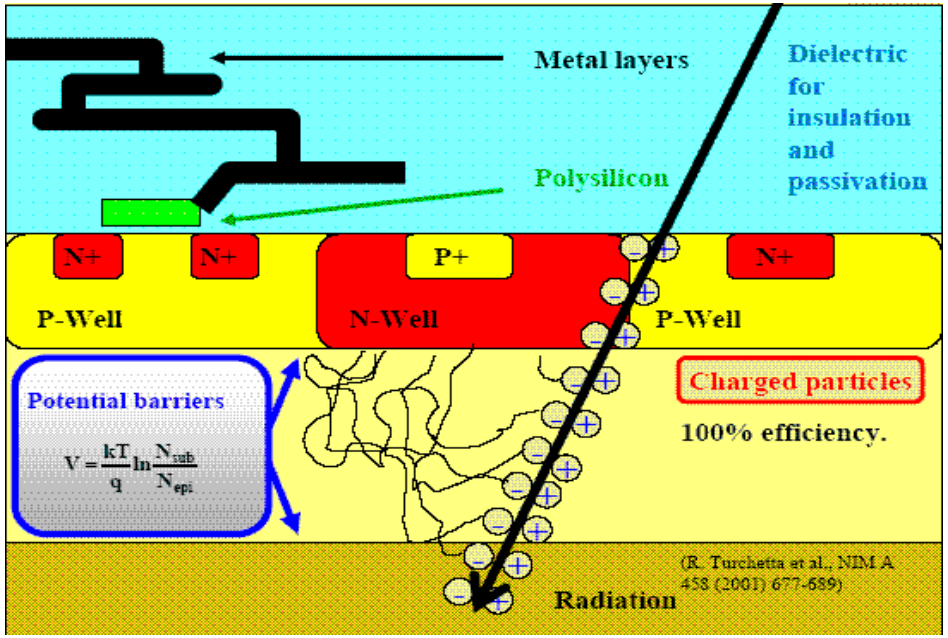
▷ **More information on IPHC Web site:** **http://wwwires.in2p3.fr/ires/web2/rubrique.php3?id_rubrique=63**

OUTLINE

- **Reminder on CMOS sensors:** *Specific advantages* *R&D framework : Vxing applicationS*
- **Achieved performances with analog output sensors** **(AMS-0.35 OPTO fab. process) :**
  Detection efficiency *Spatial resolution* *Operating temperature* *Radiation tolerance*
- **Fast read-out architecture:** *State of the art* *Plans until 2009/10*
- **Integration issues:** *Thinning* *Ladder design* *Data flow*
- **Summary**

Main Features and Advantages of CMOS Sensors

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000$ e$^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)



- Specific advantages of CMOS sensors:
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\sim$ 30–40 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ Room temperature operation
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation
    - ⋈ Very thin sensitive volume $\rightarrowtail$ impact on signal magnitude (mV !)
    - ⋈ Sensitive volume almost undepleted $\rightarrowtail$ impact on radiation tolerance & speed
    - ⋈ Commercial fabrication (parameters) $\rightarrowtail$ impact on sensing performances & radiation tolerance

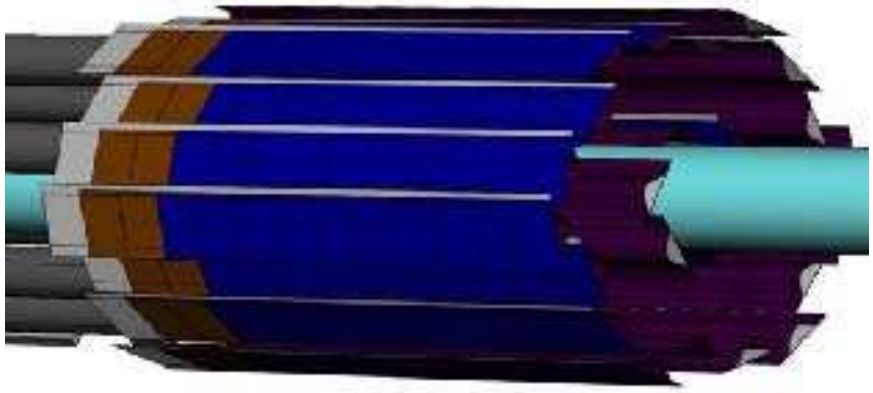
- **Numerous different chips addressing 2 types of topics :**
  - ◇ **Various generic issues influencing detection performances**
    - *fabrication technology details: epitaxy thickness, doping profile, I_{leak}, yield, ...*
    - *pixel design: charge collection, leakage current removal, ion. rad. tol. design, ...*
    - *signal processing μcircuits: CDS/pixel, discri. & ADC at column end, $\emptyset$ μcircuits, ...*
    - *repeat small prototype design with large sensors : yield, capacitive effects, offeset dispersion, ...*
    - *optimise generic design for each specific application : develop chips dedicated to each application*
  - ◇ **Specific application requirements**

- **$>$ 20 MIMOSA sensors designed, fabricated in 7 different fabrication technologies:**
  - *AMS-0.6 μm: MIMOSA-1, MIMOSA-5*
  - *MIETEC-0.35 μm (became AMI-0.35 μm): MIMOSA-2 and -6*
  - *IBM-0.25 μm: MIMOSA-3*
  - *TSMC-0.25 μm: MIMOSA-8 and -10*
  - *STM-0.25 μm: MIMOSA-21,-21A,B,C*
  - *AMS-0.35 μm without epitaxial layer: MIMOSA-4, -12 and -13*
  - *AMS-0.35 μm OPTO with epitaxial layer: MIMOSA-9, -11, -14, -15, -16, -17, -18, -19, -20 and -22*

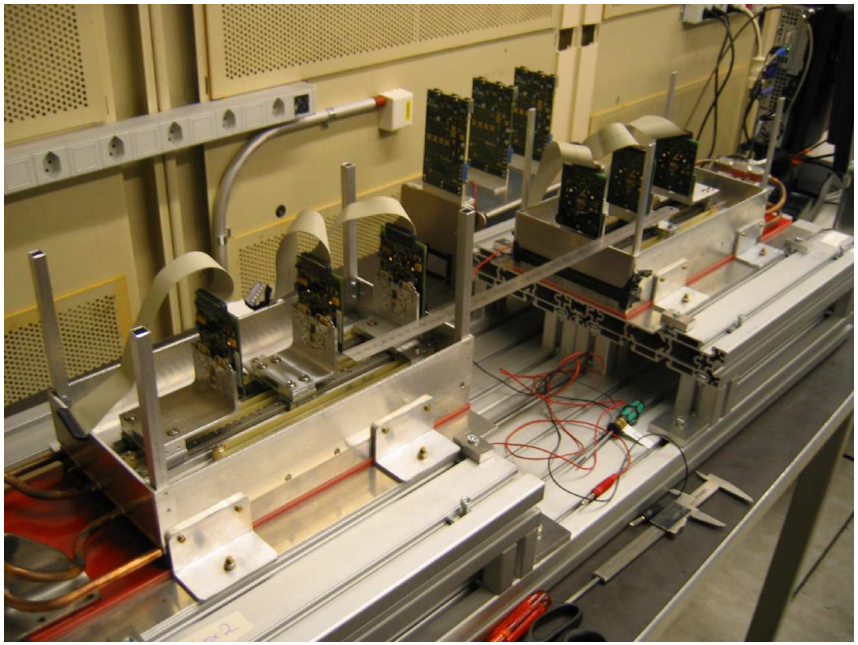
- **Specific difficulties:**
  - ◇ **Analog part of most sensors cannot be simulated reliably (lack of doping profile details, etc.)**
  - ◇ **R&D addresses simultaneously detection system & signal processing parts integrated on same substrate**

Vertexing Applications of MIMOSA Chips: Short & Mid-Term

- **Vertex Detector upgrade for STAR expt at RHIC**
  - 2 cylindral layers : $\sim$ 1600 cm^2
  - $\gtrsim$ 160 million pixels ($\leq$ 30 μm pitch)
  - 2 steps :
    - ◇ 2007: telescope (3 chips) $\longrightarrow$ BG meast, no pick-up !
    - ◇ 2008: digital outputs without $\emptyset$ ($\leq$ 640 μs)
    - ◇ 2010: digital outputs with integrated $\emptyset$ ($\leq$ 200 μs)

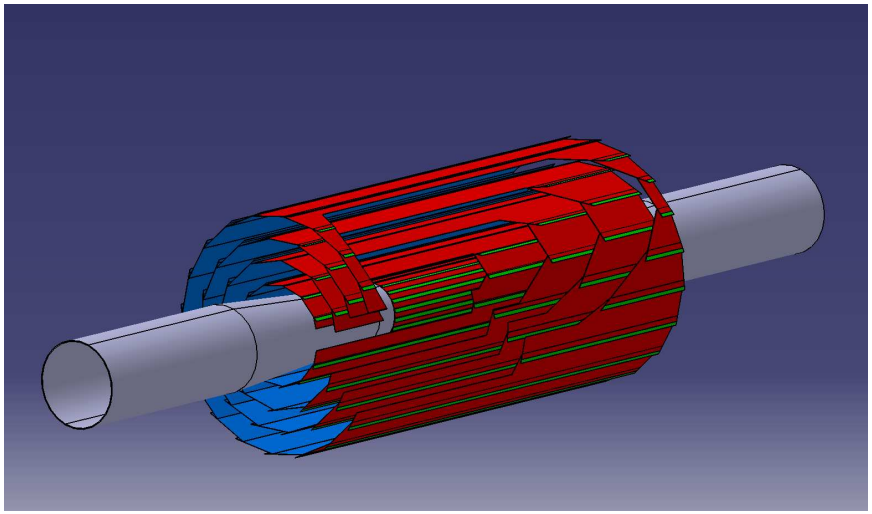


- **Beam telescope (FP6 project EUDET)**
  - 2 arms of 3 planes (plus 1 high resolution plane)
  - provide $\lesssim$ 1 μm resolution on 3 GeV e$^-$ beam (DESY)
  - 2 steps :
    - ◇ 2007: analog $\longrightarrow$ telescope commissionned & running
    - ◇ 2008: digital with integrated $\emptyset$ ($\sim$ 100 μs)

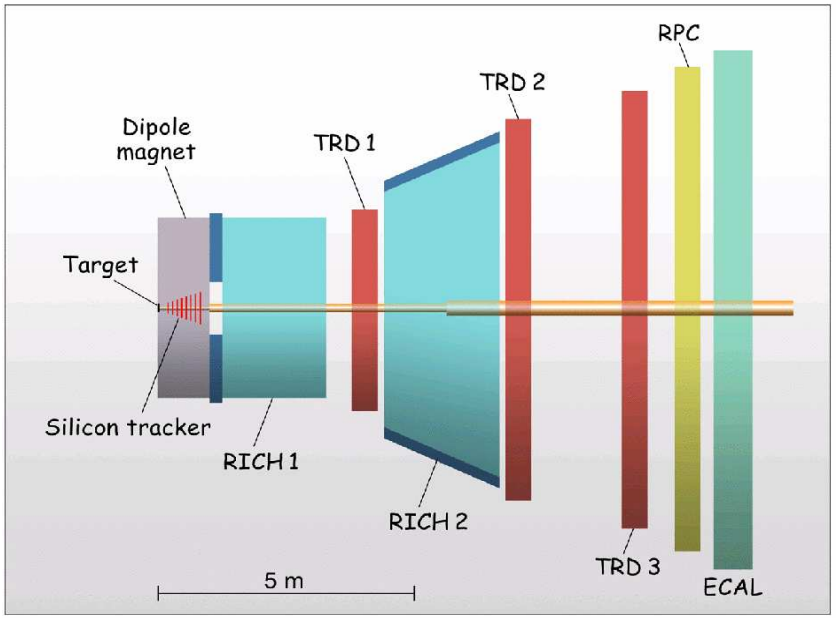


Vertexing Applications of MIMOSA Sensors: Long Term

- ILC vertex detector (option)
  - 5–6 cylindrical layers : $\gtrsim$ 3000 cm^2
  - 300-500 million pixels (20–35 μm pitch)
  - read-out times $\sim$ 25 (L0), 50 (L1) & 100 (L2-4) μs
  - 1st complete ladder prototype $\gtrsim$ 2010



- CBM vertex detector (FAIR/GSI)
  - 2 rectangular layers : $\sim$ 500 cm^2
  - 150 million pixels ($\sim$ 20 μm pitch)
  - read-out time $\sim$ 10 μs



- **Overall objective: identify $\sim$ all flavours involved in most final states**

  Ex: $\mathbf{e^+e^- \rightarrowtail ZH}$ $\Rightarrow$ **measure Br (**$\mathbf{H \rightarrowtail c\bar{c}, \tau^+\tau^-, b\bar{b}, gg, ...}$**)**

- **In practice:**

  ▷ *tag* $\mathbf{c}$ *and* τ *jets with unprecedented efficiency & purity (*$\mathbf{b}$ *tagging much less challenging)*

  ▷ *reconstruct very efficiently Vx1* $\rightarrowtail$ *Vx2* $\rightarrowtail$ *Vx3* $\rightarrowtail$ *....*

  ▷ *reconstruct vertex flavour and electrical charge ...*

  ▷ *cope with high jet multiplicity final states containing several* $\mathbf{b}, \mathbf{c}, \tau$ *jets*

  ▷ *minimise secondary interactions (missleading particle flow reconstruction)*

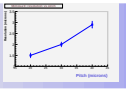
  ▷ *etc.*

- $\sigma_{\mathbf{IP}} = \mathbf{a} \oplus \mathbf{b/p} \cdot \mathbf{sin^{3/2}}\theta$ **with** $\mathbf{a} <$ **5** μm **and** $\mathbf{b} <$ **10** μm

  ▷ **limits on** $\mathbf{a}$ **and** $\mathbf{b}$ **are still "very educated guesses"** ▷ **SLD:** $\mathbf{a}$ **= 8** μm **and** $\mathbf{b}$ **= 33** μm

  - $\sigma_{\mathbf{sp}} \lesssim 3\mu\mathbf{m}$
  - $\mathbf{R}_{in} \sim$ **1–2 cm**
  - $\mathbf{R}_{out} \sim$ **4·**$\mathbf{R}_{in}$
  - **VD layer $\sim$ 0.1–0.2 % $\mathbf{X}_0$**
  - **beam pipe $\sim$ 0.1 % $\mathbf{X}_0$**

- *Constraint on* σ_{IP} *satisfies simultaneoulsy requirement on 2-hit separation in inner most layer (*$\sim$ *30–40* μm*)*



- Constraints from the Running Conditions

- **Overall objective: come as close as possible to IP $\rightarrowtail$ minimise $\mathbf{a}$ and $\mathbf{b}$ ($\propto \mathbf{R_{in}}$)**

  $\Rrightarrow$ **beam background induced by high luminosity :**

  Beamstrahlung $\mathbf{e^{\pm}}$ $\Rrightarrow$ inner layer constraints prevent $\mathbf{a}$ & $\mathbf{b}$ to be well below their upper bounds

  $\hookrightarrow$ *Inner most layer: BG generates O(10^7) hits/s while Physics generates O(10^2) hits/s*

- **In practice:**

  ▷ *experimental magnetic field should be as high as possible ($\sim$ 3–5 T) $\rightarrowtail$ sweep away most $\mathbf{e^{\pm}_{BS}}$*

  ▷ $\mathbf{e^{\pm}_{BS}}$ *rate still $\lesssim$ 5 hits/cm^2/BX at R=15 mm ($\sqrt{s}$ = 500 GeV, 4 T) $\rightarrowtail$ O(10^3) pixels /cm^2/10 μs*

  ▷ *foster high read-out speed in inner layers against occupancy $\lesssim$ few tens of μs*

  ▷ *rad. level not negligible at $T_{\mathbf{room}}$ (mat. budget ?):* ● **$\sim$ 50 kRad/yr** ● **6·10^{11} $e^{\pm}_{10\ MeV}$ $\approx$ 2·10^{10} n$_{eq}$/cm^2/yr**

  ▷ **prediction accuracy $\Rrightarrow$ prepare for 3 ? 5 ? times more BG $\rightarrowtail$** ● **$\sim$ 500 kRad/3 yr** ● **$\sim$ 2·10^{11} n$_{eq}$/cm^2/3 yr**

  ◇ **neutron dose integrated over 3 years much smaller : $\lesssim$ 3·10^{10} n$_{eq}$/cm^2 (safety factor of 10)**

- **Power dissipation : avoid increasing mat. budget & complexity with heavy cooling $\Rrightarrow$ air flow**

  ◇ *exploit beam time structure: $\sim$ 1 ms train ($\sim$ 3000 buckets) every $\sim$ 200 ms $\Rrightarrow$ duty cycle $\sim$ 1/200*

  $\Rrightarrow$ *switching off the sensors between trains may allow power reduction by factor of $\sim$ 100*

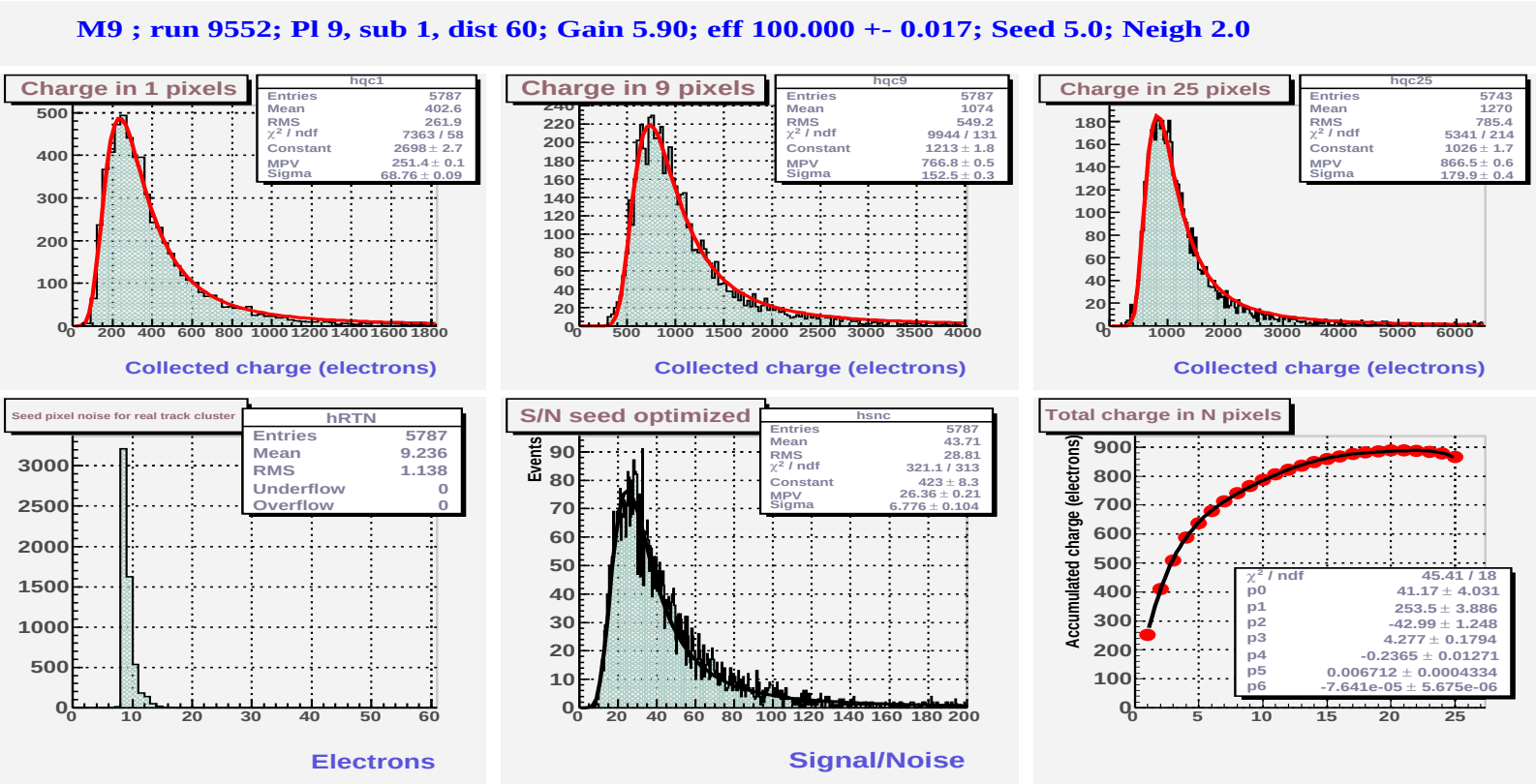
- **EMI : fear that beam delivery elements may be source of very short λ EM field**

  ◇ *R&D on sensor architecture with memories integrated in pixels started a few years ago*

  $\hookrightarrow$ *in standby since 2006 (lack of manpower) $\Rrightarrow$ not reviewed in this report*

M.I.P. Detection with CMOS Sensors

- *$\sim$ 100 chips (M1, M2, M4, **M5**, M8, M9, M11, M14, M15, M16, **M17**, **M18**) tested on H.E. beams since 2001 at CERN-SPS & DESY, mounted on Si-strip telescope (calibrated with ^{55}Fe) $\mapsto$ well established perfo. (analog output):*
  - *Best performing technology: AMS 0.35 μm OPTO $\rightarrowtail$ $\sim$ 11 & 15 μm epitaxy (called epi-14 and epi-20)*
  - *$N \sim 10\ e^-$ ENC $\mapsto$ S/N $\gtrsim$ 20 – 30 (MPV) at room Temperature*

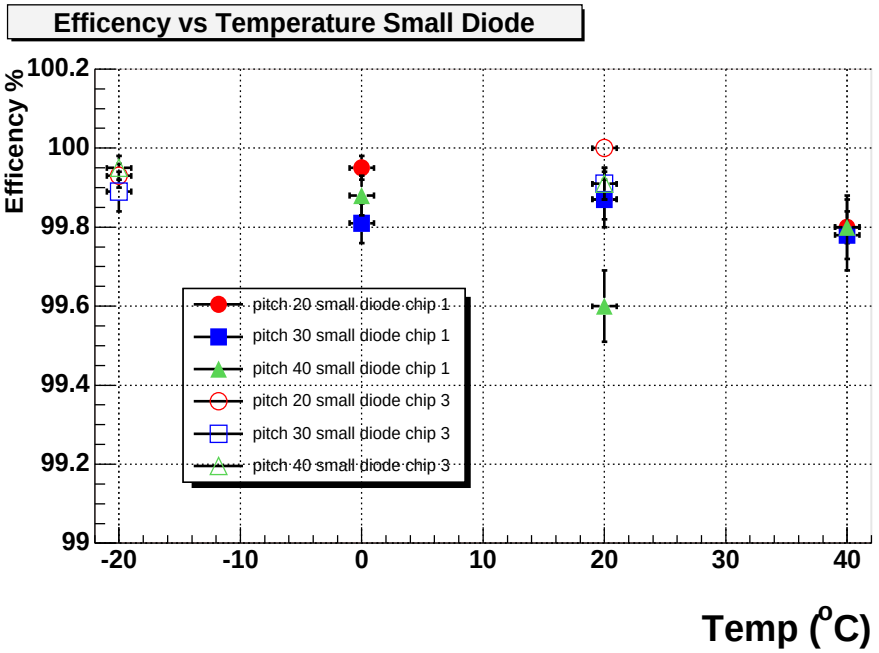


- *Technology without epitaxy also performing well : very high S/N but large clusters (hit separation $\searrow$)*
- *Macroscopic sensors : MIMOSA-5 ($\sim$ 3.5 cm^2; 1 Mpix) ; MIMOSA-20 (1x2 cm^2; 200 kpix) ; MIMOSA-17 (0.8x0.8 cm^2; 65 kpix)*

Detection Efficiency vs Fake Rate

Detection efficiency:

- *Ex: MIMOSA-9 data (20, 30 & 40 μm pitch)*
- $\epsilon_{det} \gtrsim$ *99.5–99.9 % repeatedly observed at room temperature*
- $T_{oper.} \gtrsim 40\,^{\circ}C$



Efficiency vs rate of fake clusters :

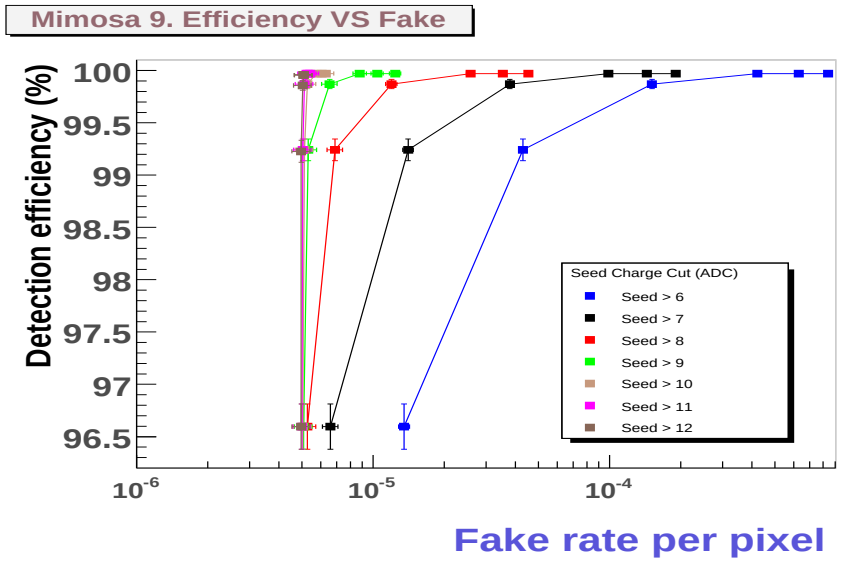
- *vary cut on seed pixel :*

  *6 $\rightarrowtail$ 12 ADC units (*N $\sim$ 1.5 ∪.ADC*)*

- *vary cut on Σ of crown charge :*

  0, 3, 4, 9, 13, 17 ADC units

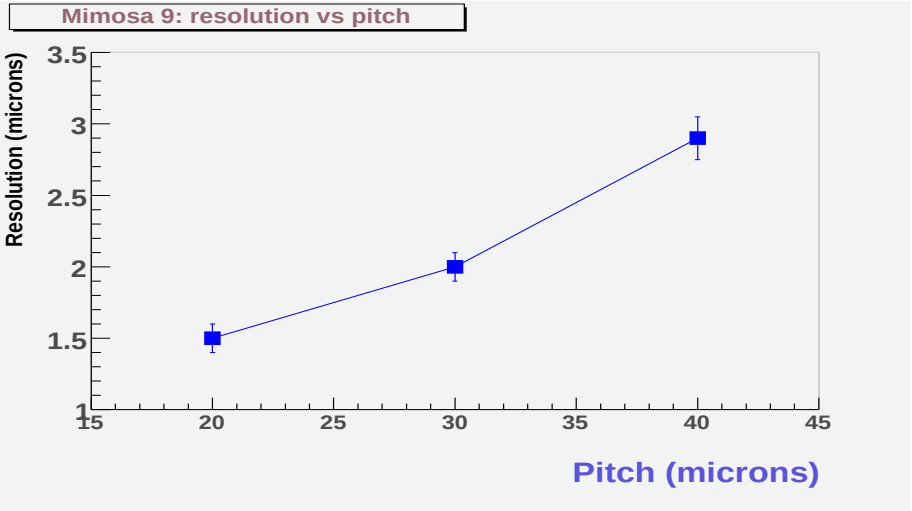
$\Rrightarrow$ $\epsilon_{det} \sim$ **99.9 % for fake rate** $\sim 10^{-5}$



Spatial Resolution (vs ADC resolution)

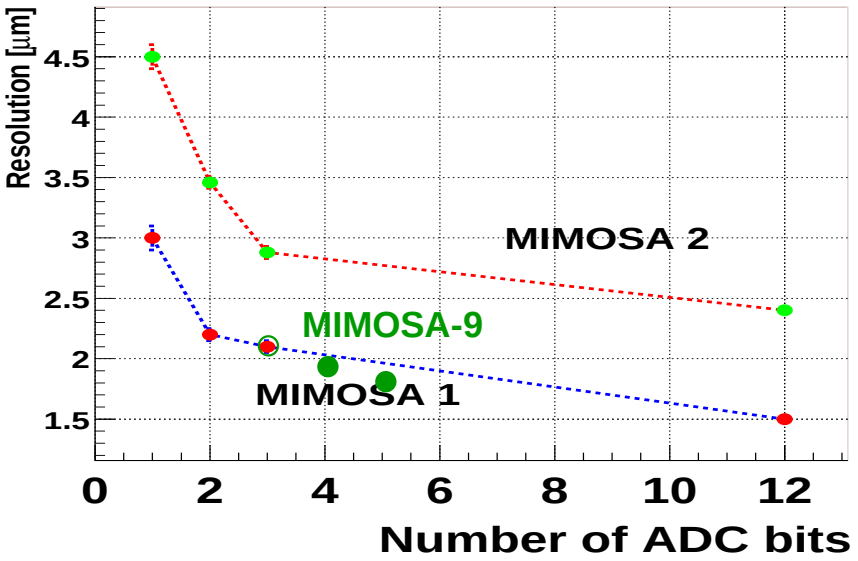
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch) $\rightarrow \lesssim 3\ \mu m$ (40 μm pitch)
- recent result: $\sigma_{sp} \lesssim 1\ \mu m$ for 10 μm pitch
- obtained with signal charge encoded on 12 bits



σ_{sp} dependence on ADC granularity:

- minimise number of ADC bits
  - $\rightarrow$ minimise dimensions, $t_{r.o.}$ & P_{diss}
- effect simulated on real MIMOSA data (20 μm pitch ; 120 GeV/c π^- beam)



- $\triangleright\triangleright$ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\rightarrow$ 1.7–1.6 μm (5 bits)
  (MIMOSA-9 : 20 μm pitch; T= + 20°C)
- Caution : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  - $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

Observed Radiation Tolerance

of MIMOSA Sensors

Radiation Tolerance: Summary of AMS-0.35 OPTO Evaluation

Requirements:

- **beamstrahlung (GuineaPig X 3) :** $\lesssim 10^3$ $e^{\pm}_{BS}$**/cm^2/25** μs $\longrightarrow$ $\lesssim$**2·10^{12} $e^{\pm}_{BS}$/cm^2/yr**
  $\hookrightarrow$ **O(100) kRad/yr – O(10^{11}) n_{eq}/cm^2/yr** (NIEL $\sim$ 1/30)
- **neutron gas:** $\lesssim 10^{10}$ **n_{eq}/cm^2/yr**

Non-ionising radiation tolerance:

- **MIMOSA-15 irradiated with O(1 MeV) neutrons tested on DESY e^- beams : Very Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 700\ \mu s$
  - **5.8·10^{12} n_{eq}/cm^2 values derived with standard and with soft cuts**

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	8.7 $\pm$ 2.	7.5 $\pm$ 2.
Det. Eff. (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2	84. $\pm$ 2.

Ionising radiation tolerance:

- **Pixels modified against hole accumulations (thick oxide) and leakage current increase (guard ring)**
- **MIMOSA-15 tested with $\sim$ 5 GeV e^- at DESY after 1 MRad (10 keV X-Ray) exposure : Very Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 180\ \mu s$
  - $t_{r.o.} << 1$ms crucial at T_{room}

Integ. Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 $\pm$ 1.1	27.8 $\pm$ 0.5	100 %
1 MRad	10.7 $\pm$ 0.9	19.5 $\pm$ 0.2	99.96 $\pm$ 0.04 %

Preliminary conclusion:

- **at least 3 years of running viable at T_{room} (or close to)**
- **further assessment needed (also with $\sim$ 10 MeV e^-) : sensors with integ. CDS, ADC, ...**

Radiation Tolerance : Low Energy Electrons

Investigation of sensitivity to $\sim$ 10 MeV electrons (NIEL factor $\sim$ 1/30)

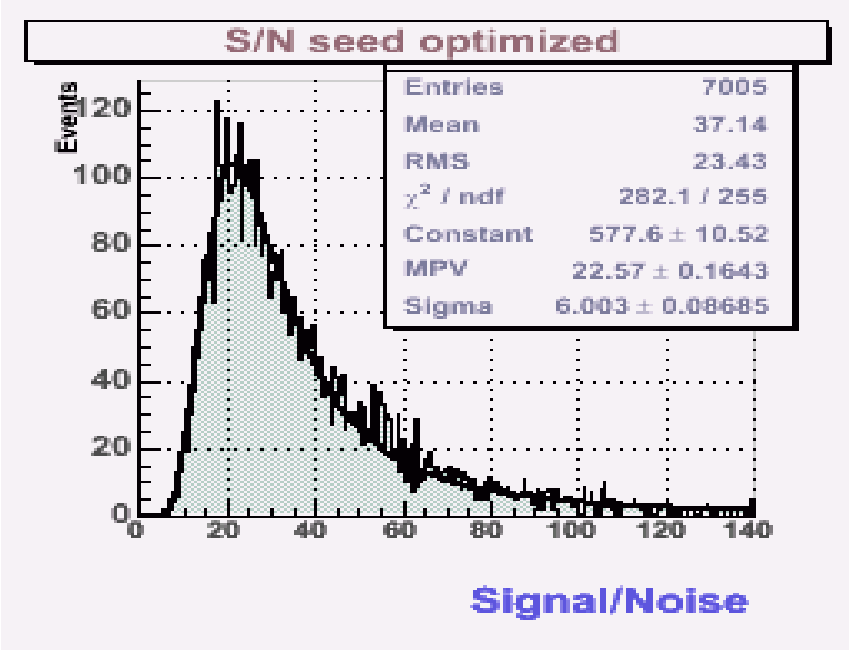
$\hookrightarrow$ **similar to beamstrahlung $e^{\pm}$ in 4 T field at 15 mm radius**

1) **MIMOSA-9 exposed to $10^{13} e^{-}_{9.4MeV}$/cm^2 in Darmstadt : equivalent to $\lesssim$ 300 kRad/cm^2 and $\sim 3 \cdot 10^{11} n_{eq}$/cm^2**

2) **Irradiated chip tested with $\sim$ 6 GeV e^- at DESY**

$\hookrightarrow$ **Test result at -20°C : S/N $\sim$ 23 $\rightarrowtail \epsilon_{det} > 99.3\%$**

(before irradiation: S/N $\sim$ 28 and ϵ_{det} = 99.93 $\pm$ 0.03 %)



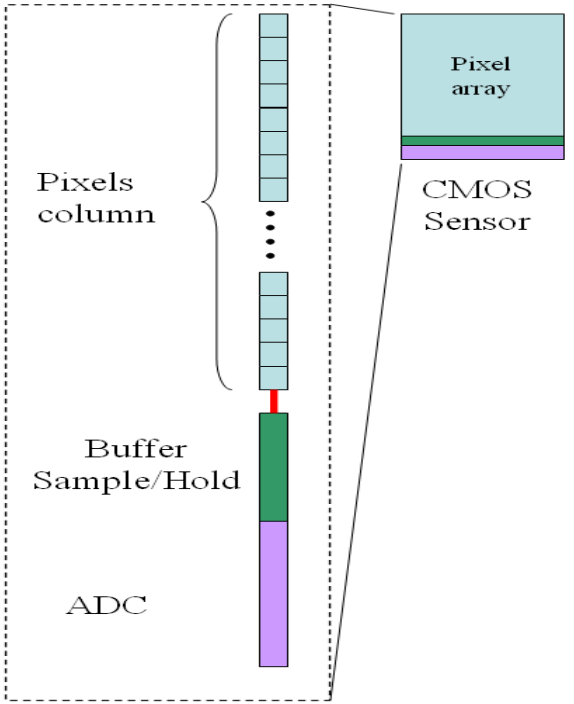
▷ **Sensors still need to be tested at room temperature (compatible with very light cooling system)**

Integration of Signal Processing

Inside Pixels and on Chip Periphery

Fast Read-Out Architecture

- **Parallel development of 3 components (analog, mixed, digital):**
  - **column // arrays with CDS/pixel & discriminated outputs**
  - **4-5 bit ADCs intended to replace discriminators**
  - **$\varnothing$ μcircuits & output memories**



- **2 stage approach :**

  1) Develop sensors for mid-term (2009) applications

  $\hookrightarrow$ less severe requirements, almost suited to 3 outer layers:

  - **EUDET: 1x2 cm^2, t$_{r.o.}$ $\sim$ 100 μs, discri. binary charge encoding (no ADC);**
  - **STAR: 2x2 cm^2, t$_{r.o.}$ $\sim$ 200 μs, discri. binary charge encoding (no ADC);**

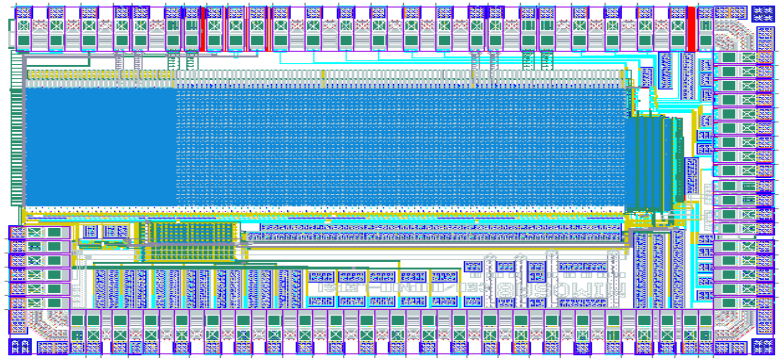
  $\hookrightarrow$ will be operated in real experimental conditions by 2009/2010

  2) Develop ILC sensors (mainly for inner layers) extrapolating from EUDET & STAR:

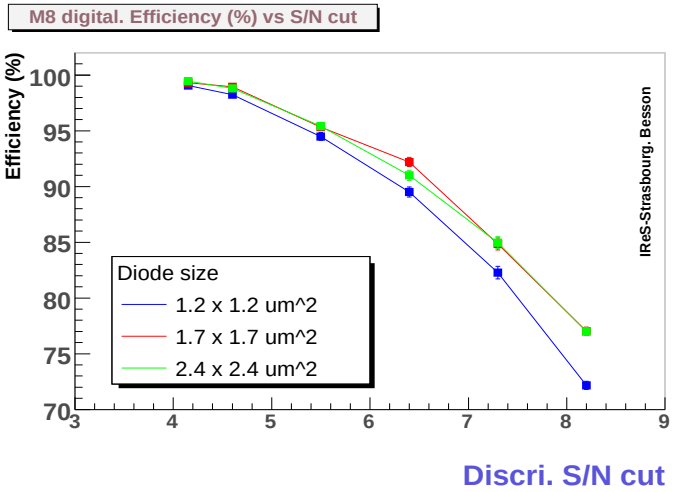
  - **increase row read-out frequency by $\sim$ 50 %**
  - **replace discriminators with ADCs**

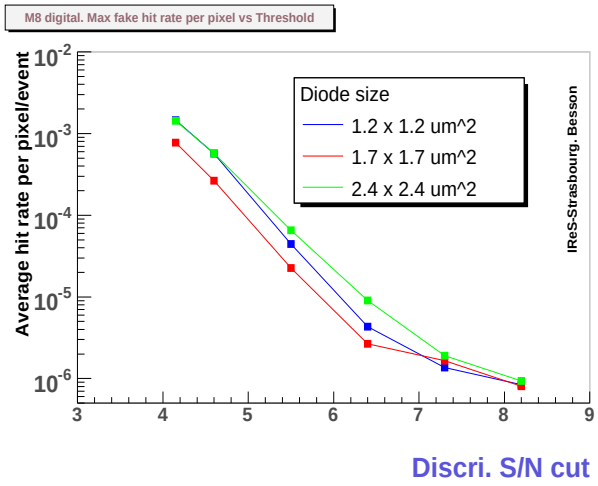
High Read-Out Speed Architecture : 1st Prototype

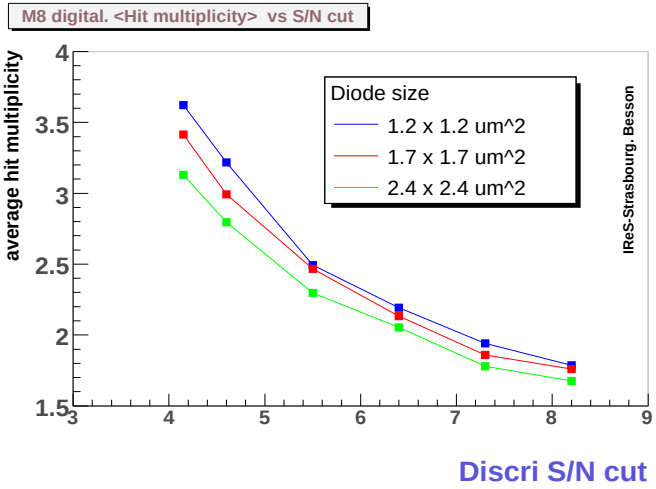
- **MIMOSA-8: TSMC 0.25 μm digital fab. process ($<$ 7 μm epitaxy)**
  - **32 // columns of 128 pixels (pitch: 25 μm)**
  - **read-out time $\sim$ 50 μs (resp. 20 μs) with (resp. without) DAQ**
  - **on-pixel CDS**
  - **discriminator (and DS) integrated at end of each of 24 columns**



- **Detection performance with 5 GeV/c e^- beam (DESY) in 2005 :**







▷▷ **Excellent m.i.p. detection performances despite modest thickness of epitaxial layer**

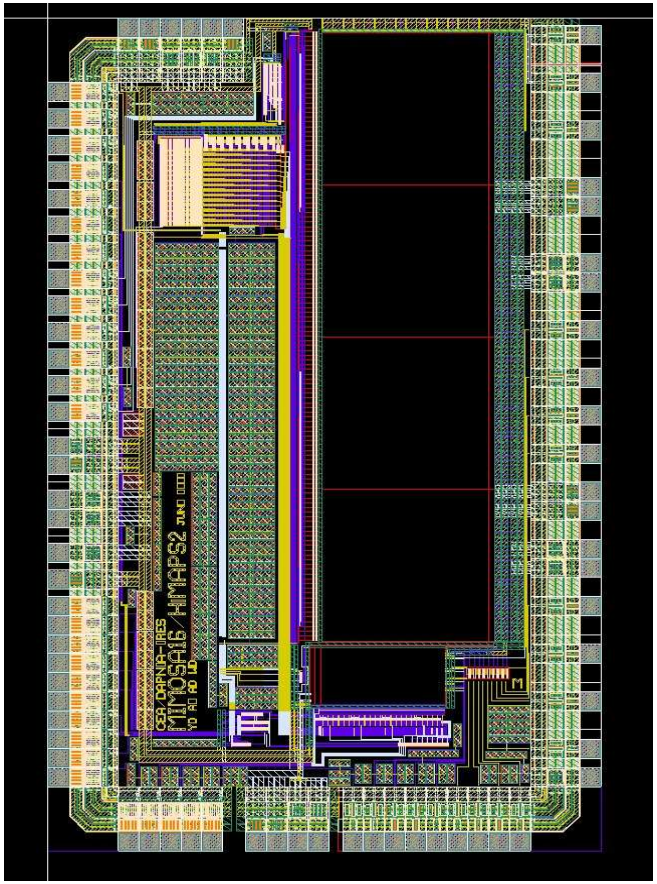
✳ **det. eff. $\sim$ 99.3 % for fake rate of $\sim$ 0.1 %** ✳ **discri. cluster mult. $\sim$ 3–4** ✳ **$P_{diss} \lesssim$ 500 μW / col.**

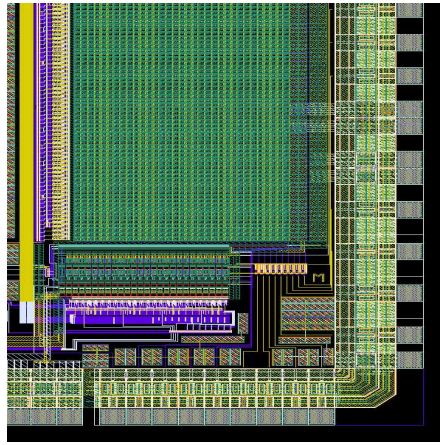
▷▷ **Architecture validated for next steps: techno. with thick epitaxy, rad. tol. pixel at T_{room}, ADC, $\emptyset$, etc.**

High R.-O. Speed Architecture : 2nd Prototype = MIMOSA-16

MIMOSA-16 design features :

- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–15 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (DS at end of each column)
- 24 columns ended with discriminator
- 4 sub-arrays :
  - S1 : like MIMOSA-8 (1.7x1.7 μm^2 diode)
  - S2 : like MIMOSA-8 (2.4x2.4 μm^2 diode)
  - S3 : S2 with ionising radiation tol. pixels
  - S4 : with enhanced in-pixel amplification
    (against noise of read-out chain)





Tests of analog part (”20” & ”14” μm epitaxy) :

- sensors illuminated with ^{55}Fe source and $F_{r.o.}$ varied up to $\gtrsim$ 150 MHz
- measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs $F_{r.o.}$

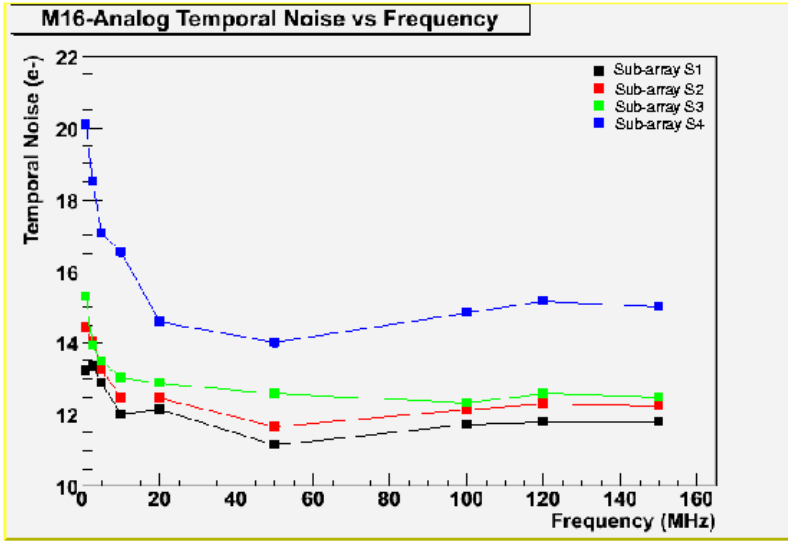
M.i.p. detection with Si-stip telescope studied at CERN in Sept. ’07 $\longrightarrow$ characterisation of digital response :

- π^- beam of $\sim$ 180 GeV/c
- measurements of SNR, det. efficiency, fake rate, cluster characteristics, spatial resolution vs discri. threshold

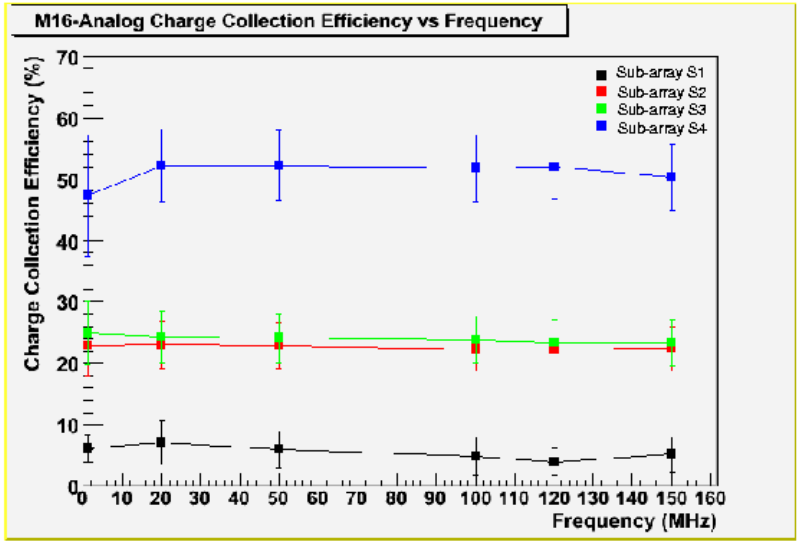
MIMOSA-16 Lab Test Results (Analog Part)

Pixel noise and charge collection efficiency (*"20 μm epitaxy* :

Temporal noise vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



Charge Collection Efficiency vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0

08/01/07 Résumé résultats Mimosa-16 chip#0 4

⇛ **Noise performance satisfactory (**like MIMOSA-8 and -15**)**

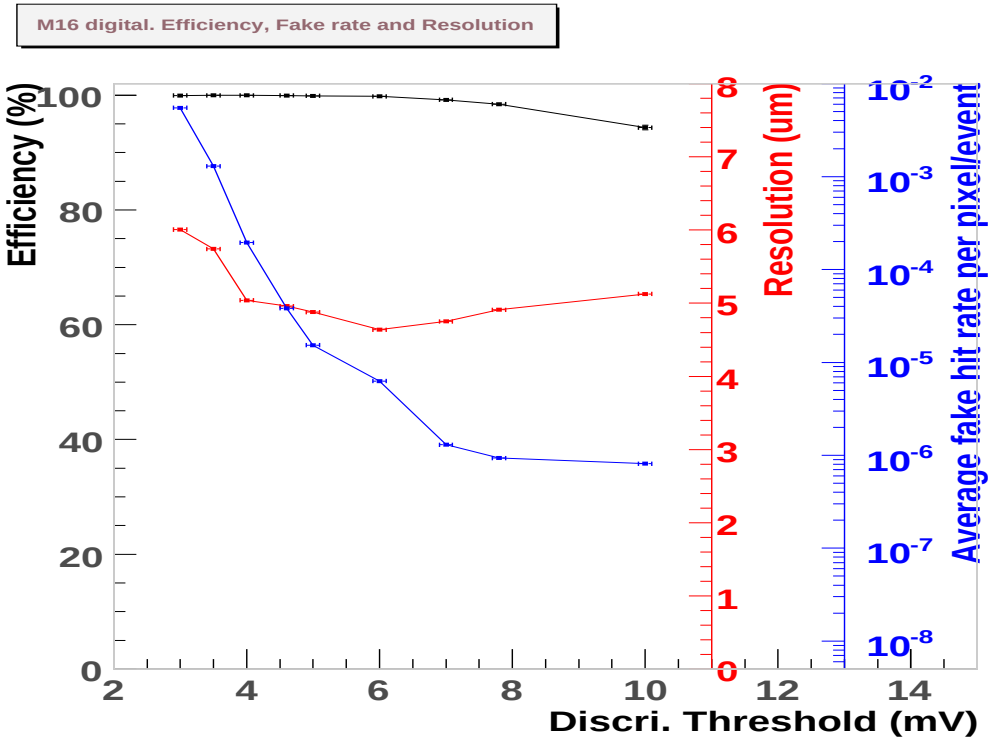
⇛ *CCE: very poor for S1 (*1.7x1.7 μm^2*) & poor for S2/S3 (*2.4x2.4 μm^2*)*

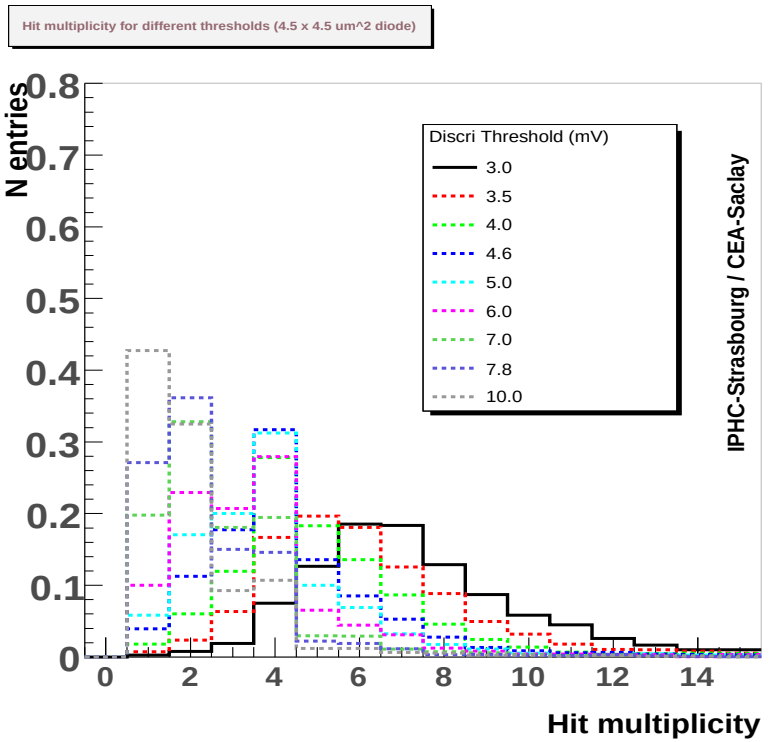
⟶ *already observed with MIMOSA-15 but more pronounced for "20 μm" option*

↪ suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 μm^2 diode)

MIMOSA-16 Beam Test Results (Digital Part)

- **CERN-SPS ($\sim$ 180 GeV π^-) $\longmapsto$ preliminary analysis results of S4 ("14 μm" epitaxy)**
- **Read-out time $\sim$ 50 μs** *($\sim$ 1/4 of max. freq. due to DAS limitations)*





- **Major result $\longmapsto$ at least one pixel architecture validated for next steps : S4 (SNR $\sim$ 16)**

Discri. Threshold	*det. efficiency*	*fake rate*	*sgle pt resolution*
4 m V	*99.96 $\pm$ 0.03 (stat) %*	*$\sim 2{\cdot}10^{-4}$*	*$\sim$ 4.8–5.0 μm*
6 m V	*99.88 $\pm$ 0.05 (stat) %*	*$<10^{-5}$*	*$\sim$ 4.6 μm*

Next steps :

- *Mid-term : EUDET, STAR $\rightarrowtail$ real experimental conditions; $\sim$ ILC VD outer layer requirements*
- *Long-term full sensor prototyping : ILC (mainly inner layers), CBM*

Integrated $\emptyset \rightarrowtail$ real scale sensors without ADC ($\sigma_{sp} \sim$ 4–6 μm) :

- ⁂ *EUDET telescope (2008)*
- ⁂ *STAR-HFT (2010)*
- ⁂ *CBM-MVD (201X)*

Integrated 4-5 bit ADC replacing discriminators and increased read-out speed :

- ⁂ *prototype for ILC-VD (2008/09)*
- ⁂ *read-out speed $\rightarrowtail$ CBM-MVD (201X)*

Status of ADC Developments

- **Several different ADC architectures under development at IN2P3 and DAPNIA**
  - **LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair**
  - **LPCC (Clermont) : flash 4+1.5-bit ADC for a column pair**
  - **DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC**
  - **IPHC (Strasbourg) : SAR 4-bit and Wilkinson 4-bit ADCs**

Lab	proto.	phase	bits	chan.	$F_{r.o.}$(MHz)	dim. (μm^2)	P_{diss}	eff. bits	Problems
LPSC	ADC1 ADC2 ADC3	tested tested fab	5 4 4	8 8 > 8	15-25 25 25	43x1500 40x943	1700 μW 800 μW	4	Offset & N
LPCC	ADC1 ADC2	tested fab	5.5 5.5	1 1	5(T)–10(S) 10	230x400 40x1100	20 000 μW 1000 μW	2.5	P_{diss} & bits
DAPNIA	ADC1 ADC2	tested fab	5 5	4 4	4 4	25x1000 25x1000	300 μW 300 μW	$\gtrsim 2$	Missing bits
IPHC	ADC1 ADC2	fab fab	4 4	16 16	10 10	25x1385 25x1540	660 μW 545 μW		

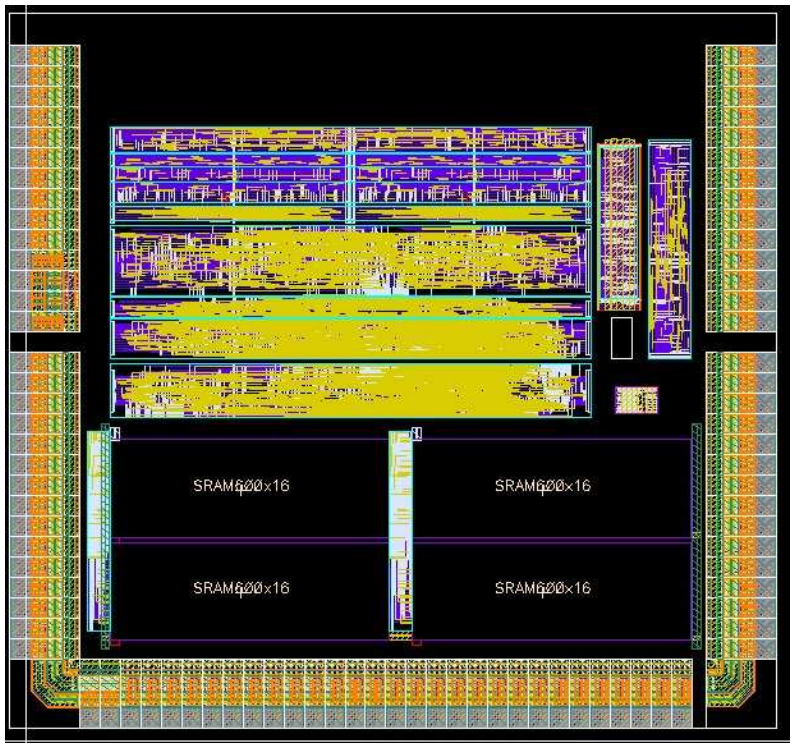
⇛ **1st mature ADC design expected to come out in 2007/08**

⇛ **Submission of 1st col. // pixel array proto equipped with ADCs in Summer 2008 (?) ⟶ with integ. ∅ in 2009**

Zero Suppression Micro-Circuit : SUZE-01 Fabrication

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - ◇ step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - ◇ step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim 3.9 \times 3.6$ mm^2
  $\hookrightarrow$ 10 keuros (funding via EUDET)



Status :

- sent for fabrication end of July
- back from foundry end of Sept. $\rightarrowtail$ tests under preparation $\Rightarrow$ test completion expected by end of year

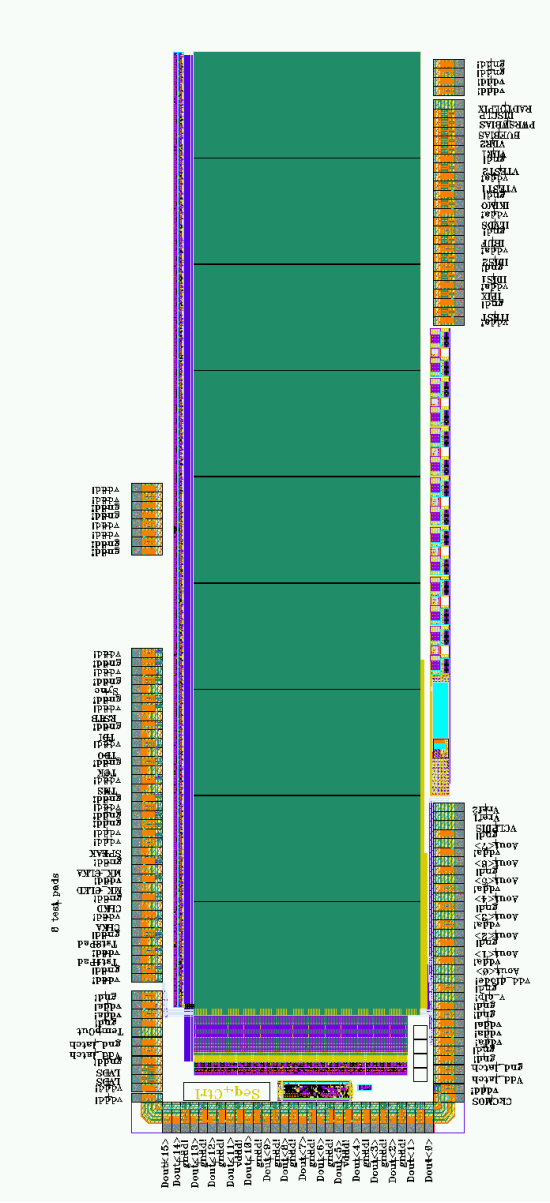
Final prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 $\rightarrowtail$ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

■ Pixel characteristics (*optimal charge coll. diode size ?*) :

- ⁂ pitch : 18.4 μm (compromise resolution/pixel layout)
- ⁂ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ⁂ 128 columns ended with discriminator
- ⁂ 8 columns with analog output for test purposes
- ⁂ 9 sub-matrices of 64 rows : various pixel designs w/o ionising rad. tol. diode

  $\Rrightarrow$ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)
- ⁂ read-out time $\sim$ 100 μs



■ Testability :

- ⁂ JTAG + bias DAC $\rightarrowtail$ programmable chip steering
- ⁂ 2 additionnal DC voltages to emulate pixel's output
  for independent discriminator performance assessment
- ⁂ output frequency $\leq$ 40 MHz

■ Status :

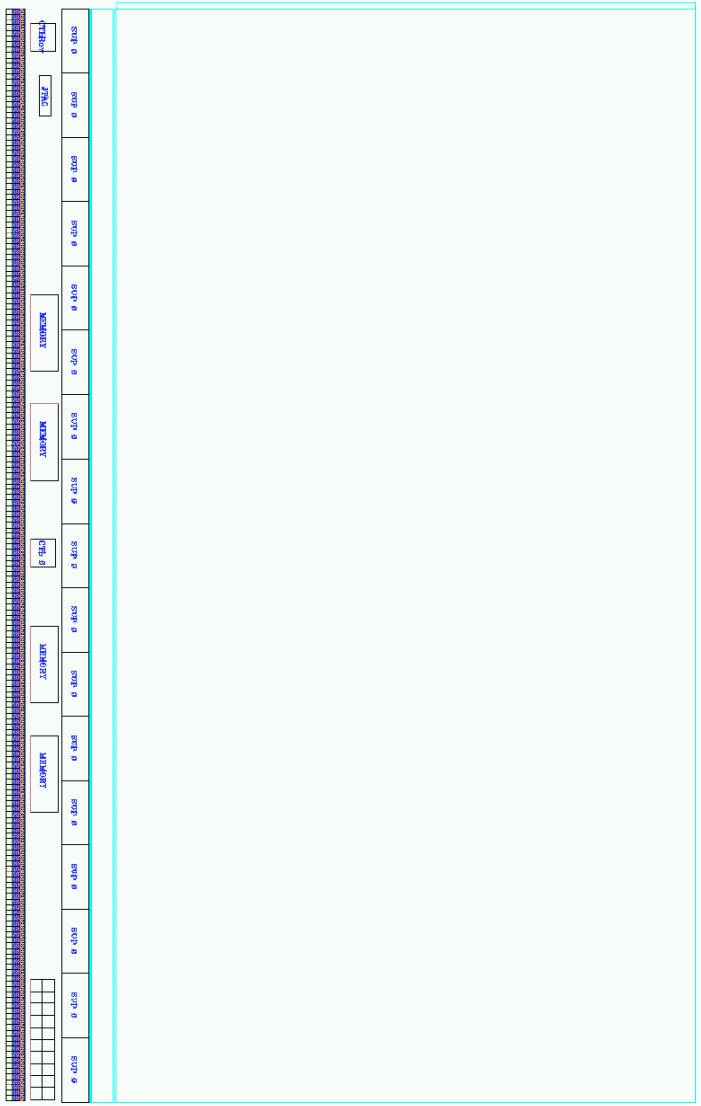
- ⁂ Design close to completion $\rightarrowtail$ submission by end of Oct. '07
- ⁂ Funding ($\sim$ 50 mm^2): $\sim$ 40 keuros (2/3 payed via EUDET)

Autumn 2008 : MIMOSA-22+ = Final EUDET Sensor

- **MIMOSA-22 complemented with ∅ (SUZE-01)**
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm^2)
- Read-out time $\sim$ 100 μs
- Chip dimensions : $\sim$ 20 x 12 mm^2

▷ Opportunity for an engineering run combining various chips (pixel+ADC ?):

$\sim$ 120 keuros for 6 diced and thinned wafers ($\sim$ 60 % via EUDET)



Devts performed in // :

- June 2008 : submission of final STAR-HFT1 sensor

  ▷ $\sim 2 \times 2$ cm^2 ✳ 400 kpix/sensor ✳ $\leq$ 640 μs ✳ 50 μm thin

  ↪ equip 2 or 3 sectors of 1 + 3 ladders (10 chips)

- Summer/Autumn 2008 : MIMOSA-16 with ADCs replacing discri.

  (24 columns of 128 pixels r.o. in //, with 4- or 5-bit ADC ending each col.)

Beyond 2008:

- **MIMOSA-22** with ADCs replacing discriminators ⟼ outer layers ⟼ inner layers
- **increase r.o. frequency** by $\sim$ 50 % (new ∅ & memory design) ⟼ inner layers

Integration Issues

- Thinning – Ladder design
- Power cycling – Data Flow

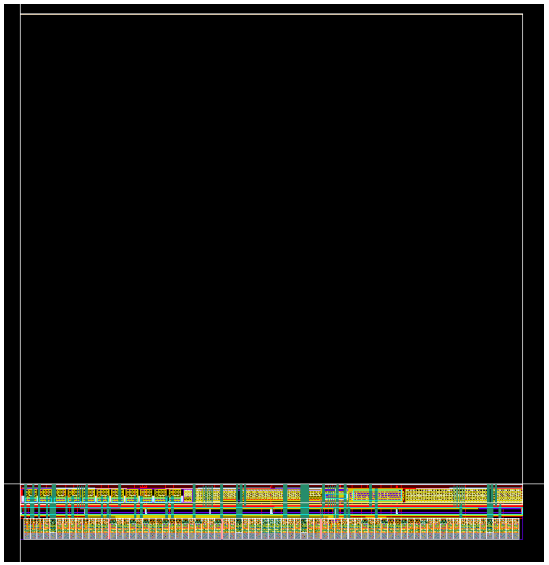
Thinning

Thinning motivations and constraints :

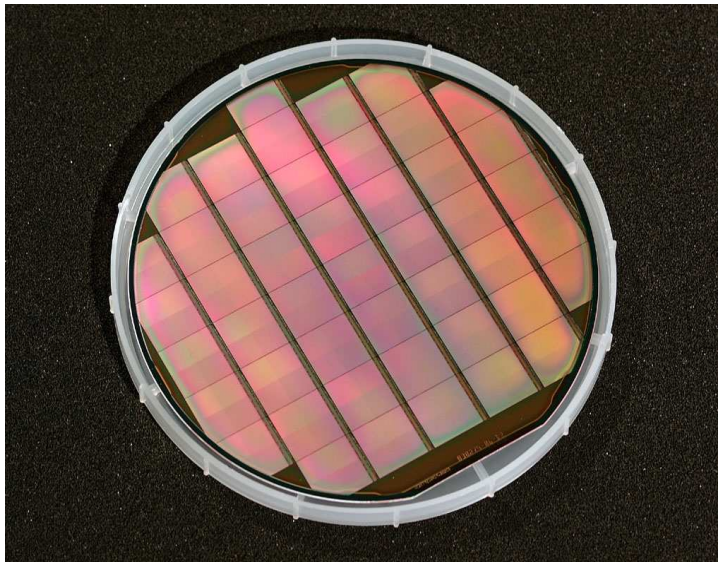
- *thin sensors to $\lesssim$ material budget of "mechanical support" (+ beampipe)*
- *minimal thickness of CMOS sensors :*

  10–15 μm (metal layers and SiO_2) + 15 μm (T + epitaxy) + 5–10 μm (substrate) $\approx$ 30–40 μm
- *thinned sensors should be "easy" to handle*
- *thinning procedure should have high mechanical yield and preserve detection performances*
- *CMOS technology fab. yield $\rightarrowtail$ foster diced sensors (despite few per-mill X_0 add. mat. budget)*
- *thinning of individual sensors seems preferable to full wafer thinning : cheaper but same quality ?*

MIMOSA-17 : 8 x 9 mm^2



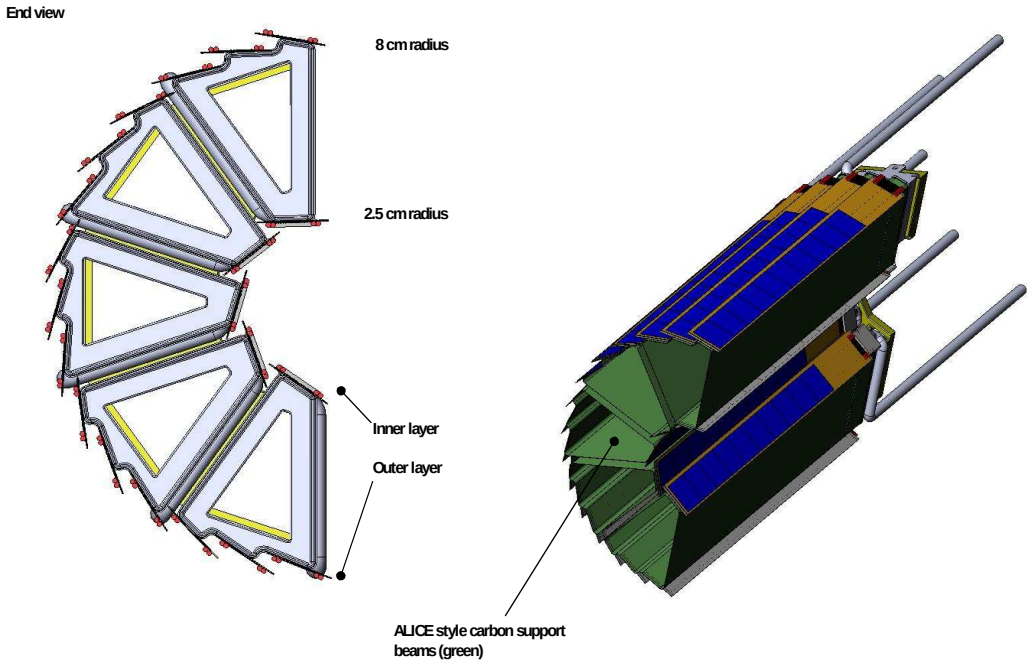
MIMOSA-5 : 6" wafer



Status of Thinning Studies and Ladder Prototyping (STAR)

- **Predominantly driven by STAR HFT project at LBNL**

Pixel support structure



- **Thinning of MIMOSA-5 wafers :**
  - *3 wafers thinned via LBNL to 50 $\pm$ 5 μm*
  - *result satisfactory (after pre-dicing):*
    sensors can be manipulated and mounted on support
  - *3 ladder prototypes fabricated at LBL ($\gtrsim$ 0.25 % X_0)*
    $\longmapsto$ up to 9 sensors mounted on ladder and tested

- **Thinning of individual sensors to $\sim$ 50 μm:**
  - *several chips of $\sim$ 0.2 – 3.5 cm^2 (MIMOSA-5, -10, -14, -17, -18, -20, etc.) thinned individually via LBNL*
  - *recent result: MIMOSA-18 prototype thinned to 50 μm was successfuly tested with ^{55}Fe at IPHC*
    $\longmapsto$ no change of performances (e.g. noise, gain)
  - *Plans:*
    - *operate thinned sensors (MIMOSA-17, -18) equipping telescopes (EUDET, TAPI, ...)*
    - *equip STAR-HFT1 with thinned sensors (2008/09) $\longmapsto$ 0.25 – 0.3 % X_0*
    - *extend development to ILC Vertex Detector (LBNL-ILC team ?) $\longmapsto$ goal $\leq$ 0.2 % X_0*

Power cycling

- *study performed with MIMOSA-5 at DESY*
- *though MIMOSA-5 not at all adapted to power cycling, it was operated with $\sim$ 1/8 duty cycle*
  - $\Rrightarrow$ *duty cycle $\lesssim$ 1/50 within reach with suited sensor design*

Data flow:

- *data flow / layer assessed at row, sensor, ladder, layer and full detector levels for BG $\times 1$ and $\times$ 3–5*
- *whole detector data flow expected to amount to $\sim$ 0.2 to 1 GB/s , depending on $e^{\pm}_{BS}$ rate*
- *instantaneous flow from row in inner most layer may be critical : up to 200 Bytes per 100 ns*

New concept of mechanical support & heat extractor:

- *objective : mount, connect & operate $\lesssim$ 10 MIMOSA-17 sensors, thinned to 50 μm, on 50–100 μm thin, aluminised, CVD diamond slabs $\equiv$ mech. support – heat extractor - cable support*
- *status : 3 diamond 3" wafers fabricated $\longmapsto$ electroplating and lithography*

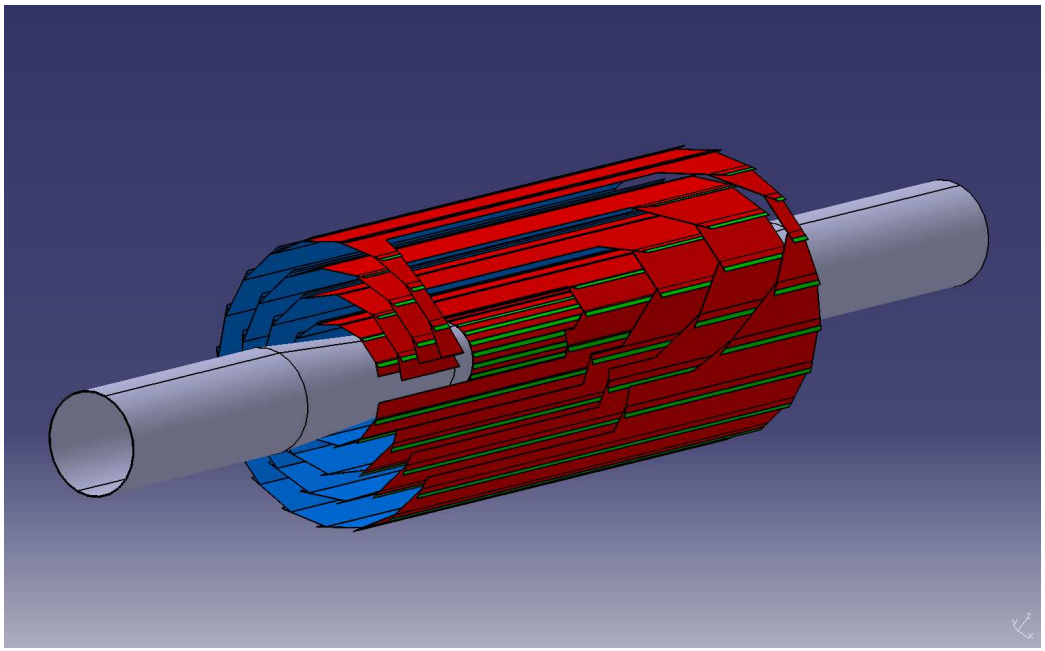
General remarks :

- *CMOS sensors call for* SPECIFIC *system integration solutions : connexions (flex cable), data flow, ...*
- **Lack of studies going on (expertised manpower) $\Rrightarrow$ may become a Problem**

Example of Basic Vertex Detector Design features

- *ILD geometry: $\gtrsim$ 5 cylind. layers (R = 15–60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96* ▷ *SiD: shorter barrel & fw/bw disks*
- *L0 and L1 : optimised against occupancy*
- *L2, L3 and L4 : optimised against power dissipation*
- *Pixel pitch varied from $\sim$ 20 μm (L0–L1) to $\gtrsim$ 30 μm (L2–L4) $\longmapsto$ minimise P_{diss}*

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P^{inst}_{diss} (W)	P^{mean}_{diss} (W)
L0	*15*	20	25	20	25	$<$100	$<$*5*
L1	$\leq$ *25*	25	50	$\leq$26	$\leq$ 65	$<$130	$<$*7*
L2	*37*	33	$\sim$100	24	50	$<$90	$<$*5*
L3	*48*	33	$\sim$100	32	80	$<$120	$<$*6*
L4	*60*	33	$\sim$100	40	150	$<$125	$<$*8*
Total				142	**330**	$<$600	**3–30**



- *Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; $\lesssim$ 40 μm thin sensors)*
- *Very low P^{mean}_{diss}: $<<$ 100 W (exact value depends on duty cycle)*
- *Fake hit rate $\lesssim 10^{-5} \longmapsto$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)*

- **MIMOSA sensors are being developed for running conditions with beam BG $>>$ MC simulations**

- **Fast read-out sensors progressing steadily :**
  - ⁂ *col. // architecture with discriminated output operational*
  - ⁂ *ADCs close to final design ($\lesssim$ Summer 2008)*
  - ⁂ *$\varnothing$ μcircuits : 1st generation (EUDET, STAR) fabricated $\rightarrowtail$ tests in Nov. '07*

- **AMS-035 OPTO fabrication technology assessed $\rightarrowtail$ baseline for R&D :**
  - ⁂ *detection efficiency (T), spatial resolution, radiation tolerance, noise $\rightarrowtail$ fake hits, etc.*
    - $\hookrightarrow$ *equip demonstrators (EUDET, CBM, STAR, ...) with full scale sensors operated in real exptal conditions (T_{room})*

- **Milestones until final chip well identified :**
  - ⁂ **1st step : final sensors with discriminated binary charge encoding for EUDET (2008) and STAR (2010)**
  - ⁂ **2nd step : replace discri. with ADC (outer layers) and increase r.o. frequency by $\sim$ 50 % (inner layers)**
  - ⁂ **also: find final fabrication process ($<$ 0.2 μm feature size)**

- **Concern :** **system integration issues not covered $\rightarrowtail$ prototype ladder ????**

- **Next :** *3DIT MIMOSA $\equiv$ 4 chip sandwich of best techno. for sensing, for analog, for mixed, and for digital circuits*

BACK-UP SLIDES

Milestones bridging the gap with the Complete Chip

Pixel design :

- adapt existing pixel architectures from 25 μm to $<$ 20 μm pitch
- adapt sensing diode dimensions to maximise CCE (surface $\nearrow$) & gain (surface $\searrow$) : optimum $\sim$ 10–15 μm^2
- ▶ find optimal pixel pitch : single point resolution (pitch $\searrow$) against reliable design (pitch $\nearrow$)

Column read-out architecture :

- adapt existing S&H and discriminators from 25 μm to $<$ 20 μm pitch
- integrate $\emptyset$ and output memories

Row and pixel steering (consequences of large surface) :

- adapt pixel steering (speed) inside column to avoid capacitance due to large nb of switches $\rightarrowtail$ pixel design
- adapt row steering to their length (2 cm)

Sensor autonomy and testability :

- JTAG + bias DAC $\rightarrowtail$ programmable chip steering
- 2 or 3 additionnal DC voltages to emulate pixel's output for independent discriminator performance assessment

Major R&D Milestones in Next 5 Years

Developments simultaneously oriented towards well focussed applications and towards generic objectives useful to several applications

Application	version	2006	2007	2008	2009	2010	2011
STAR	HFT-1	R&D	final proto.	Prod.			
	HFT-2	R&D	R&D	R&D	proto final	Prod.	
EUDET	BT-1	2 Prod.	commissioned				
	BT-2	R&D	final proto	Prod.			
Imaging		R&D	final proto	Prod. ?			
Generic topics							
Fast sensors :	○ architecture	R&D	R&D	R&D +	R&D ++	ILC proto	CBM proto
	○ ADC	R&D	R&D	final proto	↗		
	○ digital	pre-study	R&D	final proto	↗		
Radiation tolerance		R&D	R&D	R&D	R&D	↗	
Fabrication technologies		R&D	R&D	R&D	R&D	↗ ???	
Thinning		R&D	D	D	OK ???		

AMS 0.35 OPTO engineering run (fabricated in Summer 2006):

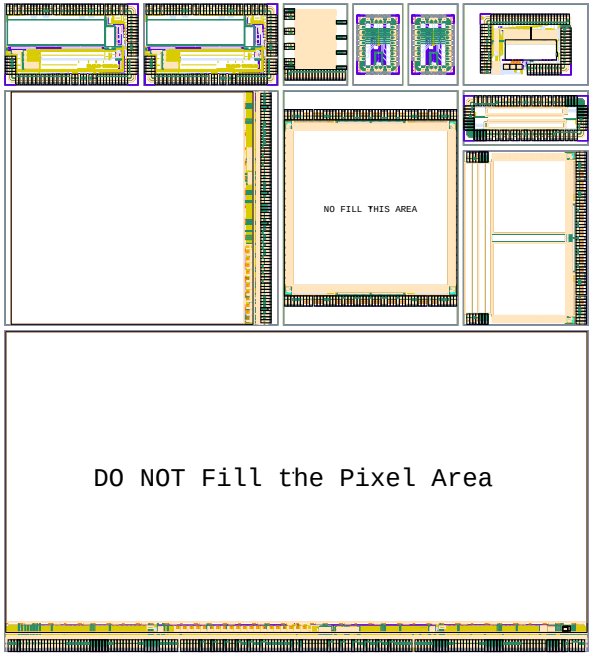
≙ 2 + 4 wafers (8" ⇛ 50 reticles/wafer) ≙ 2 epitaxy thicknesses : $\sim$ 11 & 15 μm ⇔ "14 μm" & "20 μm" options

◇ triggered by MIMO★-3 (= MIMOSA-20) fabrication :

200 kpixels, $\sim$ 2 cm^2, 2 // outputs, $t_{r.o.} \lesssim$ 4 ms

◇ includes 8 other chips :

- ✳ MIMOSA-16 : fast col. // archi. like MIMOSA-8
- ✳ MIMOSA-17 (MIMO★-3M) : 0.8 x 0.8 cm^2, rad.tol., 800 μs
  - ↪ EUDET beam telescope arms, CBM Vx Det. demonstrator
- ✳ MIMOSA-18 (IMAGER) : precision $\lesssim$ 1 μm (EUDET: DUT)
- ✳ MIMOSA-19 bio-med. imaging: special diode shape
- ✳ test structures : in-pixel amplification, discrimination, ...
- ✳ ADCs: flash from LPCC



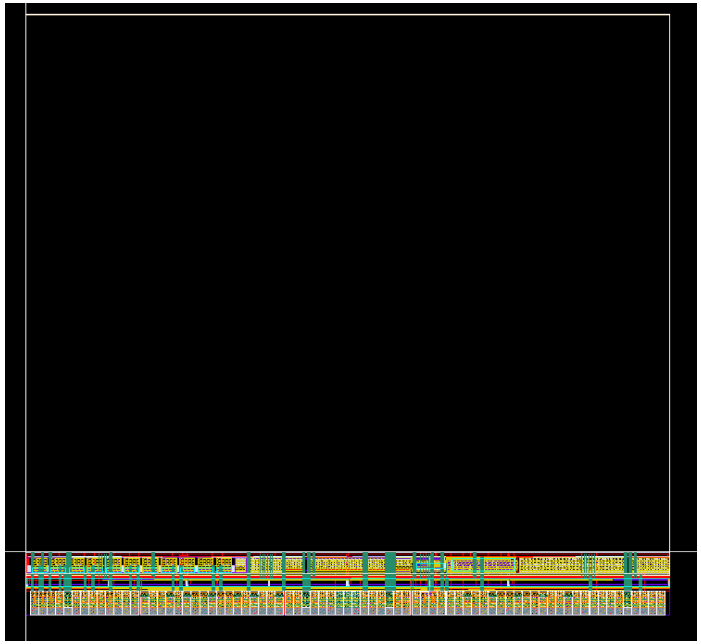
< $\sim$ 20 mm >

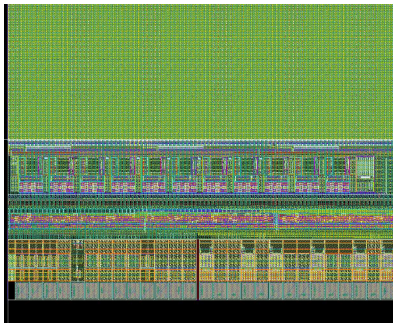
Status of tests:

◇ 2 wafers tested in 2006 (1 with "14" & 1 with "20" μm epitaxy) ↦ fab. mistake (non uniform effect on sensors)

↪ not dramatic: "20 μm" option was characterised with ^{55}Fe source

◇ Second batch fabricated in 2007 ↦ 7 wafers presently under test ⟶ fab. yield





- **New *working horse*, superseeding MIMOSA-5 :**
  - **Faster, much easier to operate, ionising rad. tol., etc.**
  - **$\Rightarrow$ equip MVD demonstrator**

- **Medium size copy of STAR final sensor prototype :**
  - **(65 000 pixels instead of 205 000)**
  - **※ manufactured in AMS 0.35 μm OPTO techno.**
    with $\gtrsim$ 11 μm and $\sim$ 15 μm epitaxial thickness
    $\longmapsto$ tests started at IPHC (and DESY)
  - **※ ionising rad. hard pixel design (validated with MIMOSA-11/-14)**
  - **※ 4 matrices of 64 x 256 pixels (30 μm pitch) treated in //**
    $\longmapsto$ active area of $\sim$ 8 x 8 mm^2
  - **※ 4 parallel analog outputs at 10 (or 20) MHz**
    $\longmapsto$ frame r.o. time = 1.6 ms (or 800 μs)
  - **※ integrated JTAG logic for steering**
  - **※ works at room temperature**

- **Equips EUDET telescope demonstrator (e.g. 2 arms of 3 planes)**
  $\longmapsto$ commissionned in Spring/Summer 2007 at DESY

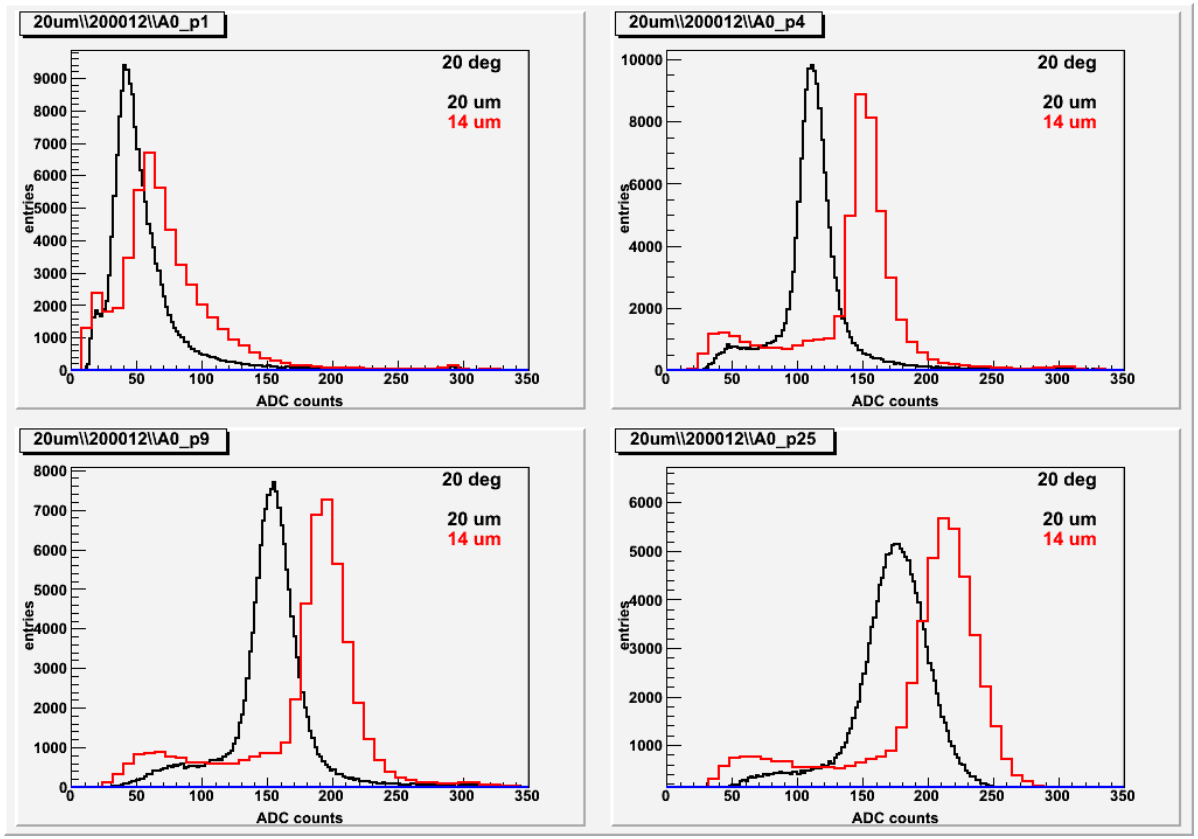
MIMOSA-20 : CCE for ”14” and ”20” μm Epitaxy

IPHC Institut Pluridisciplinaire Hubert Curien Strasbourg

Réunion Capteurs CMOS, lundi 26 fevrier 2007

Mathieu Goffe
Mathieu.goffe@ires.in2p3.fr

Comparaison pour Mimosa20 entre les deux types de couches épitaxie



IPHC, 23 rue du Loess BP 28, 67037, Strasbourg Cedex 02, France

- MIMOSA-20 (”14” & ”20” μm epitaxy) illuminated with ^{55}Fe source
  - $\rightarrowtail$ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters
    - $\rightarrowtail$ **CCE (”14” μm) $\sim$ 30–40 % higher than CCE (”20” μm)**

Main Requirements

for the ILC Vertex Detector :

physics & running condition requirements

Constraints from Required $\sigma_{i.p.}$ (1/2)

- $\sigma_{\mathbf{IP}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \mathbf{sin}^{\mathbf{3/2}}\theta$ with $\mathbf{a} <$ 5 μm and $\mathbf{b} <$ 10 μm

  ▷ limits on $\mathbf{a}$ and $\mathbf{b}$ are still "very educated guesses"

  ▷ SLD: $\mathbf{a}$ = 8 μm and $\mathbf{b}$ = 33 μm

- Upper bound on $\mathbf{a}$ drives the pixel pitch and the radii of the inner and outer layer of the Vx Det.

- Upper bound on $\mathbf{b}$ drives radius and material budget of inner layer (& beam pipe)

- Constraint on σ_{IP} satisfies simultaneoulsy requirement on double hit separation in inner most layer ($\sim$ 30 – 40 μm)

Constraints from Required $\sigma_{i.p.}$ (2/2)

Constraint on a : $z_{IP} \approx \frac{z_0 \cdot R_4 - z_4 \cdot R_0}{R_4 - R_0} \rightarrowtail a = \sigma_{IP} \approx \frac{(R_4^2 \cdot \Delta z_0^2 + R_0^2 \cdot \Delta z_4^2)^{1/2}}{R_4 - R_0}$

- Numerical examples based on $R_4 = 4 \cdot R_0$ (ex: R_4/R_0 = 60 / 15 mm or 64 / 16 mm)
  - ▷ $\Delta z_4 = \Delta z_0 = \sigma_{sp} = 3\,\mu m \Rightarrow a \approx 1.37 \cdot 3\,\mu m \approx 4.1\,\mu m$
  - ▷ $\Delta z_4 = 5\,\mu m$ and $\Delta z_0 = 2.5\,\mu m \Rightarrow a \approx 1.5 \cdot 2.5\,\mu m \approx 3.8\,\mu m$

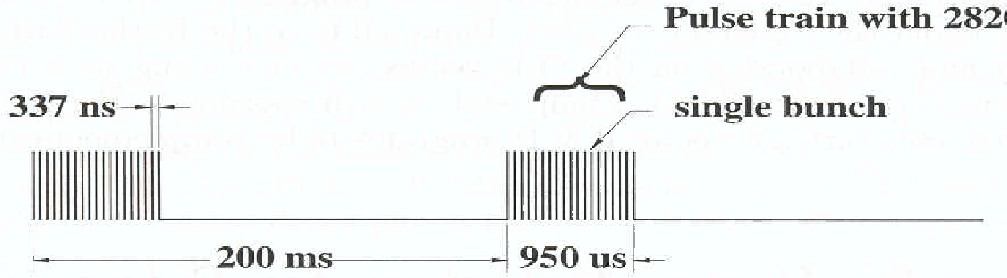
⇛ Twice larger pitch in outer layer than in inner most layer satisfies constraint $a < 5\,\mu m$

Constraint on b : $b \approx 0.0136 \cdot (1 + 0.038 \cdot \ln t/\sin\theta) \cdot R_0 \cdot \sqrt{t}$ where $t = \frac{e_{pipe}}{X_0^{Be}} + t_{L0}$

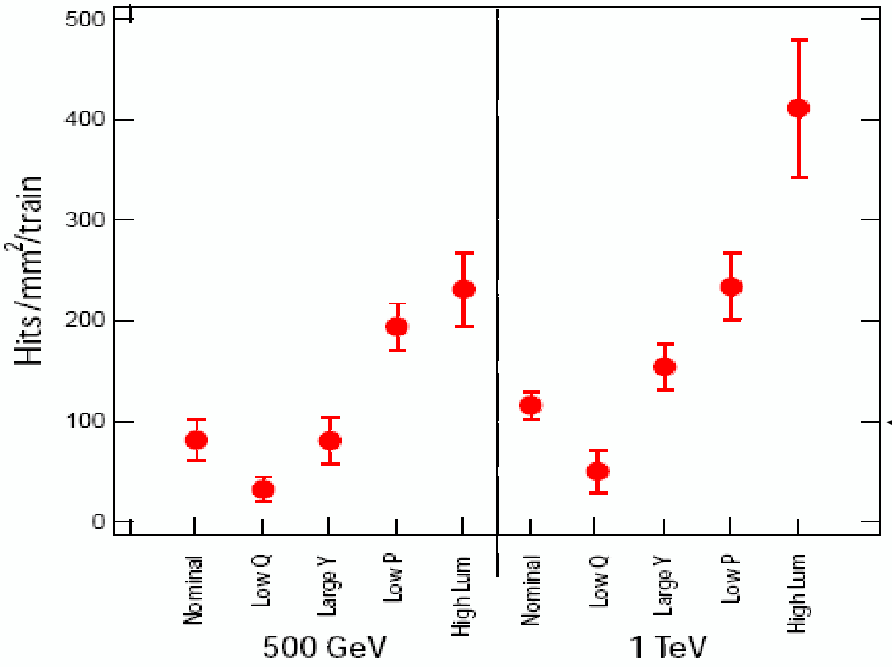
- ▷ $b < 10\,\mu m \Rightarrow t \lesssim 0.4\,\%$
- ▷ $e_{pipe} \approx 400 - 500\,\mu m \rightarrowtail \frac{e_{pipe}}{X_0^{Be}} \sim 0.11 - 0.14\,\% \rightarrowtail t_{L0} \lesssim 0.25\,\%$

- Ladders equipped with CMOS sensors & developed for STAR HFT reach already $\sim$ 0.3 % X_0

Time Structure for the ILC



Backgrounds



~0.035/mm²/bunch

M. Breidenbach

Constraints from Beamstrahlung

- **1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor**
  $\rightarrowtail \lesssim$ 1.8·10^{12} e$^{\pm}$/cm^2/yr (safety factor of 3)
  - **2nd layer: 8 times less (direct)**
  - **3rd layer: 25 times less (direct)**

- **Consequences on Occupancy in 1st layer (L0): $\lesssim$ 0.9 % hit occupancy in 50 μs (r.o. time of TESLA TDR)**
  $\hookrightarrow$ signal spread on $\lesssim$ 4.5–9 % pixels (cluster multiplicity $\sim$ 5-10)

  $\Rrightarrow$ 1) aim for shorter read-out time in L0 than in TDR $\rightarrowtail$ typically $\lesssim$ 25 μs
  (compromise with power dissipation, multiple scattering, ...)

  2) aim for shorter read-out time in L1 than in TDR $\rightarrowtail$ typically $\sim$ 50 μs (vs 250 μs)
  and presumably smaller radius (e.g. $\sim$ 20 – 22 mm)
  (use tracks extrapolated from L1-4 down to L0)

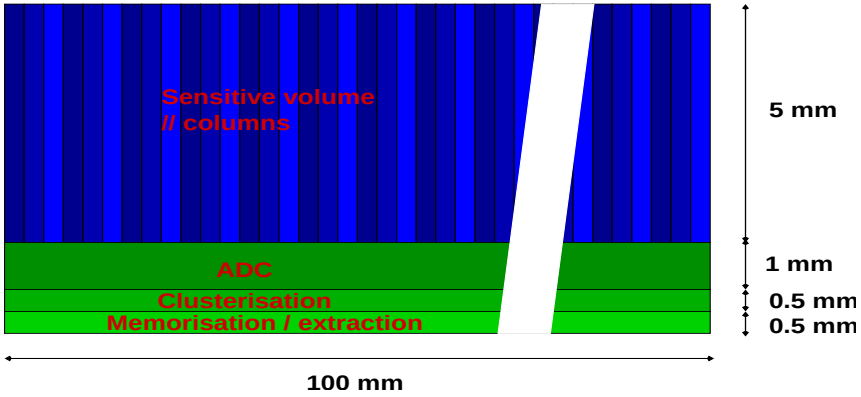
  3) aim for relaxed read-out time in L2, L3, L4: $\sim$ 100 – 200 μs (vs 250 μs)
  $\hookrightarrow$ depends on backscattered e$^{\pm}$ rate

- **Consequences on Radiation Tolerance in L0 :**
  - ※ **dose integrated over 3 years: $\lesssim$ 5.4·10^{12} e/cm^2 $\longrightarrow \lesssim$ 2·10^{11} n$_{eq}$/cm^2 (NIEL $\sim$ 1/30)**
  - ◇ **neutron dose integrated over 3 years much smaller : $\lesssim$ 3·10^{10} n$_{eq}$/cm^2 (safety factor of 10)**

Consequences on Inner Layer Design

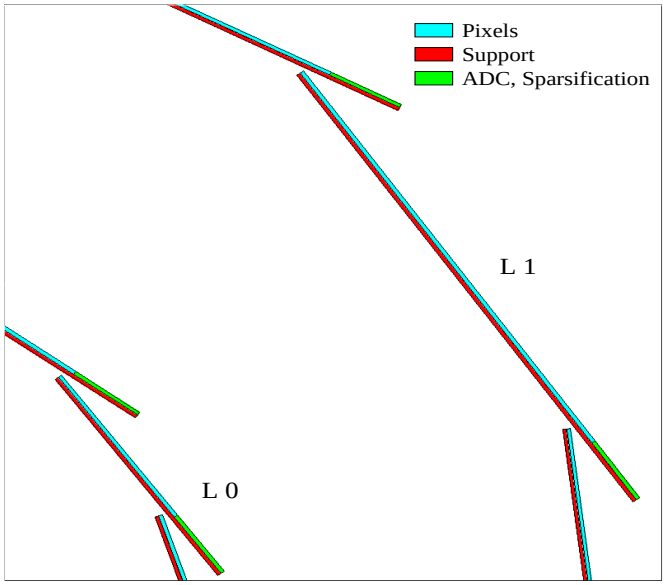
- $\lesssim$ 25 μs in L0:
  columns of 256 pixels (20 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 5 mm depth

- $\sim$ 50 μs in L1:
  columns of 512 pixels (25 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 13 mm depth



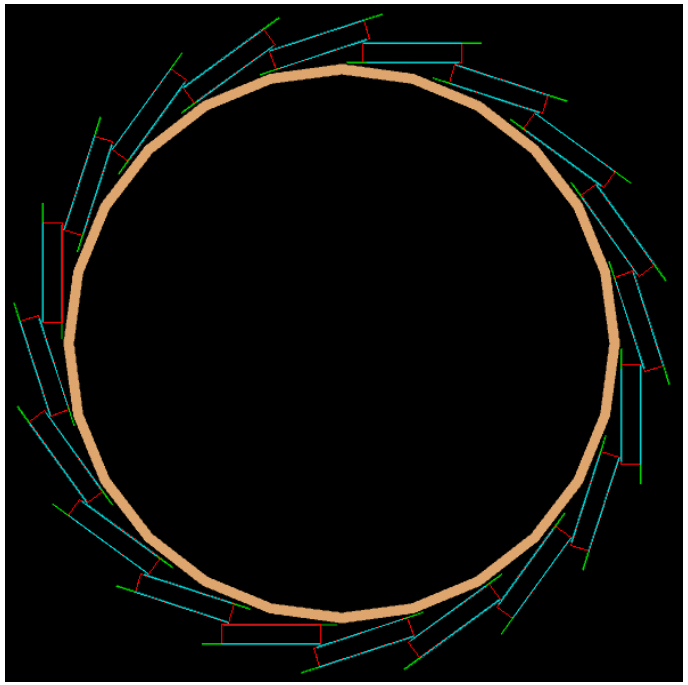
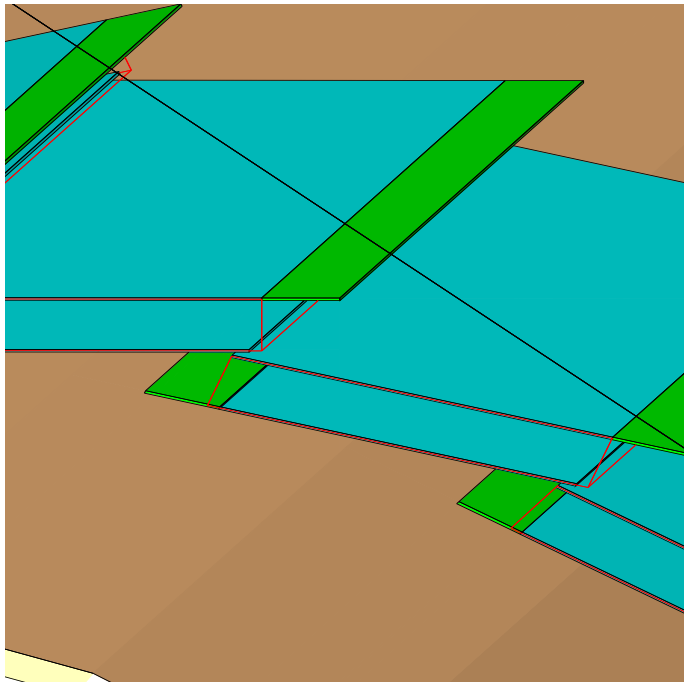
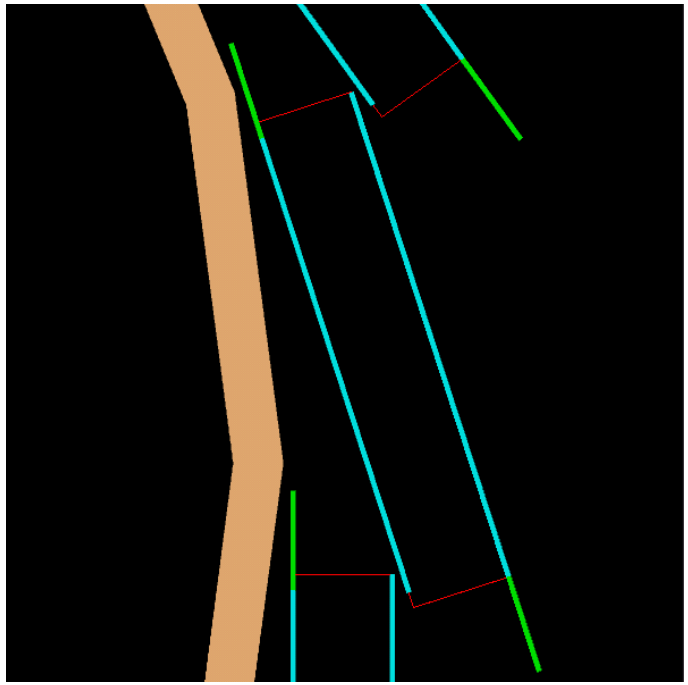
- $\lesssim$ 2 mm wide side band hosting ADC, sparsification, ...
  $\hookrightarrow$ effect on material budget SMALL :
  b increases by $\sim$ 5 – 10 %

- Option with discriminator instead of ADC :
  $\sim$ 1 mm wide side band $\Rightarrow$ effect on $\mathrm{b} < 5$ %

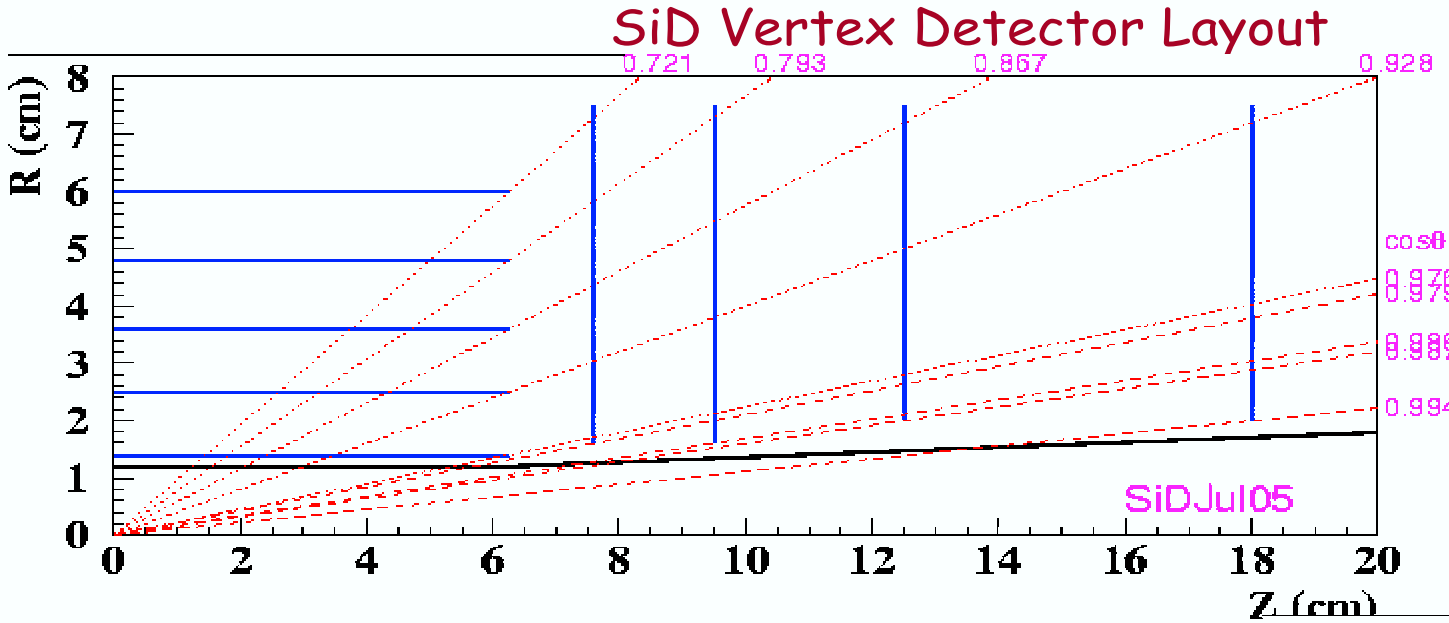


Adapting the Inner Most Layer to High Background

- Design inner most layer (L0) to minimise its sensitivity to (unexpected) high occupancy ($\gtrsim$ 10 %)
- Double sided layer $\longrightarrow \sim$ 1 mm long mini-vectors connecting impacts on both sides of layer
  - ▷ Needs a detailed feasibility (engineering) study ....

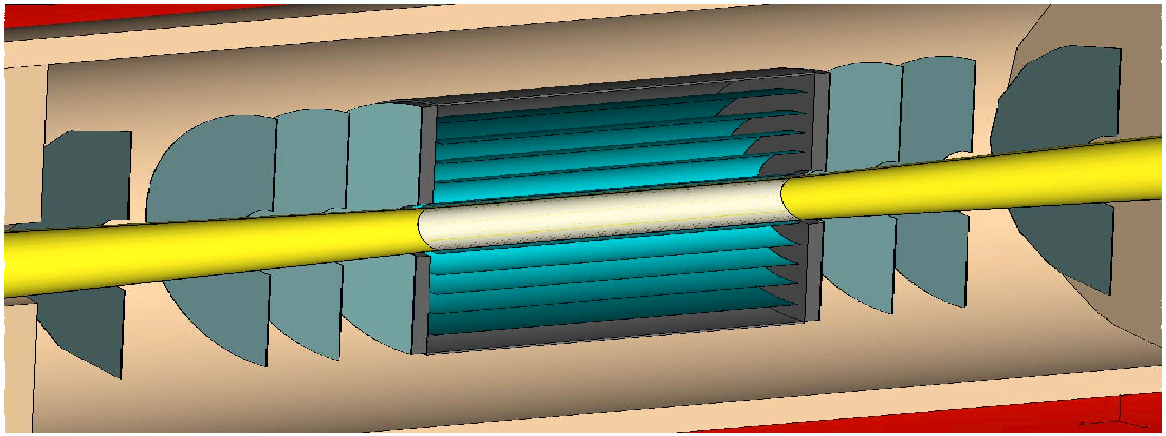




Alternative Approach : SiD Vertex Detector Geometry



5 barrel layers
4 end disks

5 Tesla



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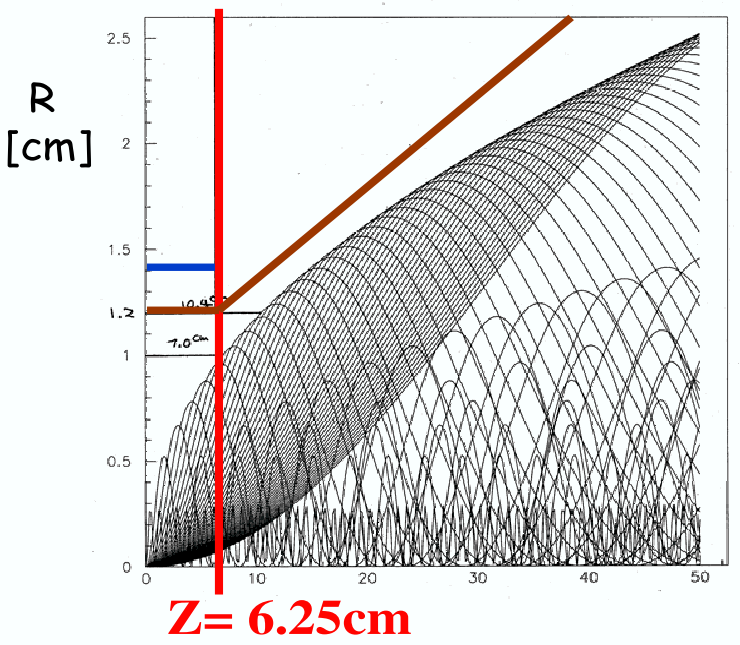


Summary of Sensor Perfo. Obtained vs Requirements

- **Impact parameter resolution :**
  - **a** $< 5\ \mu m$ ✓
  - **b** $< 10\ \mu m$ ✓ $\longrightarrow$ **thinning** ✓ **, ladder design** ✓ **(from STAR), stitching not yet investigated**

- **Radiation tolerance at room temperature :**
  - **neutrons** ✓
  - **X-Rays** ✓
  - **10 MeV electrons** ✓ $\longrightarrow$ **only assessed at T** $\lesssim$ **0°C**

- **Fast, low power, integrated signal processing :**
  - **read-out speed** ✓
  - **integrated ADC** $\longrightarrow$ **under developement**
  - **integrated sparsification** $\longrightarrow$ **studies starting**
  - **power dissipation** ✓ **(duty cycle** $<$ **1/20)** $\longrightarrow$ **pulsed powering not fully assessed for this duty cycle**

- Overall geometry :
  - ✳ matching with neighbour trackers
- Sensor geometry and features
- Heat removal
- Thermal distortions
- Handling thin silicon
- Assembly and alignment procedures
- Connections, cabling, and optical fibers
- Paths for cables, optical fibers, and air flow
- Lorentz forces

⇒ **Only few people taking care of so many crucial and delicate topics**

Observed Radiation Tolerance

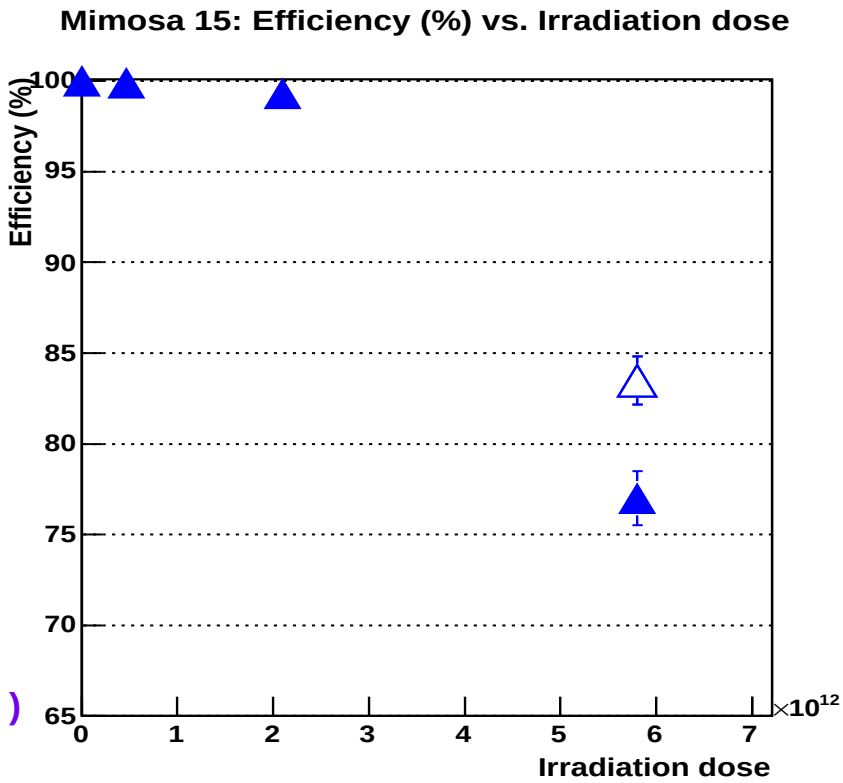
of MIMOSA Sensors

Radiation Tolerance: Non-Ionising Radiation

- **MIMOSA-15 irradiated with neutrons of O(1 MeV) at JINR (Dubna) $\mapsto$ doses of 0.47 / 2.1 / 5.8 $\cdot 10^{12} n_{eq}/cm^2$**
- **Performance assessment of sensors (20 μm pitch) installed on $\sim$ 5 GeV e^- beam at DESY (July 2006)**
  - **running conditions: T = - 20°C, $t_{r.o.} \sim 700\ \mu s$ (2.5 MHz)**
    - $\hookrightarrow$ **Very Preliminary results ...**

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
	(10^{12} n_{eq}/cm^2)				
Noise (e^-)	9.0 $\pm$ 1.1	9.2 $\pm$ 1.2	9.3 $\pm$ 1.2	9.6 $\pm$ 2.0	9.6 $\pm$ 1.9
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	*8.7* $\pm$ 2.	*7.5* $\pm$ 2.
Det. Eff. (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2.	84. $\pm$ 2.

- 5.8·10^{12} n_{eq}/cm^2 values derived with **standard** and with **soft** cuts



$\Rightarrow$ **Fluences $\gg 10^{12} n_{eq}/cm^2$ affordable with simple pixels (no CDS $\mapsto$ low N)**

provided T $< 0°$C and $t_{r.o.} \ll 1$ ms

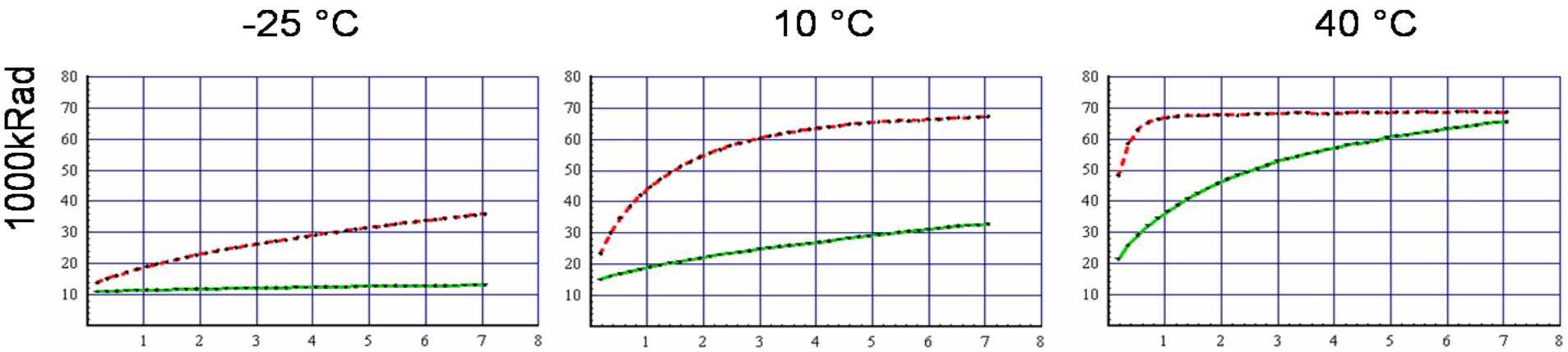
$\triangleright\triangleright\triangleright$ **Fluences $>>$ 1·10^{12} n_{eq}/cm^2 can presumably be accommodated with pixels including CDS by optimising pixel pitch, charge collection syst., fabrication techno., etc.**

Radiation Tolerance : Ionising Radiation

- Pixel design needs to be modified to withstand high radiation doses (esp. at T_{room}):
  - removal of thick oxide nearby the N-well (against charge accumulation)
  - implantation of P+ guard-ring in polysilicon around N-well (against leakage current)

- Characterisation of MIMOSA-11 in laboratory : Noise (e^- ENC) vs Integration time (ms)

  for Ordinary and Radiation Tolerant pixels, measured at T = - 25°C, + 10 °C and + 40°C



- Characterisation of MIMOSA-15 with $\sim$ 5 GeV e^- at DESY after 1 MRad (10 keV X-Ray) exposure :
  - Radiation Tol. pixels, measured at T = - 20°C with $t_{r.o.} \sim 180\ \mu s$ (10 MHz) $\Rightarrow$ Very preliminary results :

※ 1 MRad tolerance demonstrated at T $<$ 0°C

(read-out time $\ll$ 1 ms, no CDS)

Integ. Dose	Noise	S/N (MPV)	Det. Efficiency
0	9.0±1.1	27.8±0.5	100 %
1 MRad	10.7±0.9	19.5±0.2	99.96±0.04 %

※ *need to cross-check detection performance at T_{room} with pixels including CDS*

- **Reduce mean free path of signal e^- :**
  - ⁜ Reduce pixel pitch (optimise w.r.t. r.o. speed) $\mapsto$ MIMOSA-18 (10 μm pitch) $\rightarrowtail$ rad.tol tests in '07 ?
  - ⁜ Pixel architecture with improved charge collection (sensing diode, epitaxy):
    - MIMOSA-15 under study $\mapsto$ intrinsic noise higher than expected
    - MIMOSA-21 fab. in BiCMOS techno. (enhanced depletion of epitaxy) $\rightarrowtail$ tests started
  - ⁜ Optimise operation temperature
  - ⁜ Investigate annealing possibilities
- **Improve S/N performance :**
  - ⁜ Optimise pixel and r.o. architecture $\mapsto$ MIMOSA-16 sub-array
  - ⁜ Investigate thick epitaxy techno. $\mapsto$ AMS 0.35 OPTO "20 μm" epitaxy option : tests under way
  - ⁜ Optimise cluster rec. algo. (lower cuts $\mapsto$ more fake hits $\mapsto$ how much can STS tracking afford ?)
- **Equip each detector plane with 2 layers of sensors :**
  - $\hookrightarrow$ ○ 90 % detection efficiency per layer allows 99 % detection efficiency per plane
  - ○ double layer $\mapsto$ track mini-segments from loosely selected clusters $\mapsto$ improved det. eff.
  - ⁜ Thinning sensors to ultimate thickness ($\sim$ 30 μm) is particularly valuable
  - ⁜ Design mechanical support allowing double sensor layer per detector plane

Radiation Tolerance vs Detection Efficiency vs Fake Hits

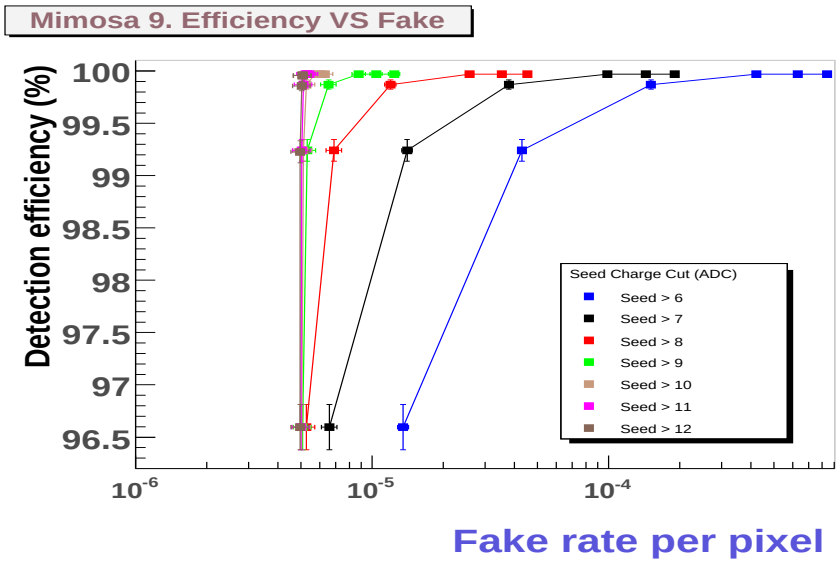
- **Effect of radiation damage : S/N decreases $\Rightarrow$ det. eff. decreases as well**

  $\hookrightarrow$ recuperate part of det. eff. loss by relaxing the requirements on pixel charge in cluster algo.

  $\Rightarrow$ rate of fake clusters will increase

- **Efficiency vs rate of fake clusters :**
  - vary cut on seed pixel : 6 $\rightarrowtail$ 12 ADC units
  - vary cut on Σ of crown charge : 0, 3, 4, 9, 13, 17 ADC unit

  $\Rightarrow \epsilon_{det} \sim$ 99.9 % for fake rate $\sim 10^{-5}$



- **Importance of fake cluster rate in irradiated MVD for track reconstruction :**
  - an accurate track extrapolation from STS to MVD allows to cope with relatively high fake rate

  $\Rightarrow$ accuracy of STS has significant consequences on tolerance of MVD to non-ionising radiation

  $\hookrightarrow$ Account for it in the design