DEPFET Active Pixel Sensors for the ILC

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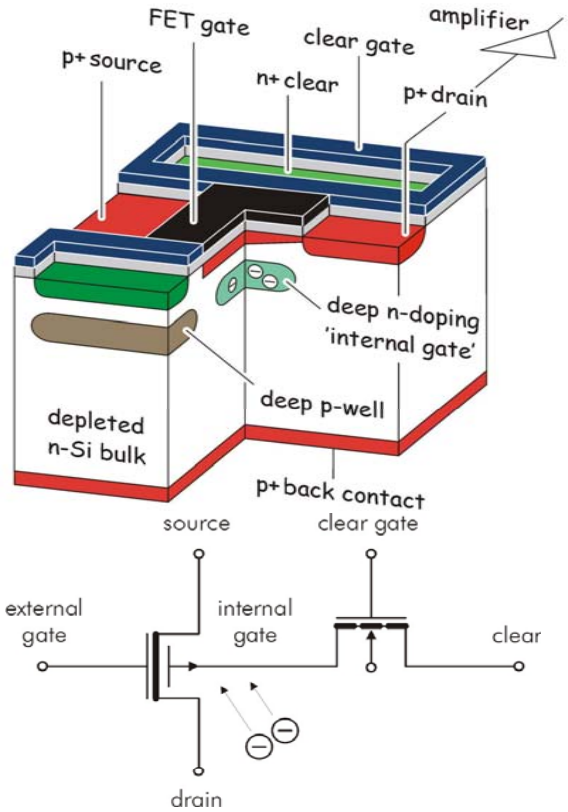
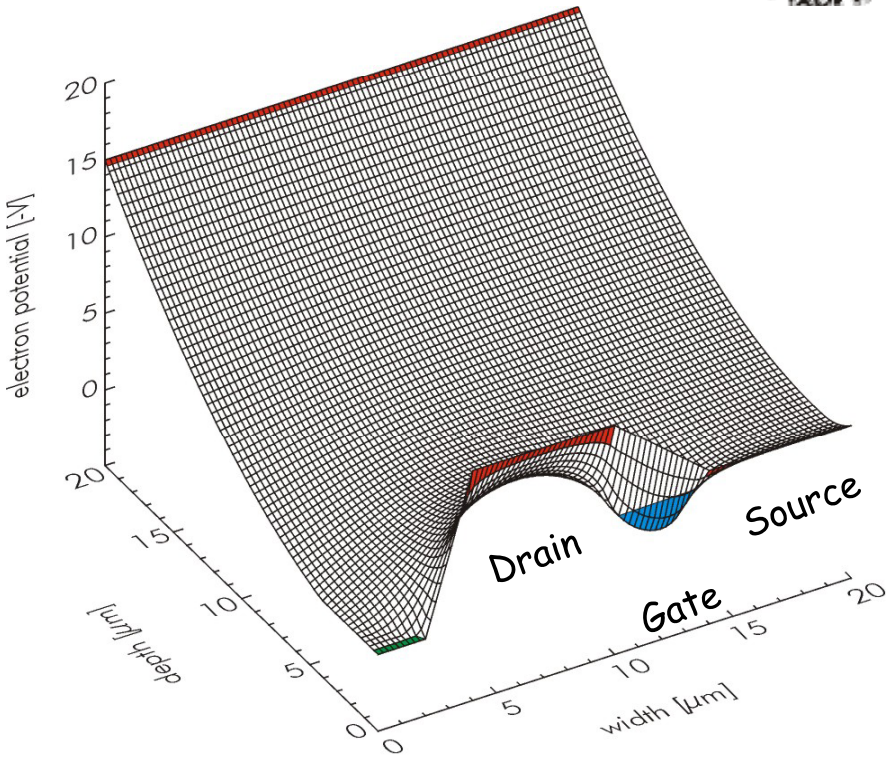
for the DEPFET Collaboration
(www.depfet.org)

DEPFET Principle

J. Kemmer & G. Lutz, 1987

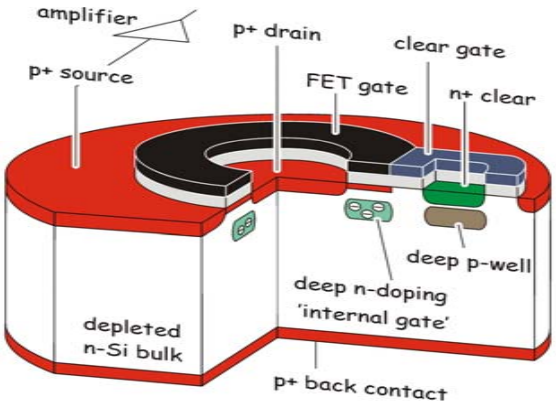
DEpleted P-channel FET





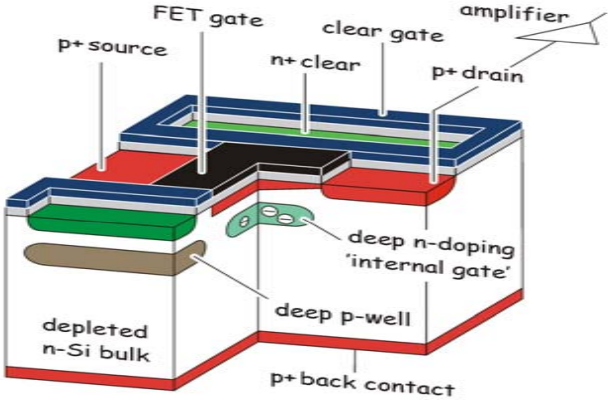
- fully depleted sensitive volume, charge collection by drift
- internal amplification → q-I conversion: 0.4 nA/e, scales with gate length and bias current
- Charge collection in "off" state, read out on demand

Overview: Types and Applications



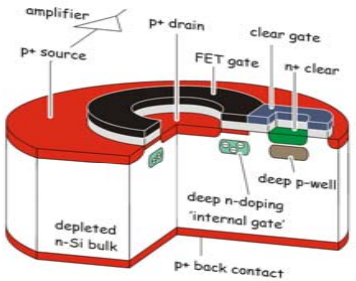
X-ray imaging spectroscopy → XEUS

- pixel size: 100µm
- r/o time per row: 2.5 µs
- Noise: ≈4 el ENC



Particle tracking → vertex detector at ILC

- pixel size: 24µm
- r/o time per row: 25
- Noise: ≈100 el ENC
- thin detectors: ≈50µm



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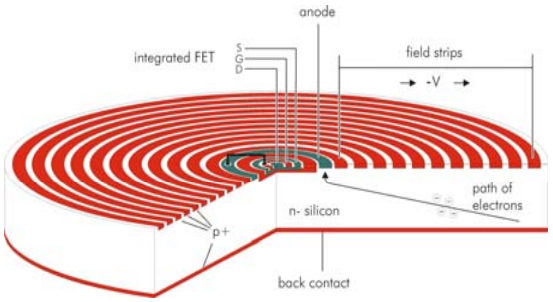
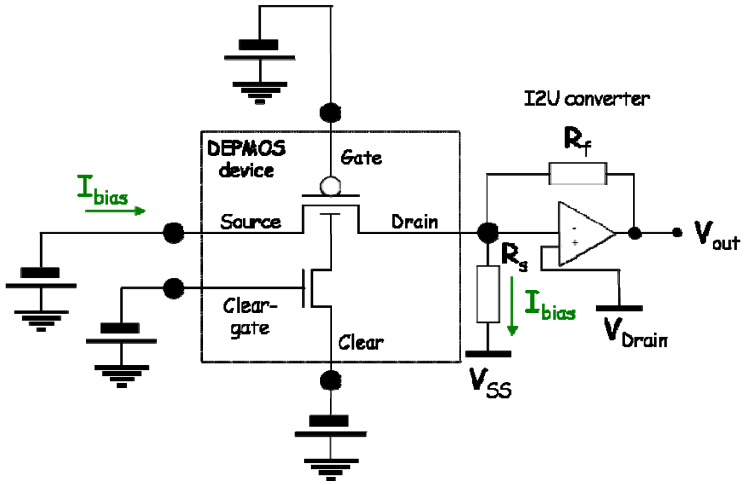


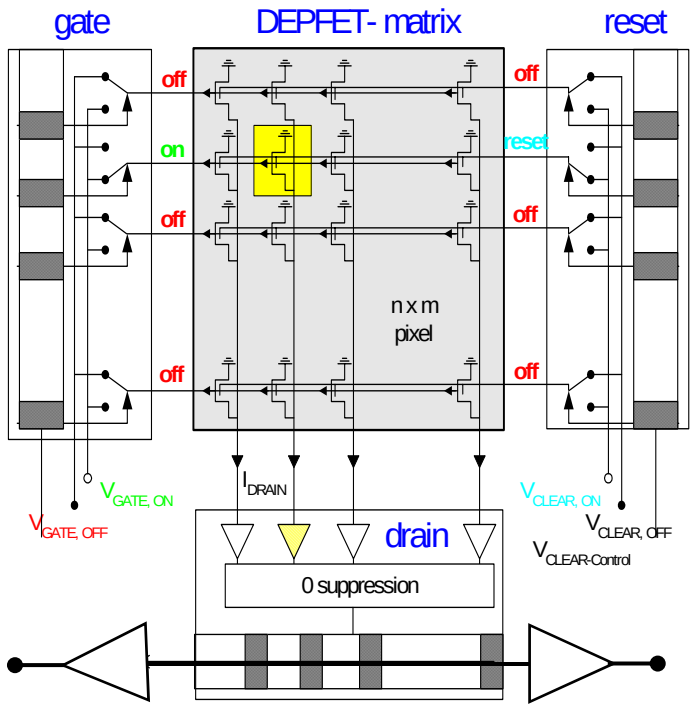
DEPFET MacroPixel
X-ray (imaging) spectroscopy
→ BepiColombo, SimbolX

- pixel size: 100s of µm

DEPFET Array - read-out at the ILC

Drain read out

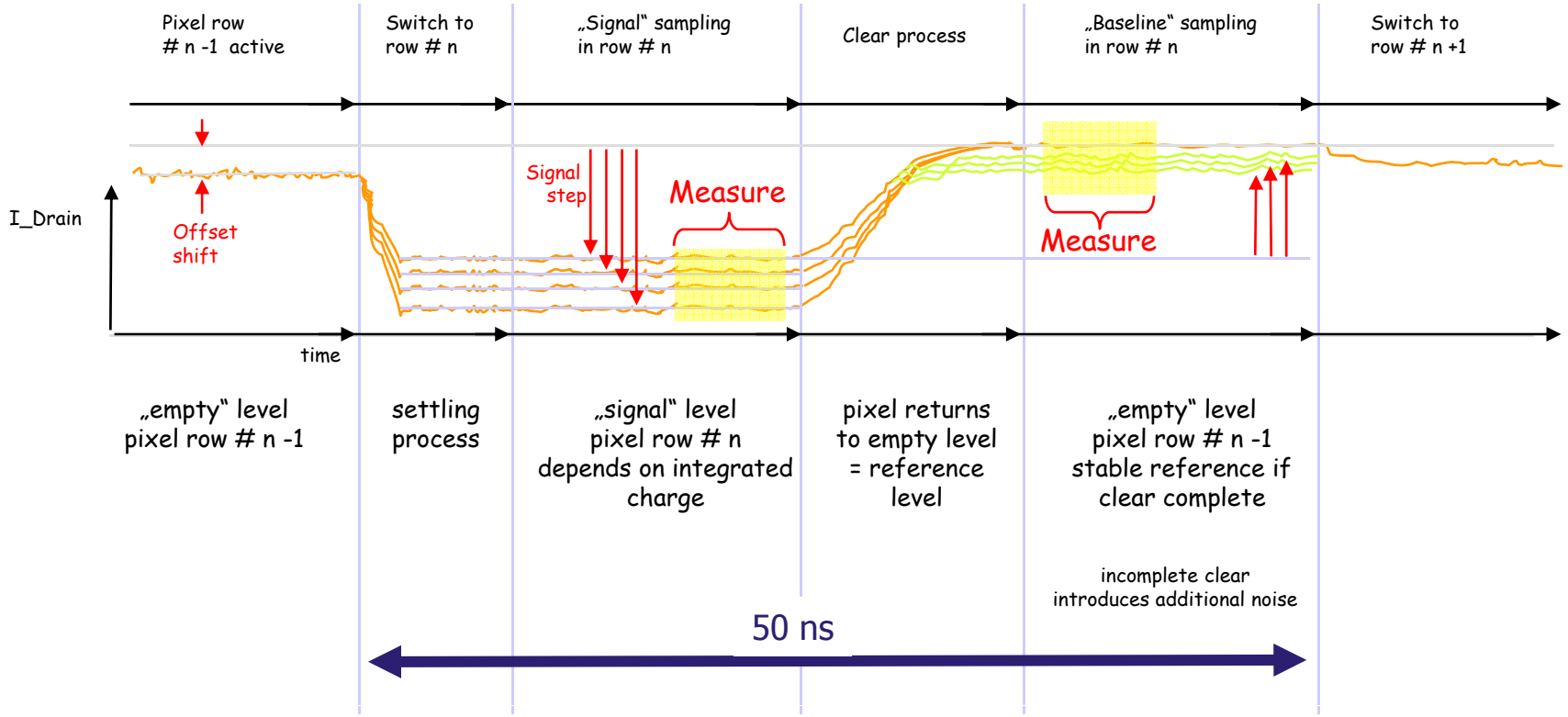




Row wise read-out ("rolling shutter")

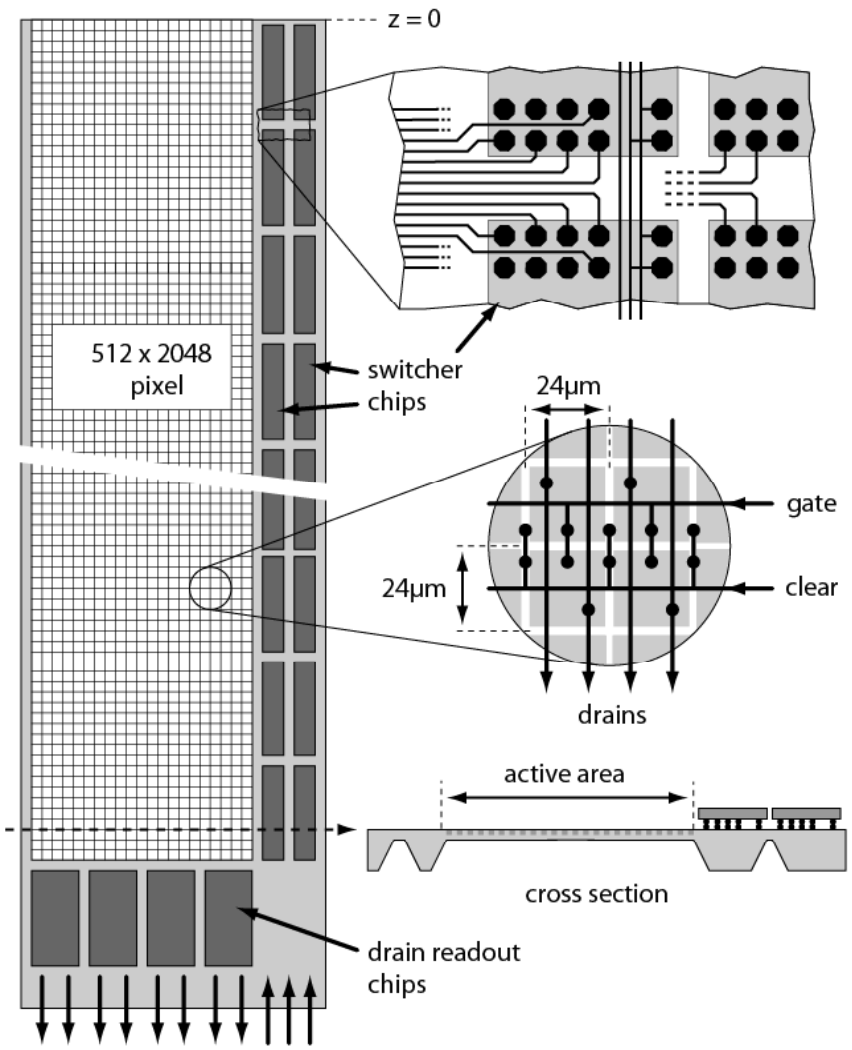
- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal
- Low power consumption
- two different auxiliary ASICs needed
- limited frame rate
- cap. load at the f/e adds noise

Row wise read-out → matrix signal



- Row wise CDS, time between the two samples ~10 ns!
- However, we need (almost..) complete clear → Hans-Günther's talk..

ILC VXD baseline design



Just as a starting point for the R&D!

- 5 layer, old TESLA layout
- 10 and 25 cm long ladders read out at the ends
- 24 micron pixel
- design goal 0.1% X_0 per layer in the sens. region

Strategy to cope with the background:

- read ~20 times per train
- store data on ladder
- transfer the data off ladder in the train pause

  → row rate of 40 MHz
- read two rows in parallel, doubles # r/o channels but:

→ row rate 20 MHz ☺

Work sharing in the collaboration

	DEPFET/Ladder Sim. and Irrad.	Auxiliary ASICs Development	System Development	System Tests and Test Beams
Aachen			X	
Bonn		X	X	X
Karlsruhe	X			
Mannheim		X	X	X
Munich	X			X
Prague			X	X
Valencia			X	X

The next 120 minutes

- Hans-Guenther: DEPFET Design and Test, Radiation Tolerance, Ladder Concept
- Ivan: ASICs: Steering and f/e ASIC
- Carlos: Test of the Prototype System
- Ariane: ILC VXD Simulation

Summary and Future Plans