DEPFET Electronics

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Gate / Clear steering chips: SWITCHER

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- SWITCHER3
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  - HV Switch & Level Shifter
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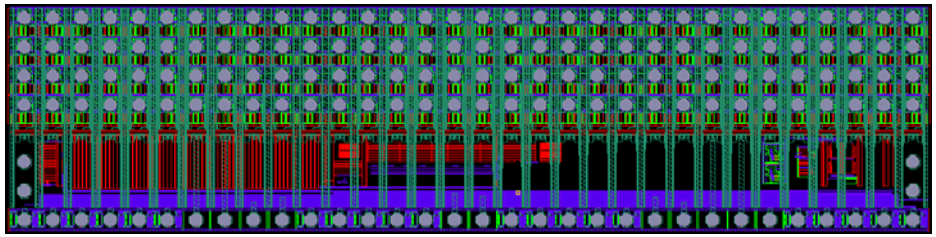
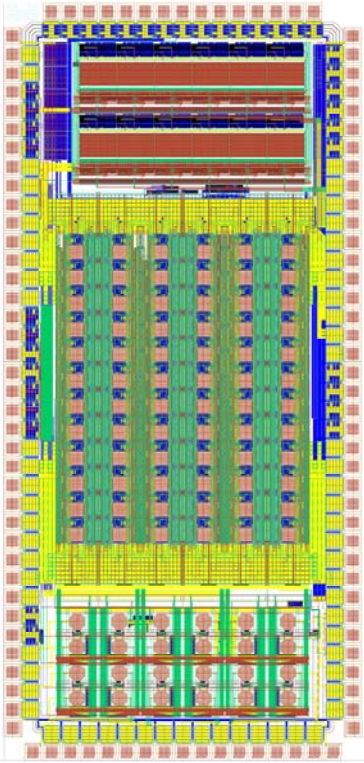
Drain Readout Chips

- Requirements
- CURO reminder
- DCD
  - Architecture
  - Noise, Speed, Power

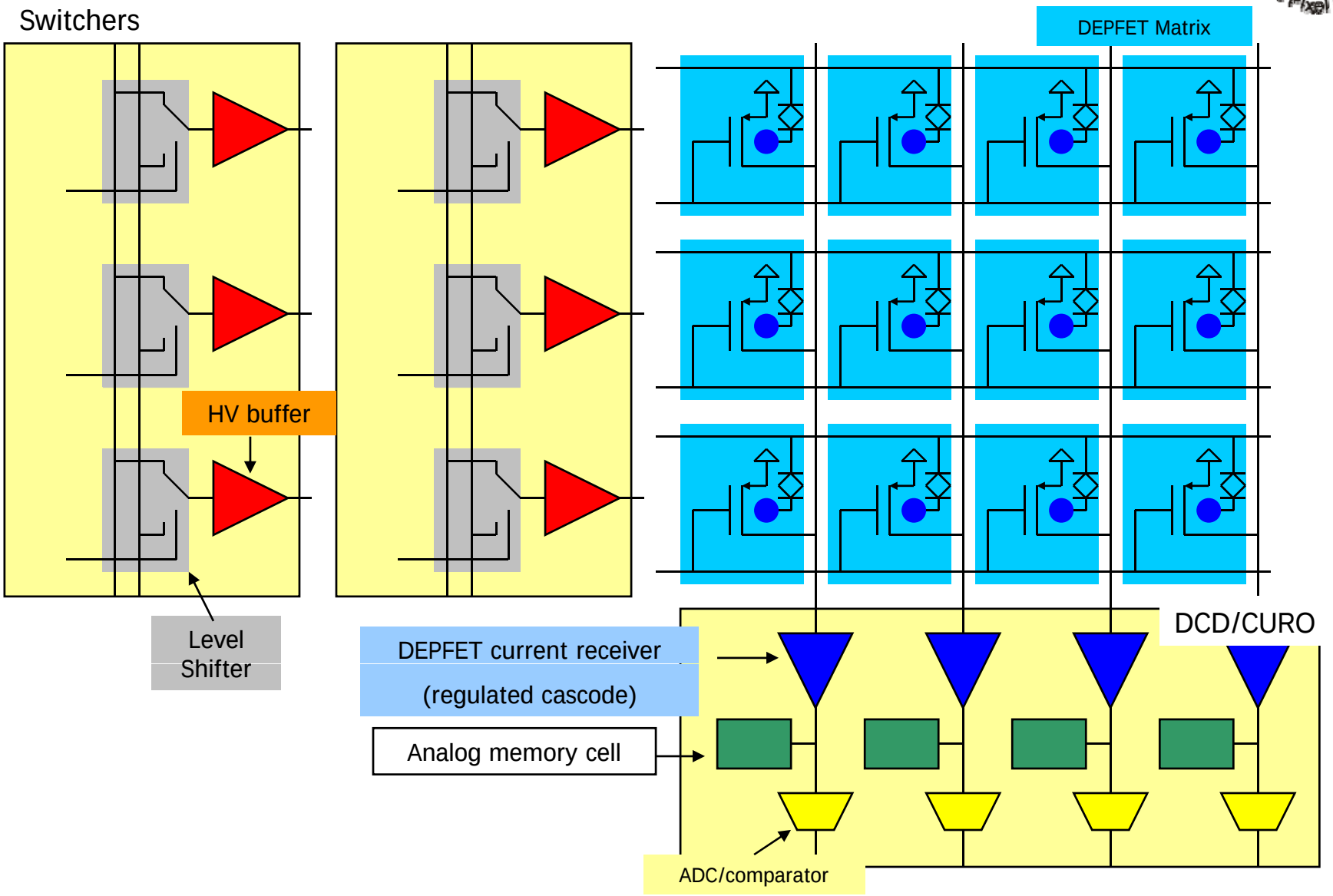


Switcher

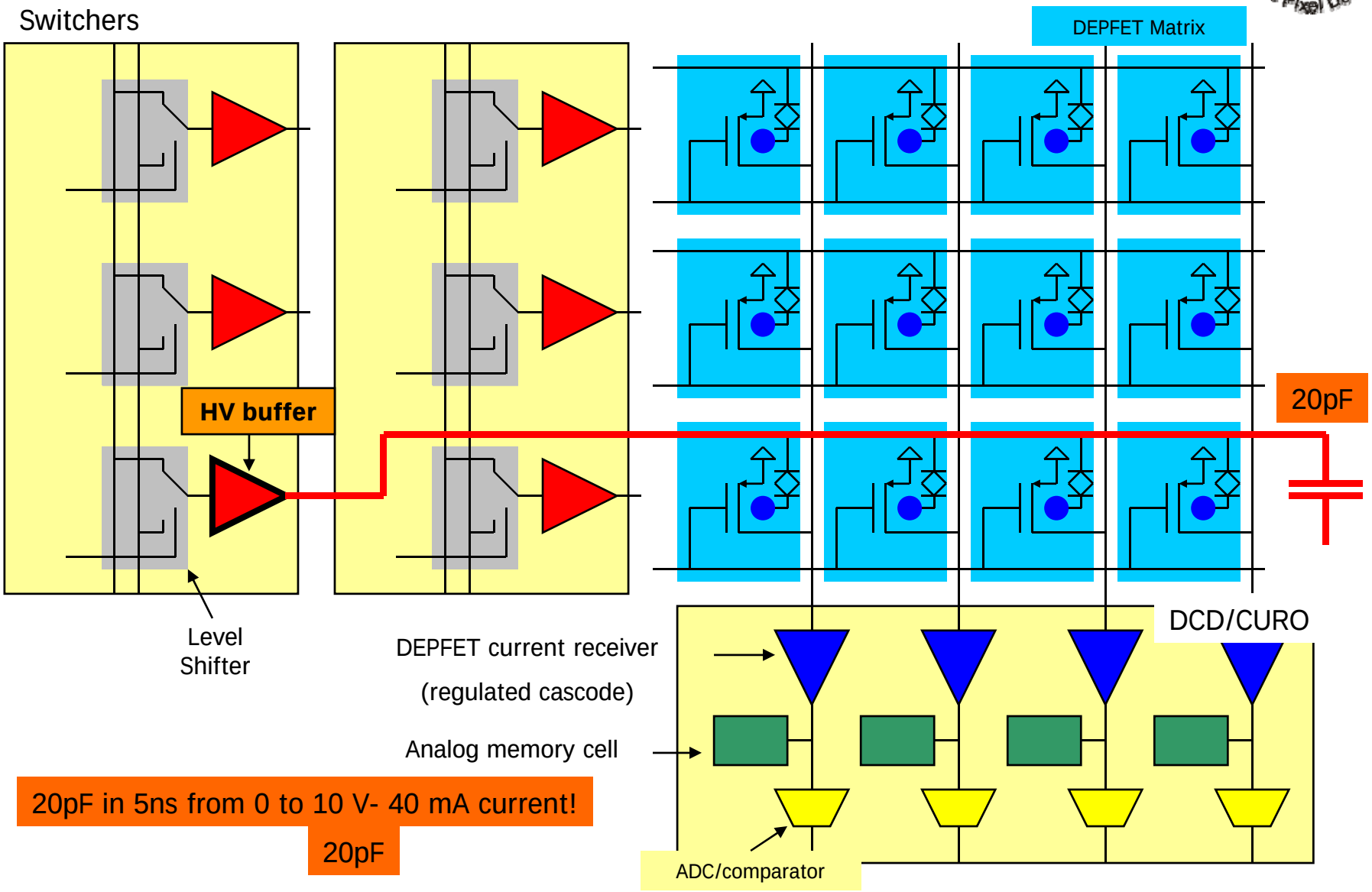


DCD

Readout Chips – Critical Parts



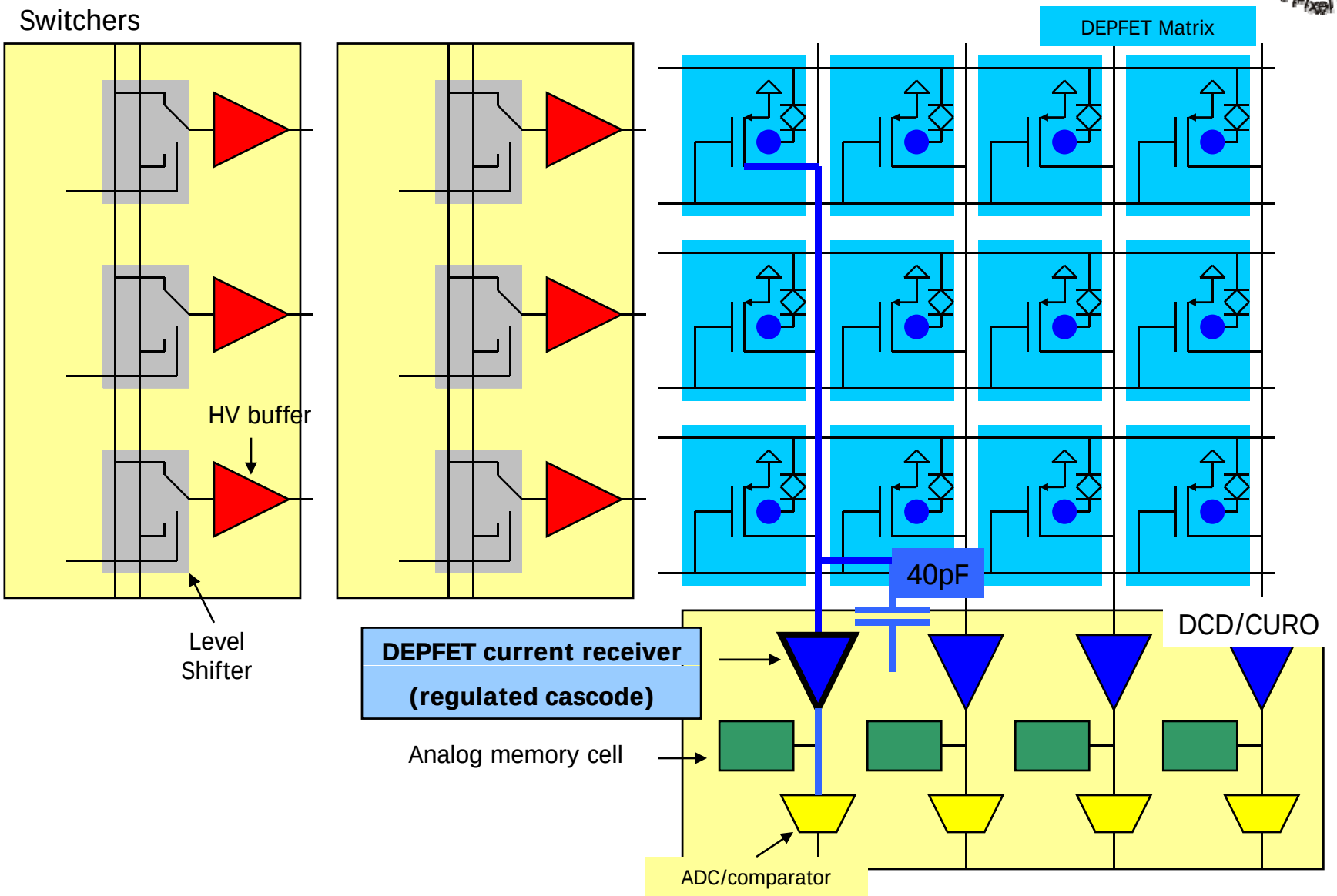
Readout Chips – Critical Parts



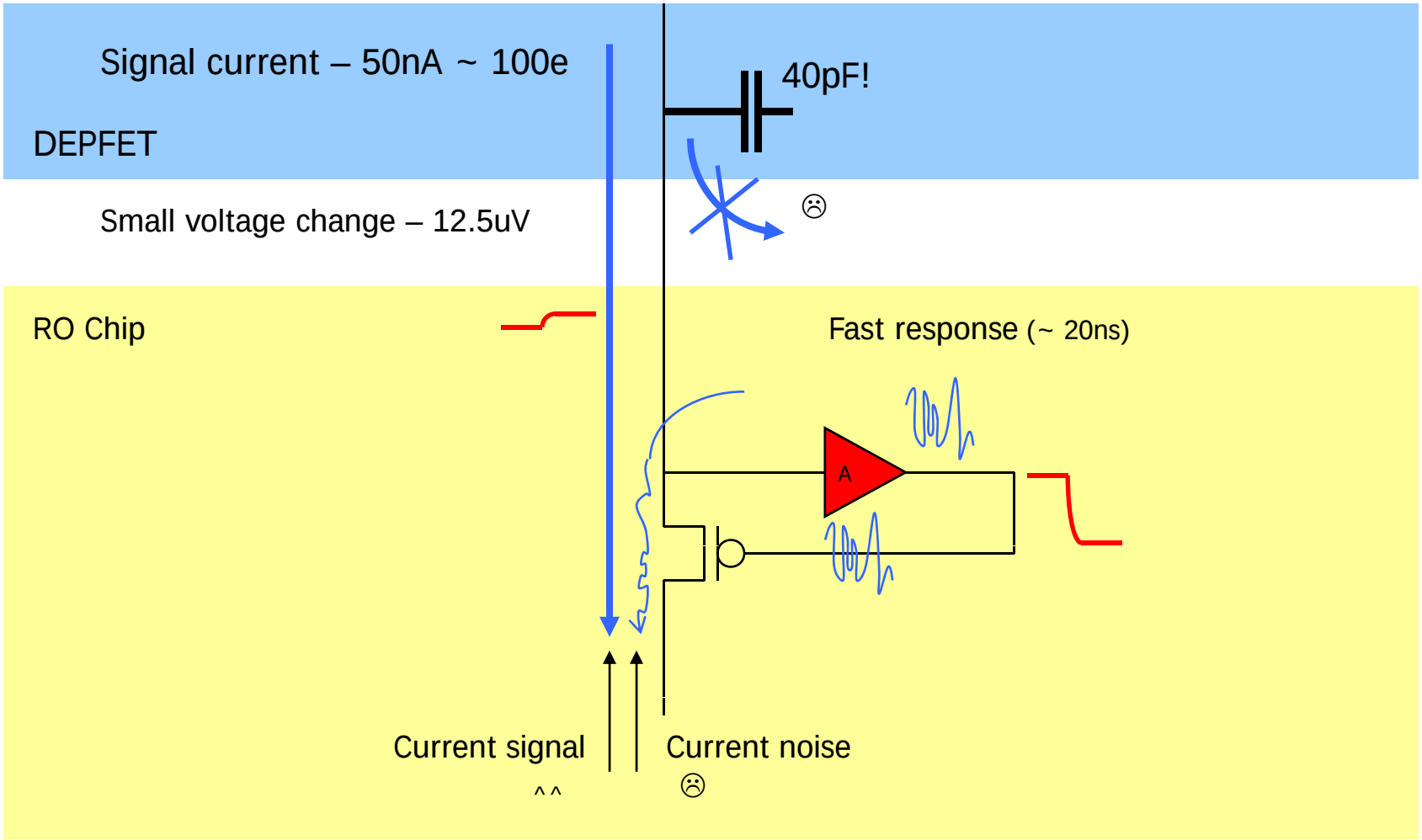
20pF in 5ns from 0 to 10 V- 40 mA current!

20pF

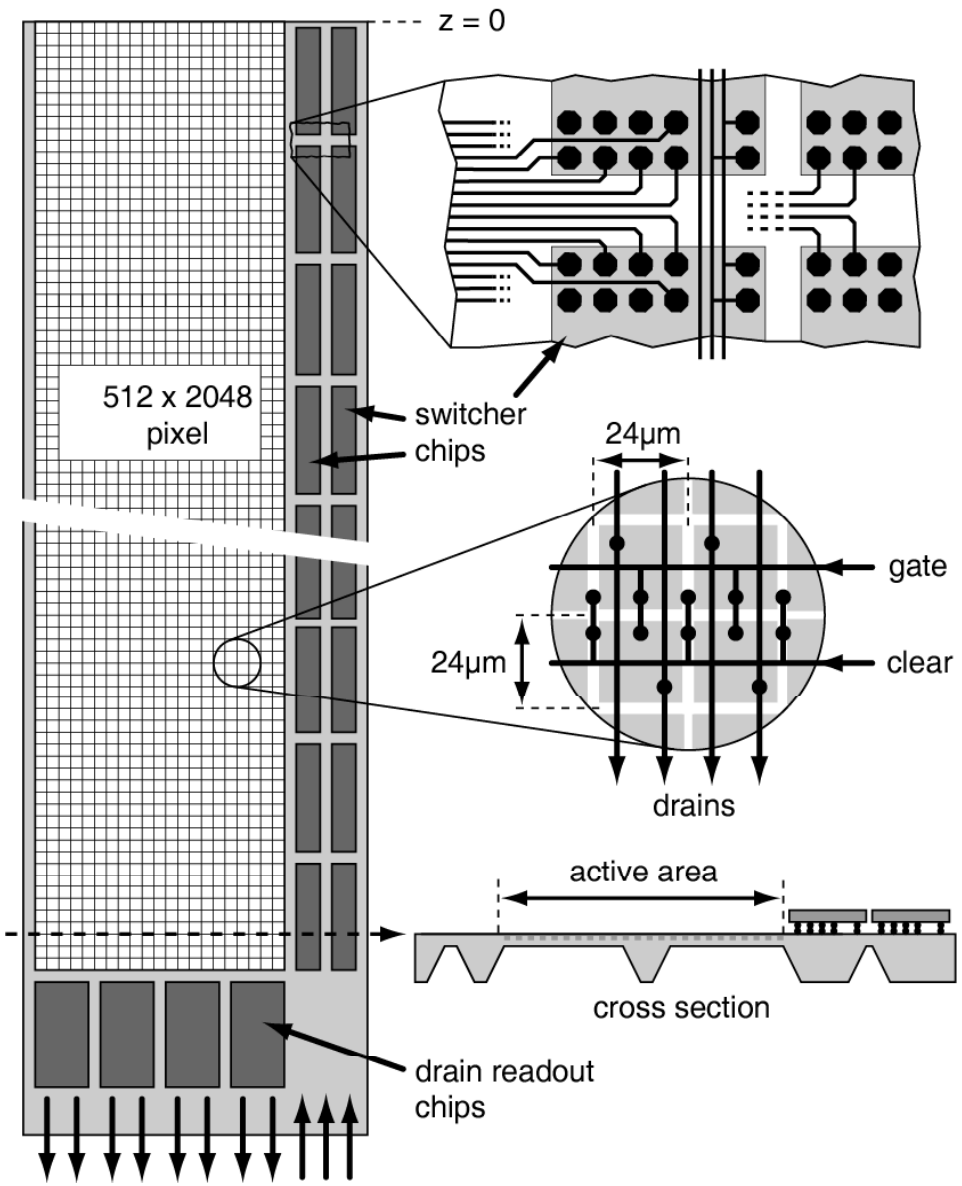
Readout Chips – Critical Parts



Regulated Cascode



Module


z = 0
512 x 2048
pixel
switcher
chips
24µm
gate
clear
24µm
drains
active area
cross section
drain readout
chips

SWITCHER: REQUIREMENTS

SWITCHER Requirements

Small and thin
(minimum material)

Small Power dissipation
(no massive cooling in the inner region)

Switch voltages of up to ~10V
(7V required for clear)

Rise/fall times of <10ns for a load of 20pF.

Radiation tolerance to some 100krad

Bump bonding pads

Minimal number of IO signals
(These must be routed along the narrow balcony)

Programmable switching pattern
(Skip broken rows, read region with high occupancy more frequently)

Many chips must be operated in parallel with no overhead

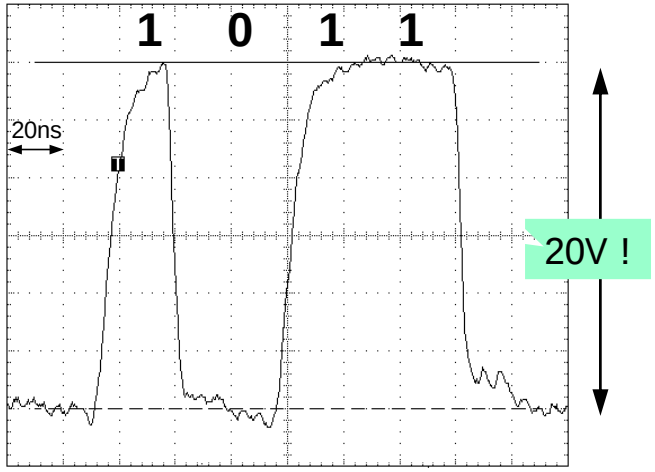
SWITCHER 2

Switcher 2

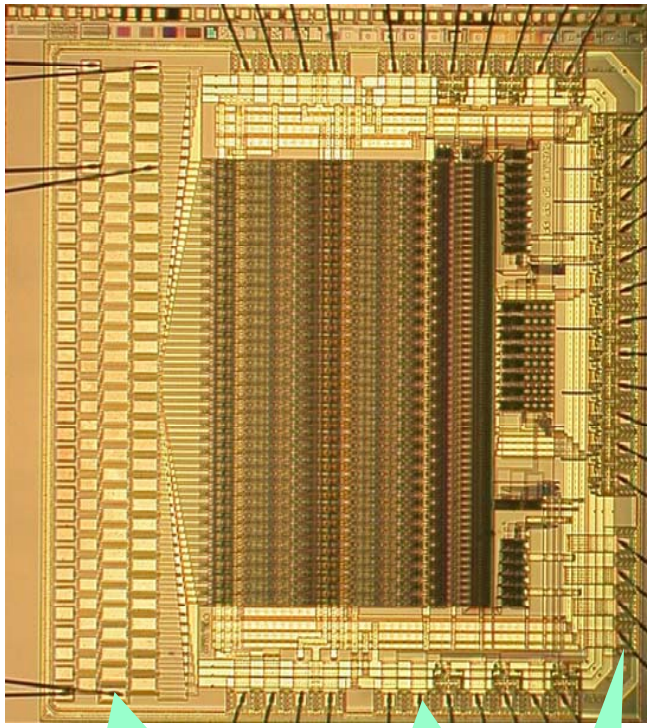
64 channels with **2 analog output**
Can switch up to **25 V**
used **very successfully** for **all existing matrix setups**

digital control ground + supply floating
fast internal sequencer (up to 80MHz)
Daisy chaining of several chips (token out)

0.8µm AMS *HV* technology – **bad radiation tolerance**!
Power dissipation: **1mW / channel @ 30MHz** (level shifter)



Switching 20V @ 30MHz



2 x 64 outputs with spare pads

Pads for daisy chain

control inputs

SWITCHER 3

Switcher3 Requirements / Features

10V switching low voltage 3.3V transistors

needs twin-well technology (AMS h35b4)

capacitive coupling of digital and analog blocks

radiation hard design

~ 20pF gate/clear capacitance

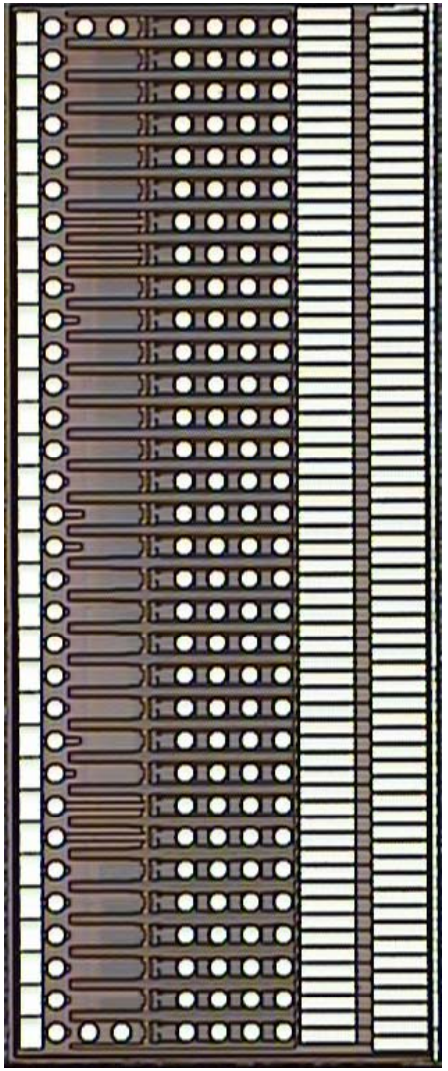
fast signal edges: ~ 5 ns fall time

128 channels

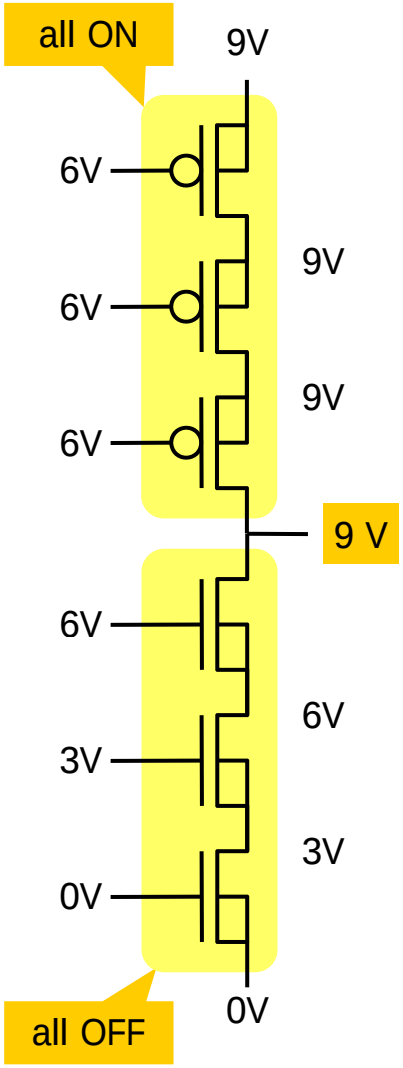
Sequencer with non trivial **switching sequences**

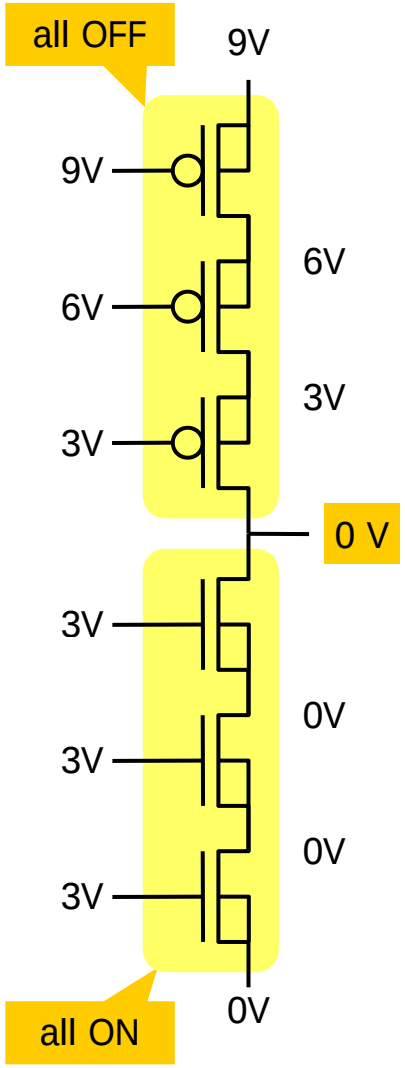
Low power

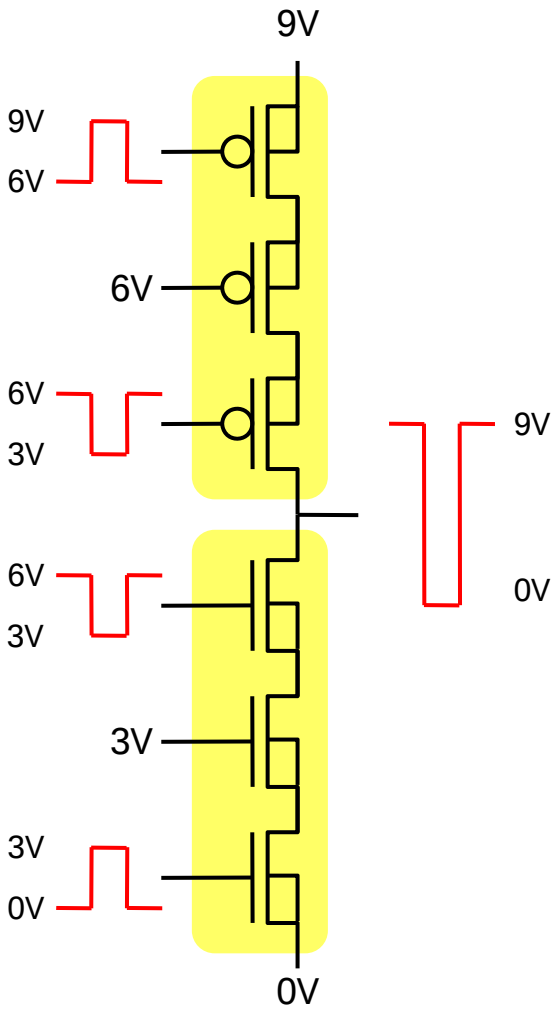
bump pitch of **180 µm, allows pixel sizes down to 24 µm**



HV Switch with Stacked Transistors (assume 3V per stage)



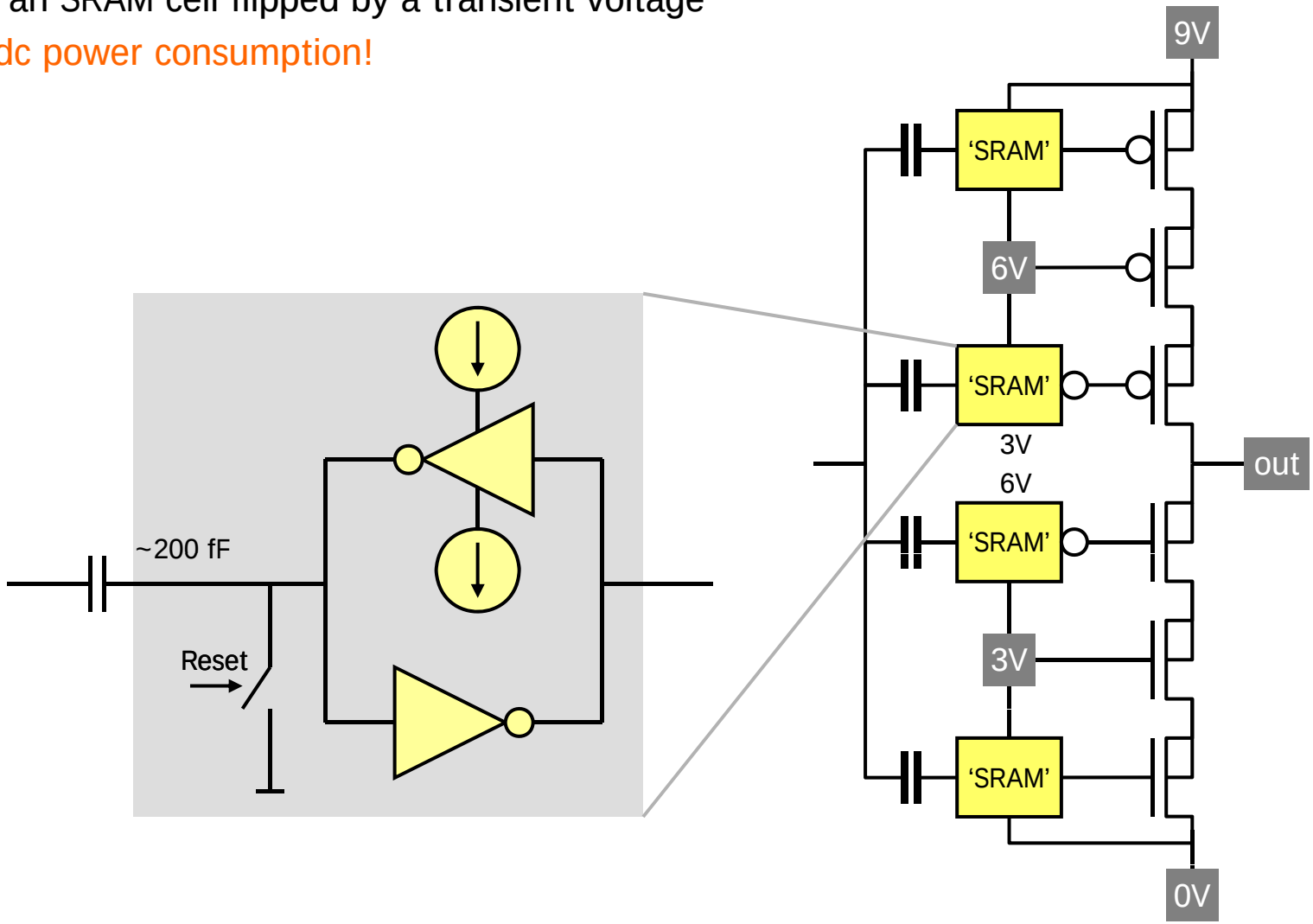




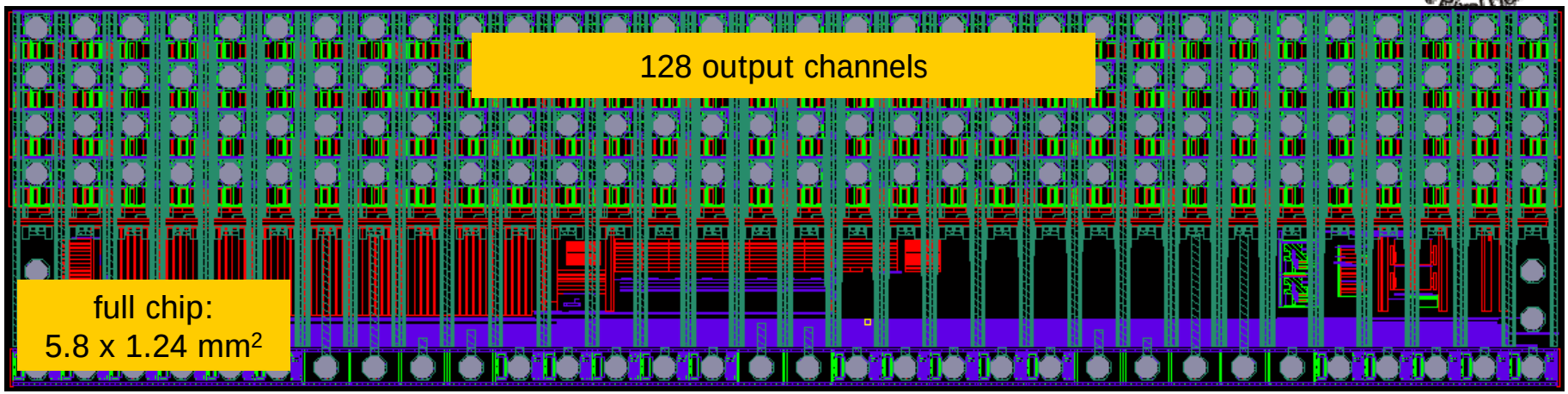
Level shifting by AC coupling – no DC current

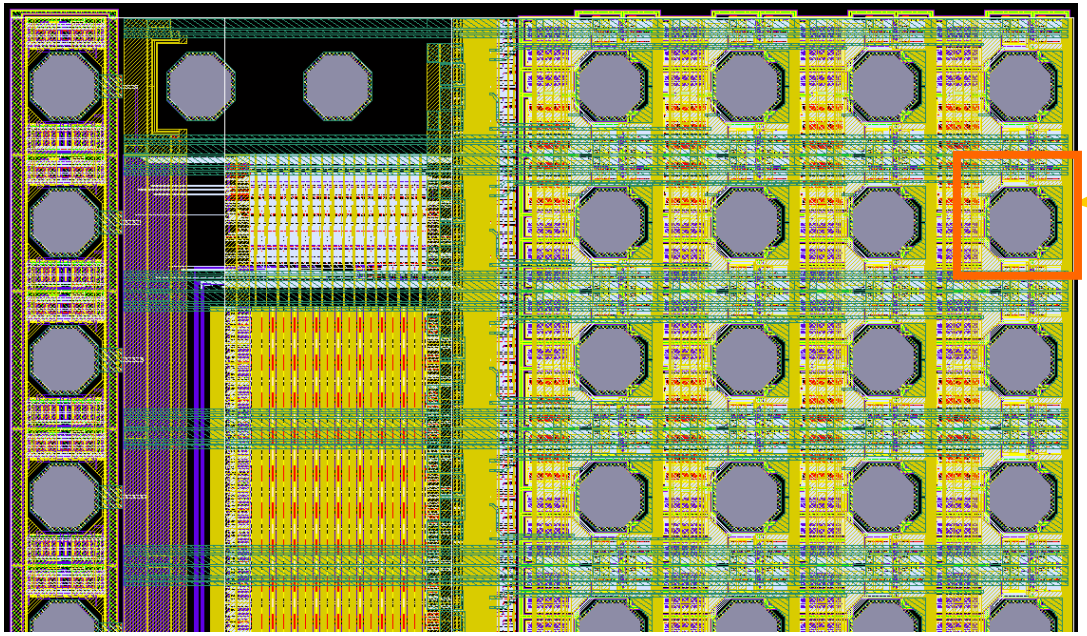
Use an SRAM cell flipped by a transient voltage

No dc power consumption!



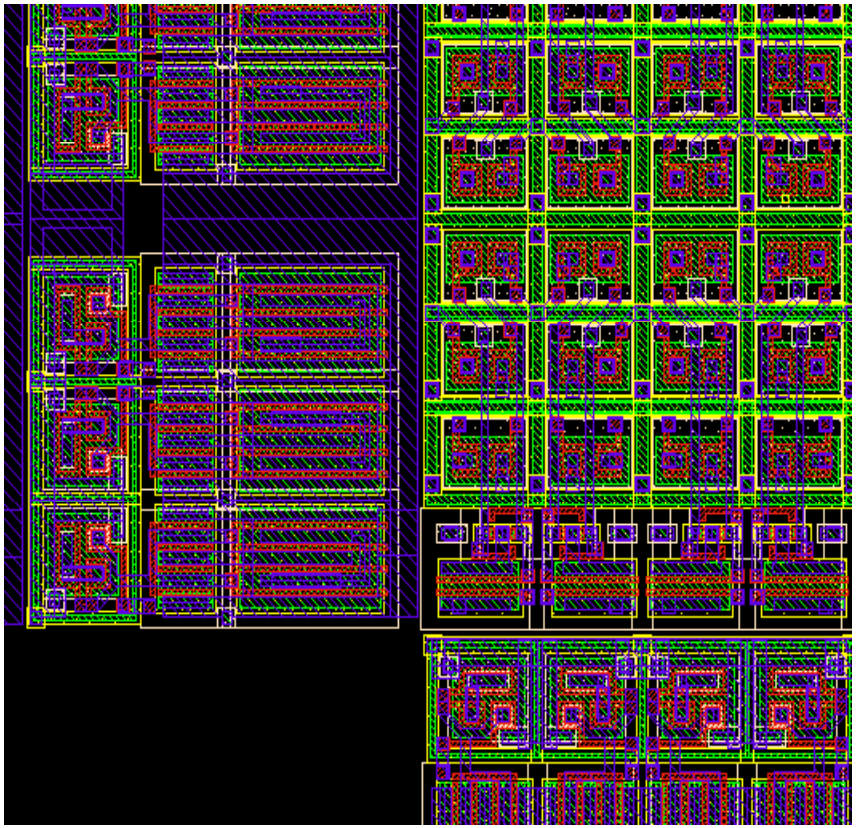
Switcher 3 Layout

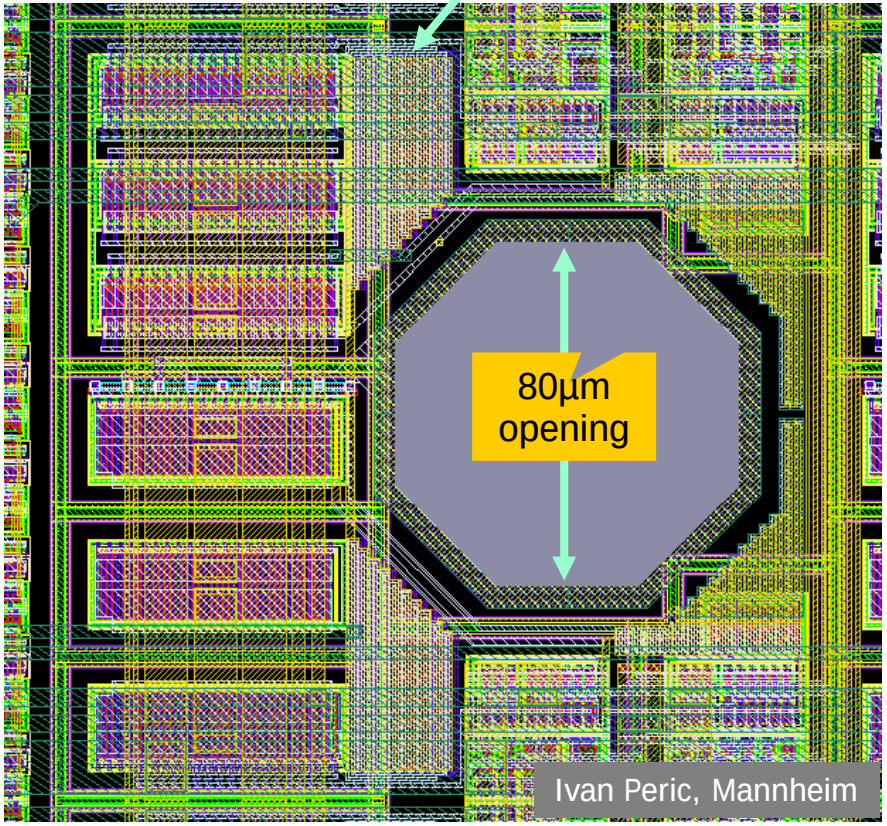




Switcher 3 Layout Details

interdigitated
AC coupling caps

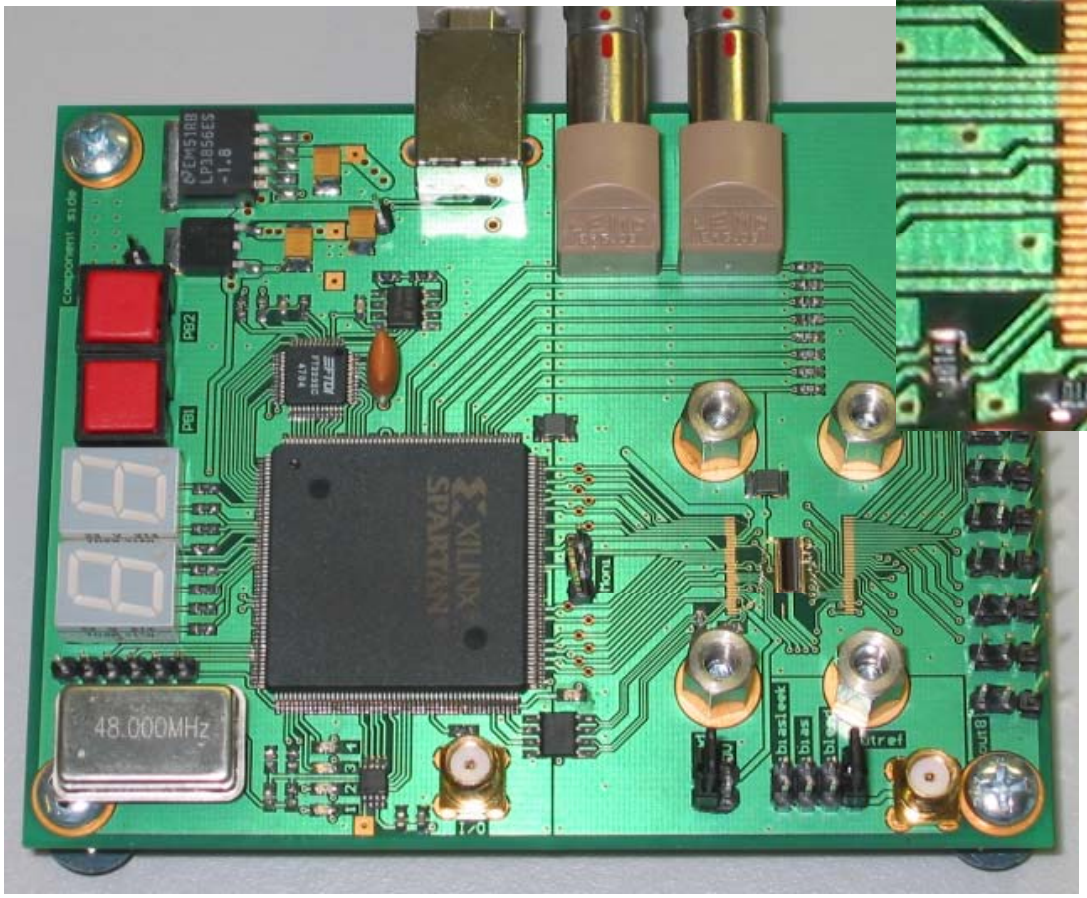


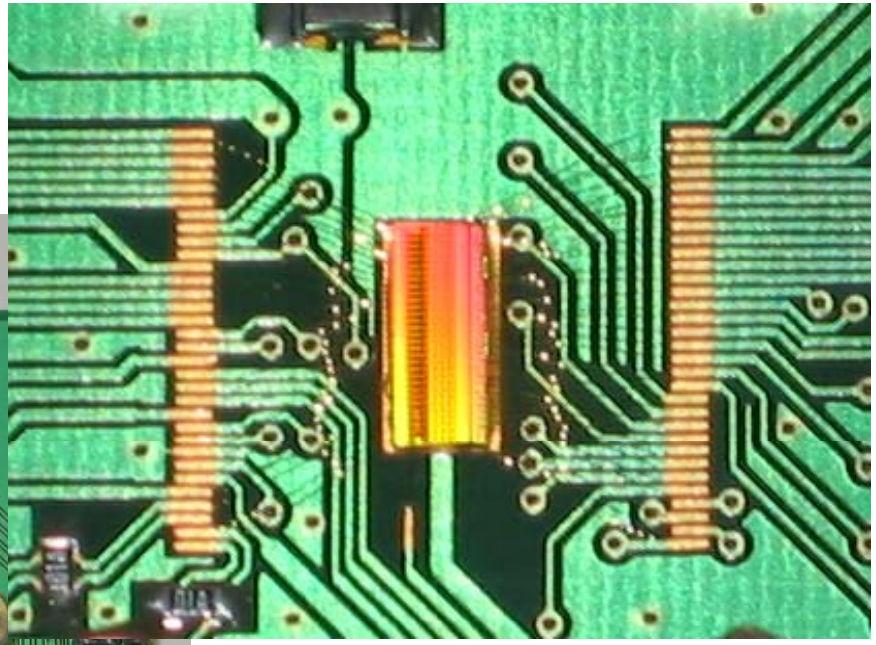


Sequencer RAM, row buffers, readout
(M2-M4 not shown)

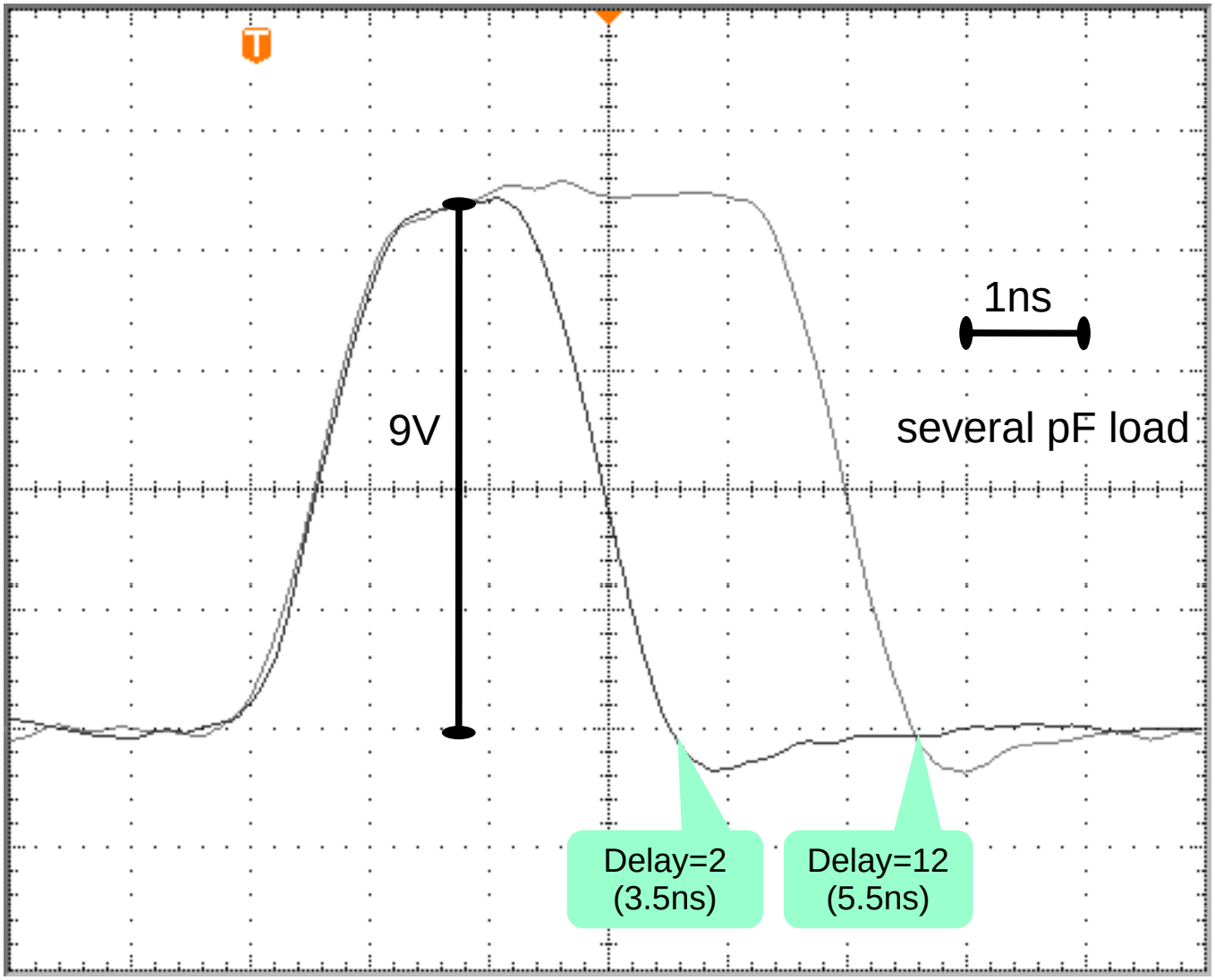
HV channel with 3+3 Switch transistors and
4 AC coupling stages (180x180µm, M4 not shown)

Measurements

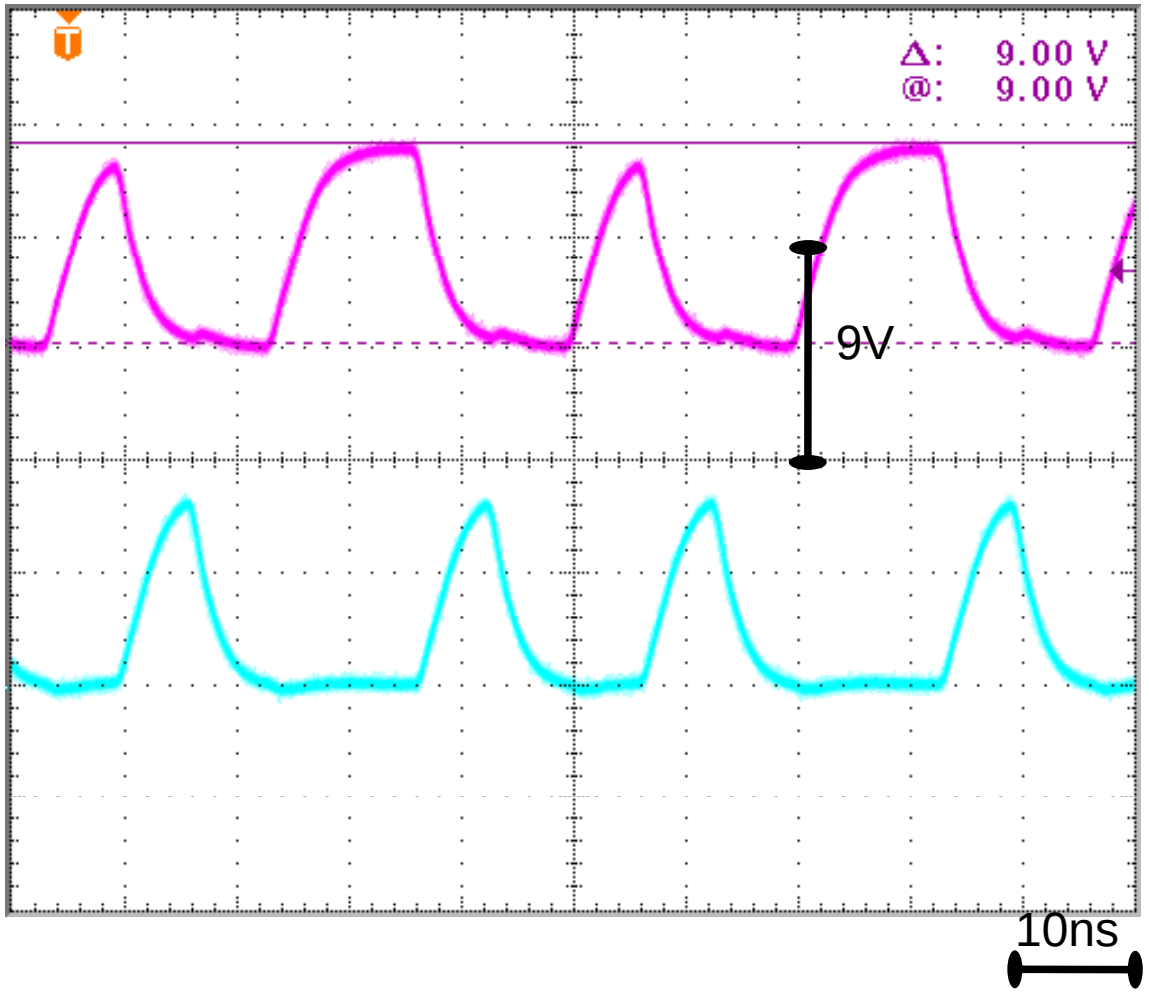




Short Pulses: Internal Strobe Generator



Sequencer - Maximum Speed with C_{load} ~ 25pF



SWITCHER3 Power Dissipation Summary

Consumption for 20pF, clocked at 20MHz, supplied with 3V (digital) and 9V(analog):

Active Chip:

- ~ 18mW (digital)
- ~ 45mW (analog)

Idle Chip:

- ~ 18mW (digital)
- **~ 0 (analog)**

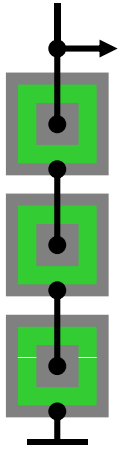
Sleeping chip (later, will use ‘hibernation’ mode to disable majority of digital part):

- < 5mW (digital)
- ~ 0 (analog)

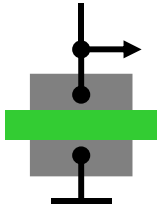
Irradiation of SWITCHER3 Rest Chip

X-ray irradiation up to ~600 krad

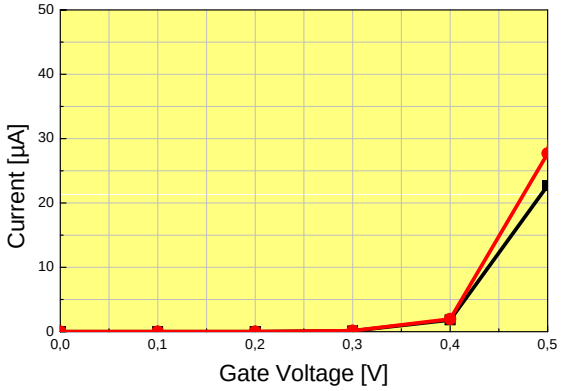
No (significant) threshold shift or leakage current for annular structures

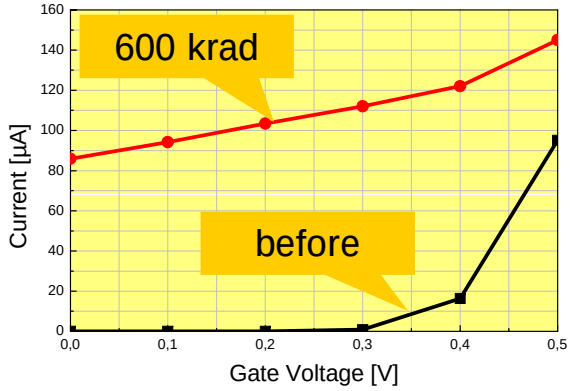


stacked 'normal' annular NMOS



'HV' NMOS, normal layout





SWITCHER3 Summary

all parts of chip are working

150MHz max speed

45mW analog for 20pF load @20MHz (for the single active chip)

18mW digital @20MHz

8ns settling time from 0V to 9V on rising edge

6.5ns settling time from 9V to 0V on falling edge

Programmable Sequencer which allows complicated readout sequences (200MHz)

Next Steps

- irradiation of full chip
- continue long term stress test (no failures after 6 weeks)
- operation with DEPFET matrices

Drain Readout: REQUIREMENTS

Requirements for Drain Readout Chips

Basic Architecture

Cascode circuit to sense the tiny drain current.

The noise contribution of this cascode must be minimized.

Bus capacitance ~ 40pF

Current subtraction

(signal / pedestal) Analog memory cells

Process the difference signal

Accommodate a drain **pitch of 12µm**

We address this by using bump bonding in DCD.

(double) row rate: **~ 20MHz**. (This corresponds to 40MHz pixel row rate.)

Noise charge**: < 200 electrons**

Power: as low as possible while still reaching speed and noise requirements…

Radiation tolerance: to some 100krad

Process I_{ped} ~ 30µA, I_{sig} ~ 6µA (i.e. 12000 Electrons at g_q=0.5nA/e)

CURO

CURO Drain Current Readout Chip

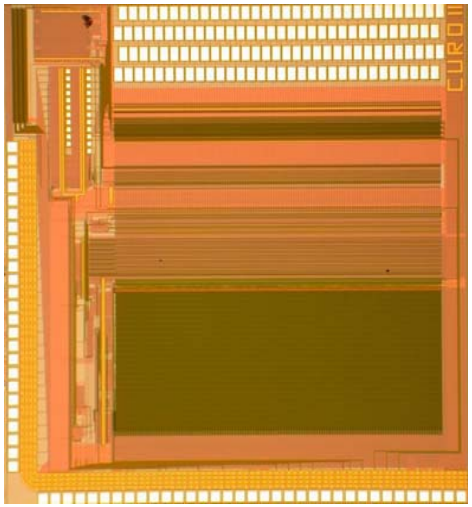
0.25µm TSMC, mostly enclosed transistors

Current **comparator** finds hits

Current Difference and hit-flag stored in **mixed FIFO**

Fast Hit-Finder scans FIFO for up to 2 hits per cycle:

- **analog currents** to outA, outB
- digital hit position stored in HIT-RAM



128 channels

Drawbacks:

Regulated cascode is too weak

Difficult shielding due to technology limitations – cross-talk

DCD

DCD features

UMC 0.18µm 1.8V technology

Similar FE part like CURO

one >= 7bit ADC per channel

- In reality, two independent ADCs work in parallel
- They are implemented as algorithmic ADCs
- 144X2 ADCs on final chip

Digital zero suppression – can be implemented in FPGA

massive parallel high speed digital output @600MHz, 18 LVDS outputs

Bump bonding with pixel logic & ADC placed around pad

Radiation Hard Design (in analog part)

NMOS in triple Well, guard ring around analog part

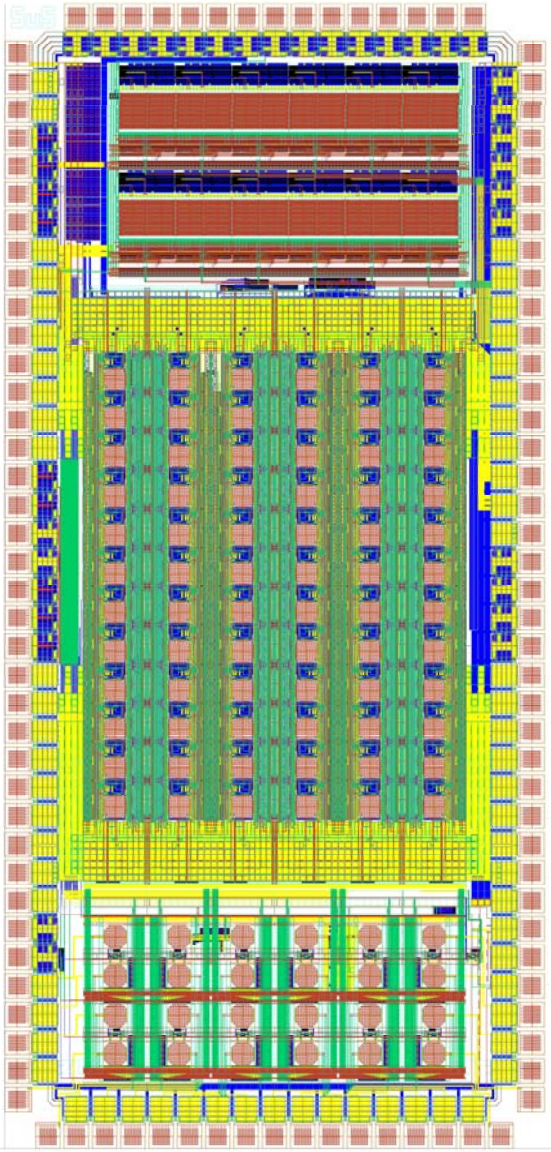
Expected power dissipation **~ 4.2 mW** per column.

Test Chip DCD

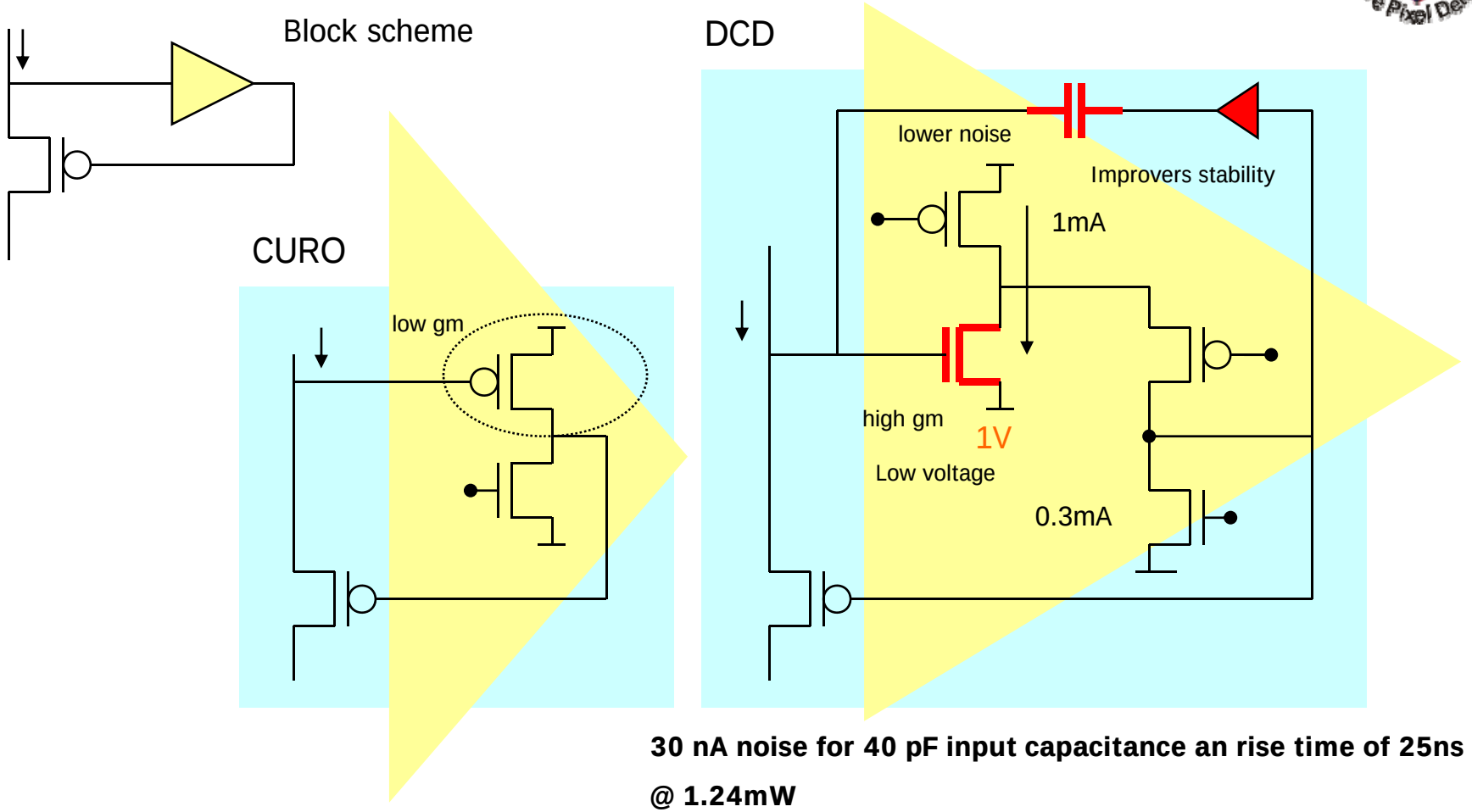
Pixels are 110x180 µm2

Input Matrix only 6 x 12 for now

but can be easily extended to full size 8 x 18

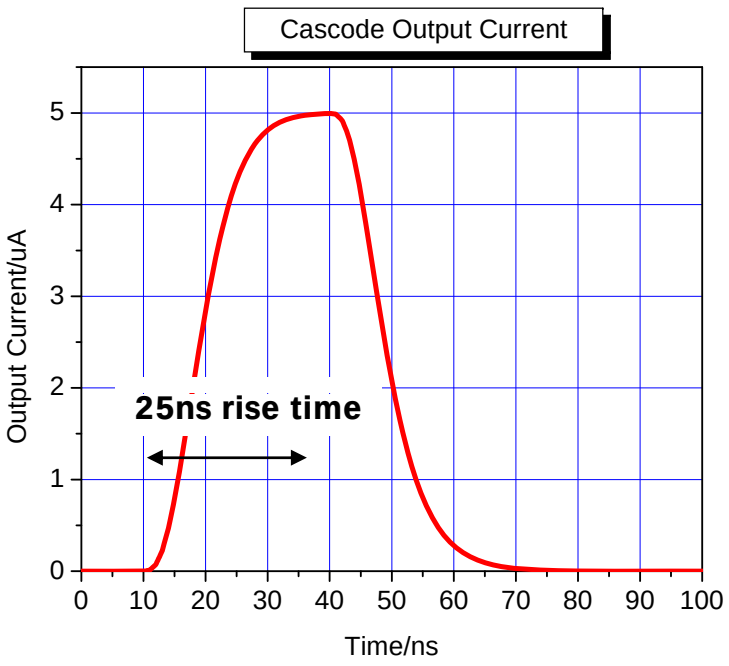


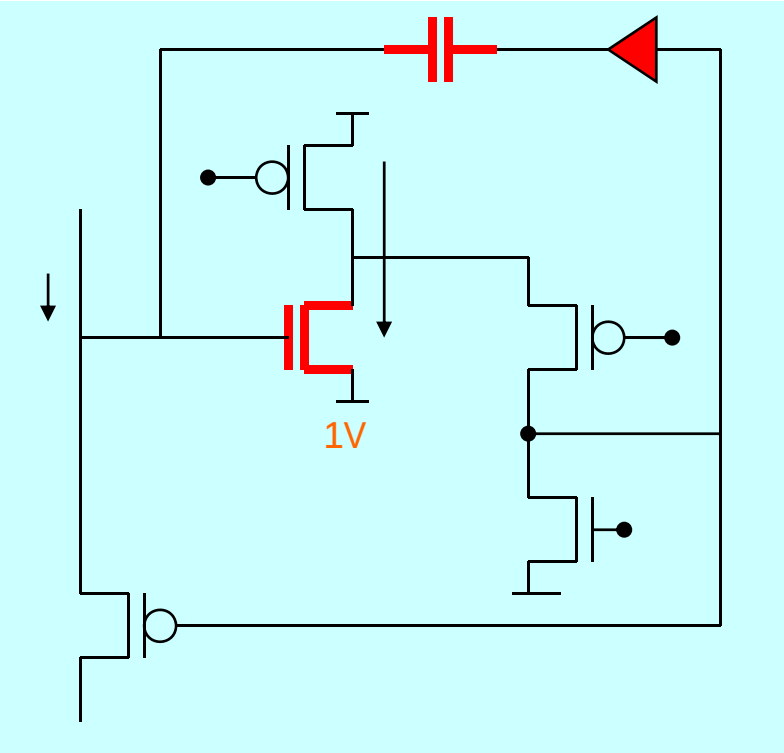
Regulated Cascode: CURO vs. DCD



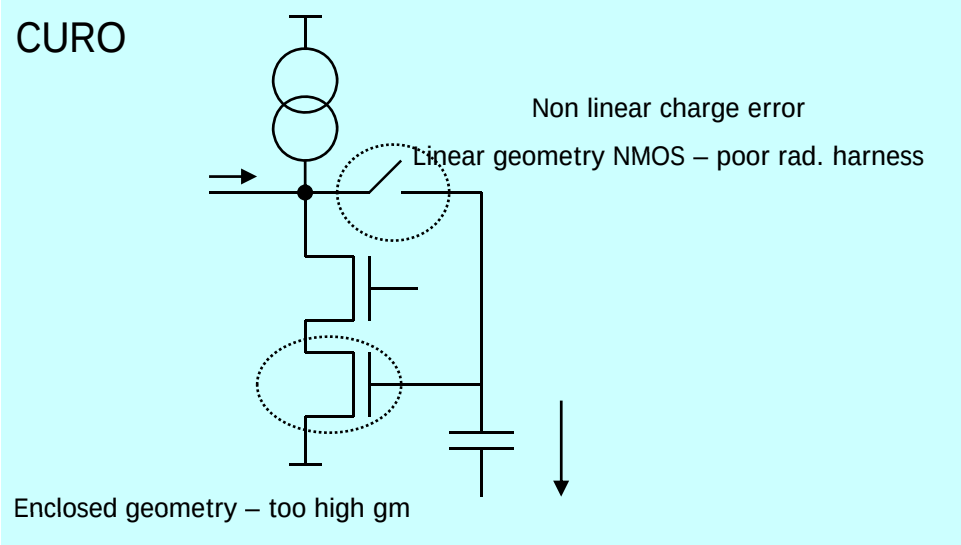
30 nA noise for 40 pF input capacitance an rise time of 25ns @ 1.24mW

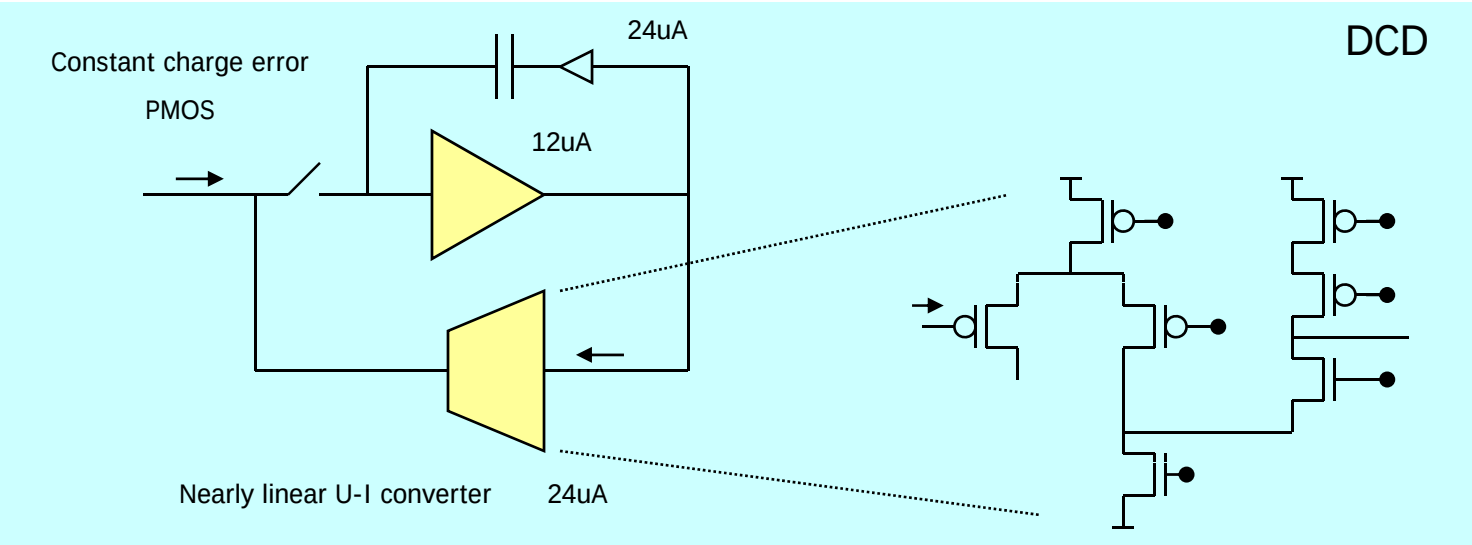
Regulated Cascode



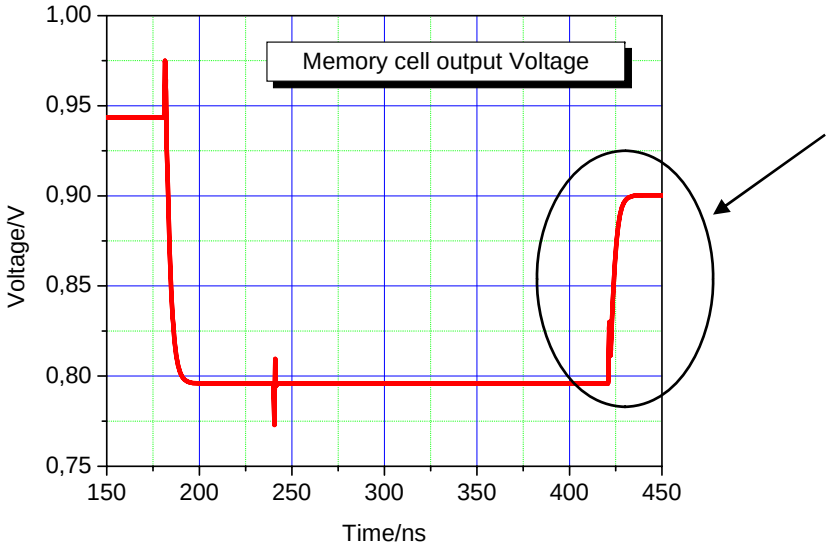


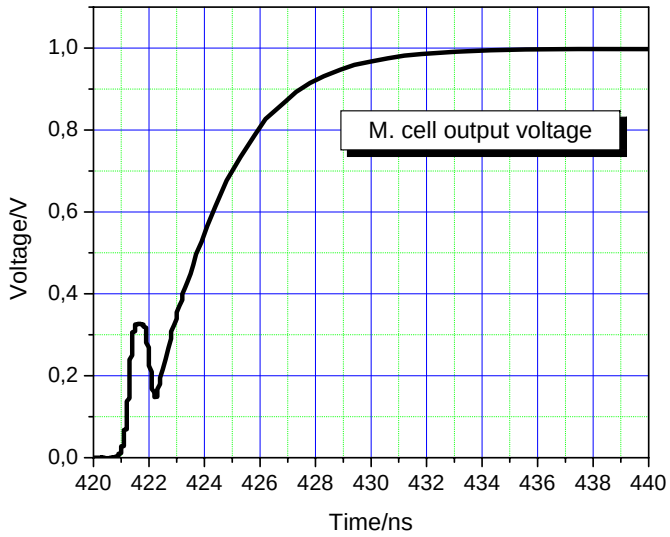
Current-Memory cell CURO vs. DCD





Novel Current Memory Cell

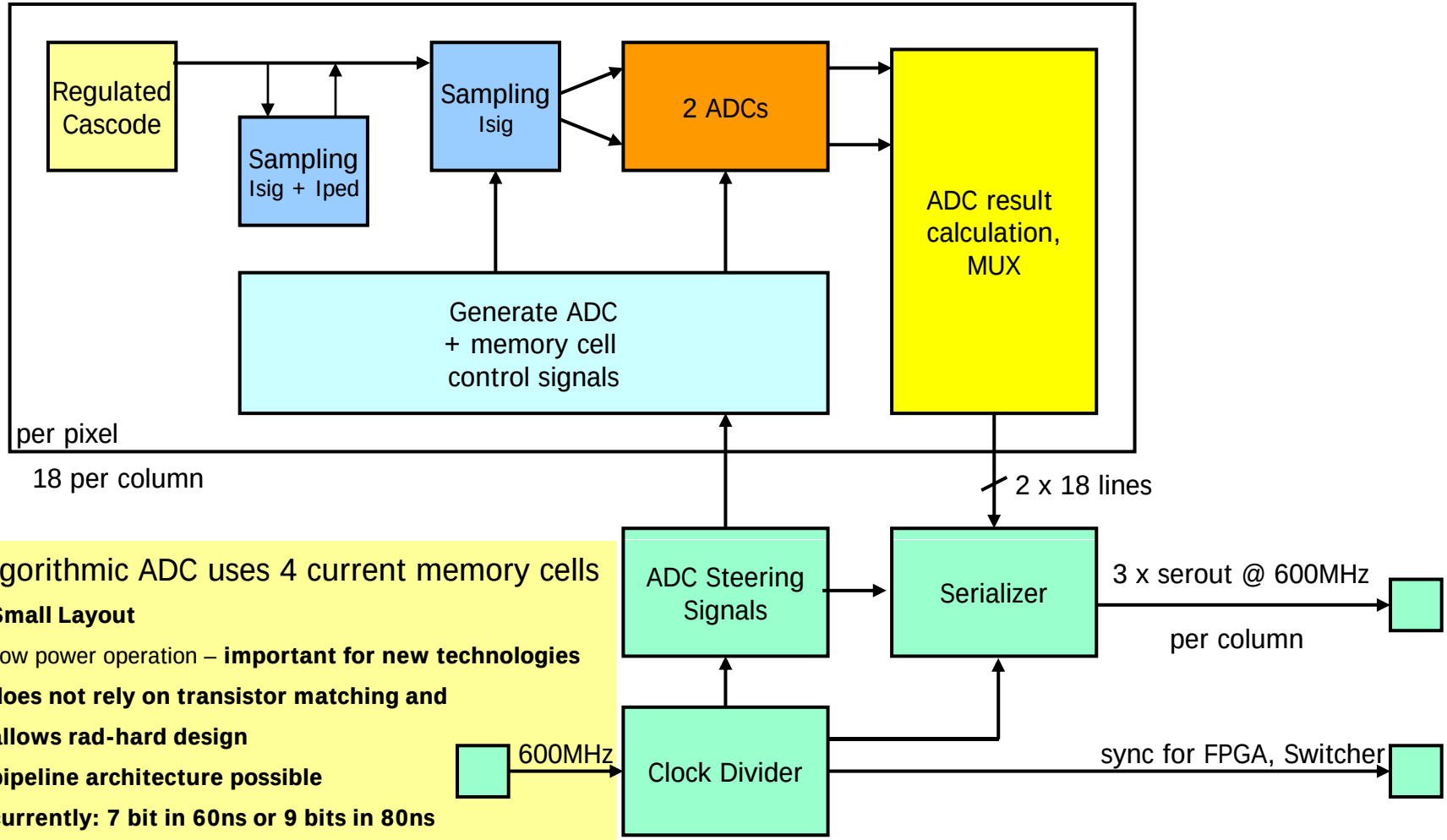




10 ns rise time

60 nA noise

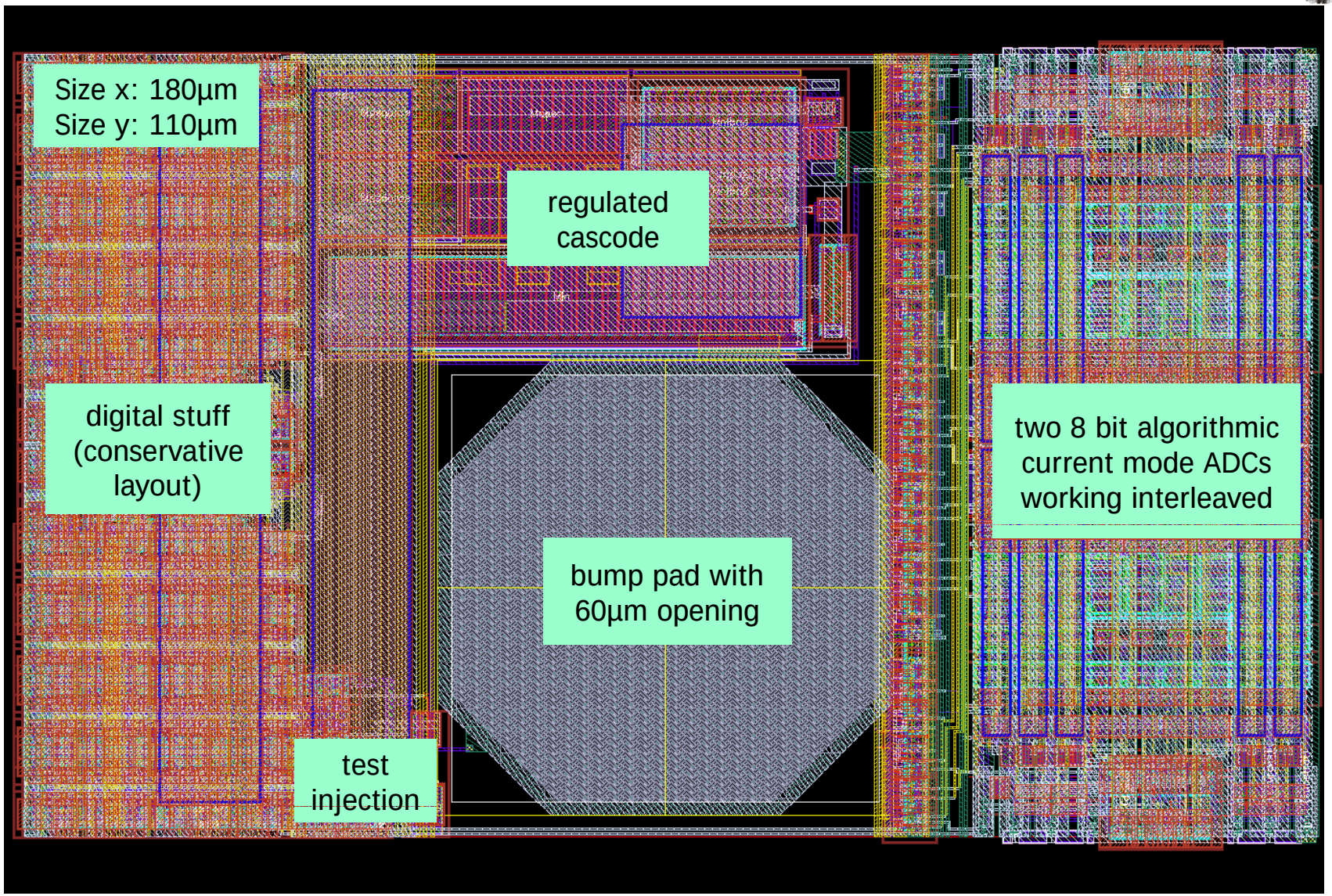
DCD Channel



Algorithmic ADC uses 4 current memory cells

- **Small Layout**
- Low power operation – **important for new technologies**
- **does not rely on transistor matching and**
- **allows rad-hard design**
- **pipeline architecture possible**
- **currently: 7 bit in 60ns or 9 bits in 80ns**
- **2mW/channel**
- **110 microns X 50 microns**

DCD Pixel Layout



DCD Summary

Test Chip has been submitted

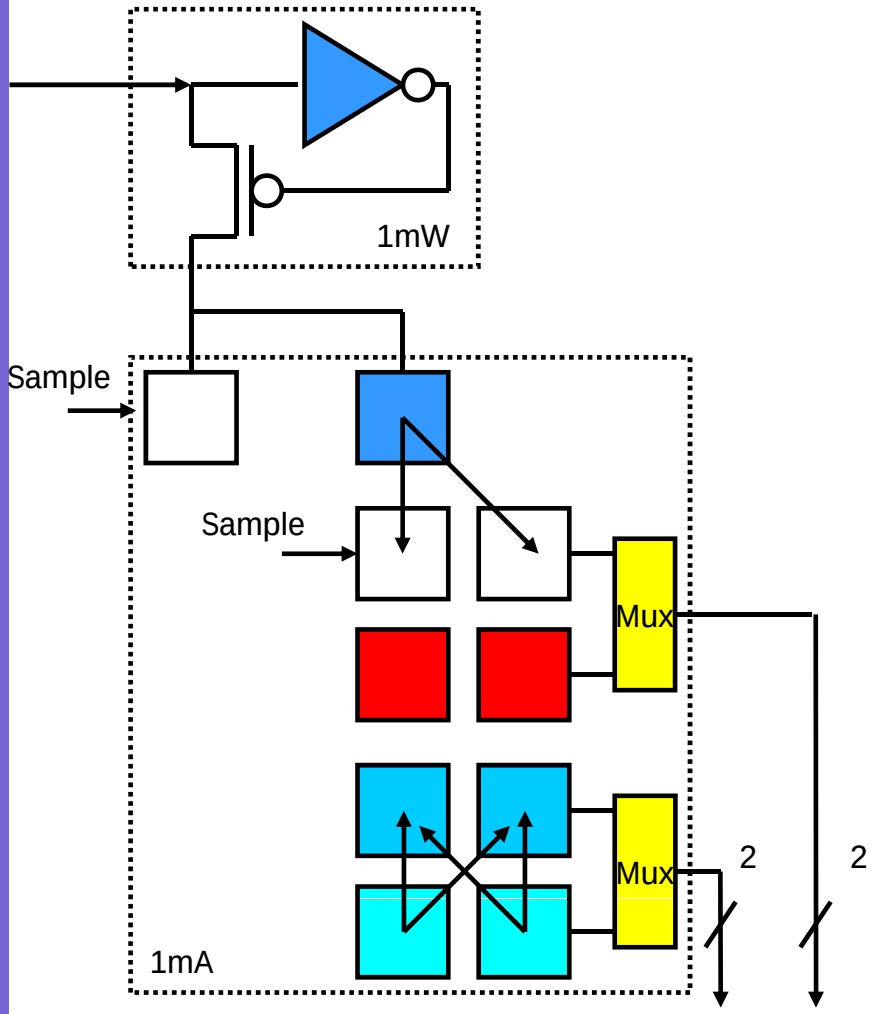
We expect 80 ns drain readout with 40pF, 9-bit ADC accuracy bin size 30 nA, noise ~ 60nA

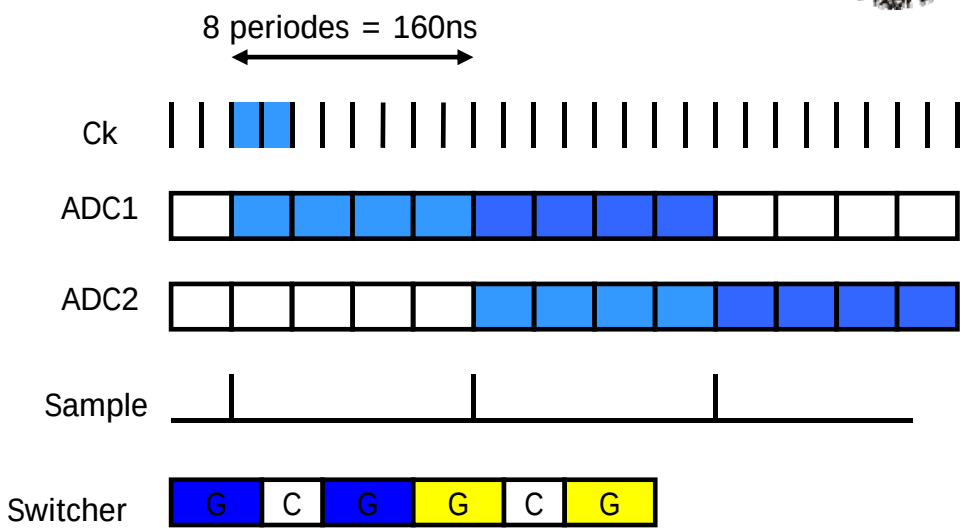
Or 60ns drain readout speed with 40pF, 7-bit bin size 120 nA

Expected power dissipation **~ 4.2 mW** per column

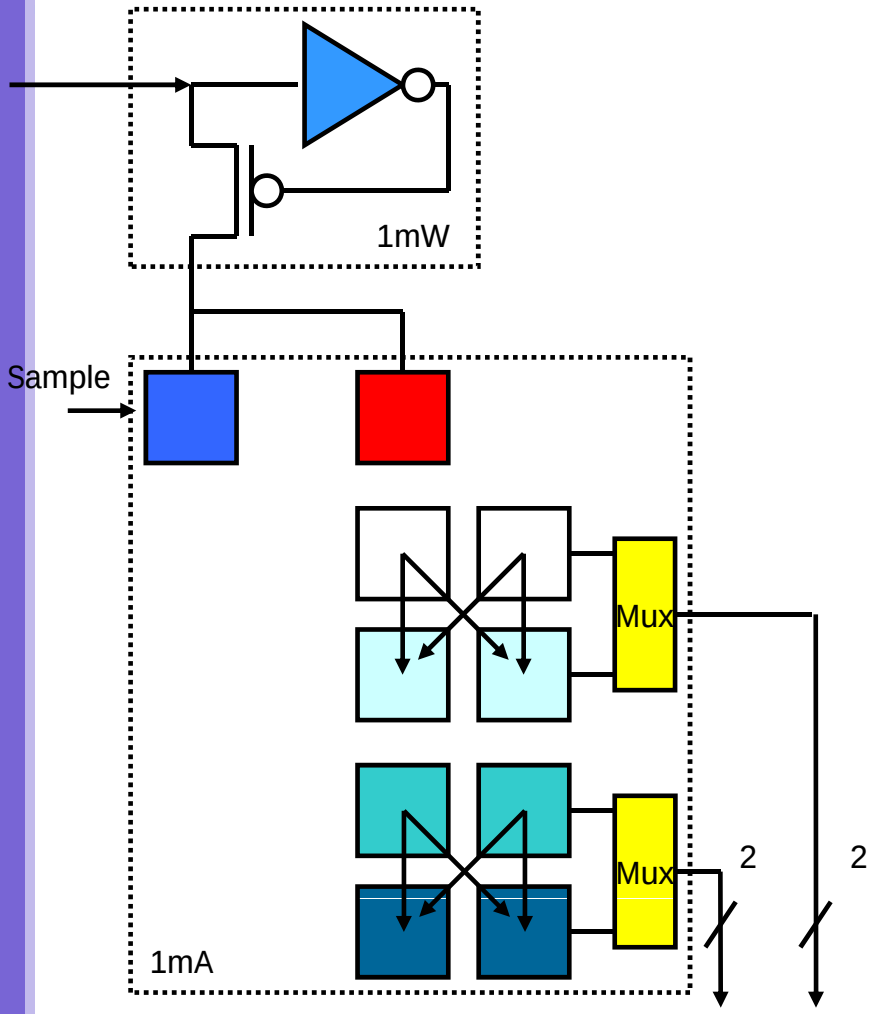
Thank you for attention!

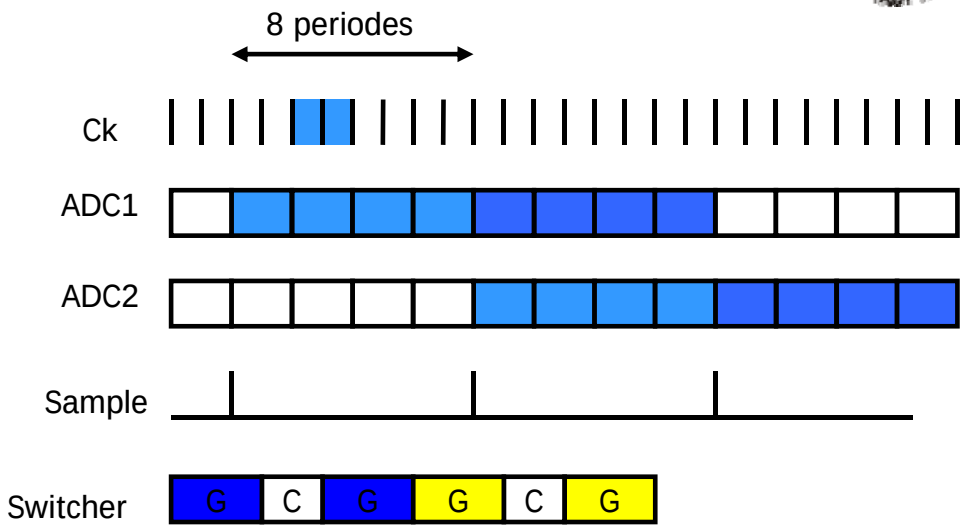
Current-Mode ADC





Current-Mode ADC





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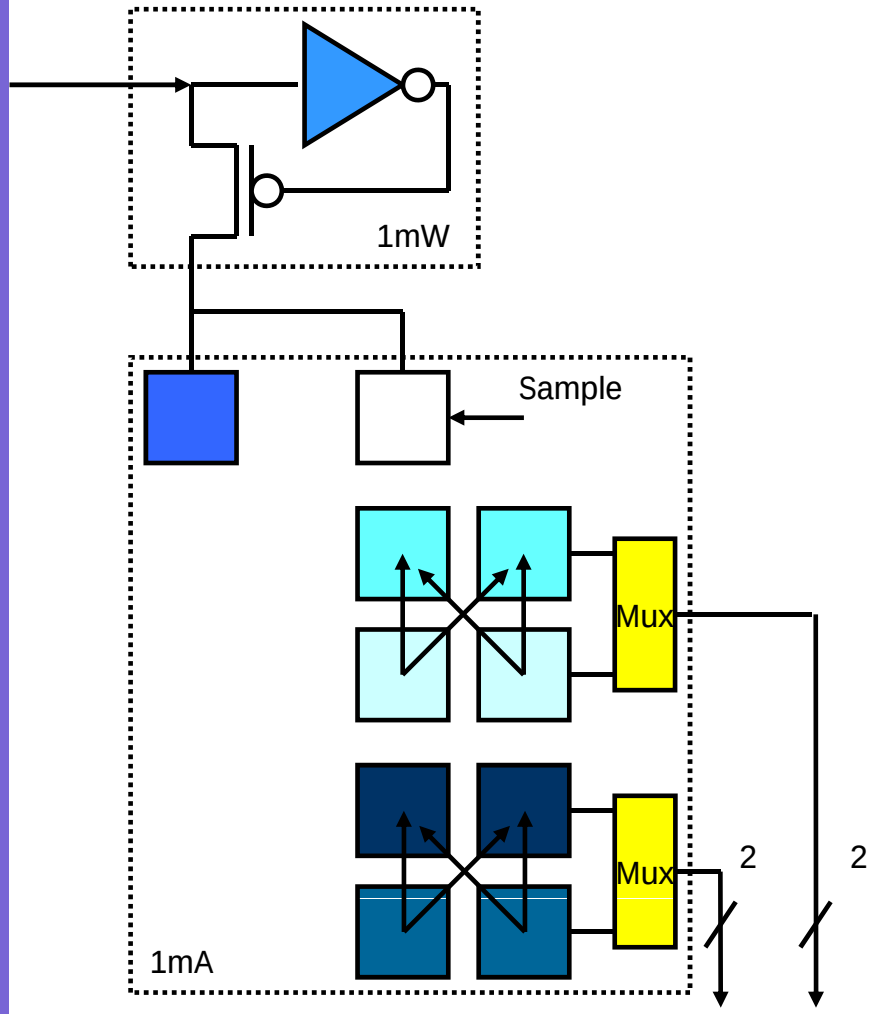
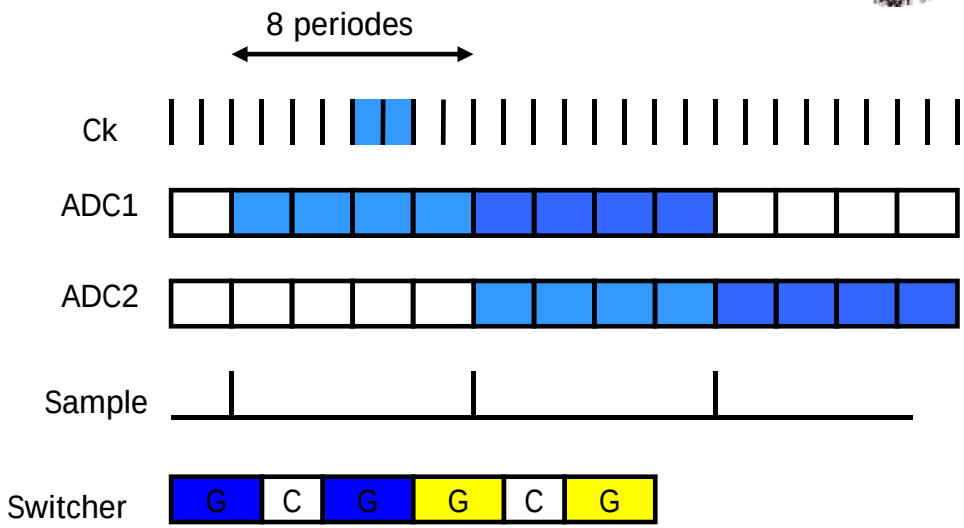
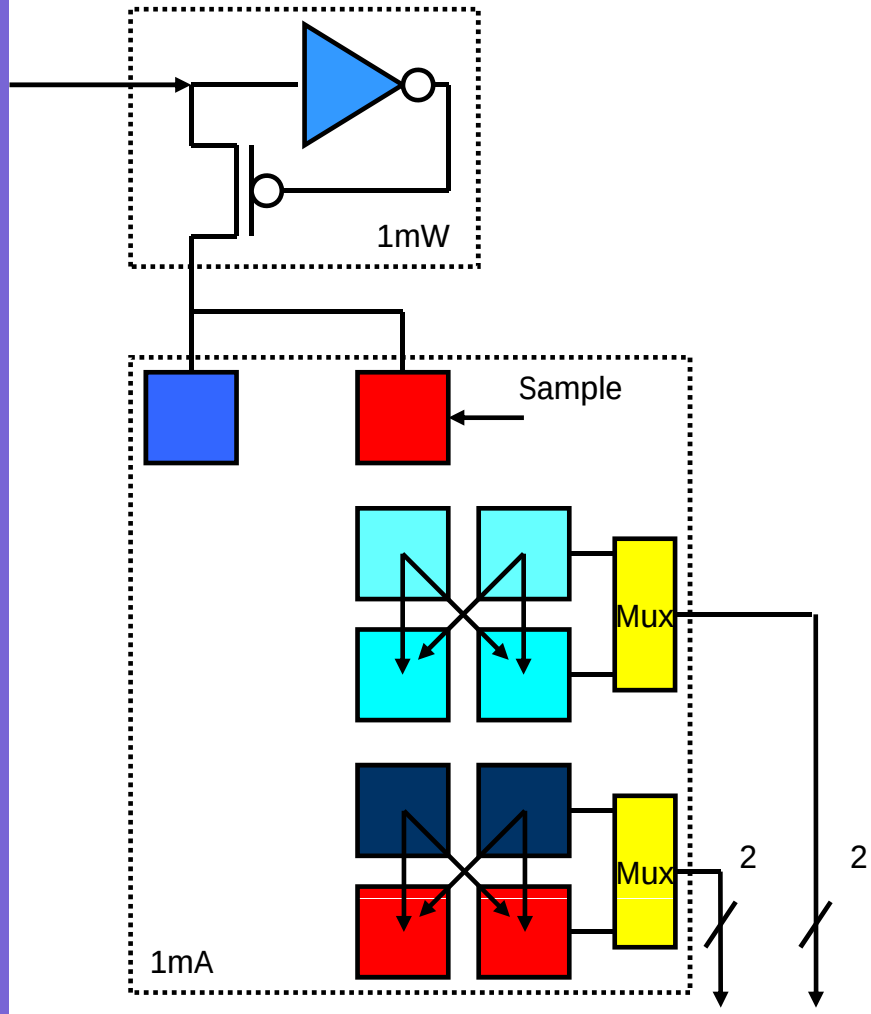
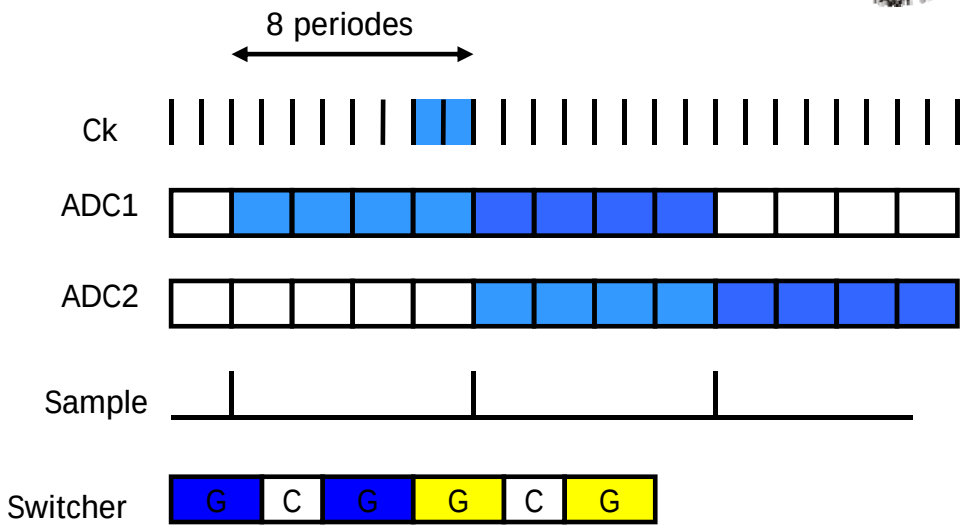


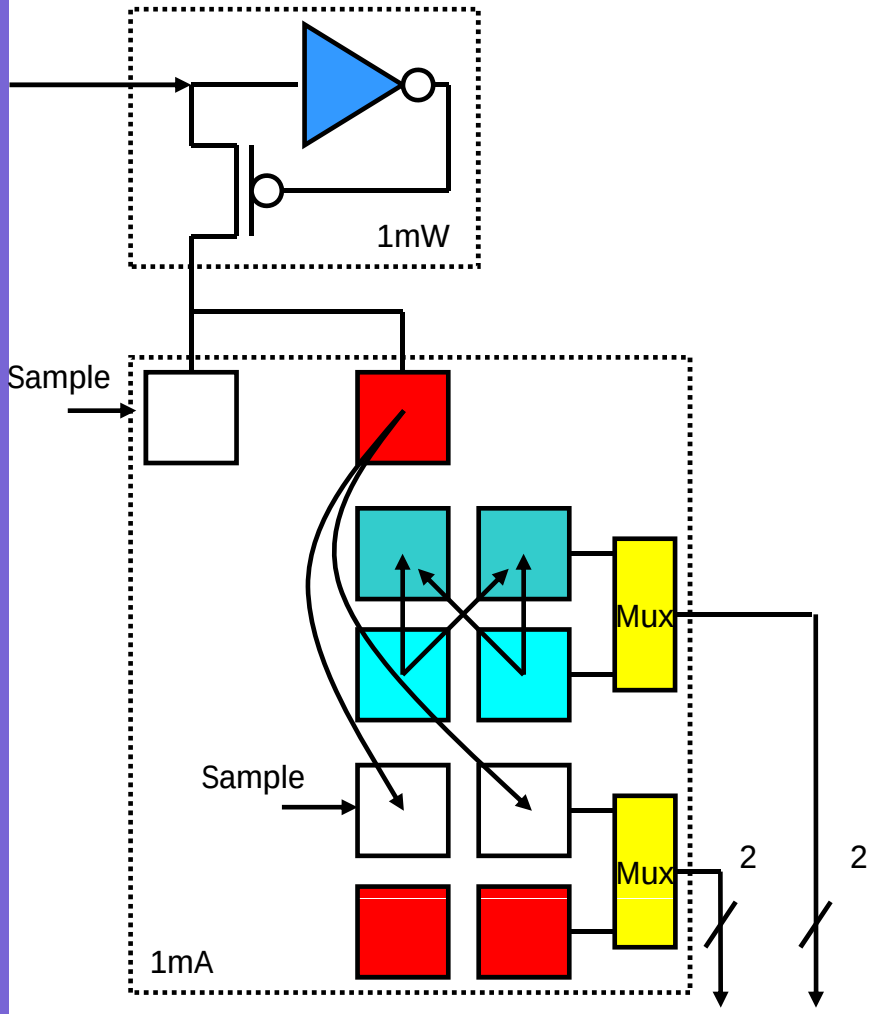


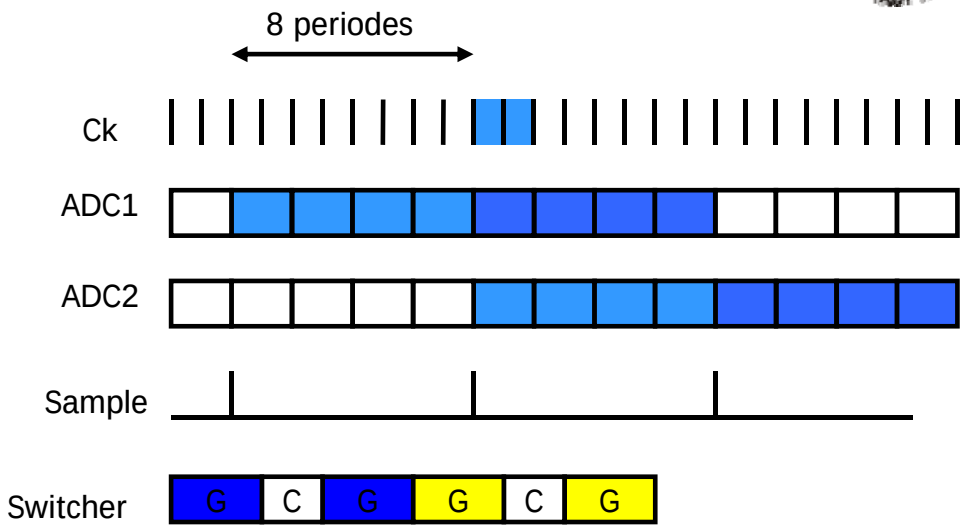
Current-Mode ADC



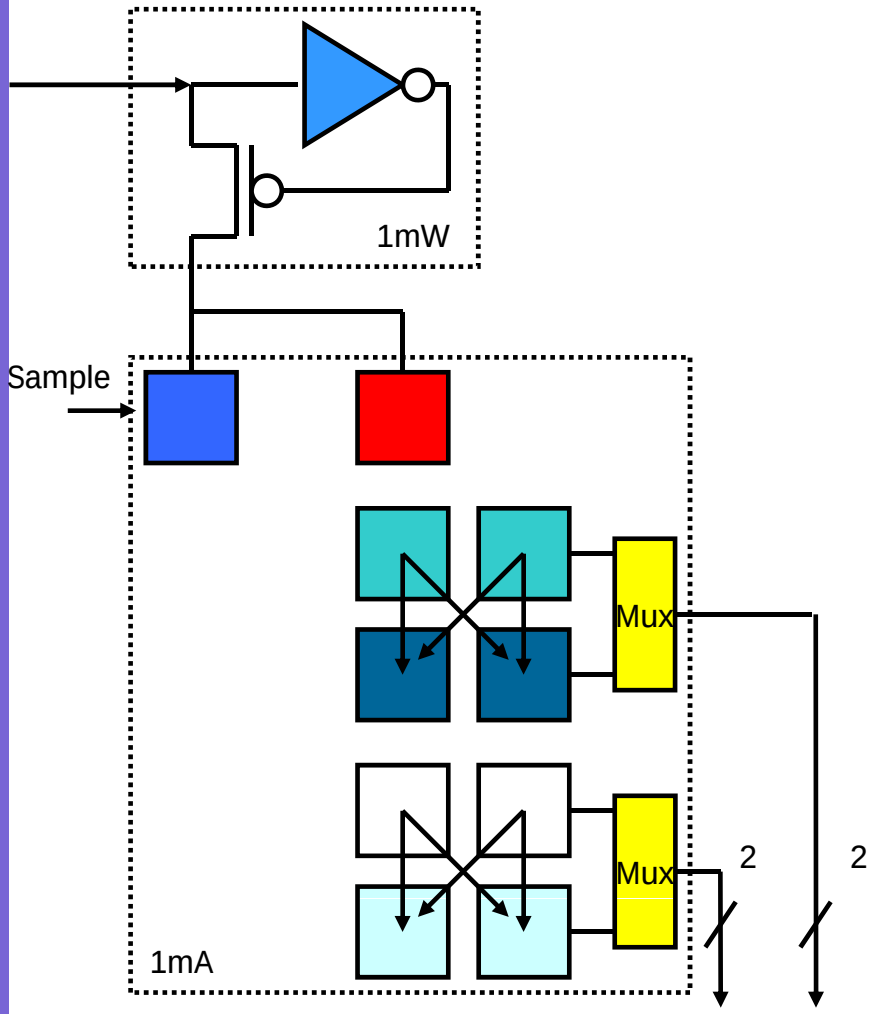


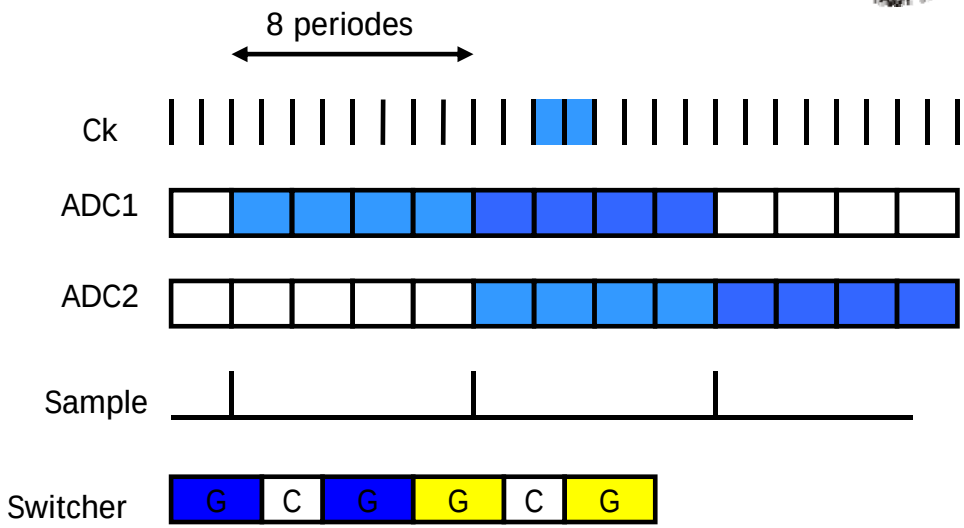
Current-Mode ADC



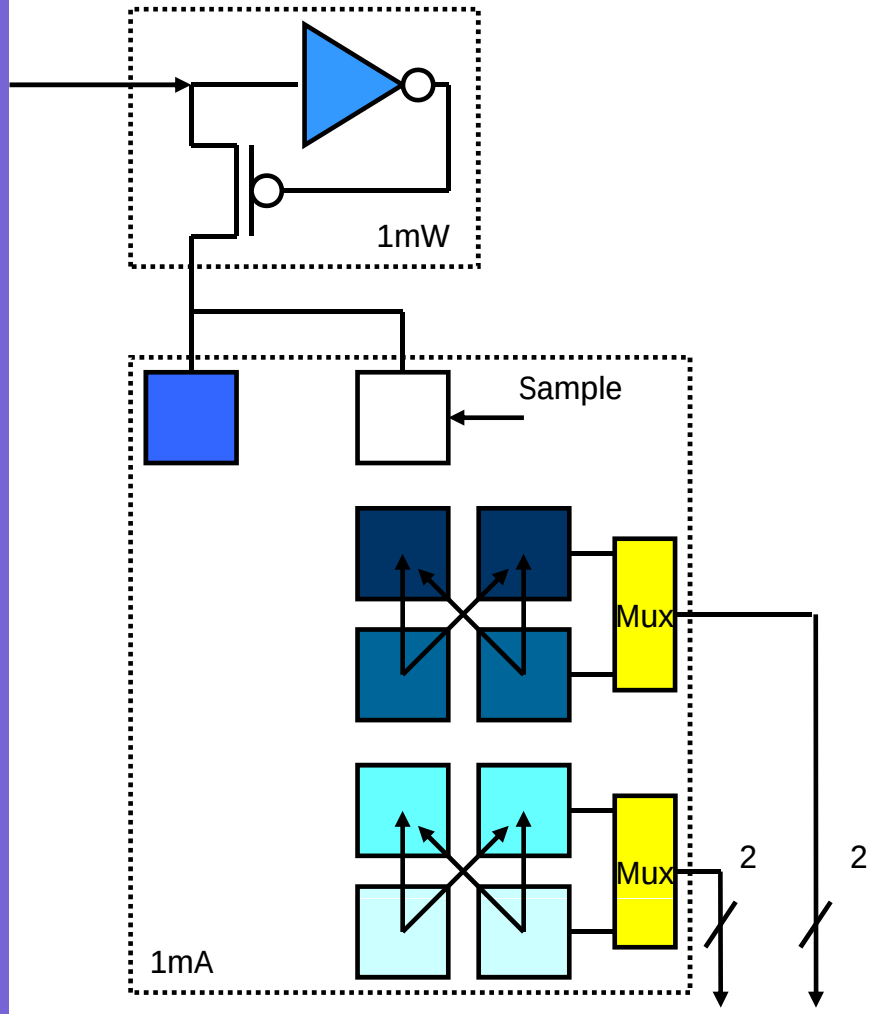


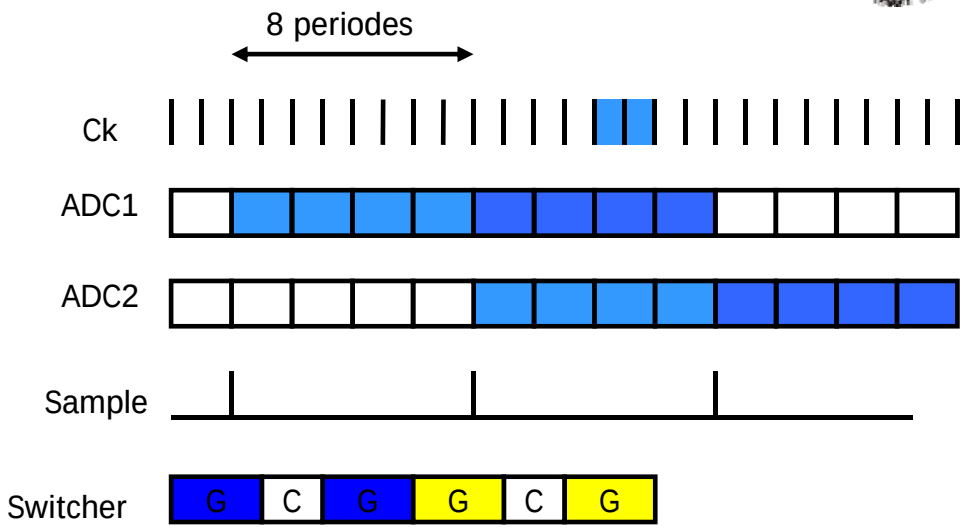
Current-Mode ADC



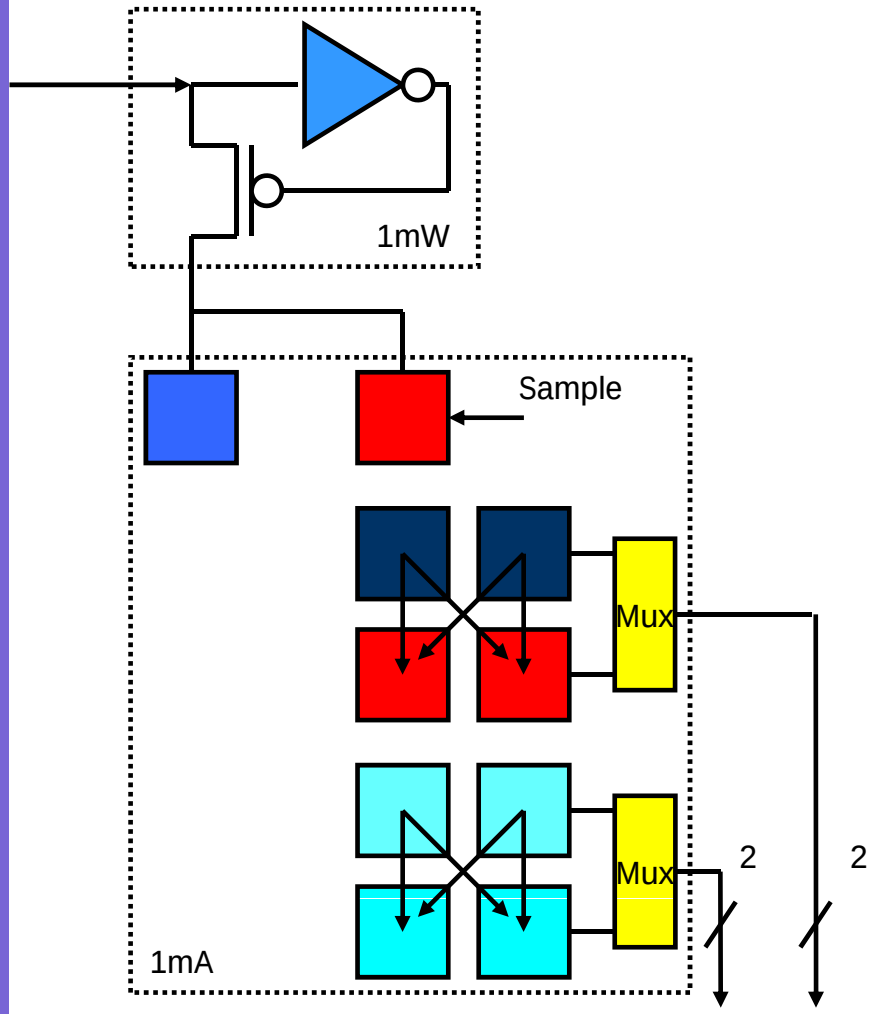


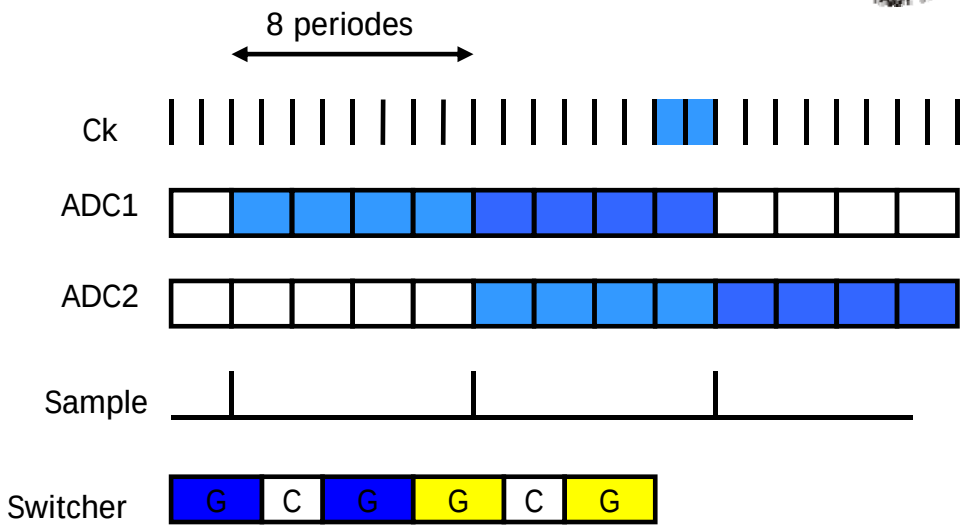
Current-Mode ADC





Current-Mode ADC





Current-Mode ADC