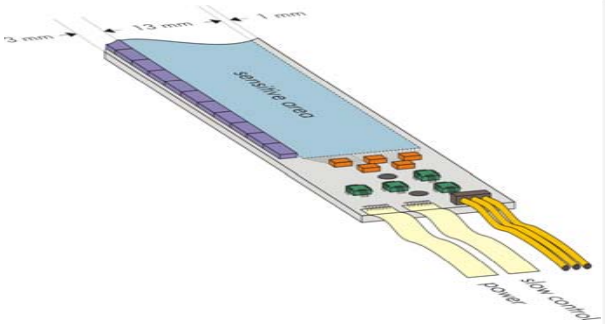
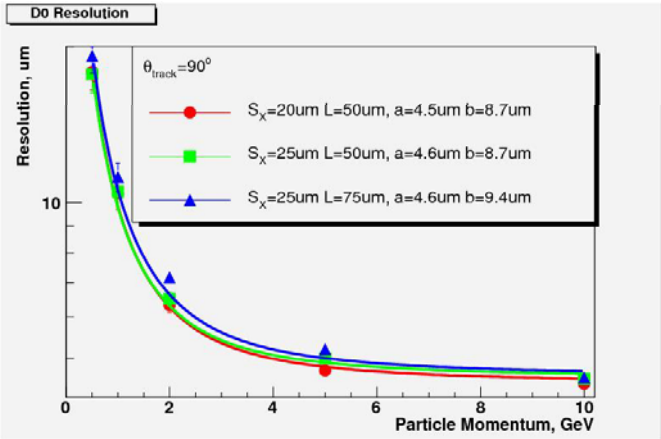
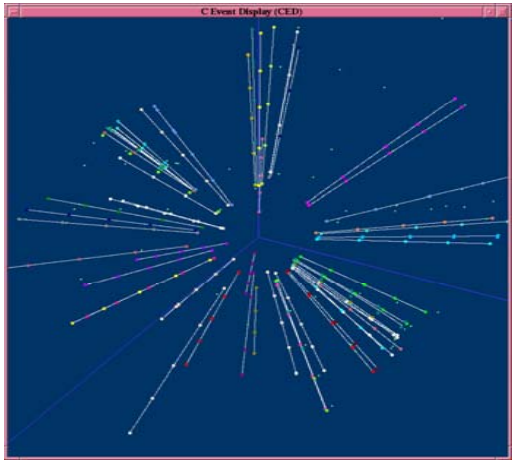
DEPFET Vertex Detector Simulation and Physics Performance

Ariane Frey

for the DEPFET Collaboration
(www.depfet.org)







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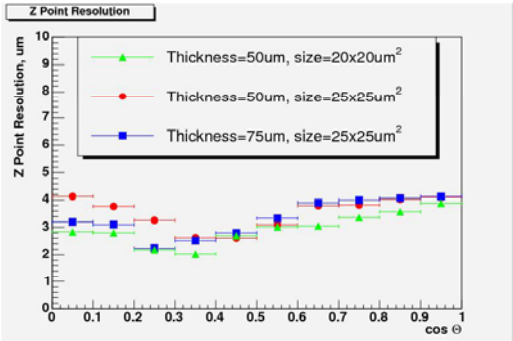
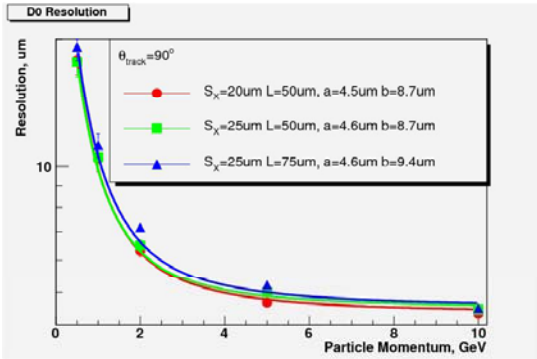
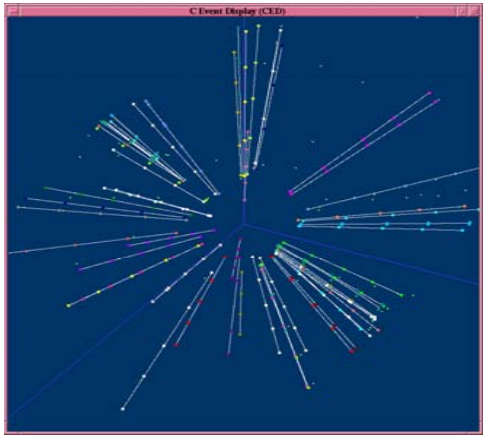
We need:

- Realistic description of geometry including support material
- Realistic simulation of the sensor response
- Validation of the simulation with data from beam tests
- Evaluation of the physics performance

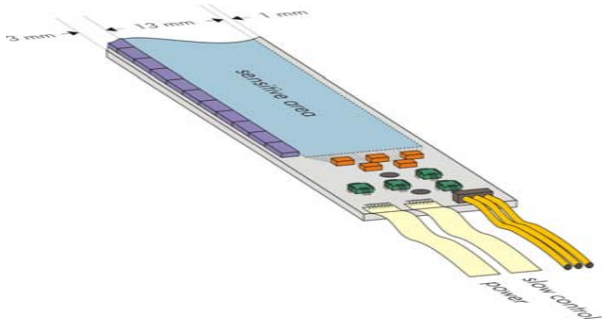


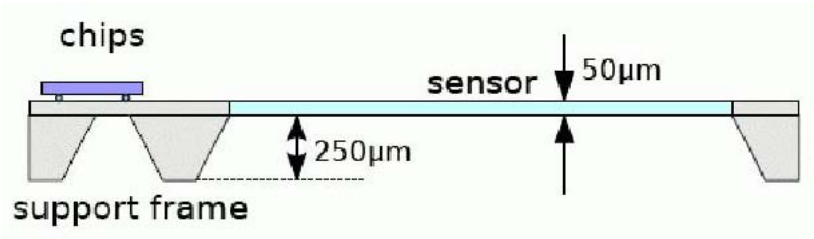




Simulation of the DEPFET VXD geometry

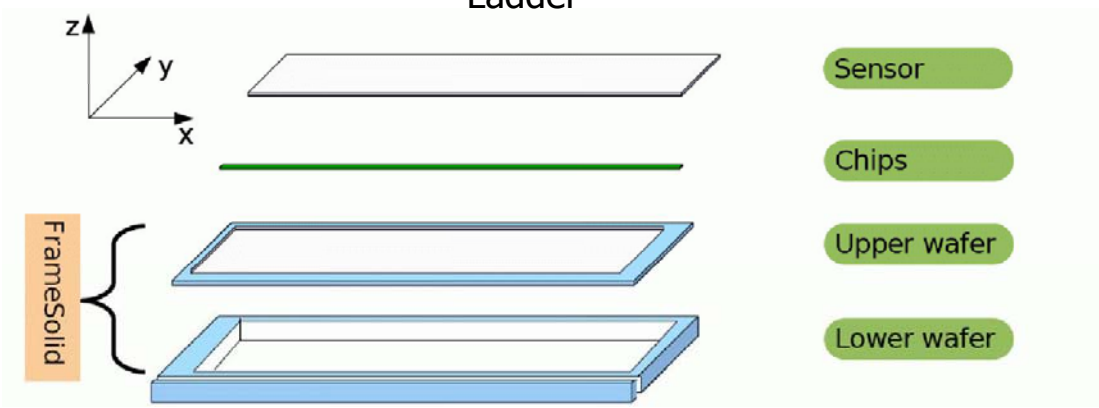
Realistic description of module design including electronics and support structure



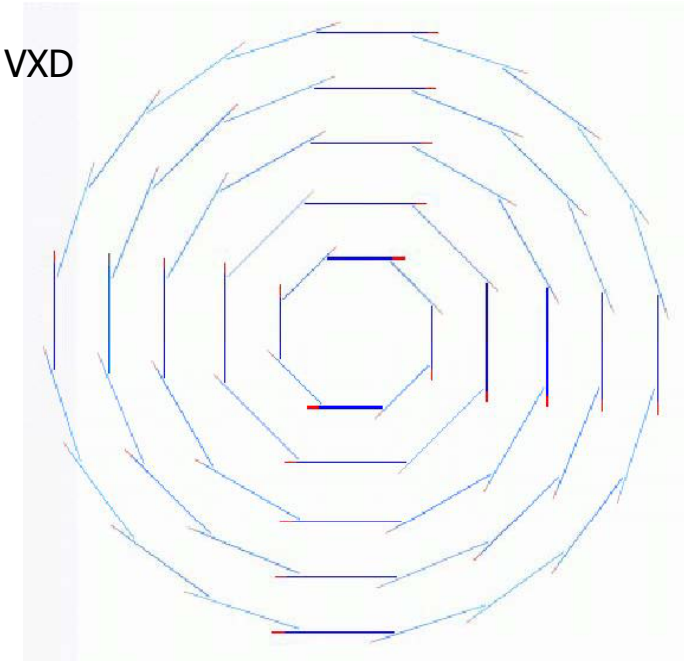


Model in GEANT 4

Ladder

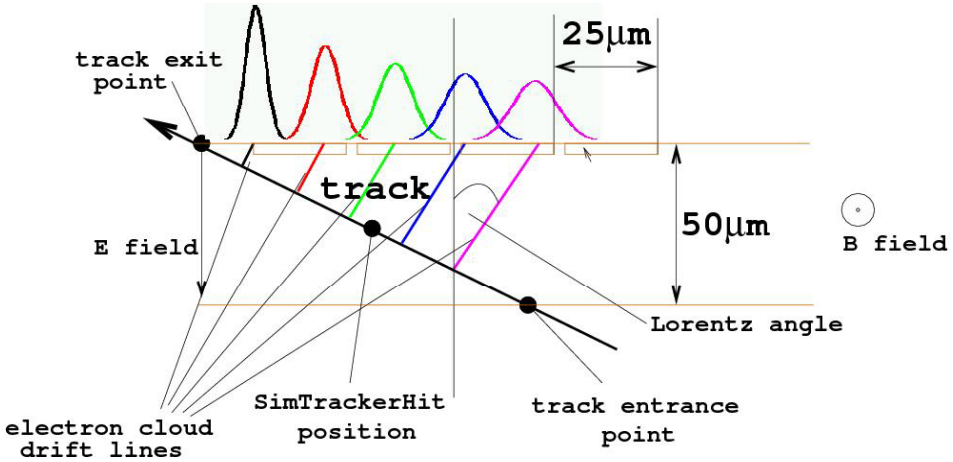


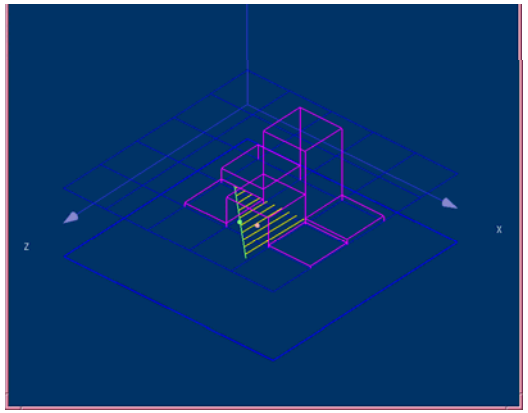
VXD



"outside" support structures simplified and preliminary

Sensor response





Digitization is implemented taking into account

- Landau fluctuations of specific energy loss along track path
- charge transport and sharing between neighboring pixels; diffusion
- Lorentz shift in magnetic field
- electronic noise effects

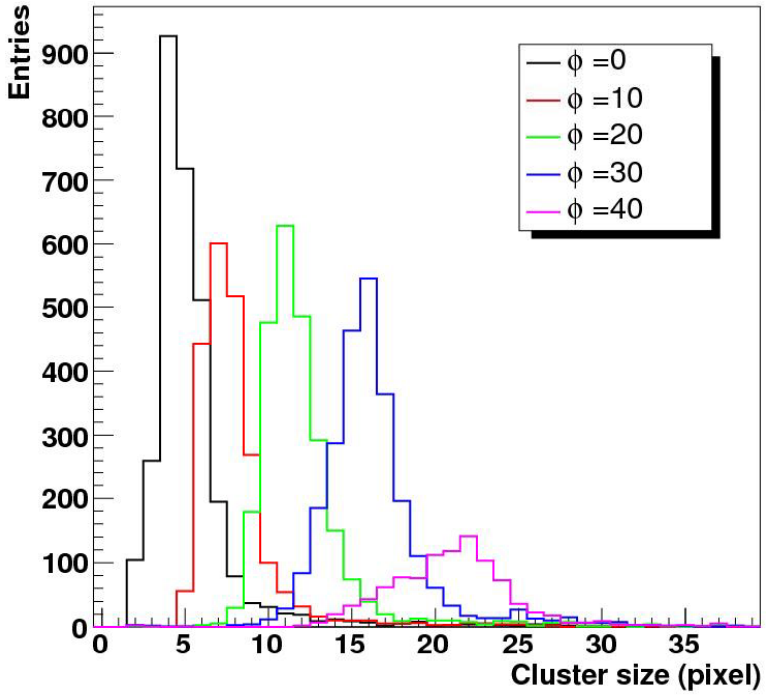
Validation with Test Beam Data

Comparison with data from DESY 2005 testbeam, 6 GeV electrons

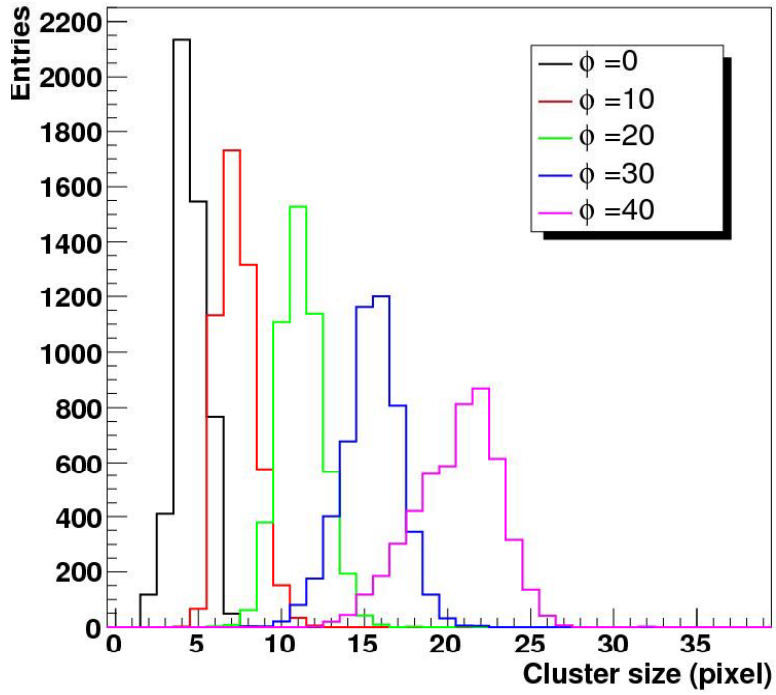
- Thickness 450 µm, pixel size 36 x 22 µm
- no B field, noise set to 300 e^-
- Track incident angles from 0 to 40 degrees

Cluster Size

Data



MC



Validation with Test Beam Data

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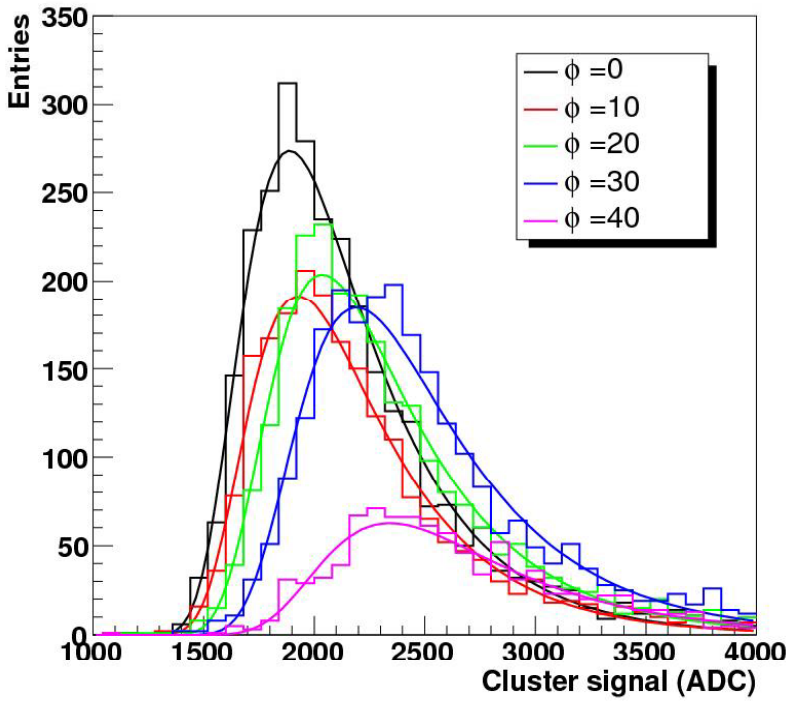
Cluster Signal

Data



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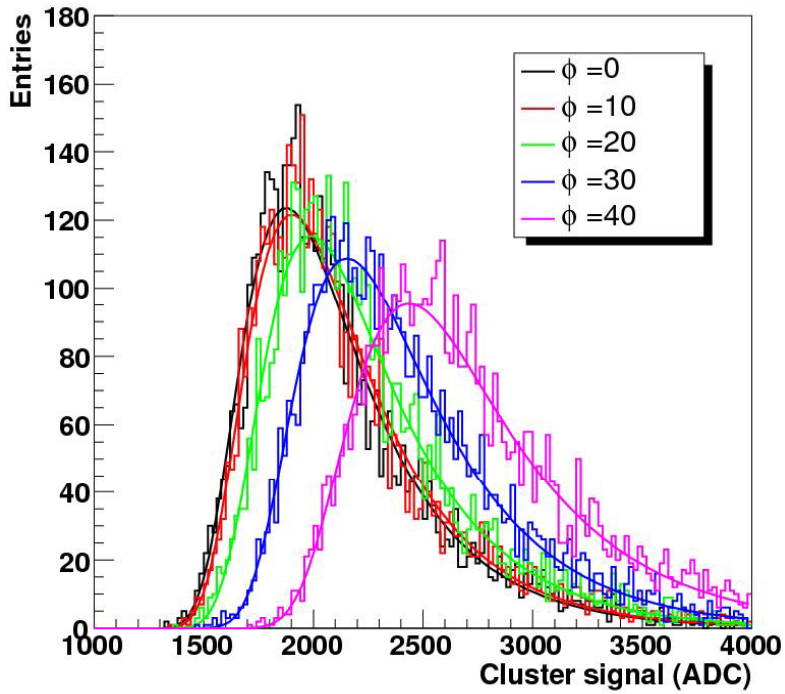

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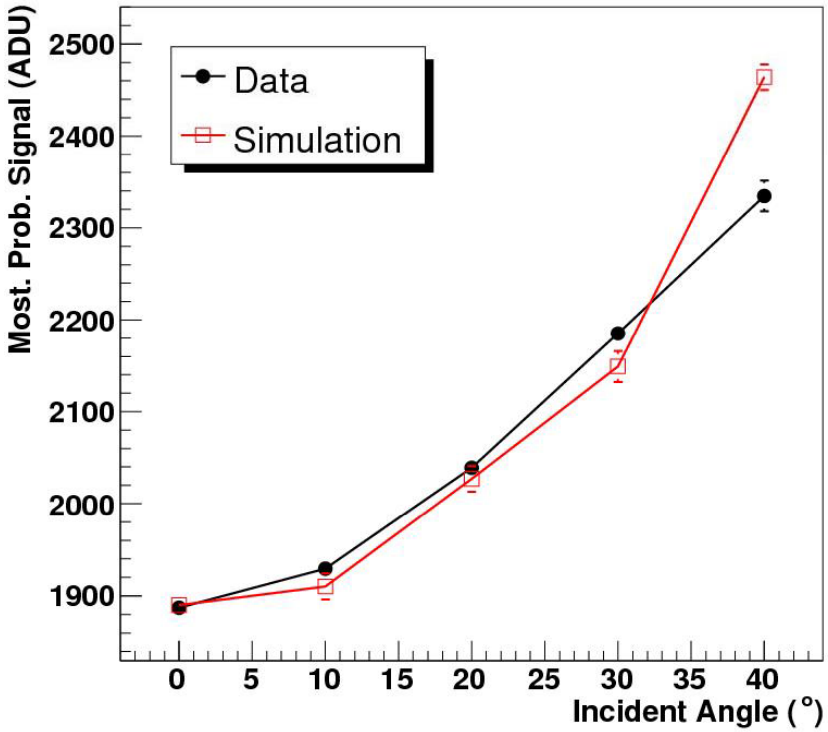
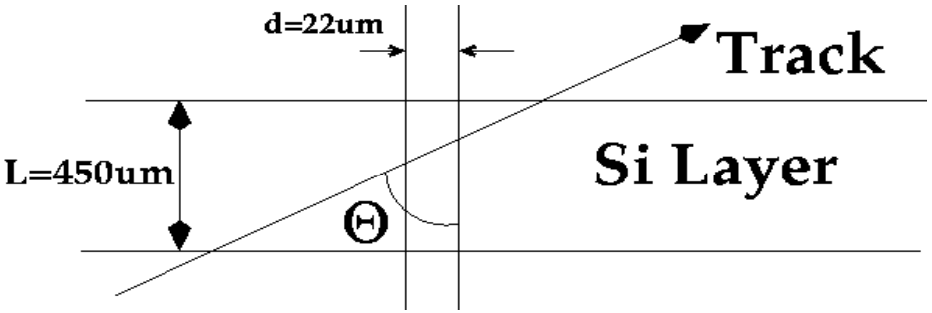


Good agreement of test beam data and simulation

Thin sensors

Important: validate the simulation of energy loss in thin sensors (50 µm)

Use test beam data at inclined angles to probe straggling functions at short flight distances



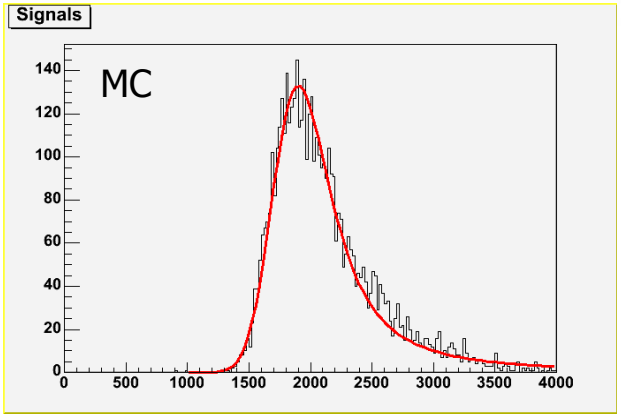
G4 simulation can be probed @ scales **≈ d/sinθ**

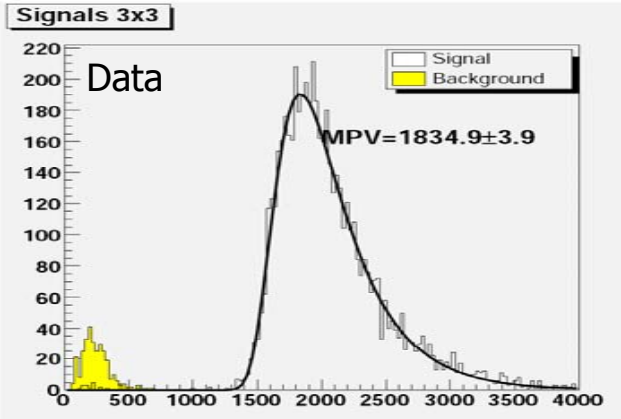
Expected signal $A_{row,column} \approx A_0\, d_{x,y} / (L \cdot \sin(\theta,\phi))$

(d – pixel size
Θ – incident angle)

Data collected at normal incidence is used to find the conversion

$E_{loss} \leftrightarrow$ ADC counts





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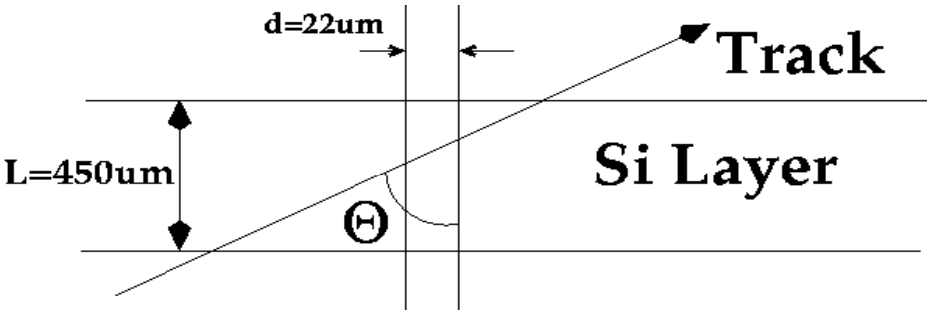

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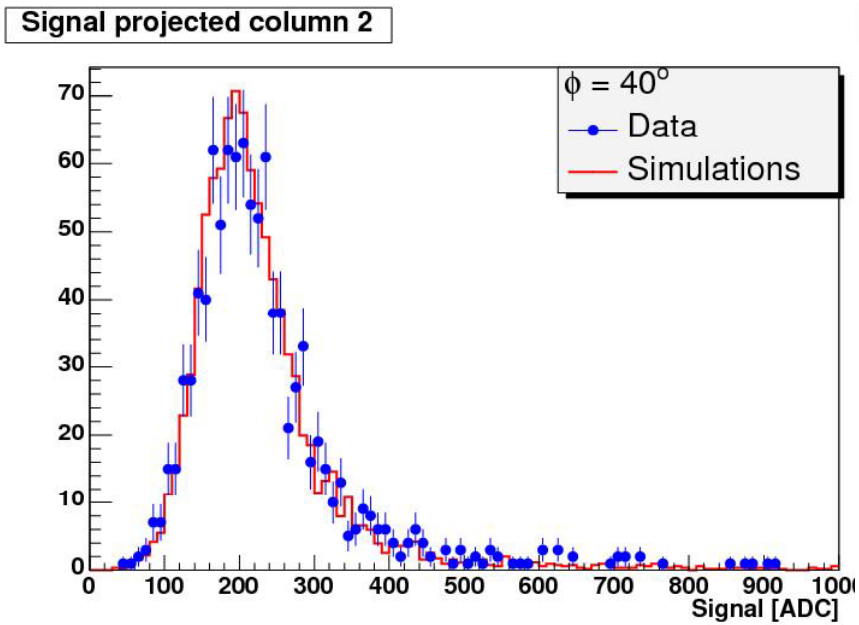
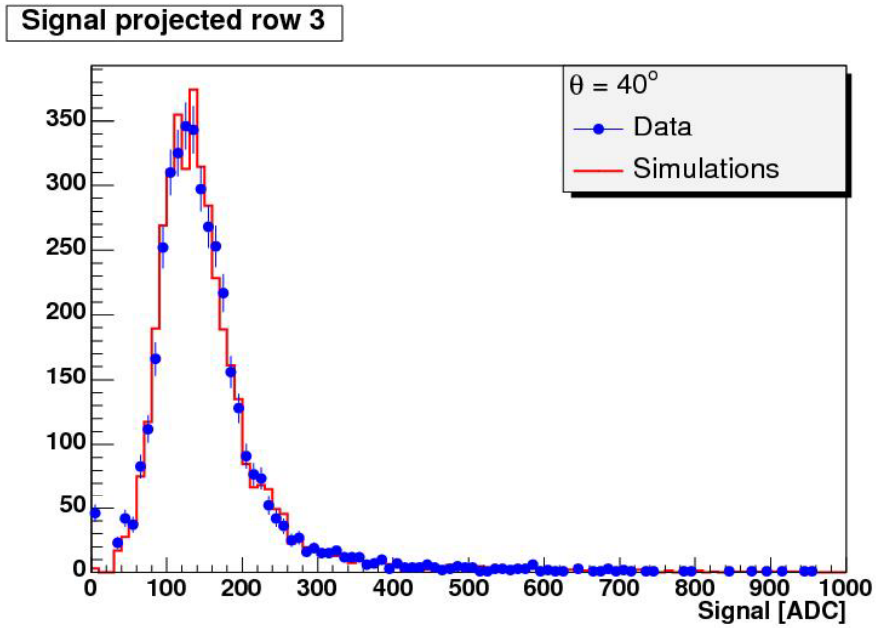
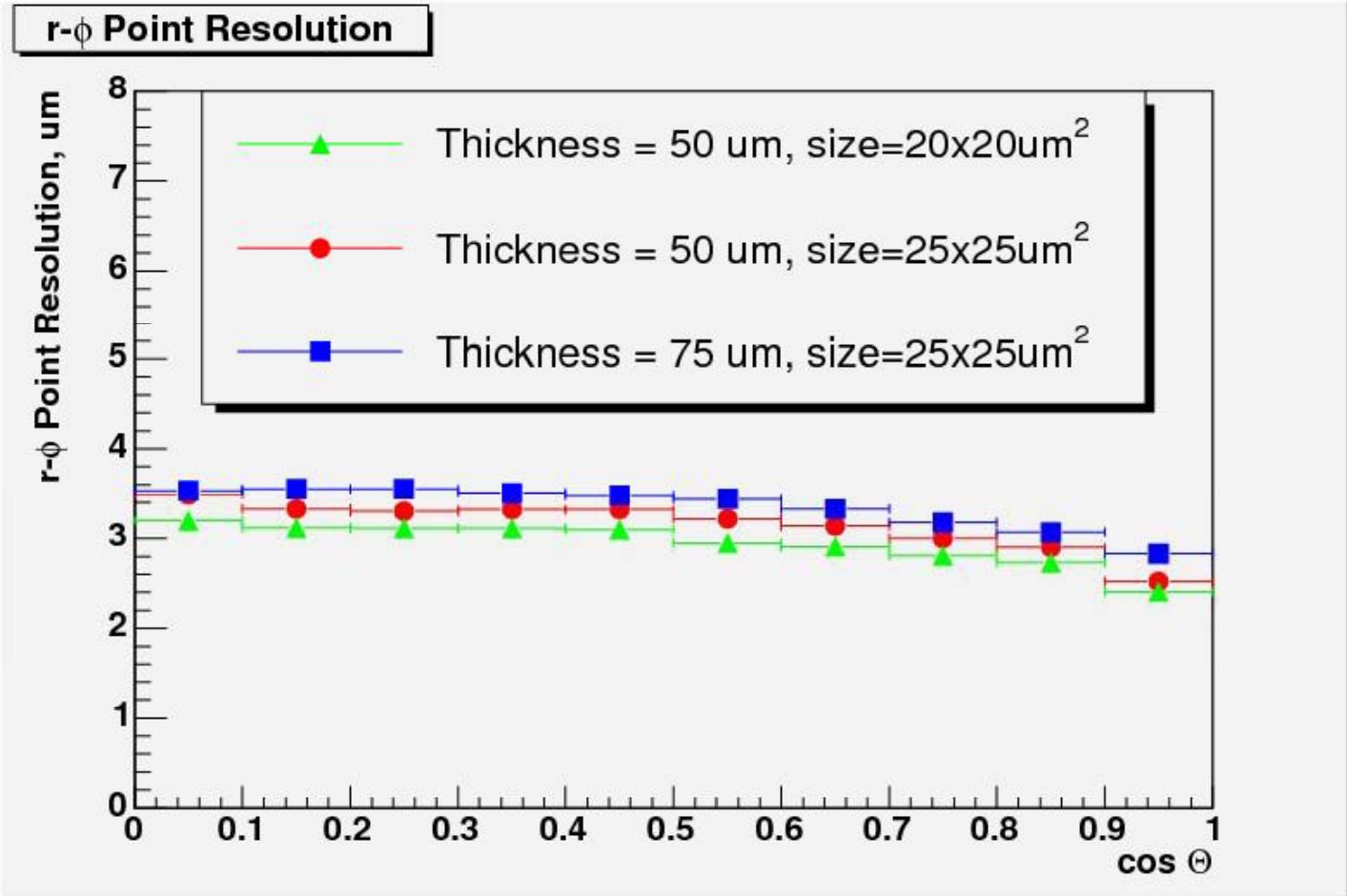




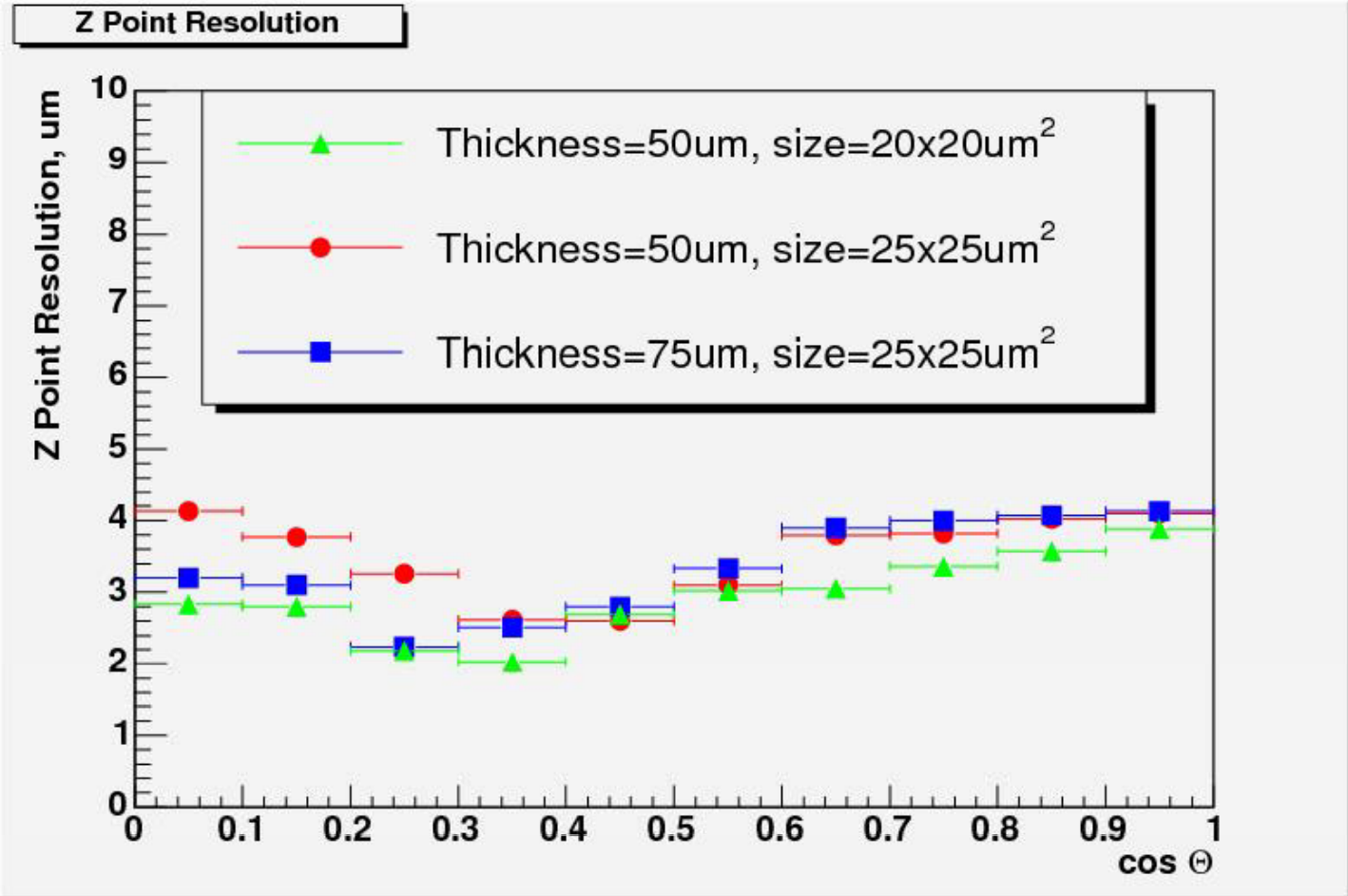
VXD performance: Spatial point resolution

Perpendicular to the B field



VXD performance: Spatial point resolution

Along the B field

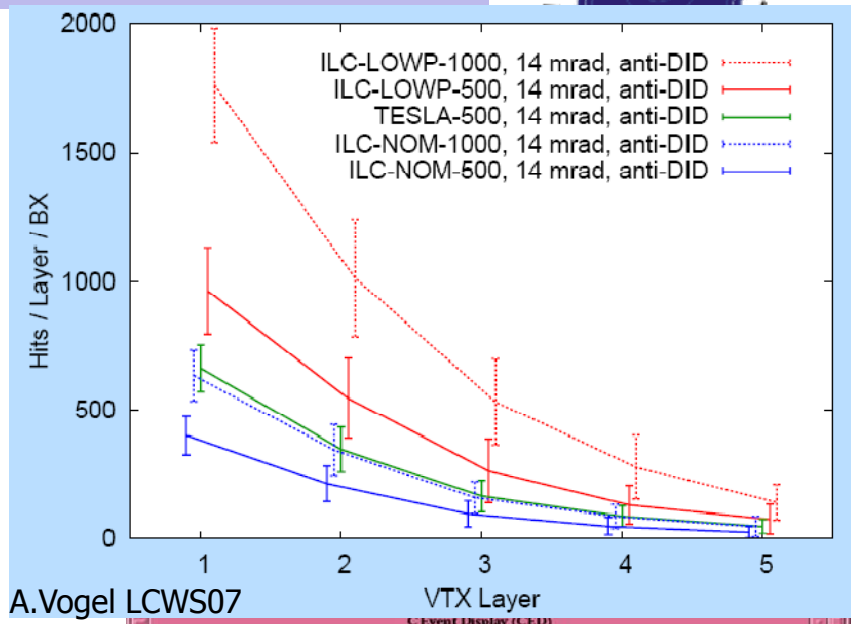


DEPFET VXD in the ILC environment

- Stand-alone tracking
- Able to operate with beam background
- Impact parameter resolution

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta}\right)^2}$$

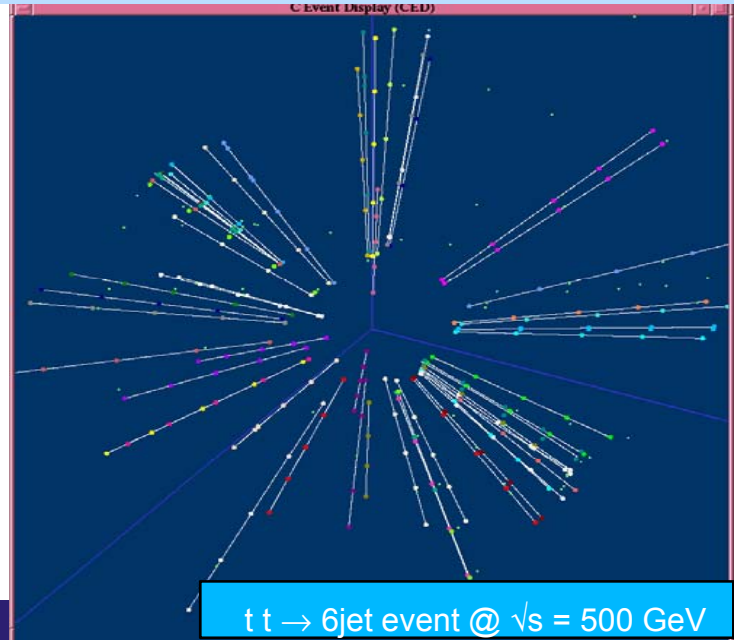
Req: a < 5 µm (point precision)
b < 10 µm (mult. scattering)



A.Vogel LCWS07

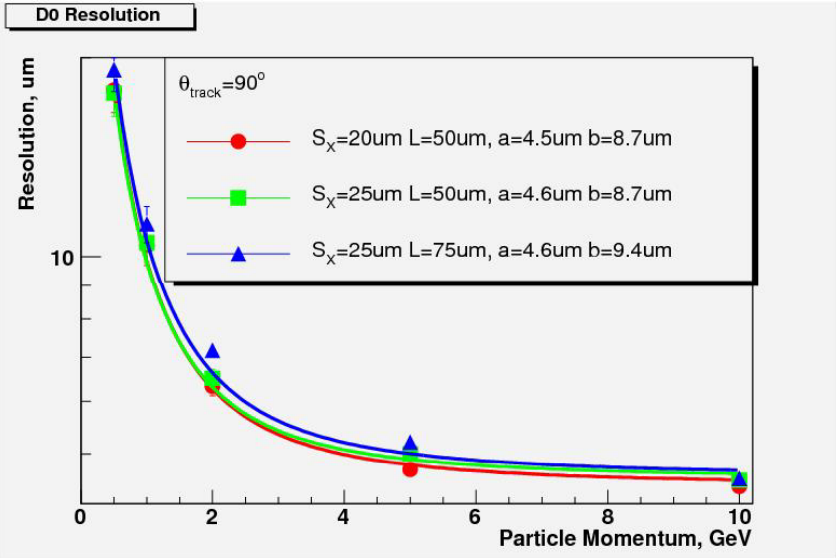
- Developed pattern recognition and Vtx tracking code

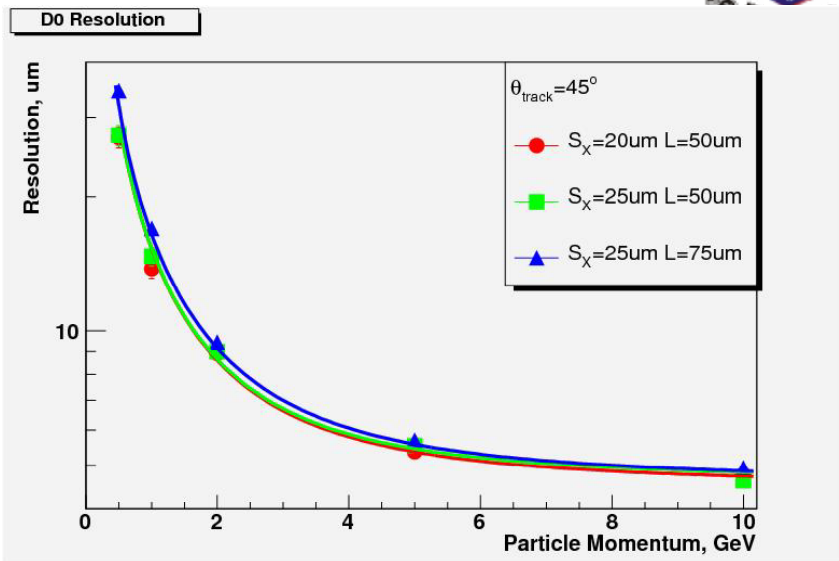
  Algorithm features:
  - Starts with finding triplets in the outer layers
  - Inward search for additional hits
  - Good χ^2 of helix fit – main criterion to accept track candidates
  - Additional loose cuts against fake tracks composed of background hits



t t → 6jet event @ √s = 500 GeV

Performance

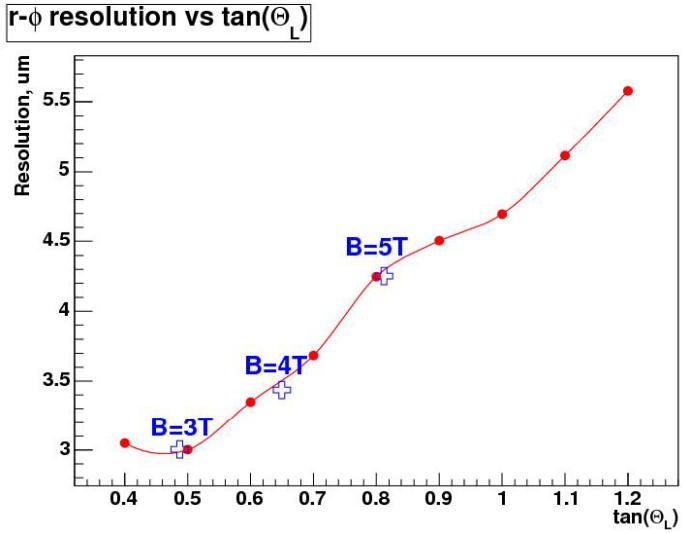




$\sigma = a \oplus b / (p \cdot \sin^{3/2} \theta)$

<u>Result:</u> a = 4.6 µm < 5 µm

b = 8.7 µm < 10 µm



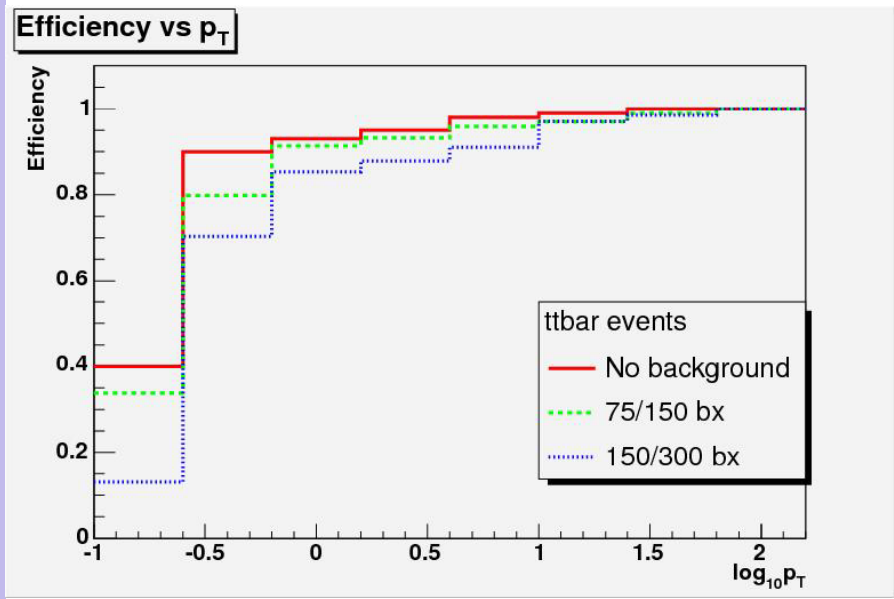
Spatial resolution as a function of B field

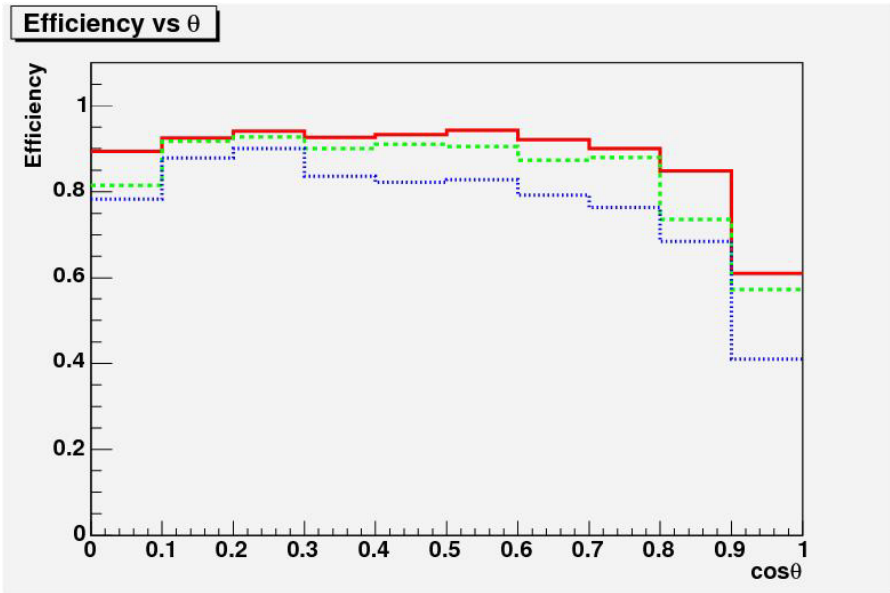
$\Rightarrow$ Performance ok for B = 3-5 T

With background: Tracking efficiency, fake tracks

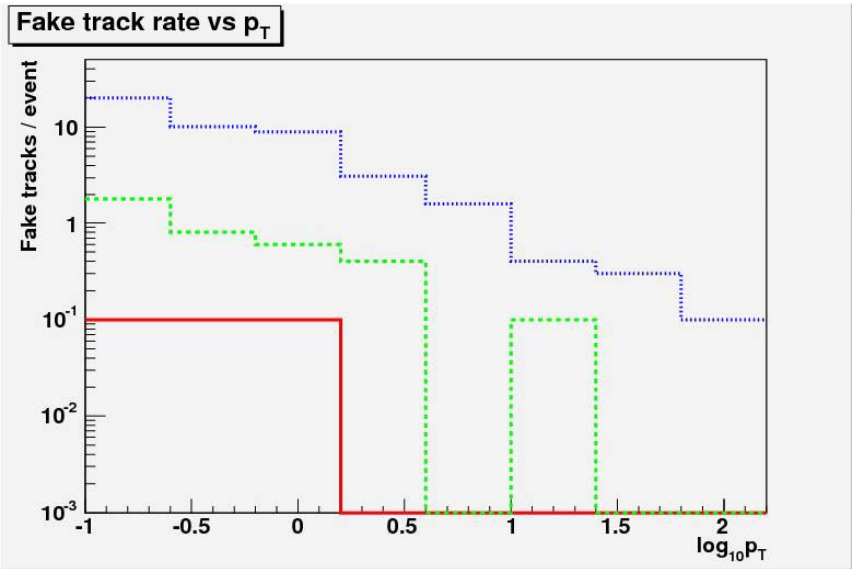
Studied 3 scenarios:

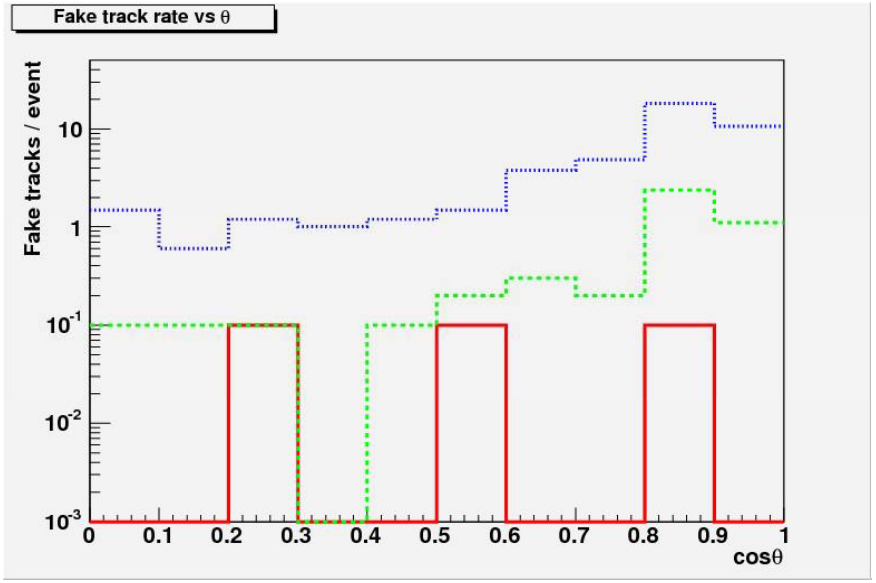
- no background ⇒ 400 hits in layer1
- Integration time of 25 μs(50 μs) in layer1(outer) ⇒ ∫ 75(150) BX, 30k hits in layer1
- Integration time of 50 μs(100 μs) in layer1(outer) ⇒ ∫150(300) BX





With background: Tracking efficiency, fake tracks

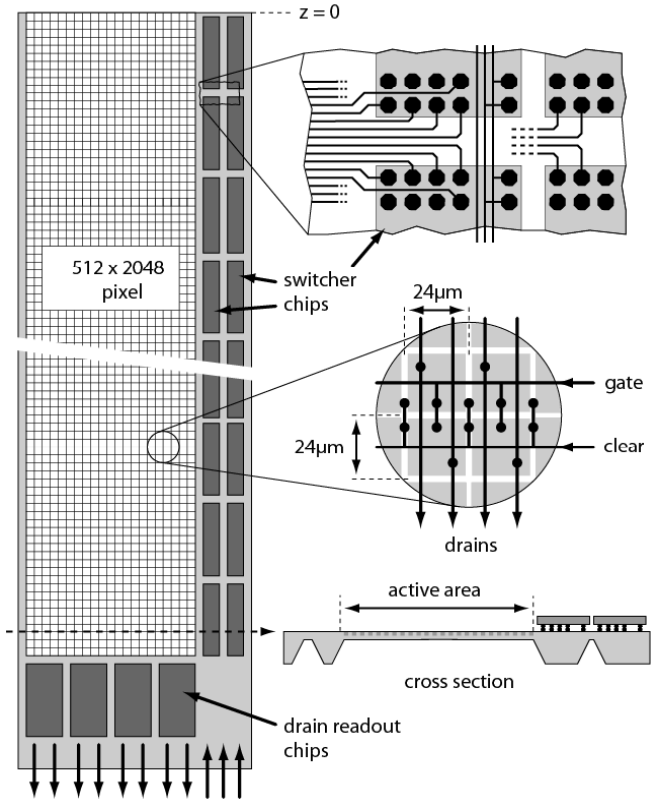


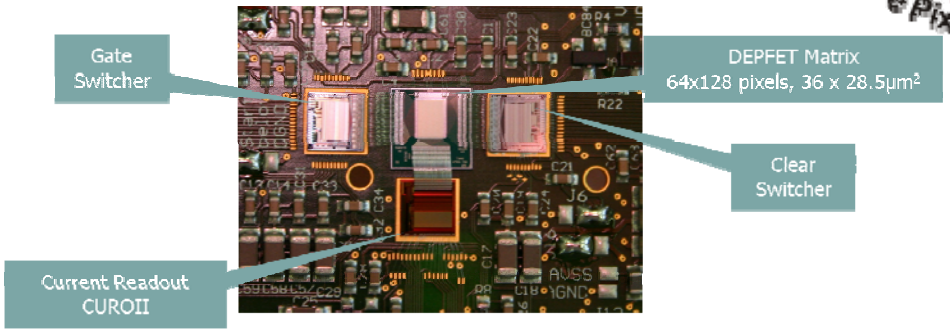


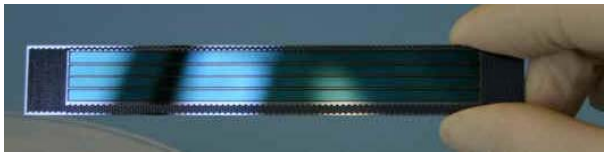
Scenario	Fakes per event	Track finding efficiency, %	
		$p_T > 0.1$GeV	$p_T > 0.5$GeV
1	0.3	88	94
2	4.2	84	91
3	45	79	86

$\Rightarrow$ Fast read-out is vital !

In Summary: Achievements







- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
  - ✓ S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2
- ✓ Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.

In Summary: Prospects

- ✓ Production of 2nd iteration DEPFETs was finished summer 2007, expect higher internal amplification (g_q=0.4nA/e → almost 1 nA/e), better S/N
- ✓ New Switcher3 chips tested and functional
- ✓ New r/o chips DCD designed for read-out of large matrices is under test

Power Consumption for the ILC VXD (baseline design) with these new chips

layer 1: 8 ladders, 4096x512 pix./ladder → ~ 12W/ladder → ~100 W/layer

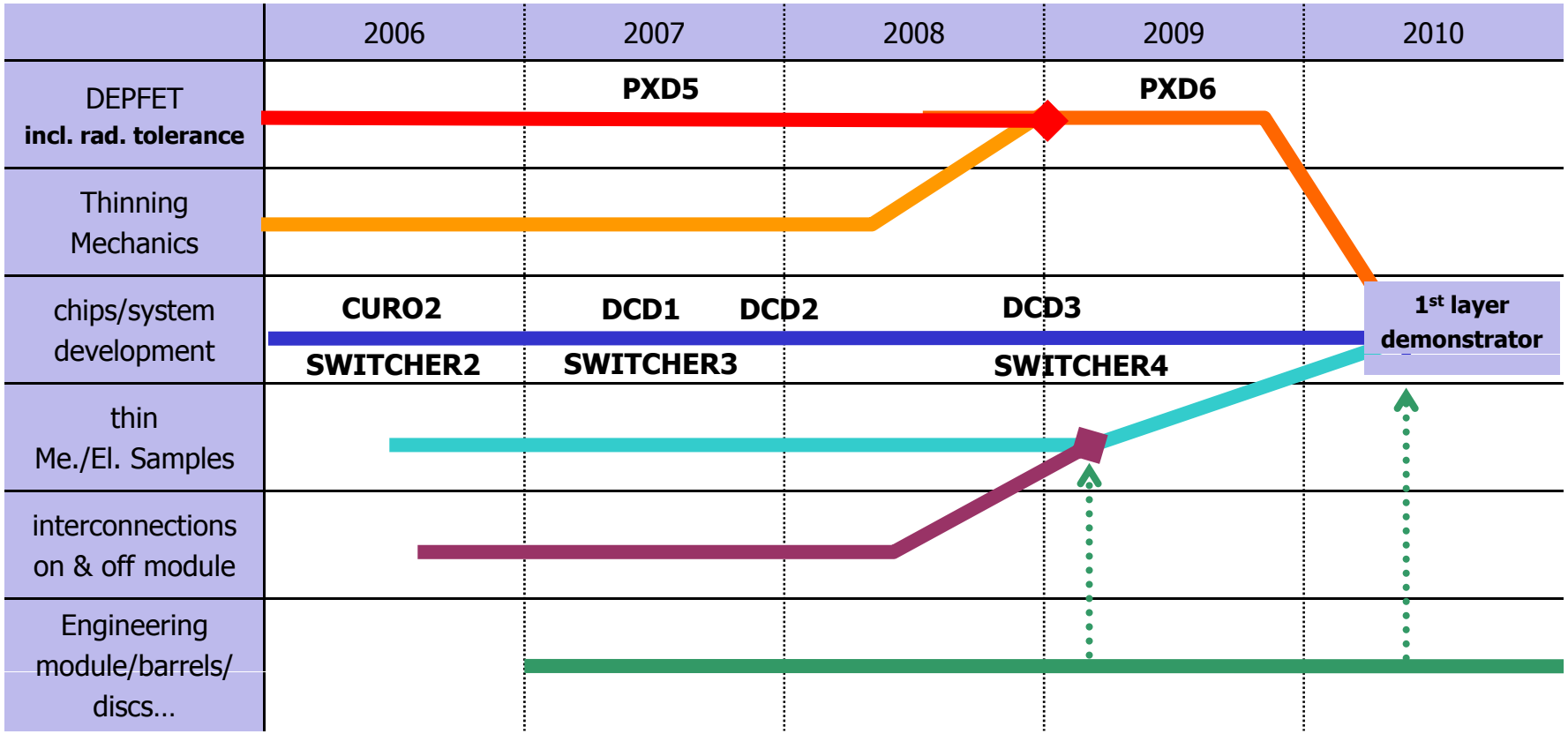
layer 2-5: 56 ladders, 10496x928 pix./ladder → ~ 21W/ladder → ~1200 W/ 4 layers

→ 1300 W → **6.5 … 13 W** with pulsed power operation 1/200 - 1/100

About 90% of the power is dissipated at the ladder ends (r/o chips DCD)

Based on the experience made with the prototype system, we are confident that the DEPFET in the **present baseline design** can meet the requirements at the ILC VXD. In this concept, with the read out at the end of the ladders, the biggest challenge is the required row rate and the capacitive load at the f/e inputs. There are several ideas how to increase the "head room" in this respect, one of those being the use of the emerging 3D technologies. This will be one of the future R&D directions.

....towards a thin demonstrator (in baseline design)

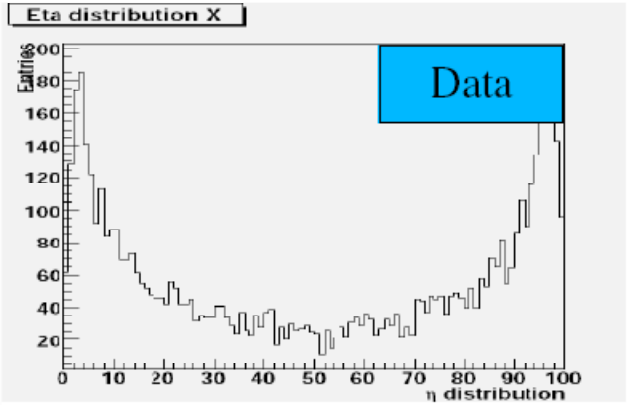


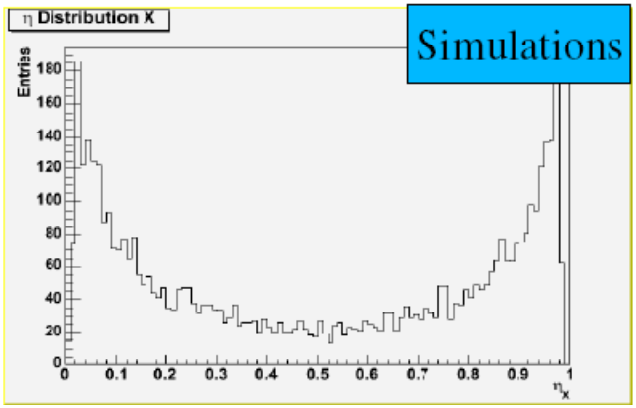
- ✓ ASIC production: UMC, AMS, IBM, TSMC.... use the best available process
- ✓ DEPFET prototyping and series production of the sensors at the MPI Halbleiterlabor

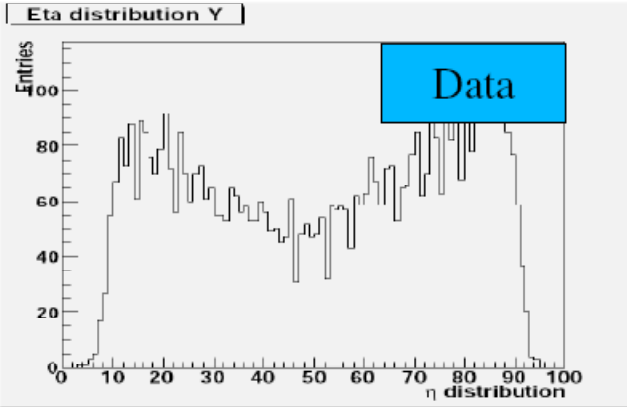
Backup

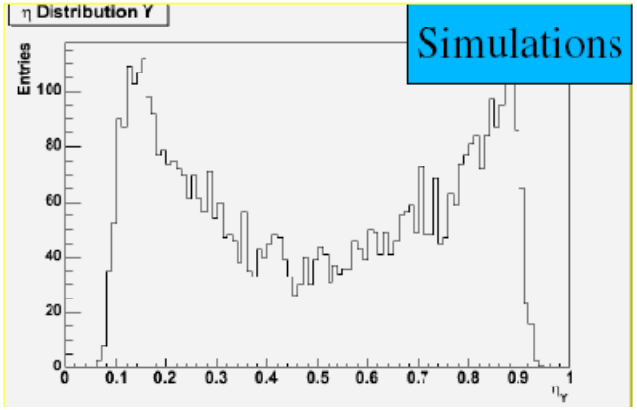
- Validation with Test Beam Data

η-Distributions :
Testbeam Data vs. Simulations

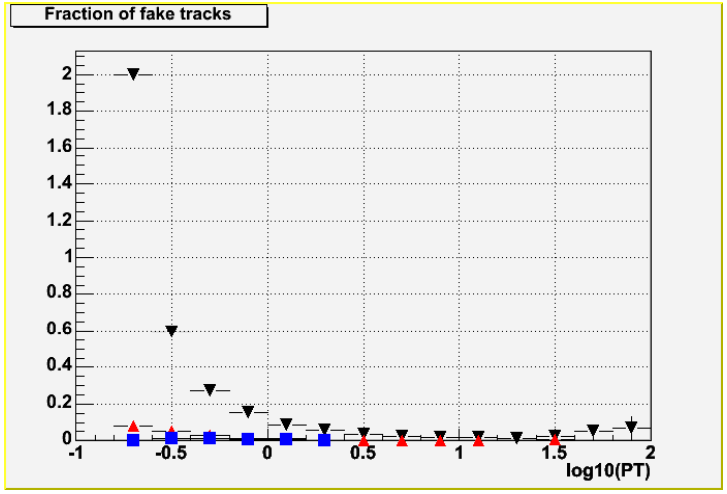


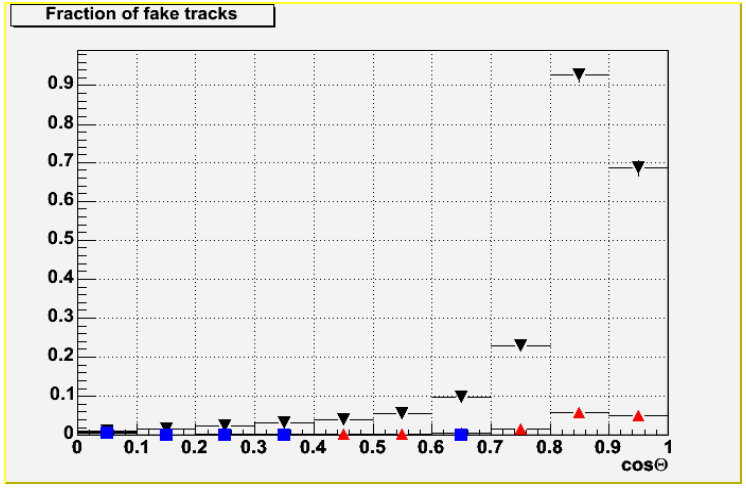




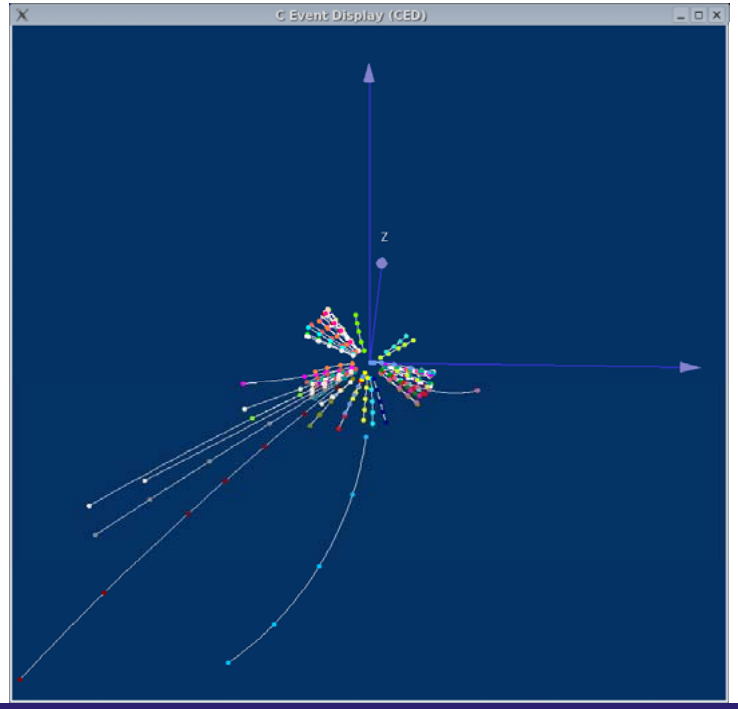


Fake tracks

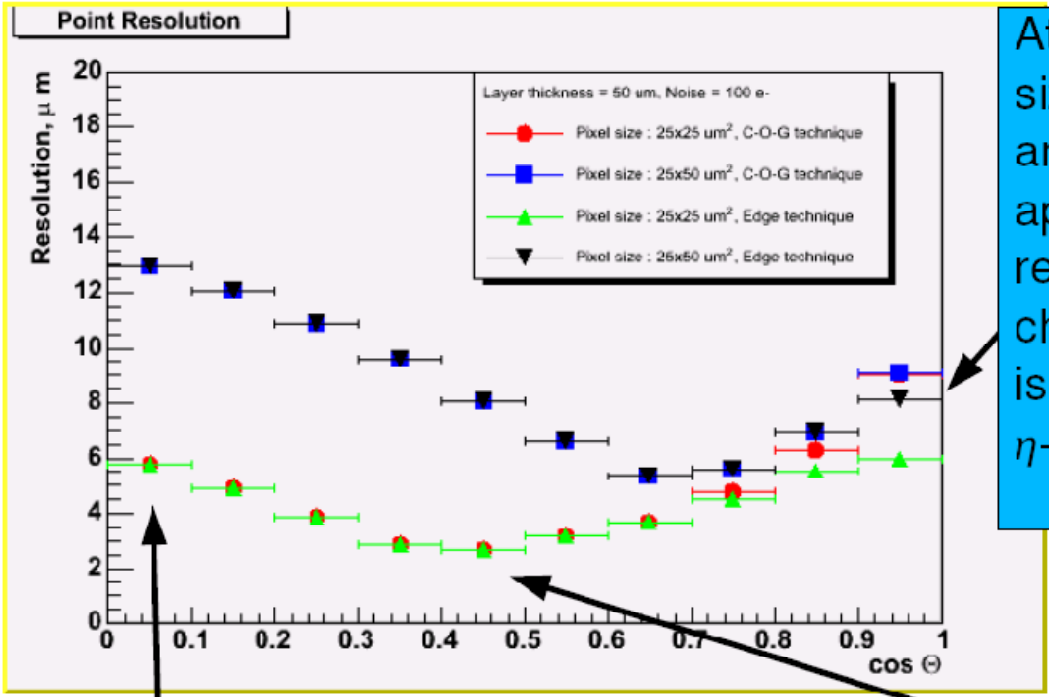




Inclusion of forward tracking helps in discarding fake tracks



Point Resolution in Z



At shallow angles cluster size gets extremely large and simple centre-of-gravity approach yeilds poor resolution due to inter-pixel charge fluctuations. Resolution is improved by means of η-algorithm (edge-technique)

In many cases at normal incidence only one row is fired :
resolution is limited by pixel size

When track is inclined more than one row is fired -> resolution gets better

DEPFET Array - different ways for read-out

1. Row wise read-out

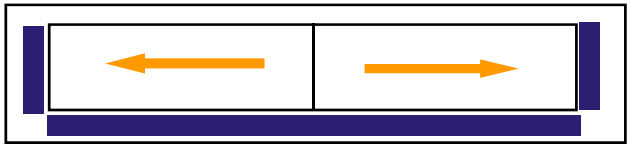
- select row with external gate, read current, clear DEPFET, read current again

Advantage

- Low power consumption!
- No advanced interconnection technologies needed

Disadvantage

- limited frame rate



3. Combination of those two

- subdivide large arrays into smaller units
  - → smaller cap. load
  - → more relaxed row rate
- challenging interconnection (→"3D"?)

→ find optimum for a specific application balancing the pros and cons

under consideration for the **ILC VXD**

2. Hybrid-pixel-like approach: one amp. per pixel

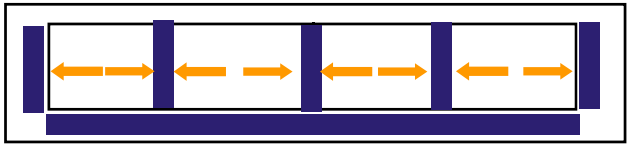
Advantage

- fast! (~ns), frame rate comparable with hybrid pixels

Disadvantage

- challenging interconnection between sensor and r/o chip
- high power consumption

Foreseen for the focal plane at the **XFEL**



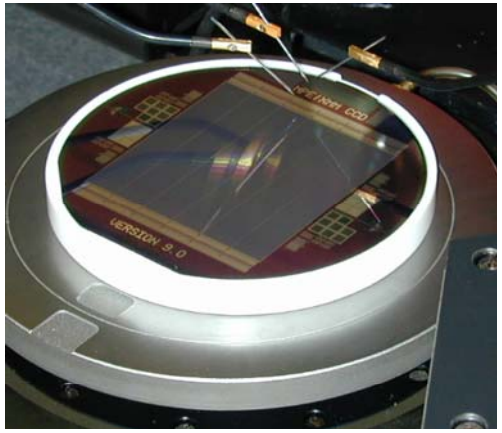
The MPI Semiconductor Laboratory (**H**alb**L**eiter**L**abor)

- Common Institution of the Max-Planck-Institutes for Physics and for Extraterrestrial Physics
- Founded in 1992, since 2000 at the Siemens Campus in Munich
- ~50 Scientists, Engineers, Technicians, Students

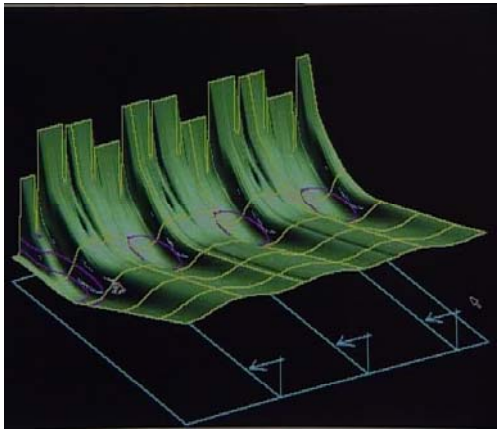
The MPI Semiconductor Laboratory (**H**alb**L**eiter**L**abor)

800 m² cleanroom up to class 1 … … with modern, custom made equipment …… for a full 6" silicon process line

mounting & bonding

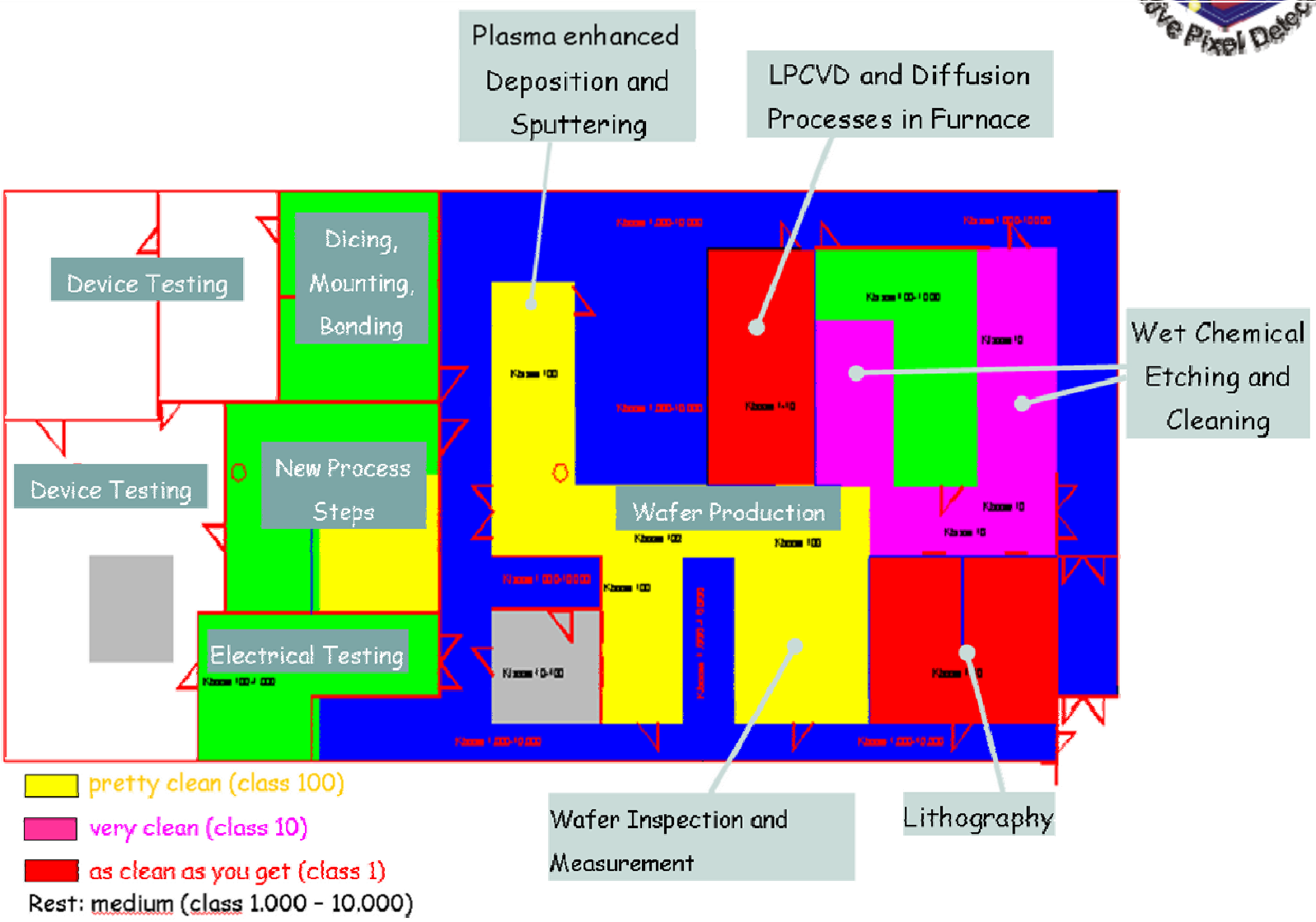


test & qualification



simulation, layout & data analysis

Inside the HLL



The Structure of the MPI HLL