First test of prototype ADC for LumiCal detector

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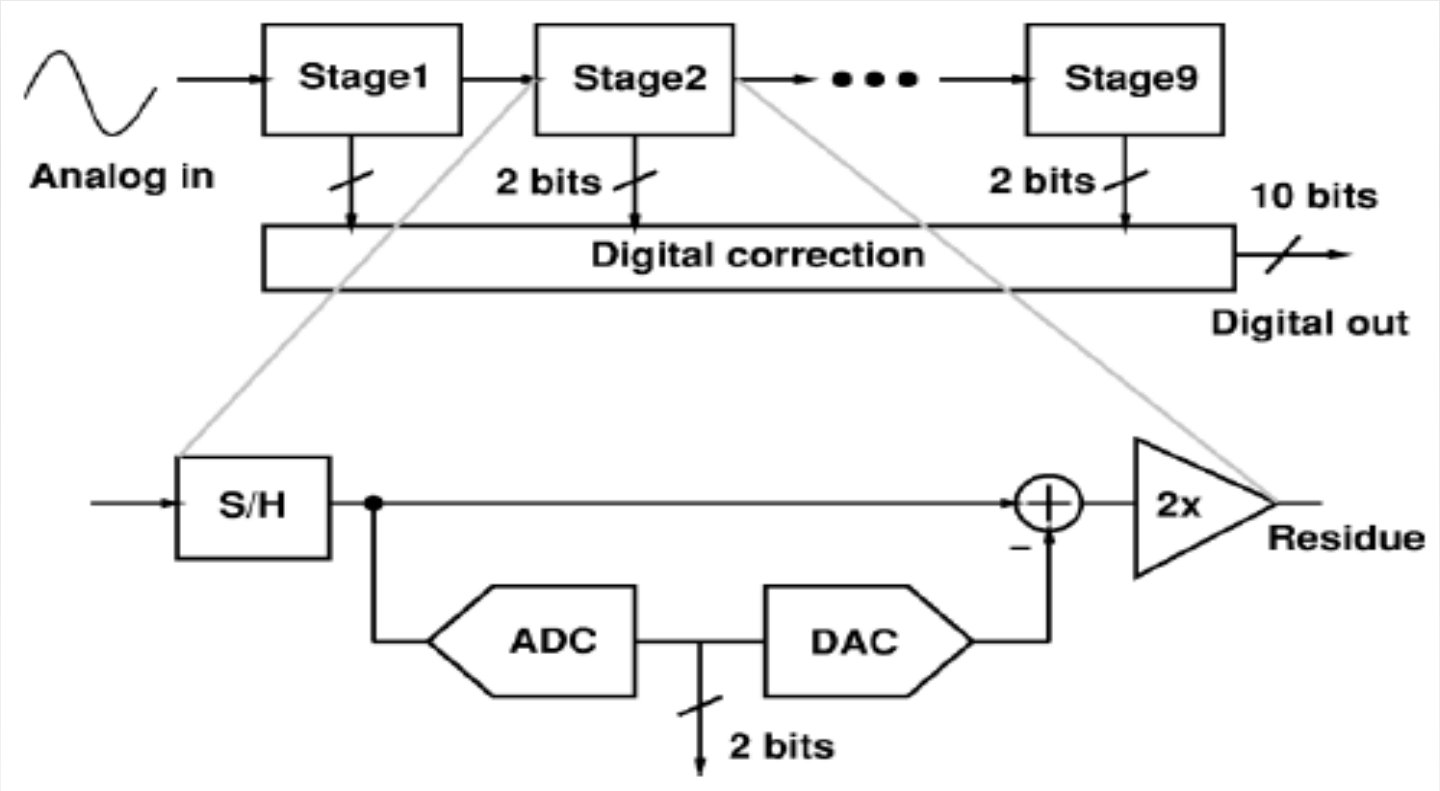
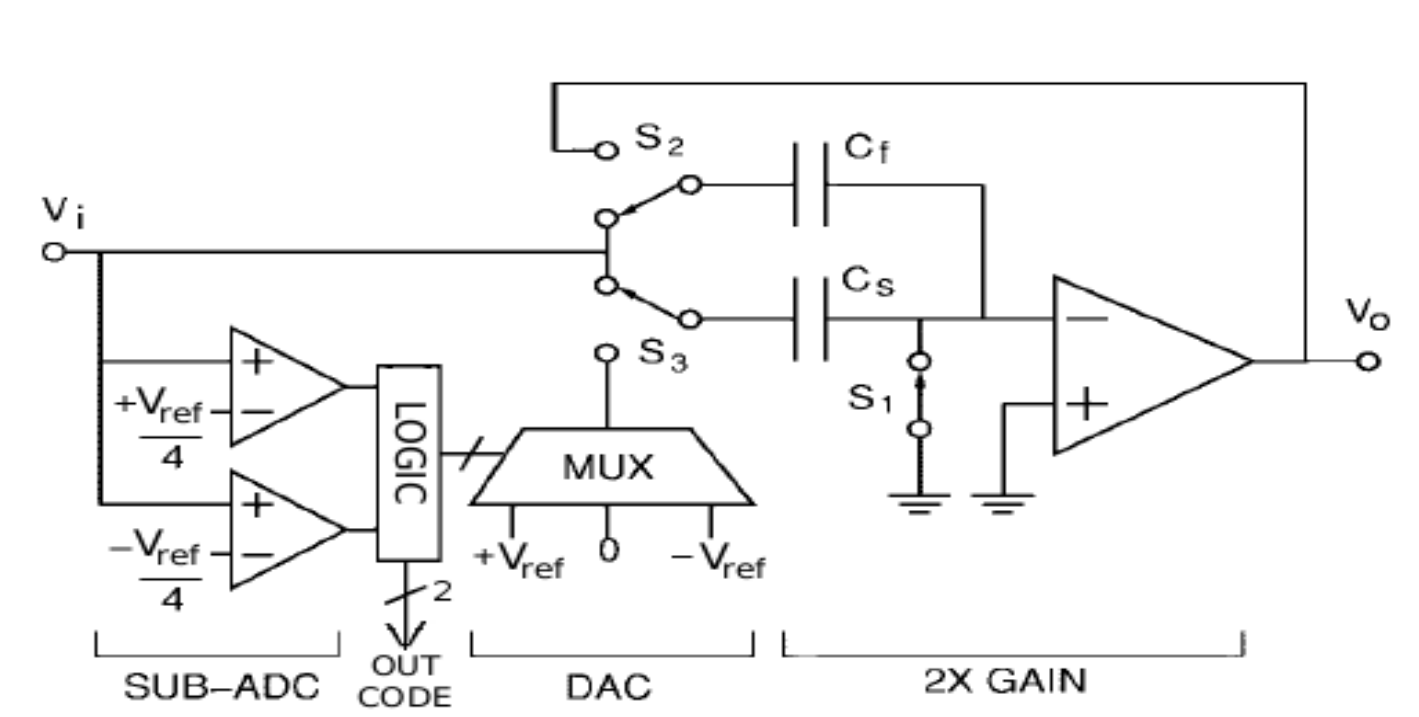
Pipeline ADC concept



Last stage is simplified

- 9 stages for 10 bit
- A stage produces 2 bits and multiplies signal by 2
- Digital correction relaxes comparator requirements

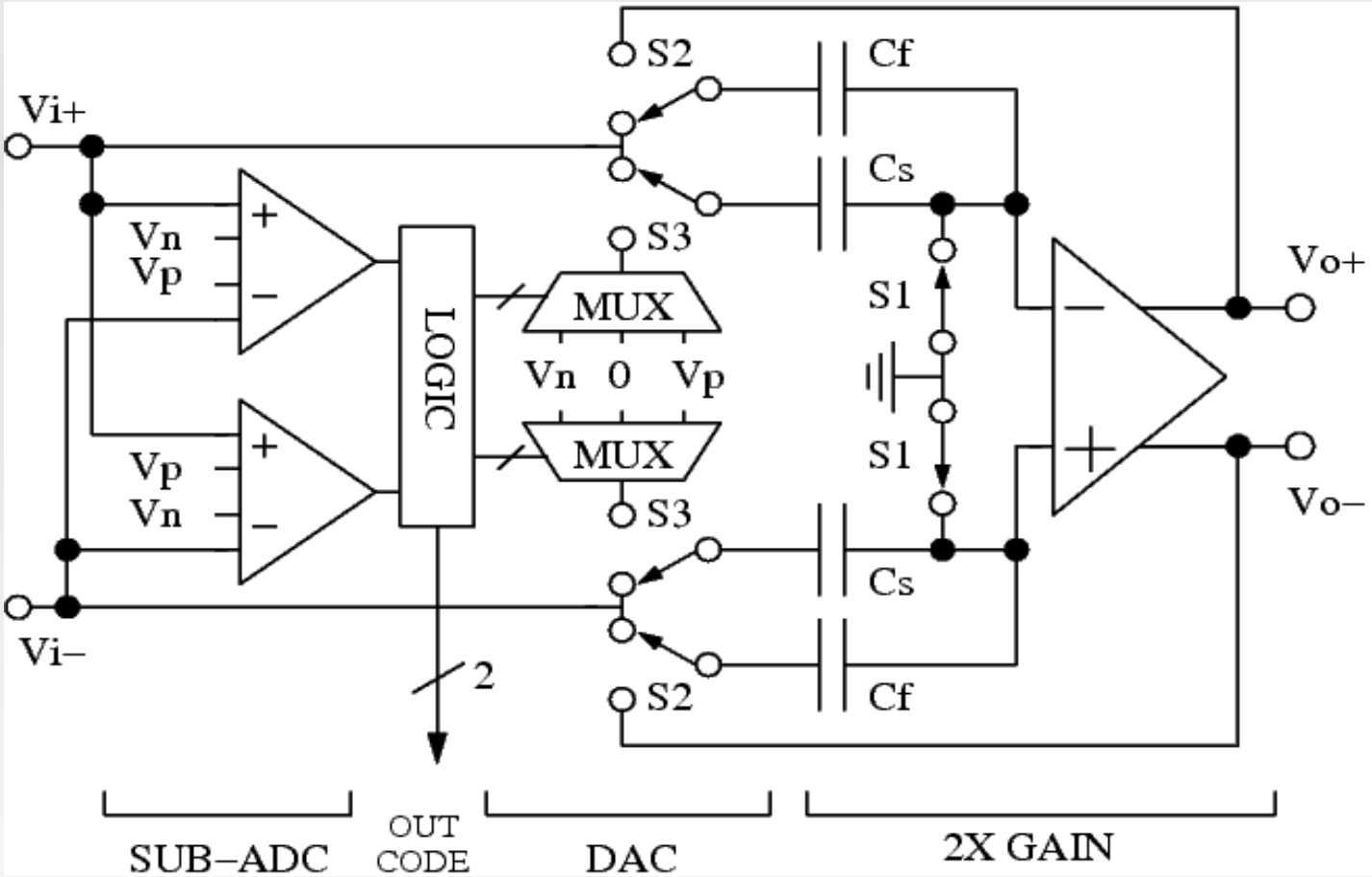
One 1.5bit stage



3 different output values coded on 2 bits: ***00, 01, 10*** so it is called 1.5 bit stage

- Switch capacitor circuit – needs clock
- Two phases:
  1) charging capacitors
  2) multiplication by 2 and subtraction

Fully differential implementation

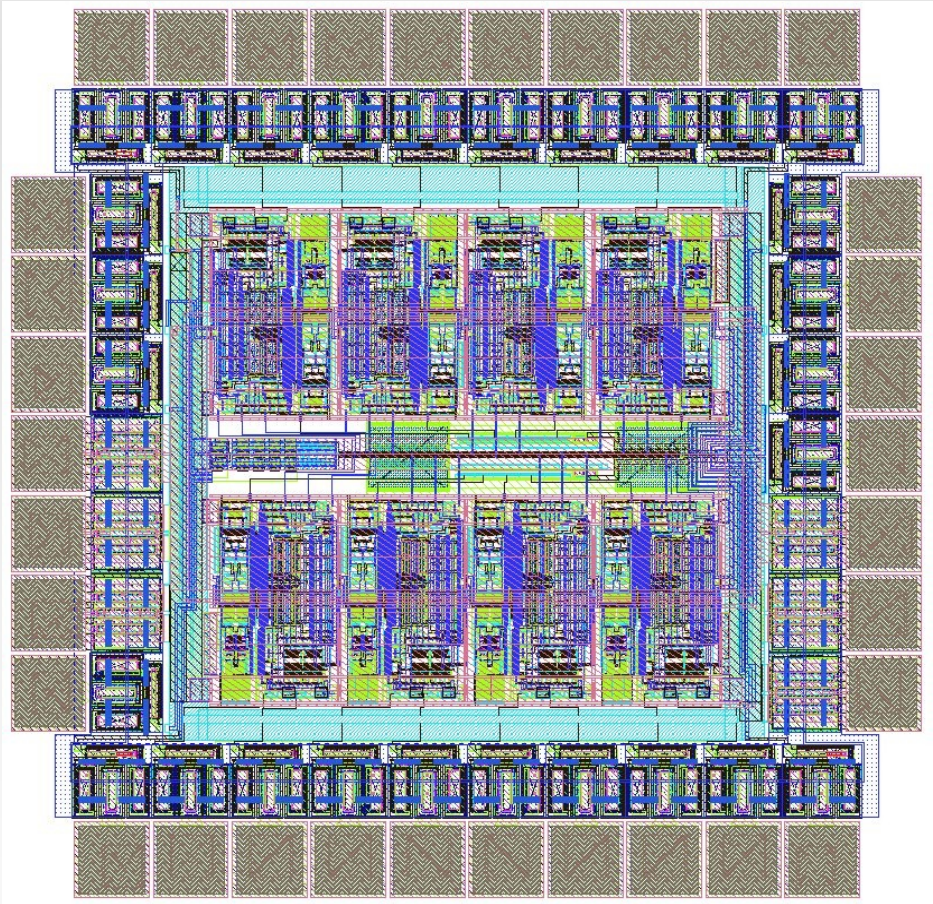


Doubled elements:
- capacitors
- switches
- MUXes

Differential elements:
- compar.
- amplifier

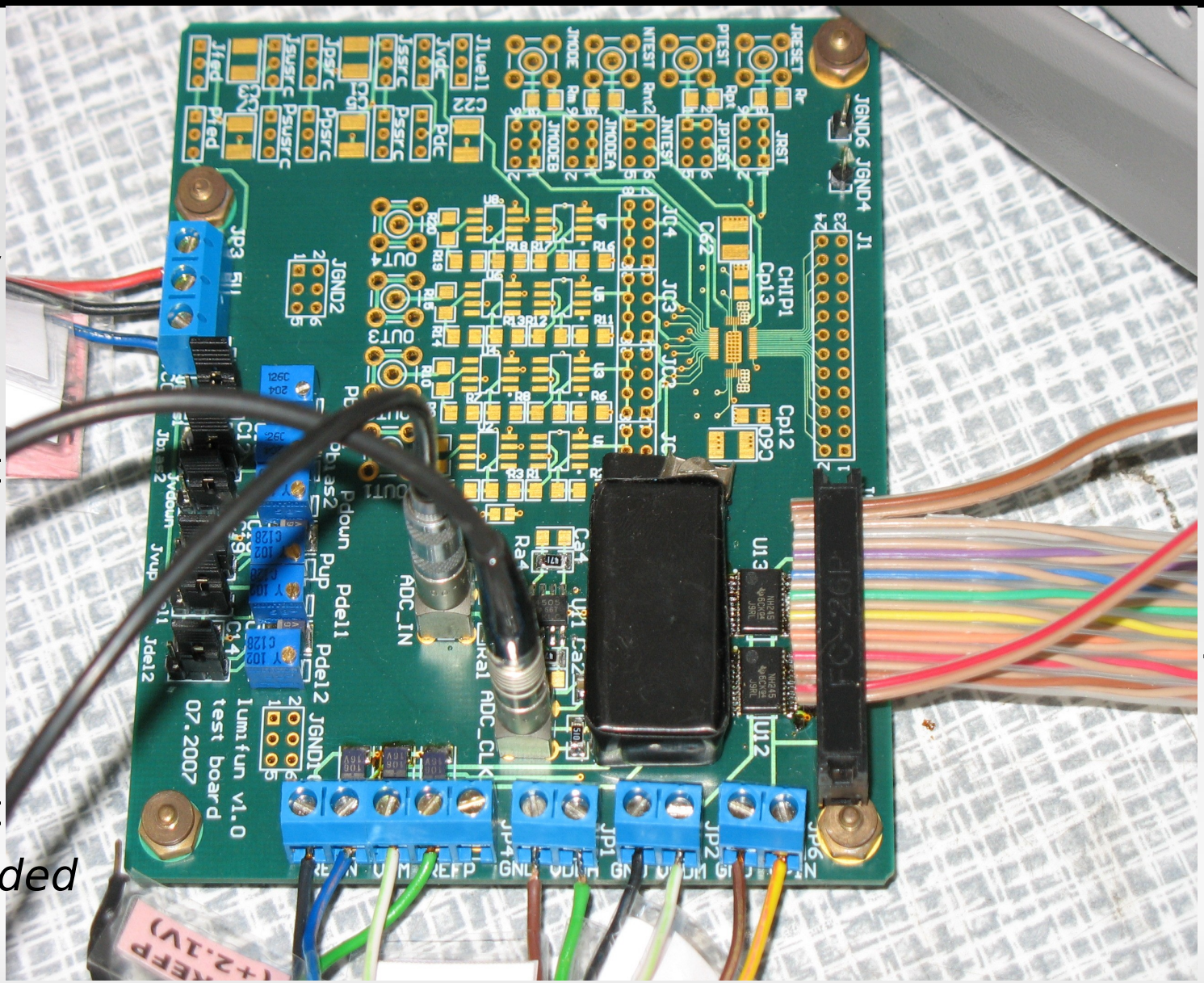
- Differential signal is not sensitive to disturbances from e.g. digital elements

First simple prototype



- submitted in June
- only 8 stages
- no digital correction in chip
- external biasing
- size 1.15x1.11 mm
- differential input

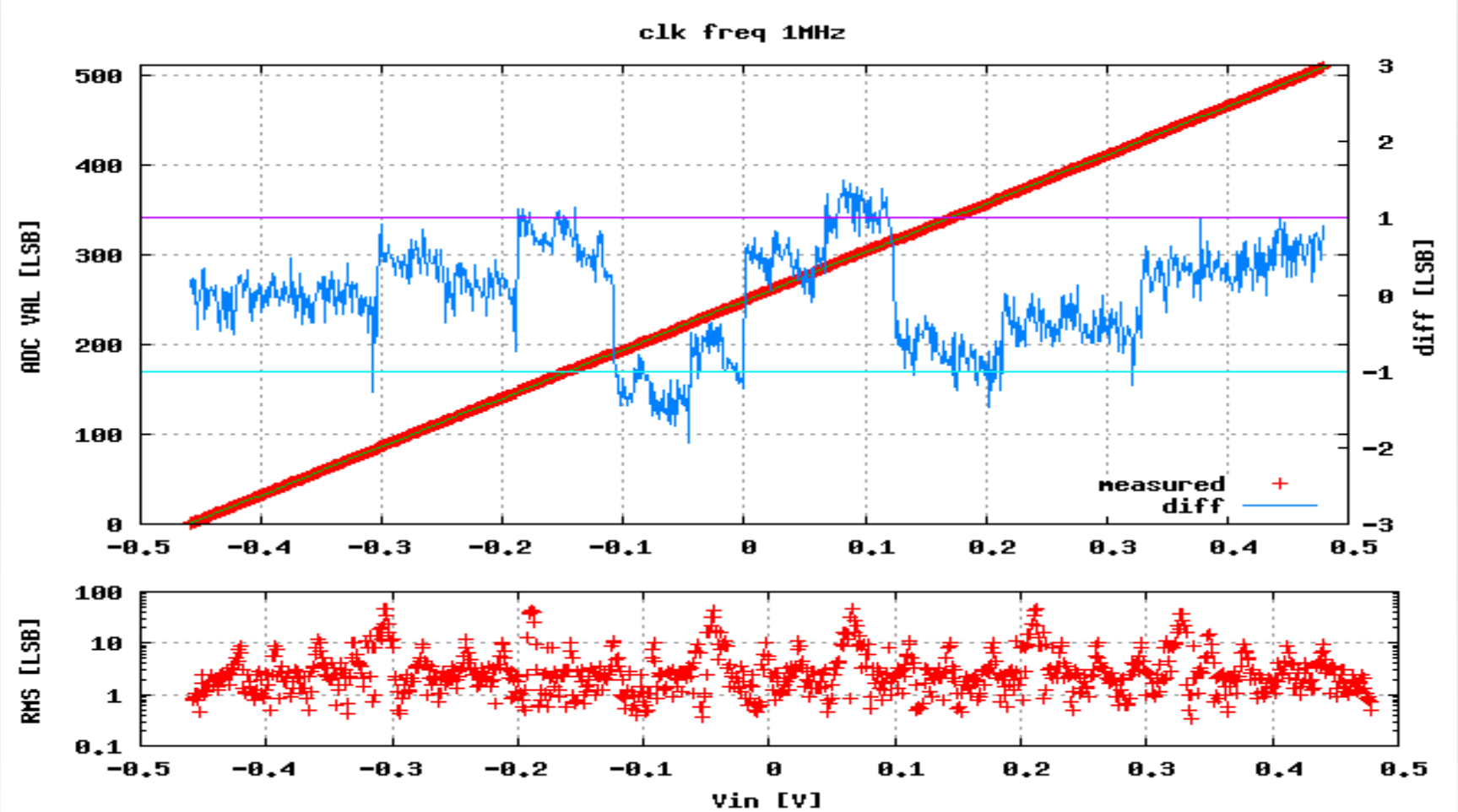
Printed Circuit Board



Test Setup

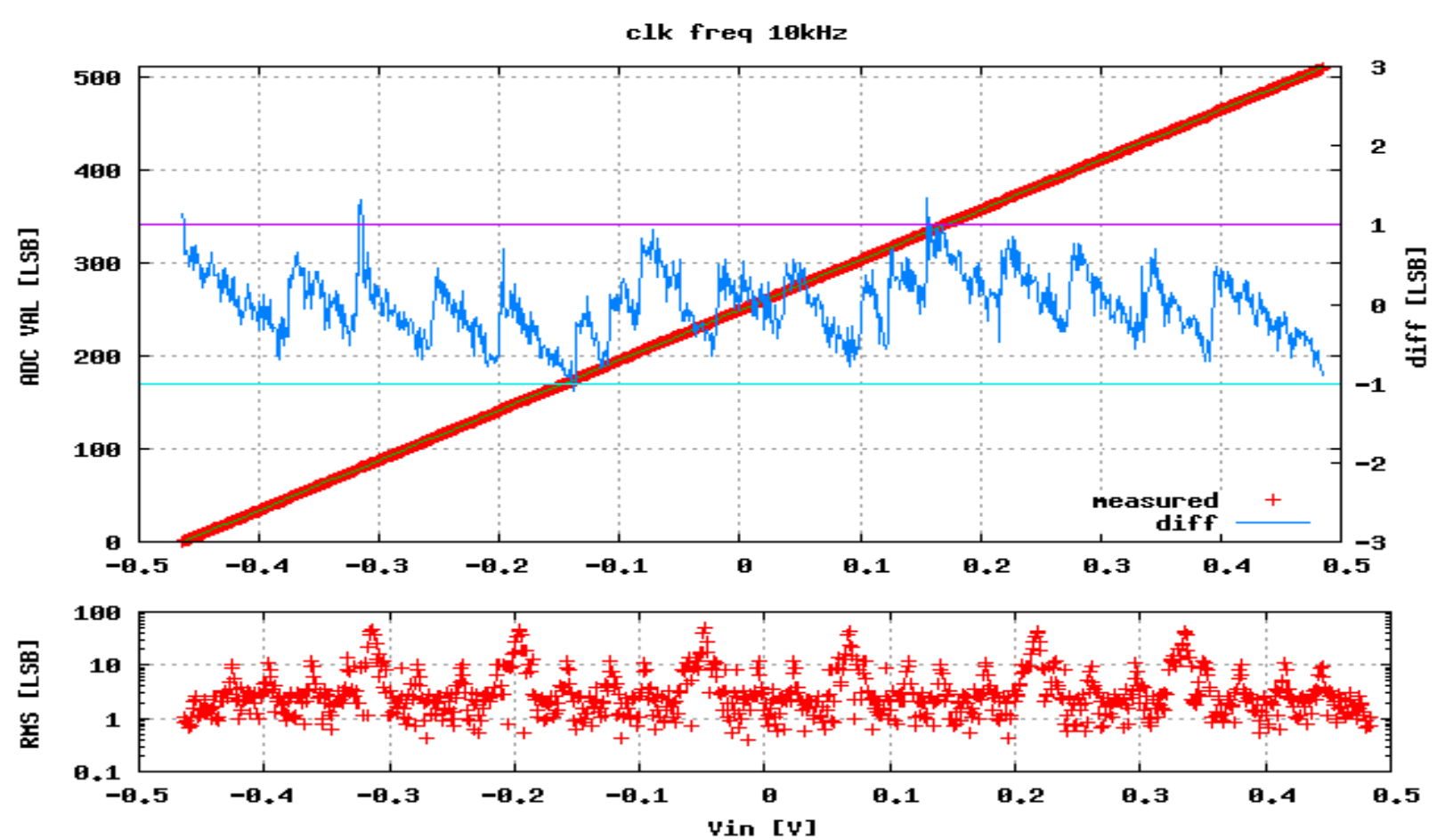
... during mesurement

Very preliminary results



- Static (DC) meas.
- Not proper ADC readout
- Fluctuations
- Average as a ADC out

Very preliminary results 2



- Other clk freq — other result ?!
- Timing problems but looks promising

Conclusions

- Very preliminary ADC measurement
- We have only look on static behaviour
- Results look promising but ...
- We need
  - improve DC test setup
  - make dynamic tests
  - measure ADC parameters