BeamCal Electronics Status

FCAL Collaboration Meeting
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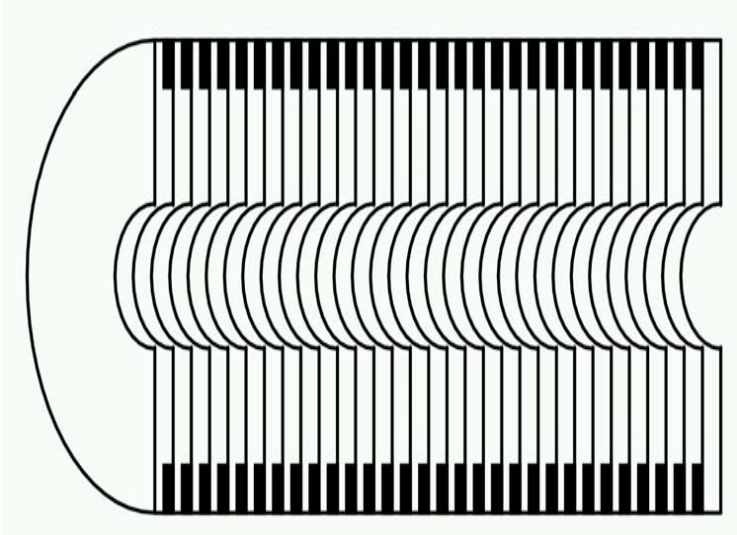
Presentation Outline

- The BeamCal detector
- BeamCal electronics challenges
- BeamCal electronics operation
- High level design
- Amplifier design
- Filter design
- ADC and memory issues
- Fast feedback design
- Radiation hardness requirements
- Tentative design schedule
- People

The BeamCal detector

- Mission:
  - To provide feedback for instantaneous luminosity tuning via beamstrahlung pairs
  - To extend the calorimeter hermeticity to the very forward region (low polar angles)

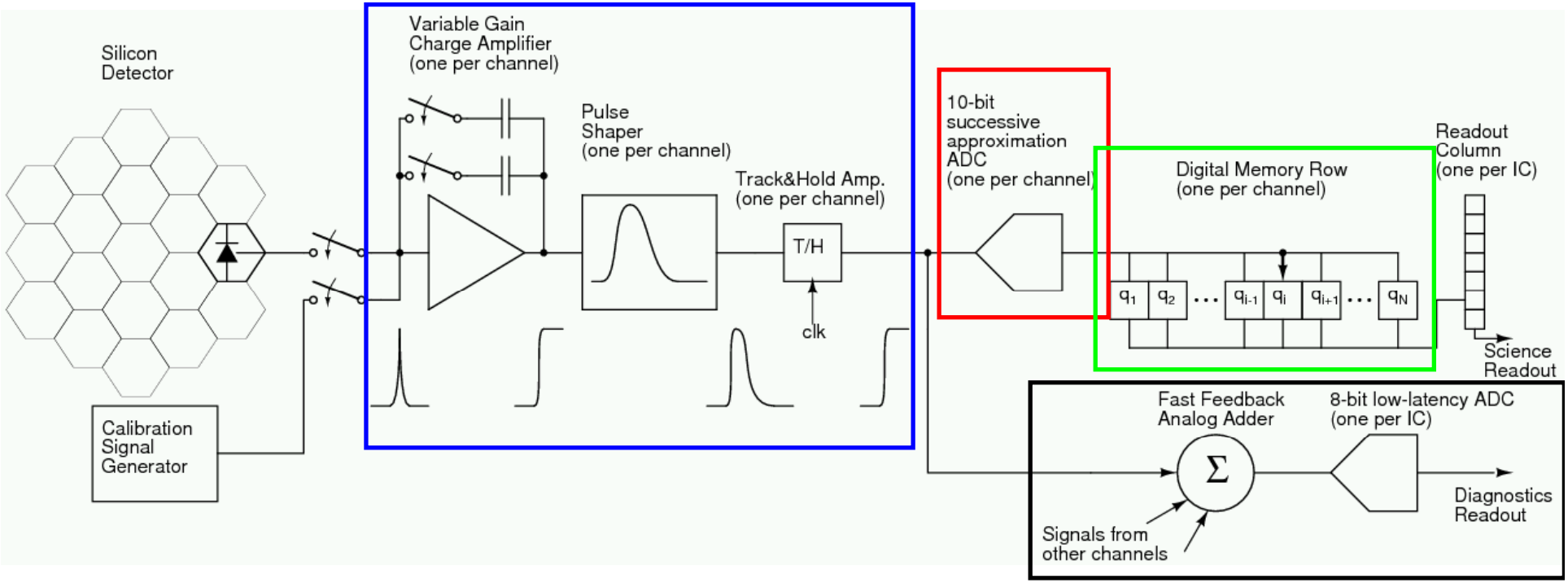


- BeamCal structure
  - 2 end caps ×
  - 30 Silicon – Tungsten sandwiched layers per cap ×
  - 1512 channels per layer
  - Total channel count: 90,720
  - At 32 channels per chip, this implies 2836 chips

BeamCal electronics challenges

- 32 channels per chip
- Large input signals, up to 40pC
- High occupancy, all data is read out at 10 bits for science purposes; gated reset is necessary
- Low latency output, sum of all channels is read out after each bx at 8 bits for beam diagnosis (fast feedback)
- Dual-gain front-end (50× ratio), for normal operation and physical signals calibration
- Radiation hardness requirements
- Parasitics due to 15-cm wires between detector and chip, detrimental for front-end performance
- Minimum power dissipation
- Prototype in 0.18-μm TSMC CMOS technology

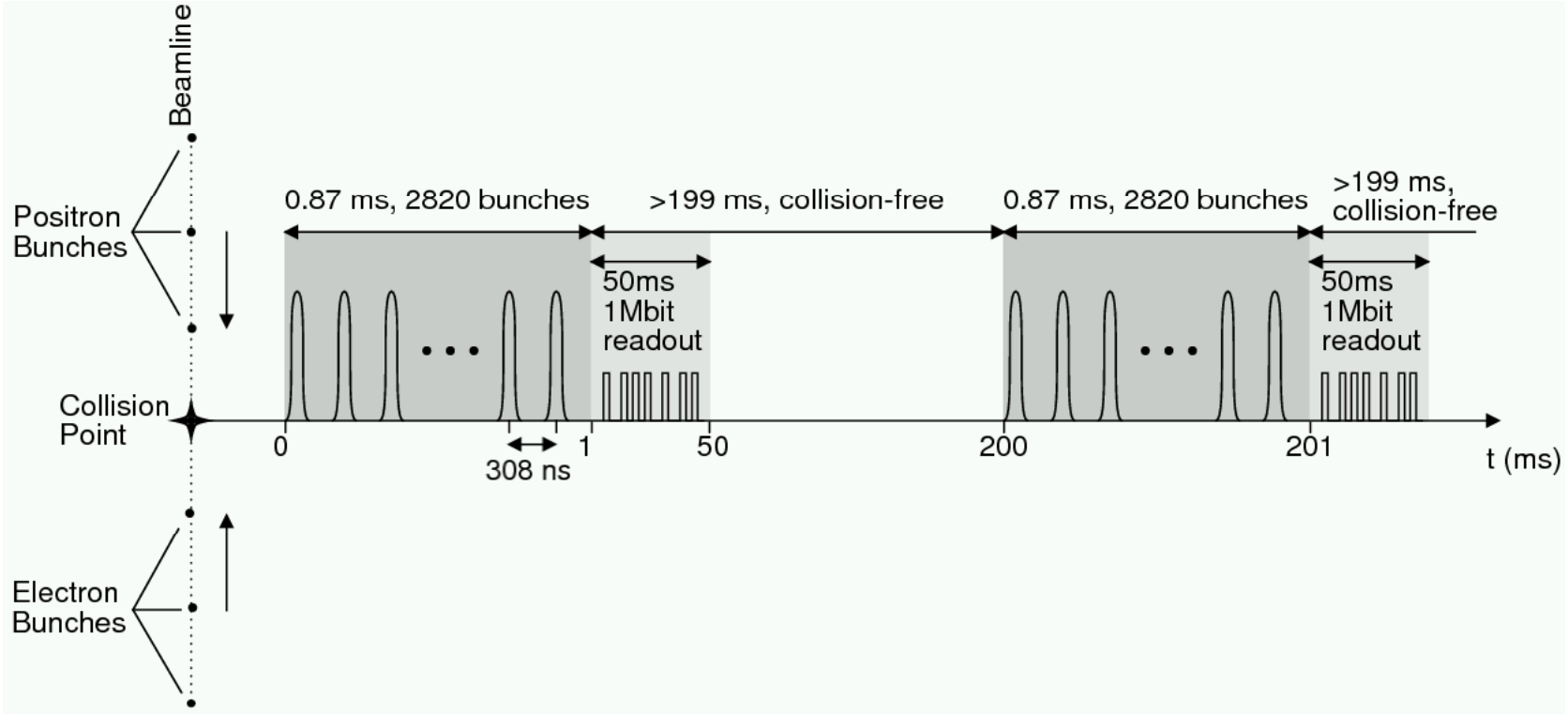
BeamCal electronics operation



- Dual-gain front-end electronics: charge amplifier, pulse shaper and T/H circuit
- Successive approximation ADC, one per channel
- Digital memory, 2820 (10 bits + parity) words per channel
- Analog addition of 32 channel outputs for fast feedback; low-latency ADC

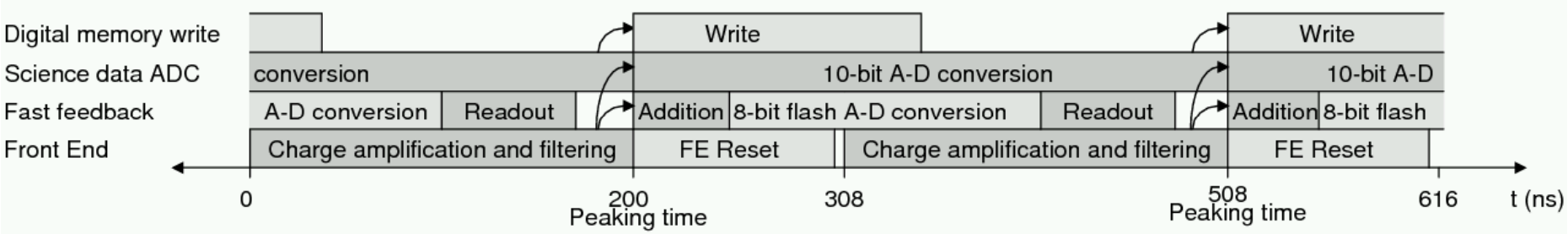
BeamCal electronics operation

Timing diagram: between pulse trains



BeamCal electronics operation

Timing diagram: between individual pulses



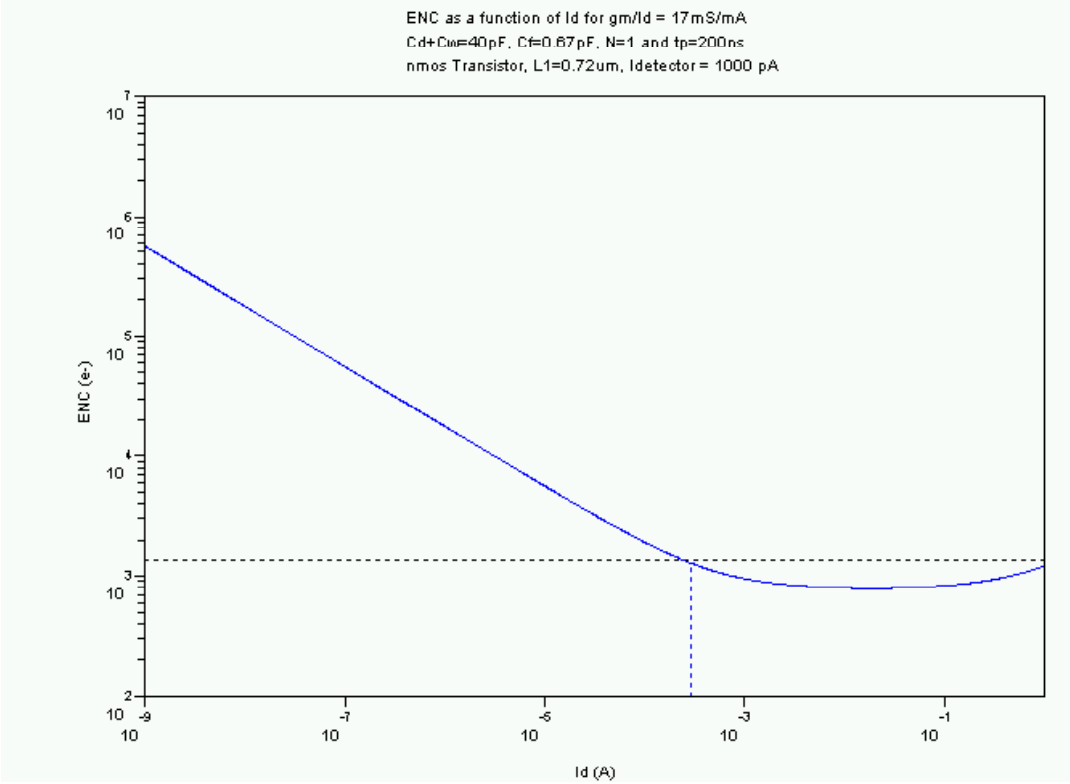
- Pipelined timing
- Exact timing could be mode-dependent

High level Design

- Behavioral simulations carried out to find:
  - Best architecture
  - Expected performance
  - Expected power consumption
- Conclusions
  - Charge amplifier current: about 300μA
  - Filter design: CR-RC (bandpass)
  - Peaking time: 200ns

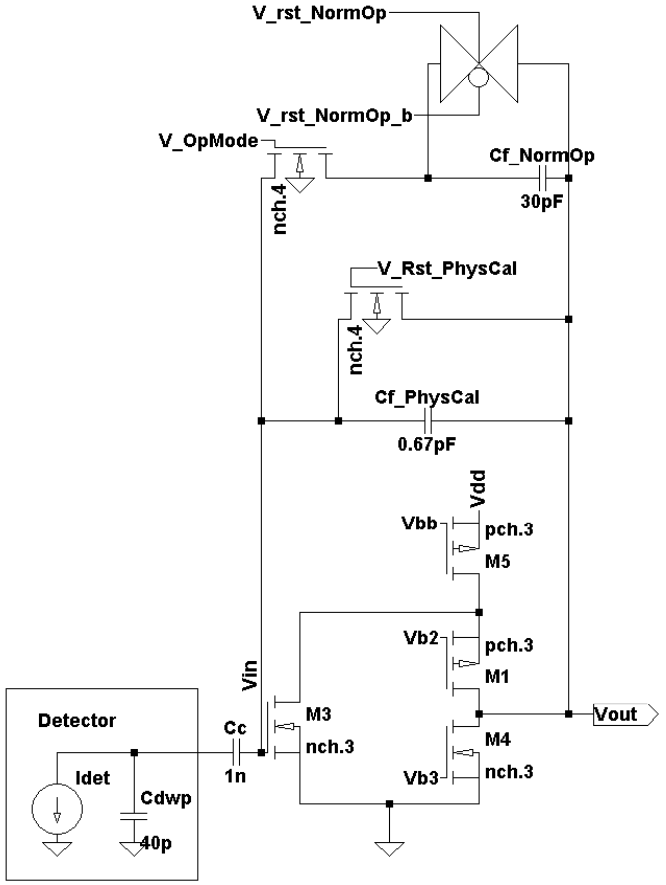
High level design

- Noise simulation, physics calibration mode



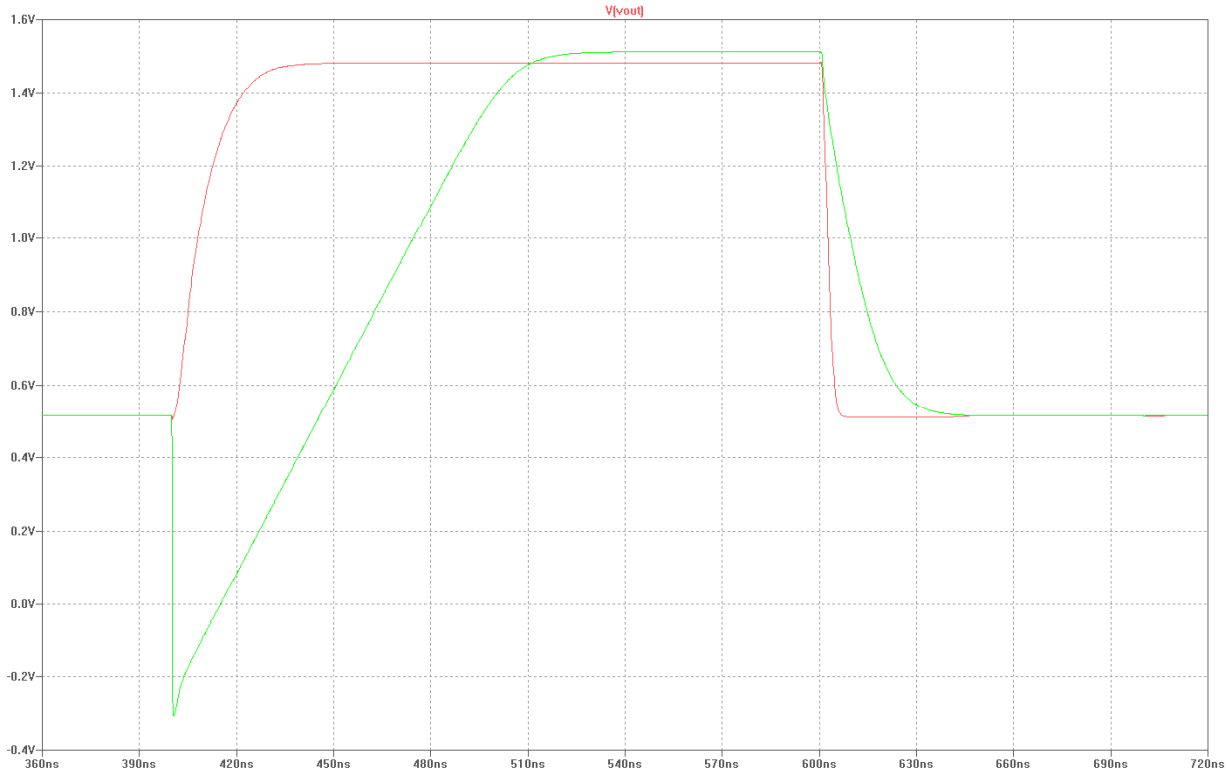
Amplifier design

- Basic charge amplifier – a voltage amplifier and capacitive feedback
- Low noise design (input transistor, gm/Id approach)
- NMOS input device
- Two feedback capacitors for different gains
- Switches for mode selection and reset
- 1-V output swing



Amplifier design

- SPICE output waveforms, normal operation and physics calibration

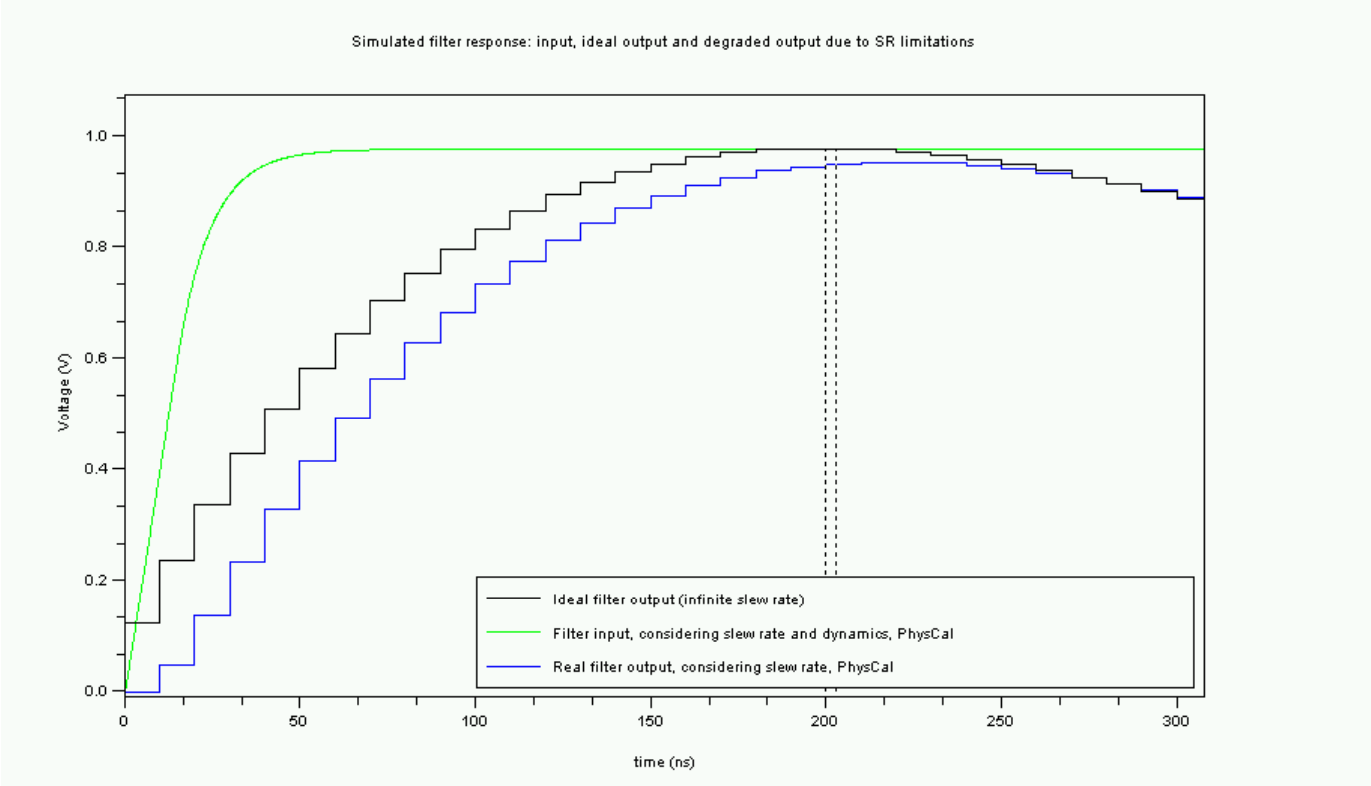


Filter design

- Filter domain
  - Continuous time: issues for τ calibration
  - Sampled time: precisely adjustable τ
- Filter topology
  - CR-RC: inadequate for gated reset
  - Biquad: perfect for gated reset
- Implementation details
  - Fully differential, switched-capacitor biquad implementation
  - Using SC inverting integrators (backward Euler integration)
  - Filters voltage across feedback capacitor – good PSR
  - 100MHz switching frequency does not affect frequency response in band of interest
  - 25MHz switching frequency does affect frequency response and requires an increase in charge amplifier current in order to meet noise specs

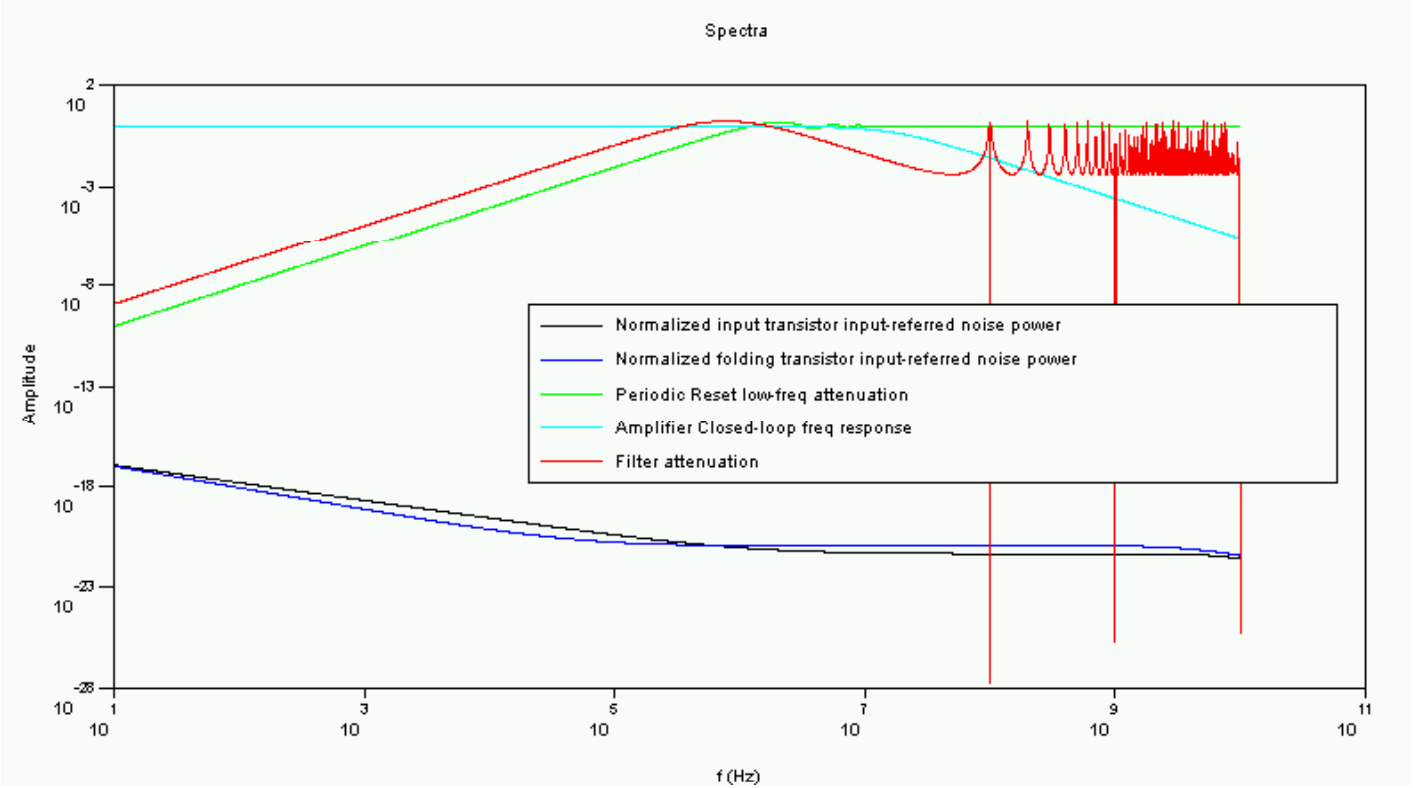
Filter design

- Filter output waveforms, behavioral simulation



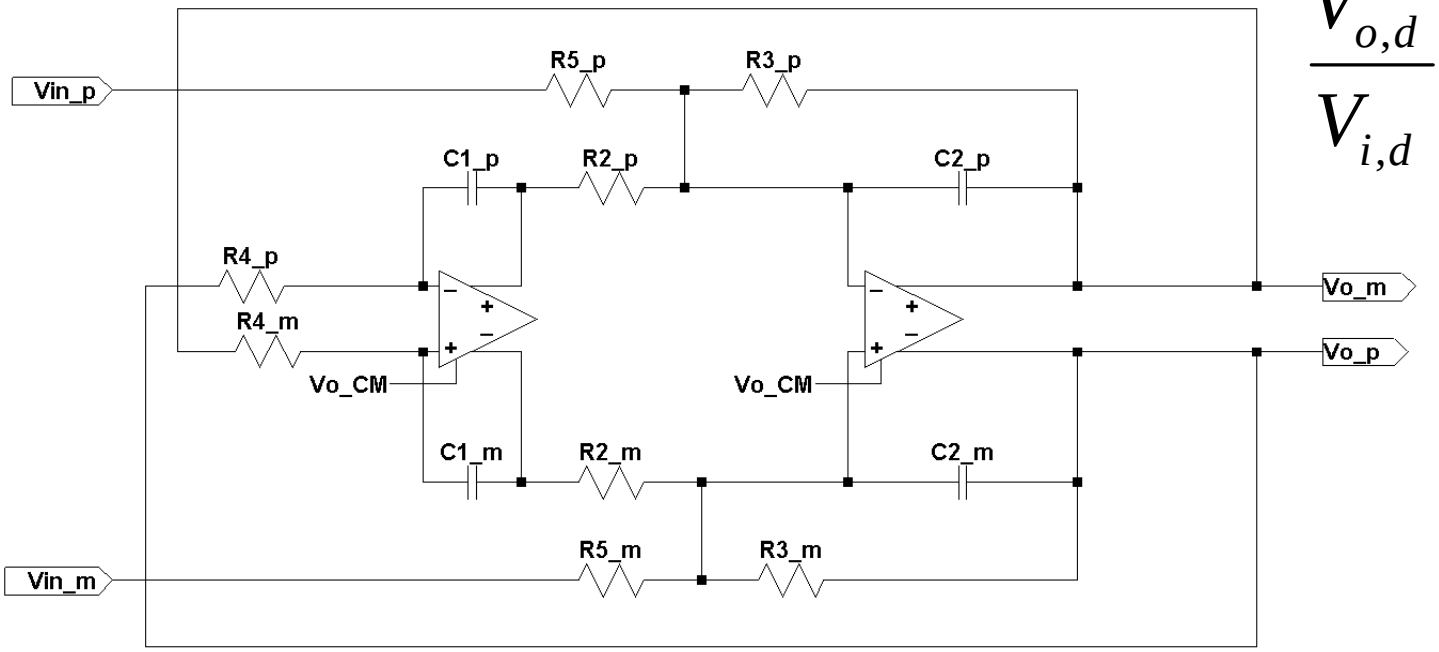
Filter design

- Amplifier and filter spectra



Filter design

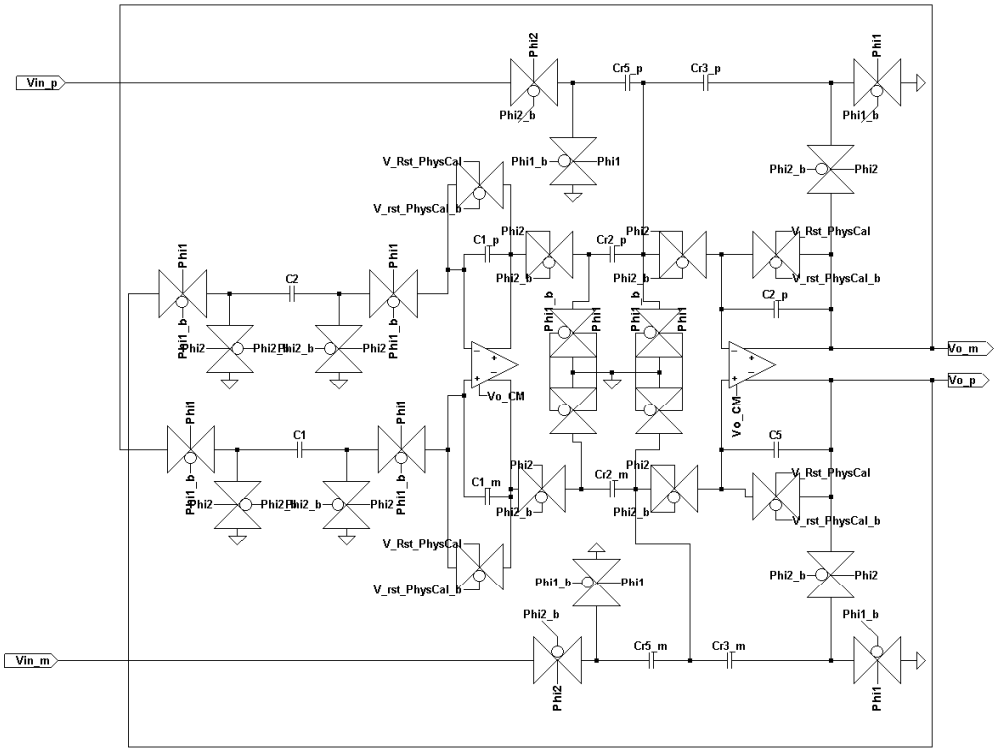
- Differential, continuous-time biquad…



$$\frac{V_{o,d}}{V_{i,d}} = \frac{A_0 s\tau_p}{\left(1+s\tau_p\right)^2}$$

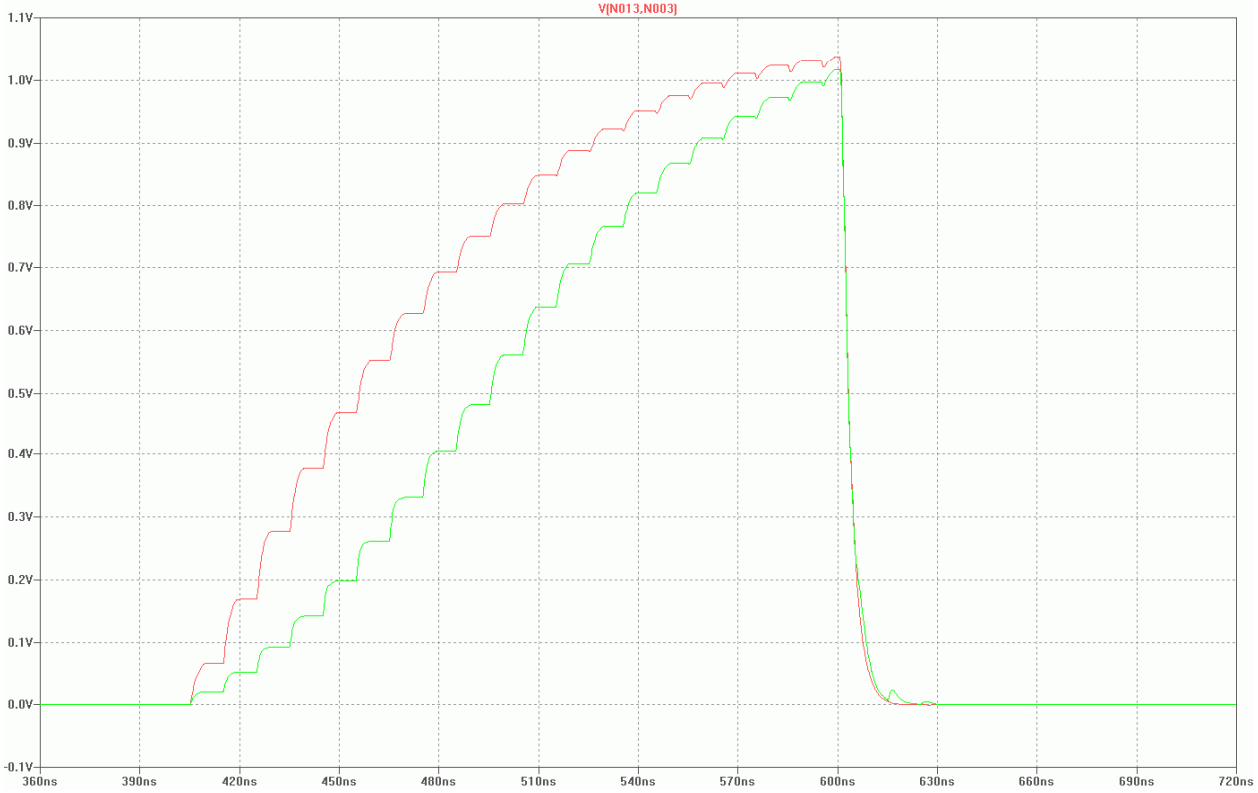
Filter design

- Conversion to SC + reset transistors



Filter design

- Output waveforms, normal operation and physics calibration

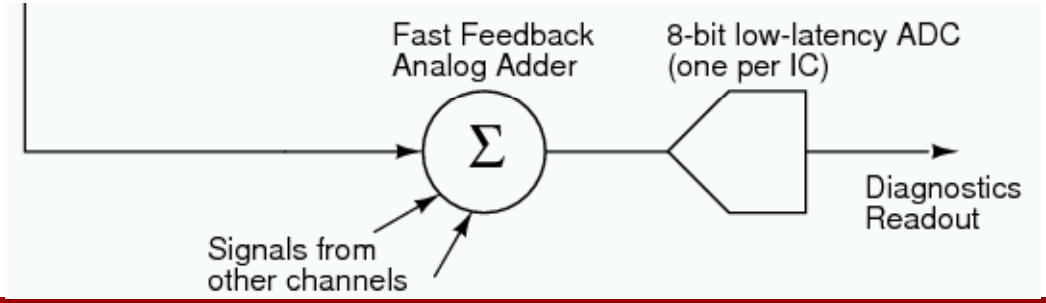


ADC and memory issues

- ADC power consumption is lightly dependent on the number of ADCs
  - one channel per ADC is simple in terms of operation
  - many channels per ADC are efficient in terms of area
  - successive approximation ADCs present a balanced tradeoff, could eventually assign a single channel per ADC without a significant increase in area
- Memory choice: analog or digital?
  - Analog memory problems:
    - high droop rate due to switch leakage in TSMC018 (especially after irradiation)
    - radiation-tolerance techniques are not simple nor flexible
  - Digital memory problems:
    - more area
  - Digital memory will be used mainly due to flexibility

Fast feedback design

- Each channel's analog signal is extracted at the track-and-hold circuit output
- Analog adder generates the chip fast feedback signal
- A fast (low-latency) ADC is used to produce the digital output



Radiation hardness requirements

- Chip must be able to tolerate 1Mrad(SiO_2) total ionizing dose (TID)
- TSMC018 is naturally tolerant to TID, but some sensitive circuits in the chip require additional protection
- This can be done by using mitigation techniques:
  - Enclosed-layout transistors
  - Guard rings
- Consequences in circuit design:
  - Power consumption increases by 2× or more, depending on the circuit
  - Chip area increases by 2.5× in some circuits
- First prototype will not be radiation-tolerant, but will allow to:
  - assess the technology tolerance to radiation
  - detect the most radiation sensitive circuits

Tentative design schedule

- April 2007: High level design complete
- July 2007: Charge amplifier designed
- October 2007: Filter designed
- January 2008: ADC designed
- February 2008: Memory designed
- March 2008: Fast feedback designed
- April 2008: Bias and supporting circuits
- July 2008: Circuit layout complete
- August 2008: Verification complete
- October 2008: Prototype ready
- January 2009: Prototype tests complete

People

- Angel Abusleme (PhD student)[2]
- Professor Martin Breidenbach[1]
- Dietrich Freytag[1]
- Gunther Haller[1]
- Professor Bruce Wooley[2]

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