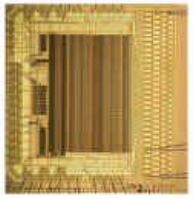
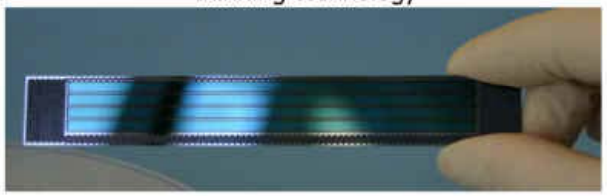
The DEPFET ILC VTX Project

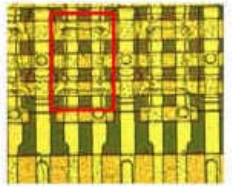
✓ steering chips Switcher



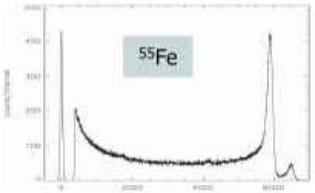
✓ thinning technology

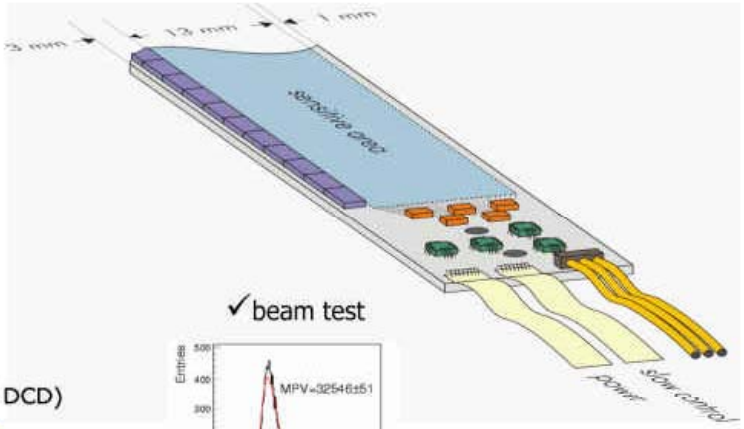


✓ sensor development

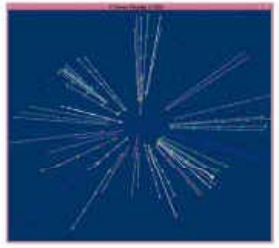


✓ radiation tolerance

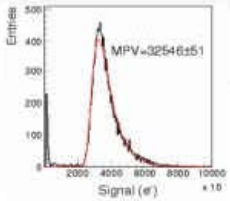




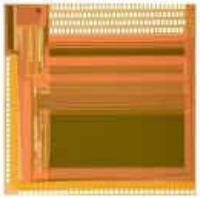
✓ Simulation



✓ beam test



✓ r/o chips (CURO & DCD)



See DEPFET Backup Document at www.depfet.org

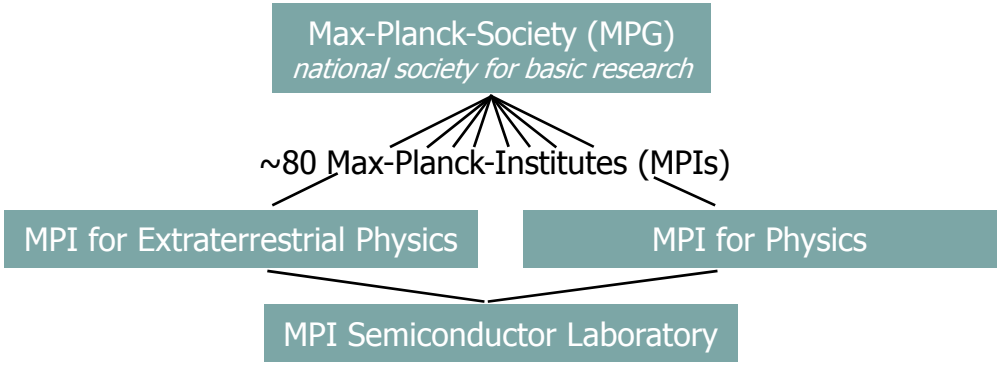
- Introduction of the DEPFET collaboration and MPI Semiconductor Laboratory
- DEPFET in a nutshell
- Current achievements
- Future Plans

- Work sharing in the collaboration

(www.depfet.org)

	DEPFET/Ladder Sim. and Irrad.	Auxiliary ASICs Development	System Development	System Tests and Test Beams
Aachen			X	
Bonn		X	X	X
Karlsruhe	X			
Mannheim		X	X	X
Munich	X			X
Prague			X	X
Valencia			X	X

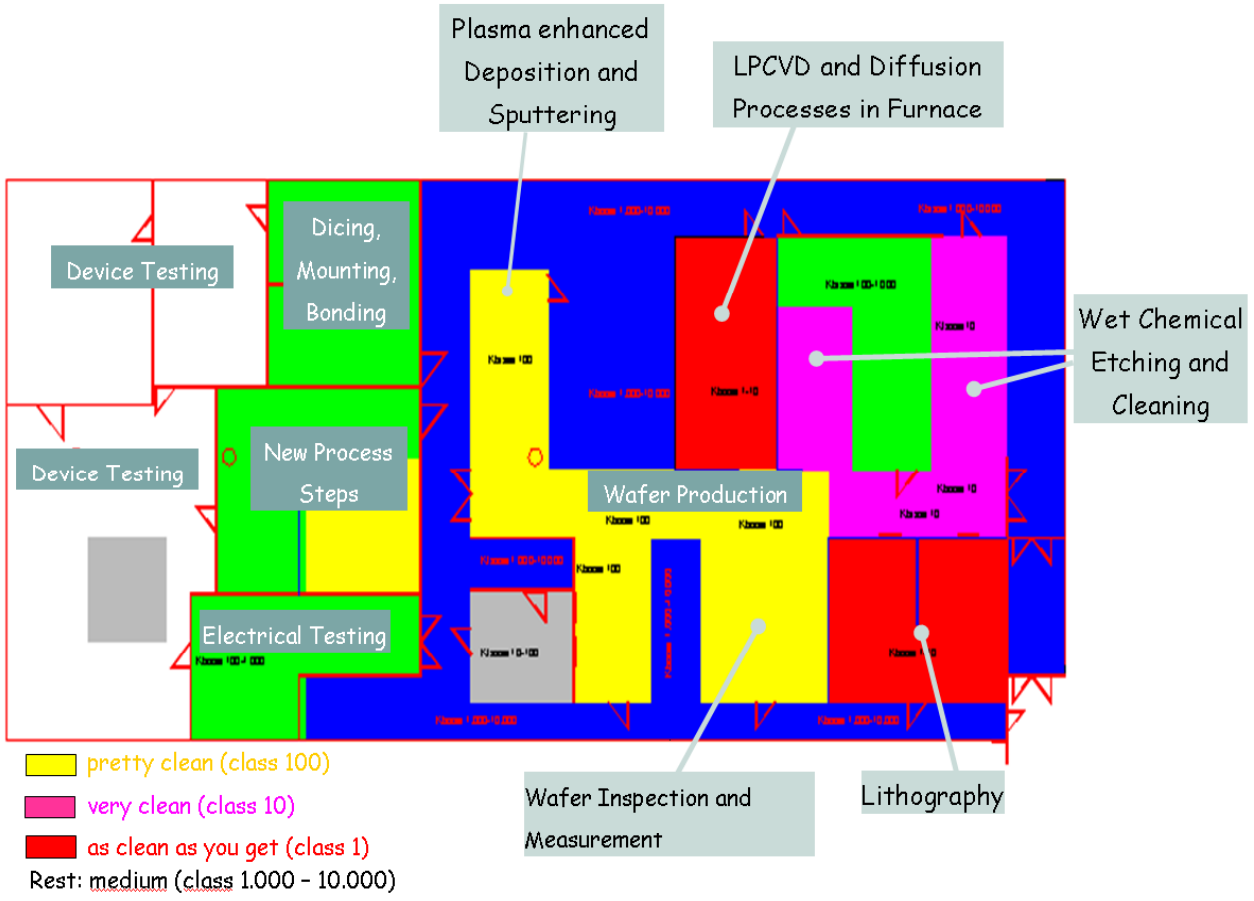
The MPI Semiconductor Laboratory (**H**alb**L**eiter**L**abor)



- Founded in 1992, since 2000 at the Siemens Campus in Munich
- ~60 Scientists, Engineers, Technicians, Students …. design, produce, and test …
- ..silicon detectors (CCD, APS, SiPM..) for experiments in HEP, X-ray astronomy, synchrotron radiation …

Inside the HLL

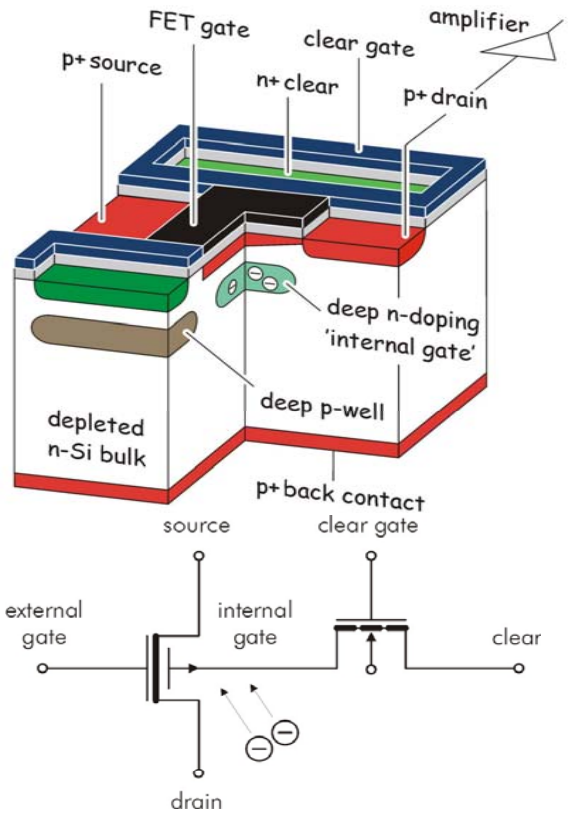
~ 800m^2 Clean room with a full 150 mm process line, including mounting, bonding, and test..

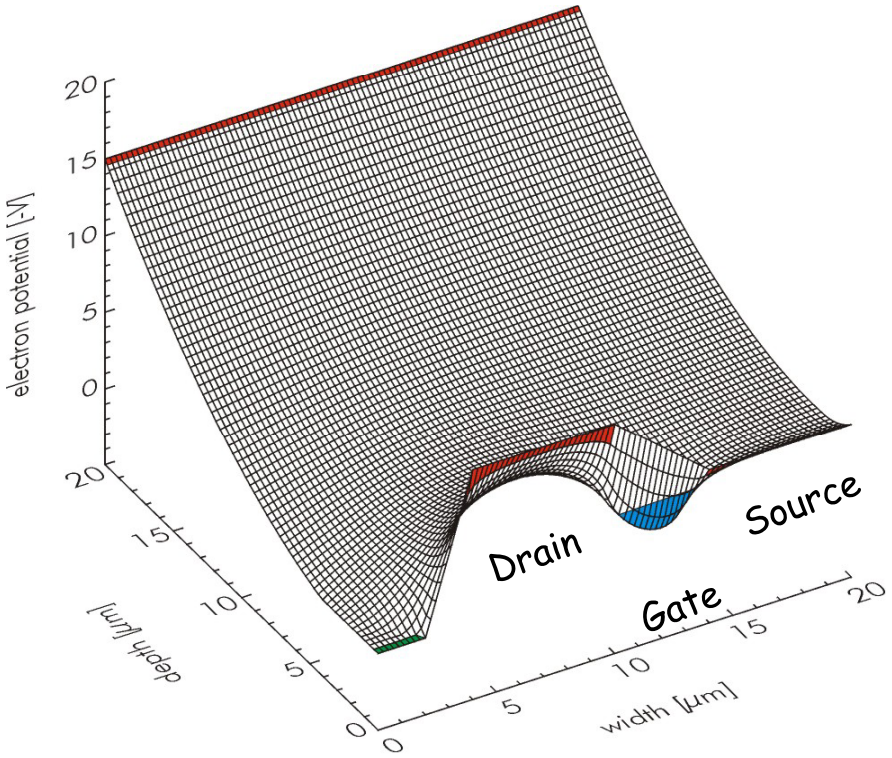


DEPFET Principle

J. Kemmer & G. Lutz, 1987

DEpleted P-channel FET

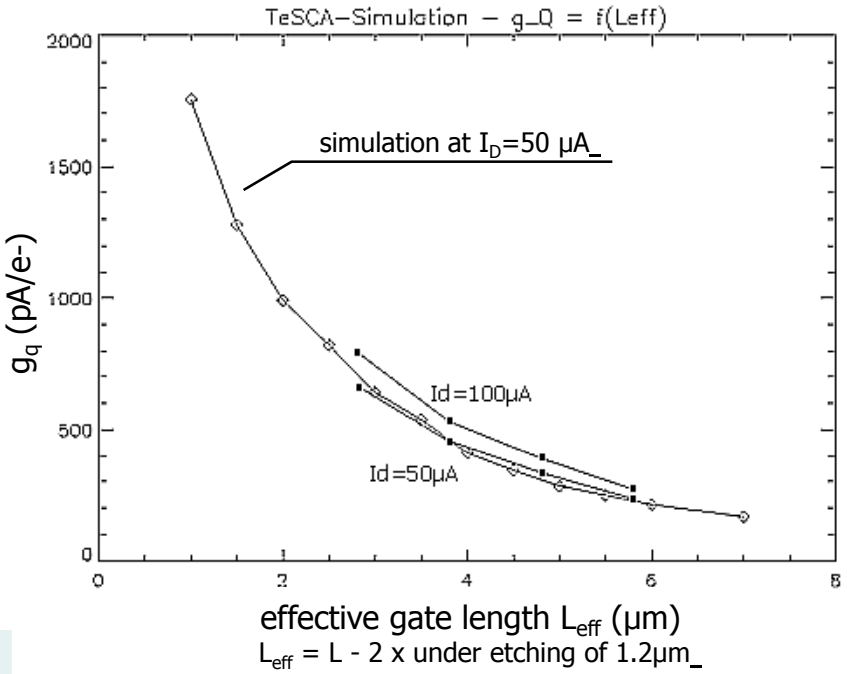


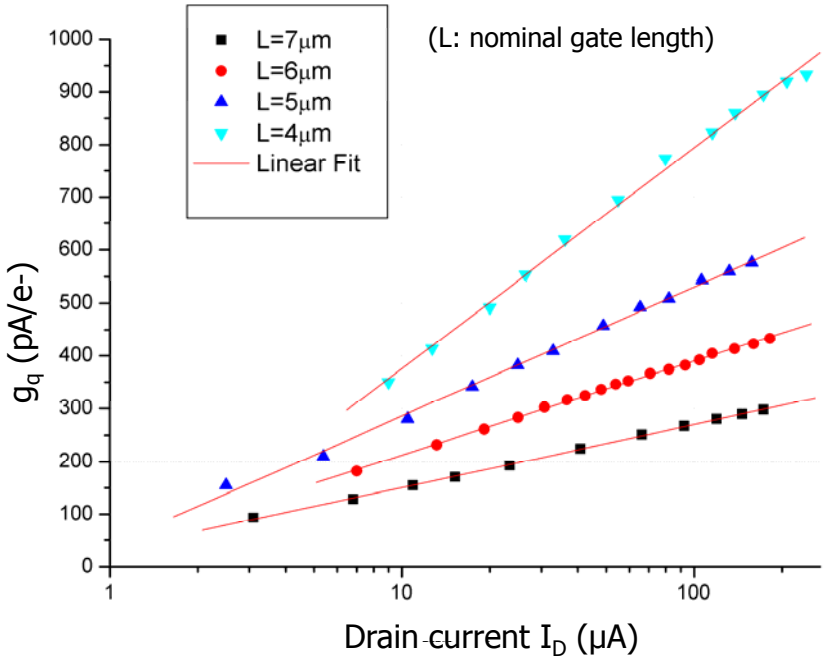


- fully depleted sensitive volume, charge collection by drift
- Charge collection in "off" state, read out on demand
- internal amplification → q-I conversion, scales with gate length and bias current

Internal amplification g_q

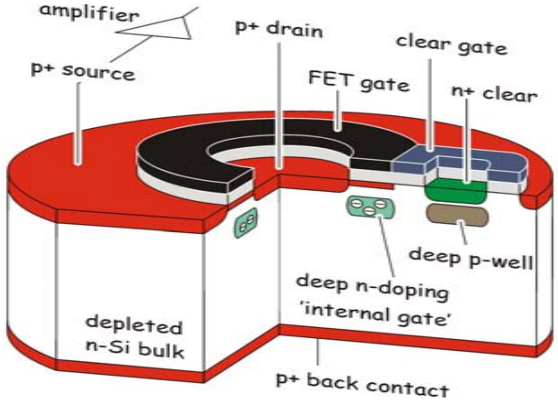
$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)





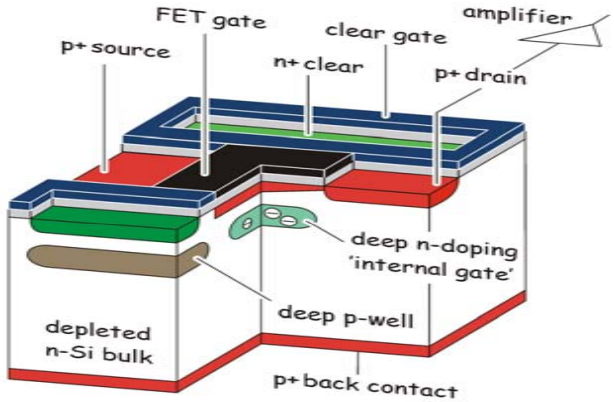
As long as noise is dominated by r/o chip → S/N linear with g_q

Overview: Types and Applications



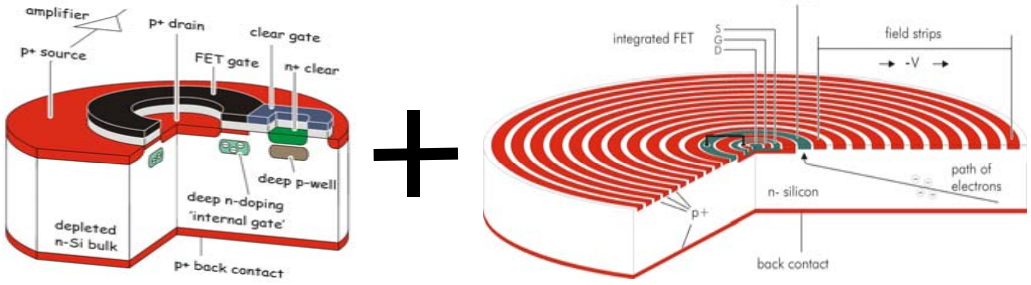
X-ray imaging spectroscopy → XEUS

- pixel size: 100µm
- r/o time per row: 2.5 µs
- Noise: ≈4 el ENC



Particle tracking → vertex detector at ILC

- pixel size: 24µm
- r/o time per row: 25 ns
- Noise: ≈100 el ENC
- thin detectors: ≈50µm

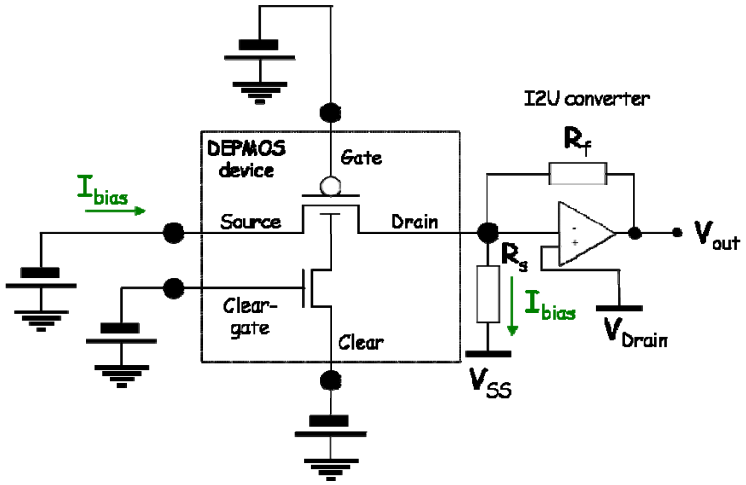


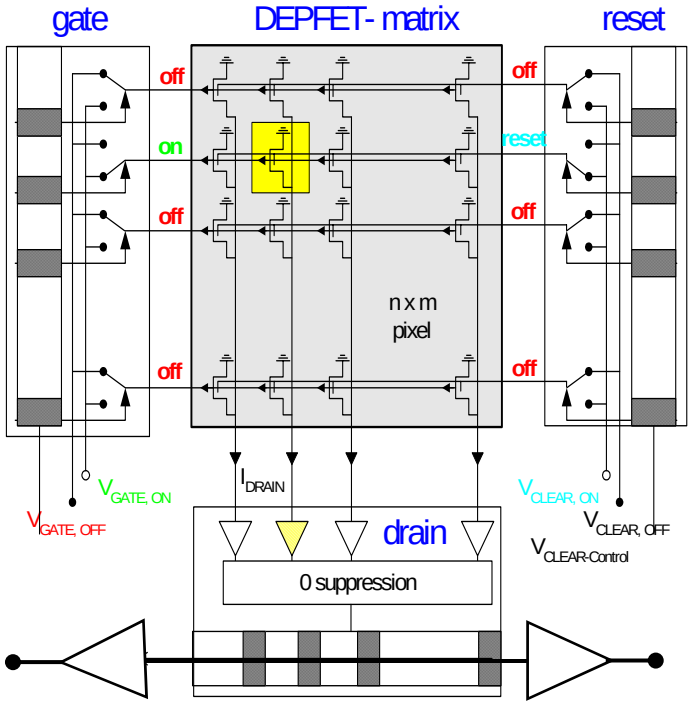
DEPFET MacroPixel
X-ray (imaging) spectroscopy
→ BepiColombo, SimbolX

- pixel size: 100s of µm

DEPFET Array - read-out at the ILC

Drain read out

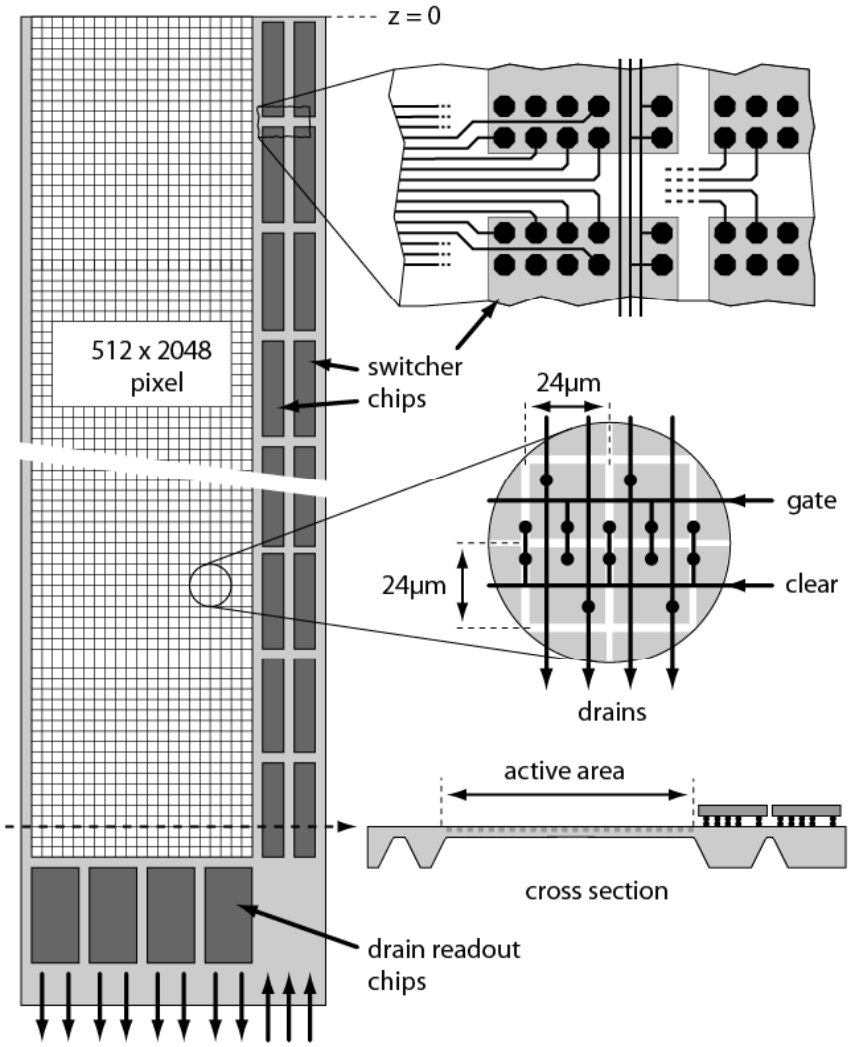




Row wise read-out ("rolling shutter")

- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal
- Low power consumption
- two different auxiliary ASICs needed
- limited frame rate
- cap. load at the f/e adds noise

ILC VXD baseline design



Just as a starting point for the R&D!

- 5 layer, old TESLA layout
- 10 and 25 cm long ladders read out at the ends
- 24 micron pixel
- design goal 0.1% X_0 per layer in the sens. region

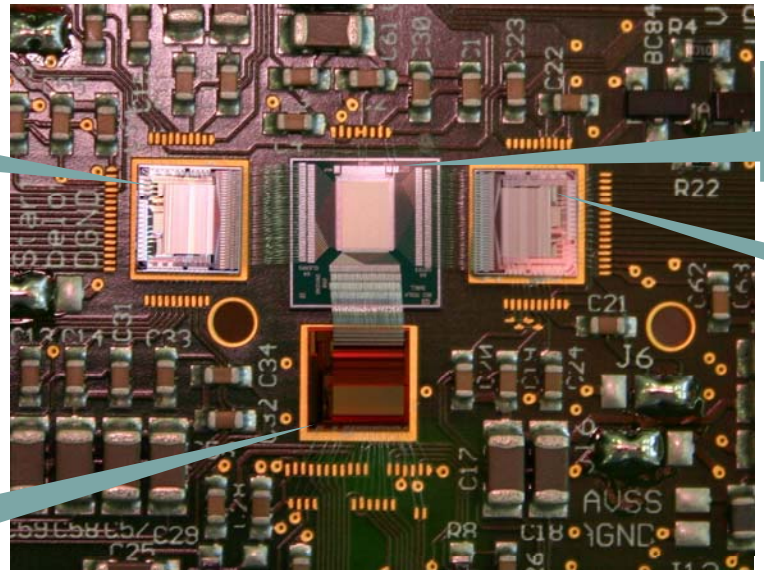
Strategy to cope with the background:

- read ~20 times per train
- store data on ladder
- transfer the data off ladder in the train pause

  → row rate of 40 MHz
- read two rows in parallel, doubles # r/o channels but:

→ row rate 20 MHz ☺

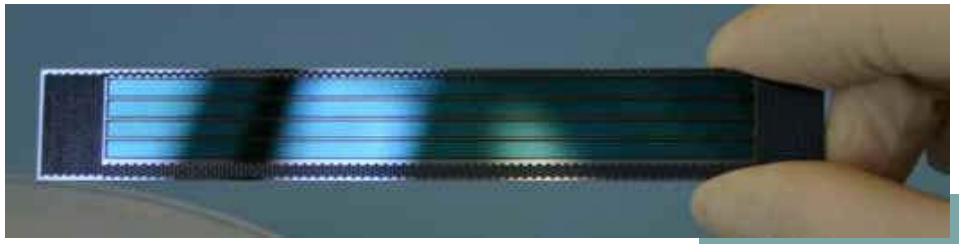
ILC Prototype System

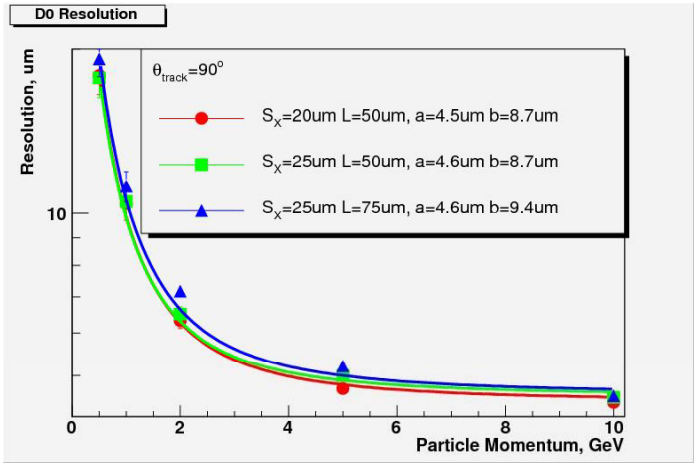


- ✓ current based 128 channel readout chip
- ✓ 50 MHz band width in the f/e
- ✓ On-chip pedestal subtraction by switched current technique (CDS)

- ✓ 2 analog MUX outputs with
- ✓ 64 channels each
- ✓ Can switch up to 25 V
- ✓ 0.8µm AMS HV technology

In Summary: Achievements





- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
  - ✓ S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2
- ✓ Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.

- ✓ Production of 2nd iteration of DEPFETs was finished summer 2007
- ✓ New Switcher3 chips tested and functional
- ✓ New r/o chips DCD designed for read-out of large matrices are under test

The challenge: read-out speed in long ladders!

1. Row wise read-out

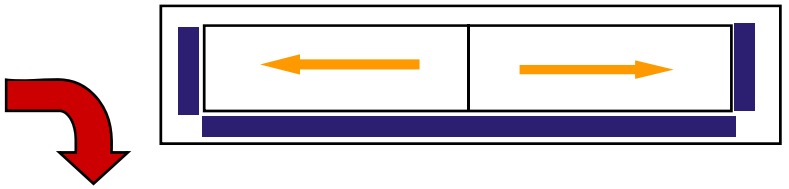
- row wise CDS with the r/o chips at the short side of the ladder

Advantage

- Low power consumption!
- No advanced interconnection technologies needed

Disadvantage

- limited frame rate
- high capacitive load (long drain lines) at the input



3. Combination of those two

- subdivide large arrays into smaller units
  - → smaller cap. load
  - → more relaxed row rate
- challenging interconnection (→"3D"?)

→ find optimum for a specific application balancing the pros and cons

under consideration for the **ILC VXD**

2. Hybrid-pixel-like approach: one amp. per pixel

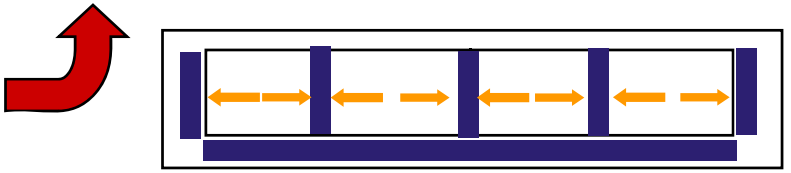
Advantage

- fast! (~ns), frame rate comparable with hybrid pixels

Disadvantage

- challenging interconnection between sensor and r/o chip
- high power consumption

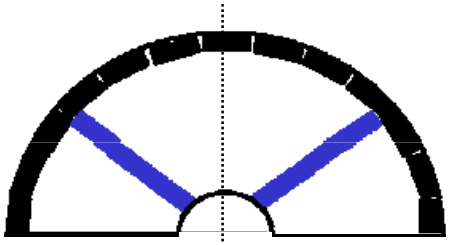
intended for the focal plane at the **XFEL**



Reasons…

Why SiD VXD layout for the DEPFET?

- Main difference is long barrel ←→ short barrel with endcap
- in layers 2..5: 25 cm ladder → 12.5 cm ladder
- lower C_{load} at the input, relaxed speed requirements in these layers



R_{in}= 14 mm, R_{out} =71mm

Why DEPFET for the SiD?

- wafer scale sensors (150 mm) in barrel and discs
- 1 ladder/wafer or ½ or ¼ disc per wafer, no stiching needed
- thinned all-silicon ladders or discs with or without supporting frames
- DEPFET is an active pixel sensor, first amplification in pixel → good candidate for 3D integrated detector systems.
- MacroPixels (DEPFET + Drift Detector) could be a natural extension of the VXD technology into a pixelated tracker…

Potential Issues …….

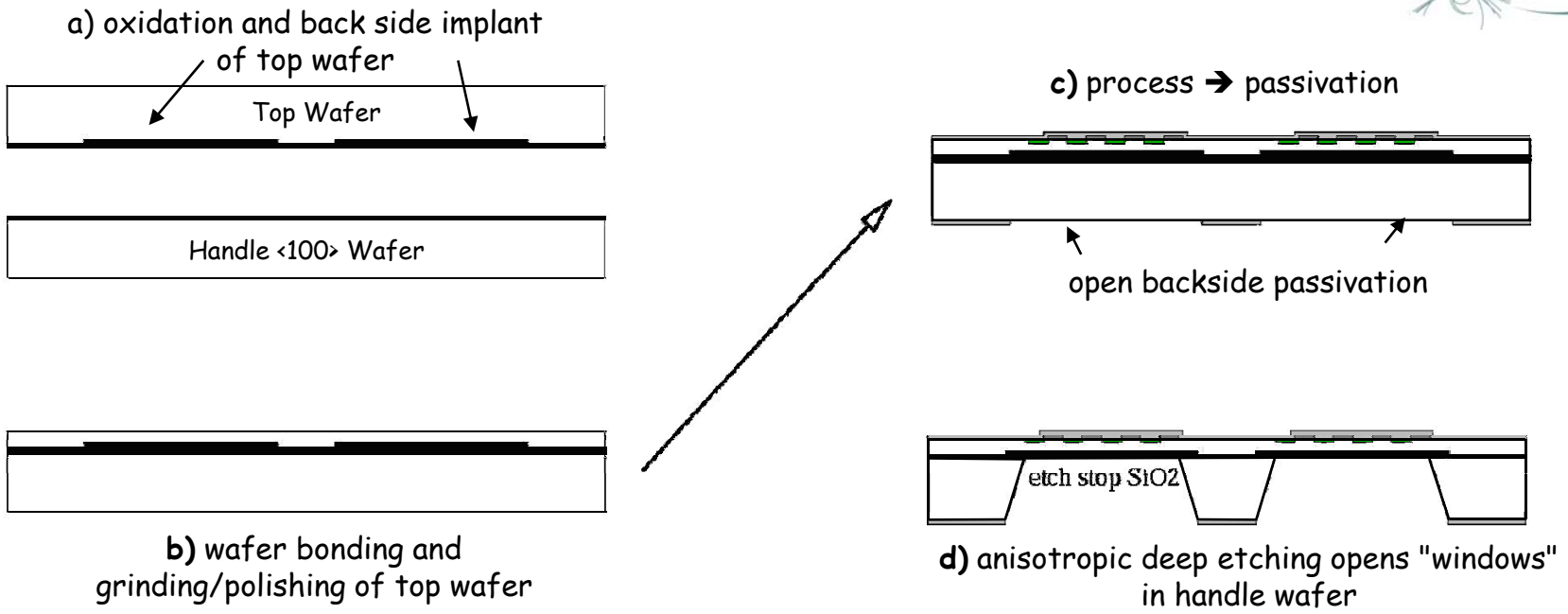
- insensitive area at the end of the ladder needed for the r/o and data transmitting ASICs → 3D integration could help here
- additional material at the end of barrels (services)
- concerning the discs: it is just an idea so far, we need a design study to come to sound proposal…the layout is pretty tricky!

Possible Areas of Collaboration

- ✓ MC studies: short barrels and discs ←→ long barrels
- ✓ Mechanics and all-silicon VXD: We can certainly make some mechanical samples for the construction of a mechanical model.
- ✓ We started already a project to see the feasibility of the 3D integration approach. Sharing the experience and results with the group at FNAL could be very helpful.

- Backup

Thinning Technology

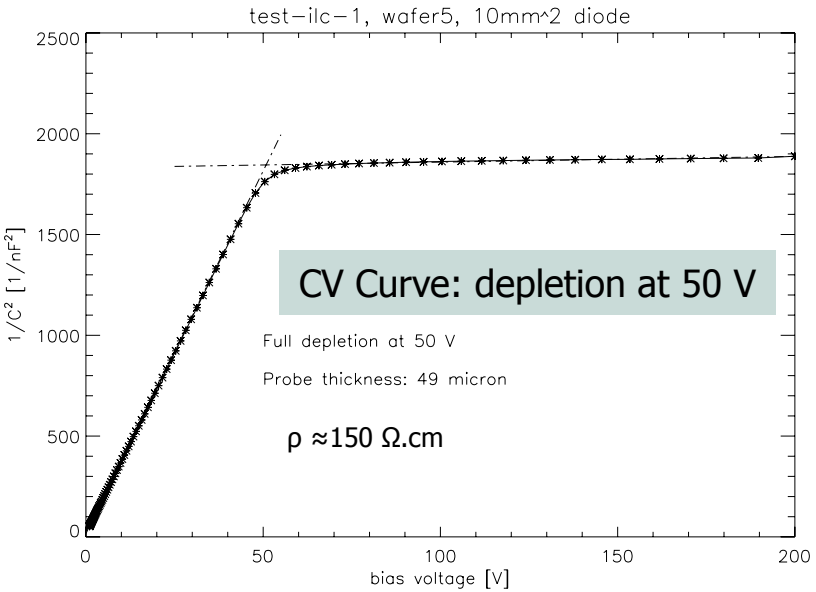


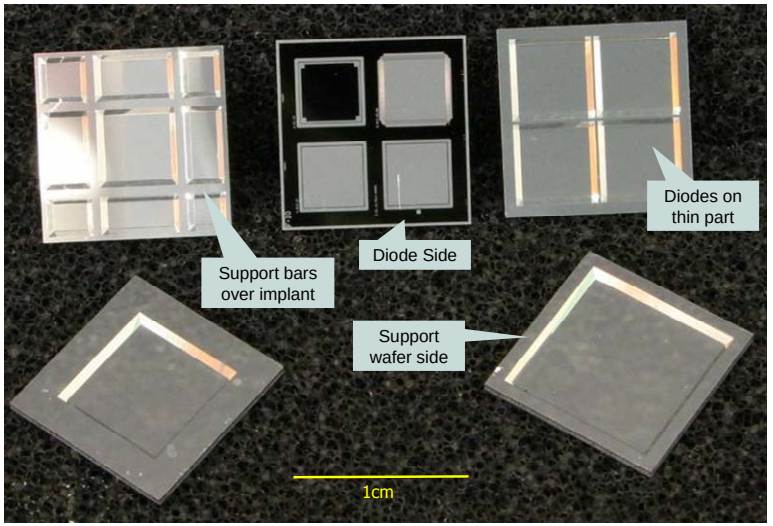
New: **150mm** Ø wafers!
New: Wafer bonding and thinning in **industry**
New: Compatibility with the main production line tested

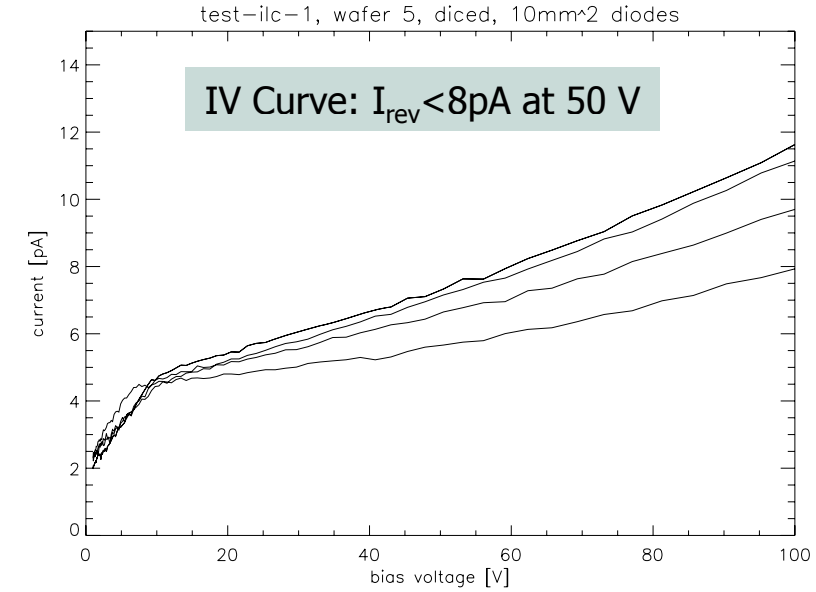
So far: mechanical samples & test structures on SOI wafers

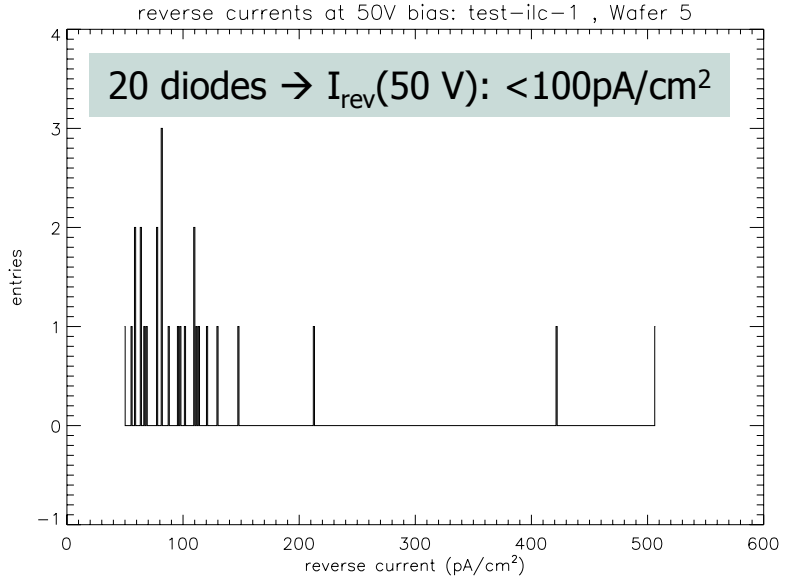
Plans 2007: production of thin (50, 100, and 150 µm) ATLAS pixel sensors for sLHC upgrade

PiN Diodes on thin Silicon

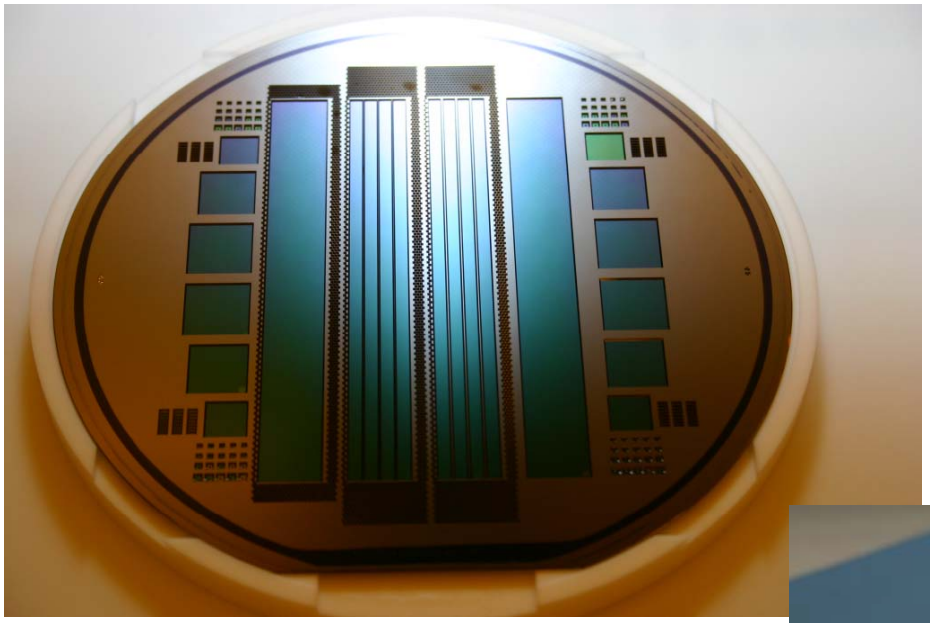


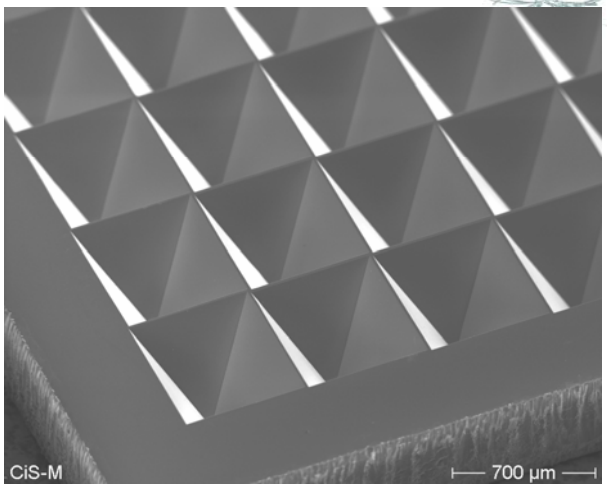


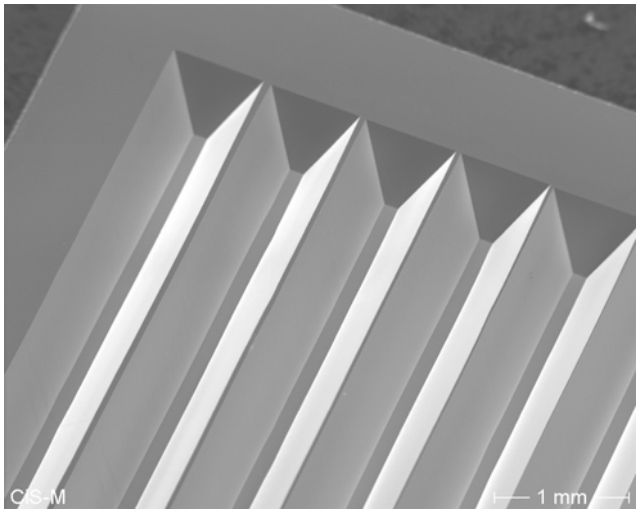


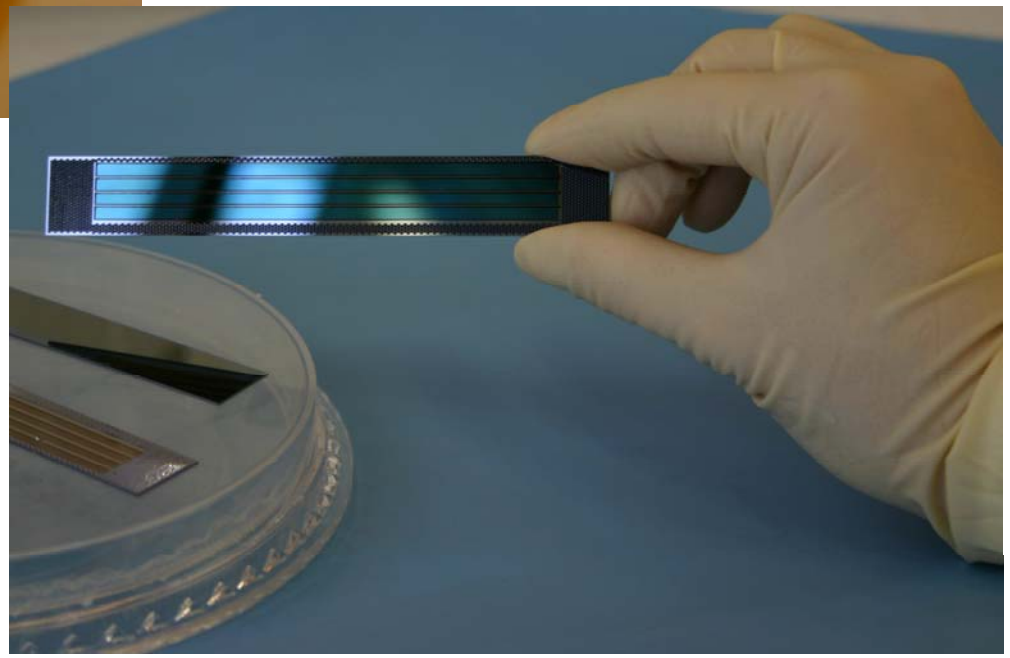


Thinning : mechanical samples

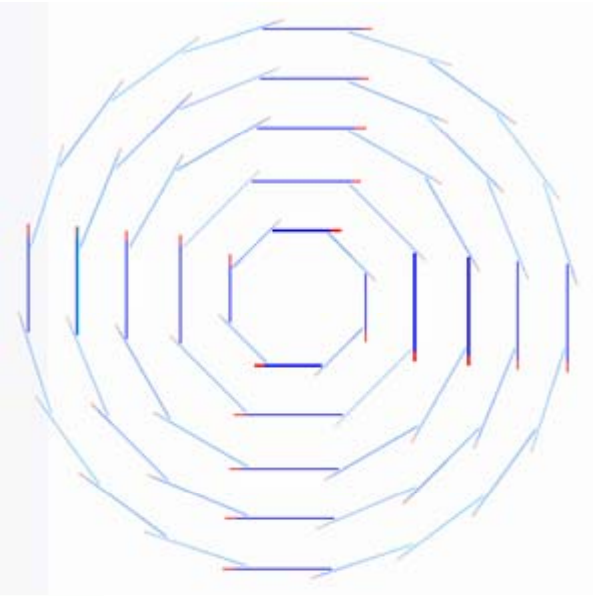






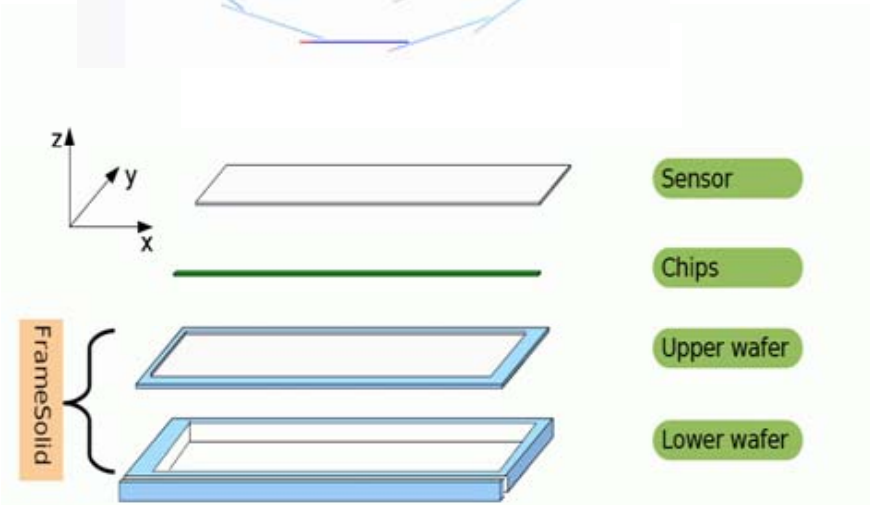


Simulation: LDC Geometry description

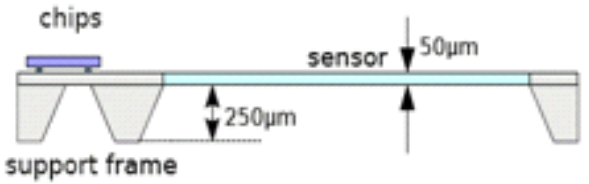


Sensitive layer thickness = 50 μm
Pixel size = 25×25 μm^2

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2×12.5
3	3.8	12	2×12.5
4	4.9	16	2×12.5
5	6.0	20	2×12.5



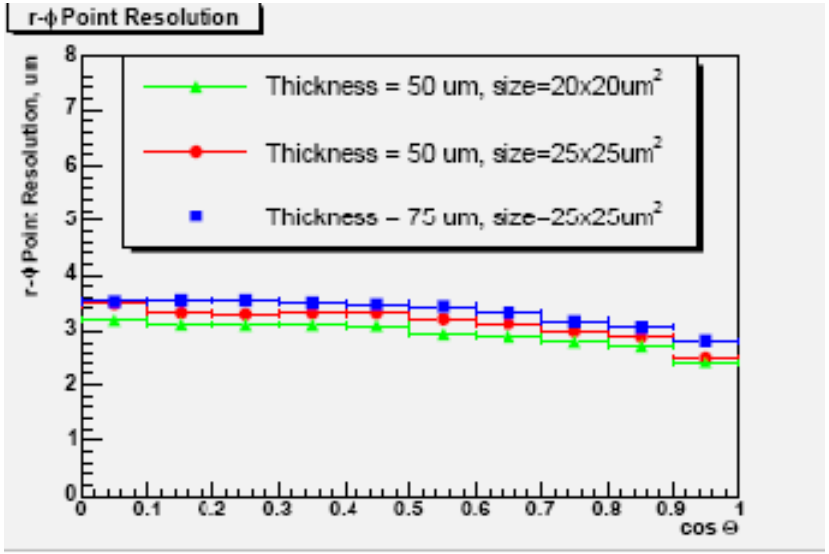
→ LDC ladders with support frames

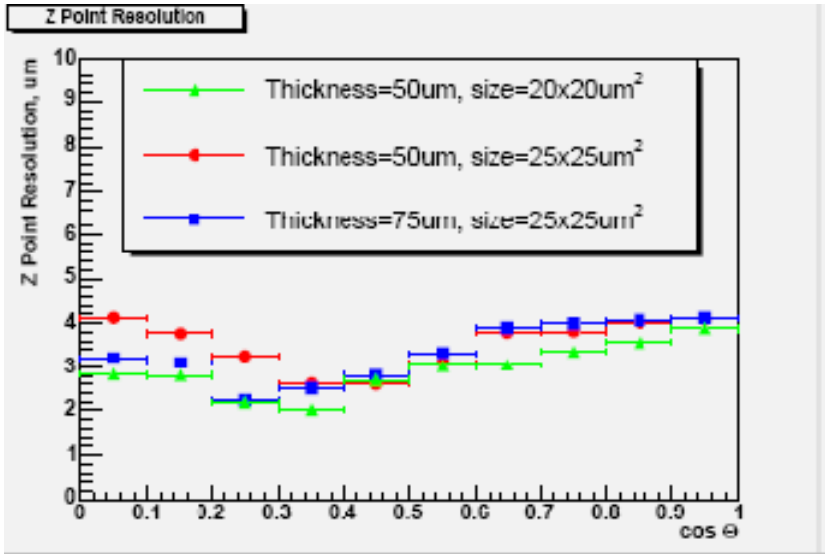


Material up to first layer : beam pipe (500 μm beryllium)

MC Studies

Spatial resolution for 50 mm thick 25 x 25 mm^2 pixels: <3.5 mm (r-φ), <4.0 mm (z)





Impact parameter resolution
(5 layers, frames, 500 mm Be beam pipe)

$$\sigma(IP)_{r\text{-}\phi} = 4.5\ \mu m \oplus \frac{8.7\ \mu m}{p(GeV/c)\ \sin^{3/2}\theta}$$

ILC requirements fulfilled