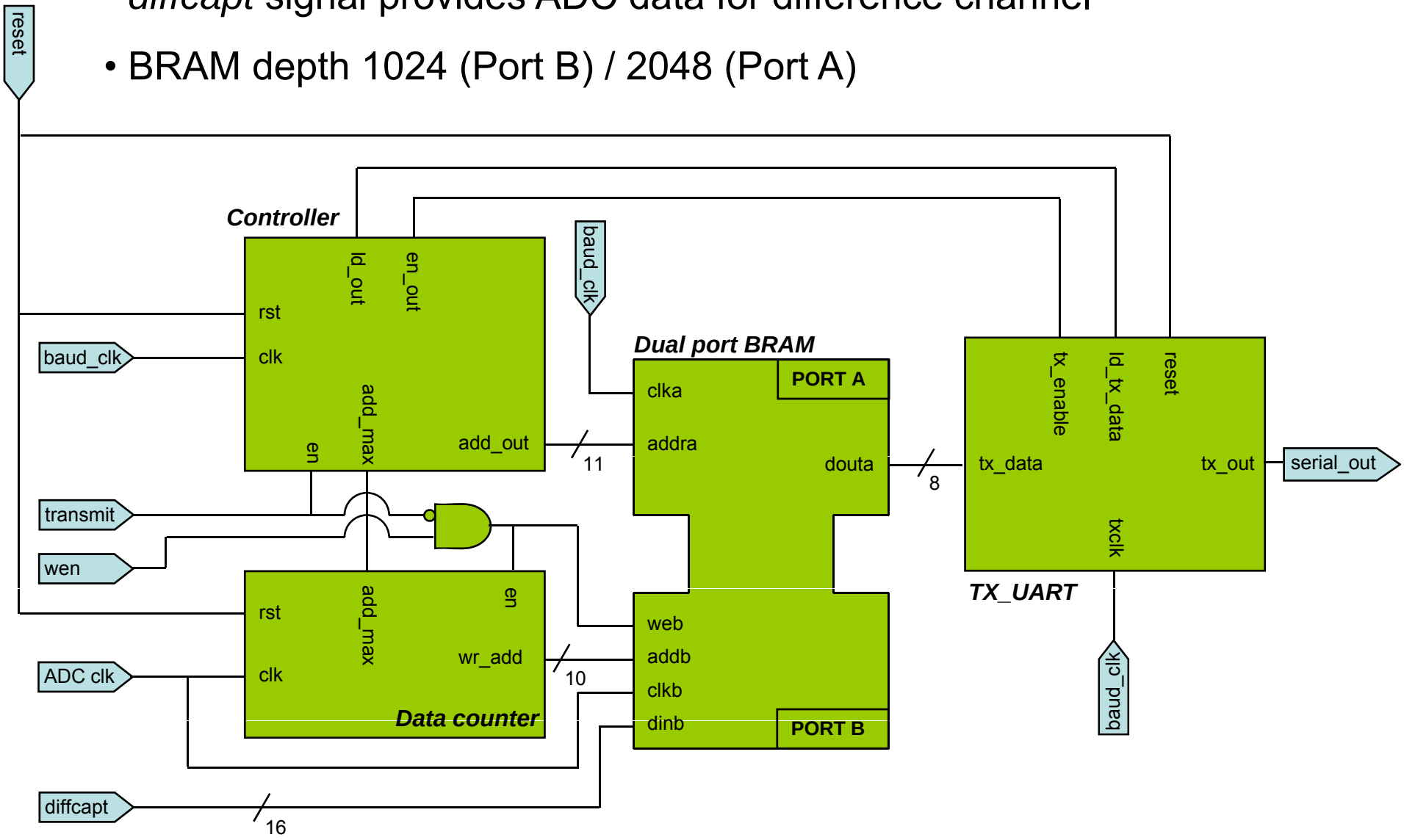
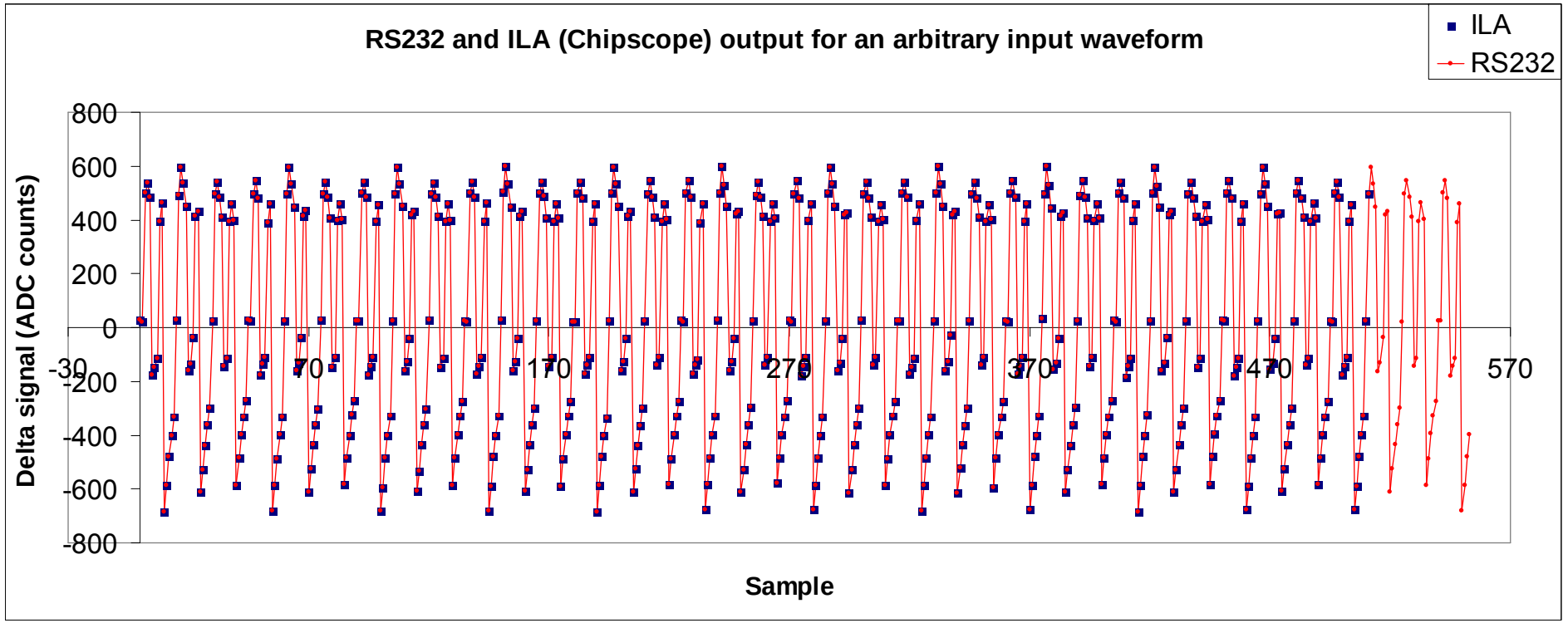
RS232 UART Status

- RS232 output working for difference channel
- Problems were:
  - Timing constraints not met due to counter
    - Changed counter to use baud clock rather than 357 MHz, fixing the timing error
  - UART enable not applied to storage of captured data, so that transmitted data were not synchronised with Chipscope ILA
    - Applied correct enable signal

- All modules below written in Verilog
- Baud clock of 115200 Hz generated on-chip (derived from 357 MHz)
- *diffcapt* signal provides ADC data for difference channel
- BRAM depth 1024 (Port B) / 2048 (Port A)





- Synchronised data sets
- Output match is bit-for-bit perfect
- ILA maximum consecutive output of 512 samples
- RS232 maximum consecutive output effectively unlimited
- Currently difference channel only (sum channel in progress)