Fig. 1. The Input Splitter (RPS-2-30) loaded on the comparators. Its second output (shown) delivers the input signal to the Synchronous Detector.
The loss is about (–3.6)dB. The rise time is <200ps.

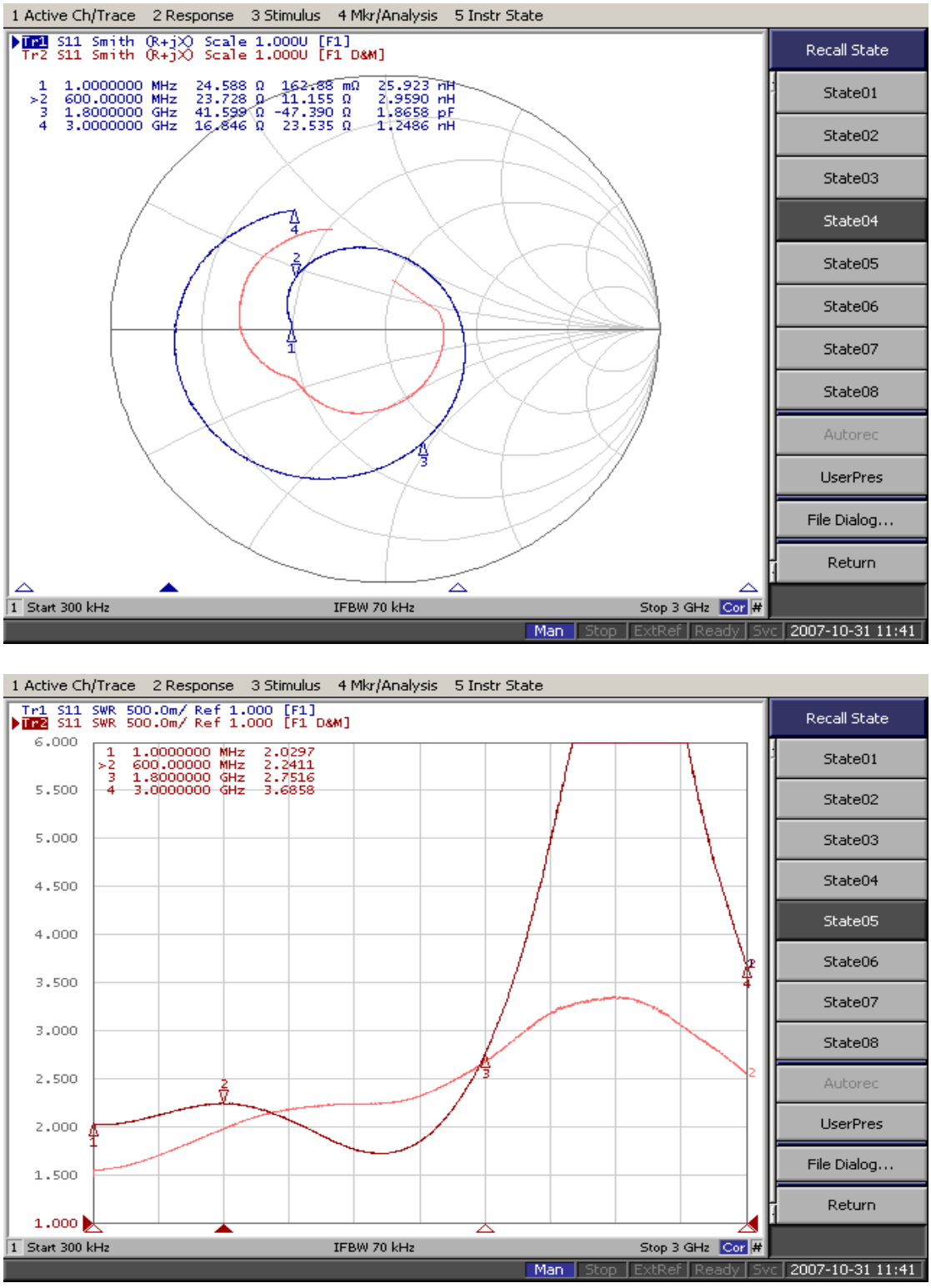

Fig. 2. The Input Splitter (RPS-2-30) loaded on the comparators. Its second output (shown) delivers the input signal to the Synchronous Detector.
The input (blue and dark red) impedance. The output (red and red) impedance. Both are as poor as given in the datasheet.

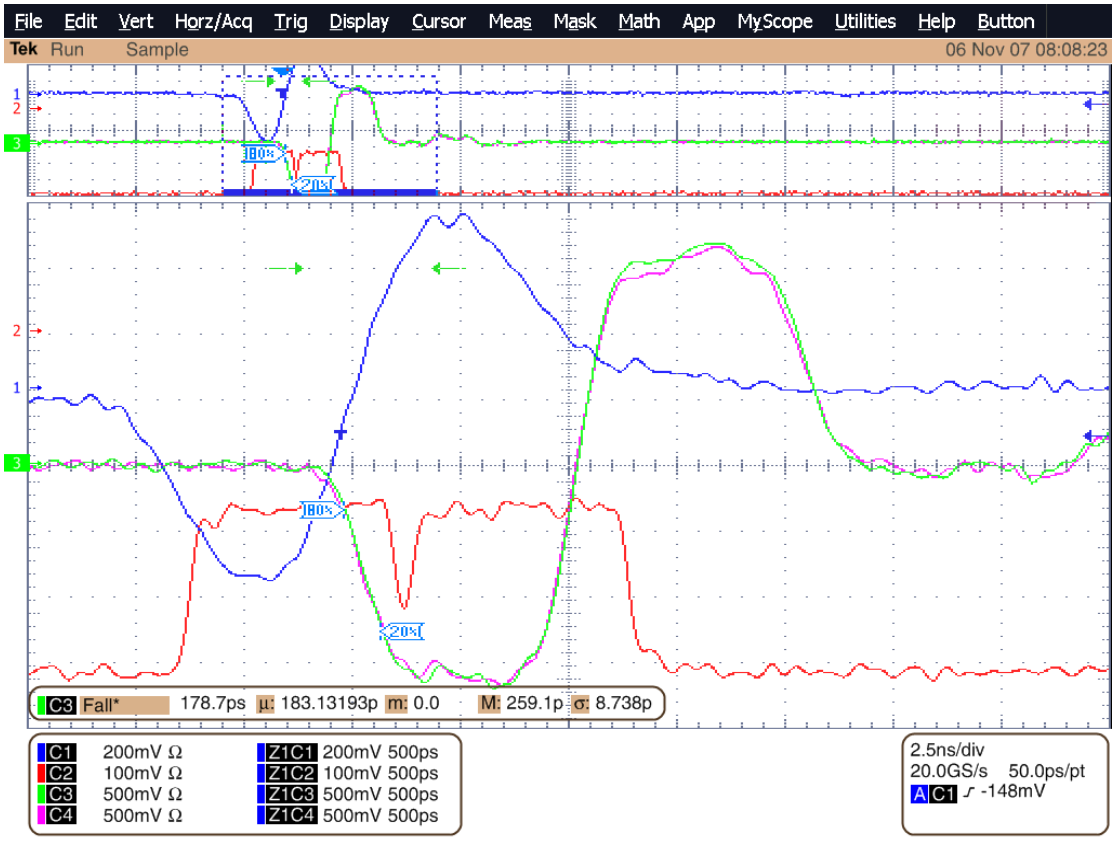

Fig.3. A SD CLOCK for sum-dif BPM.
The input signal (blue) is from a 500MHz sine-wave single coupler. The start signal for ADC CLOCK is shown red. It is a (comp1 nor comp2) CML. Two parallel SD clock outputs are shown green and purple. Each is an amplified (comp1 CML nor comp2 (–CML)). The amplitude is 1.6V. The fall/rise time is <200ps.

The MERA-533 amplifier in this circuit got a small signal excitation at about 6GHz. The RF2360 (also used in the BPM input amplifier) was substituted for MERA. The oscillograms above are with RF2360.

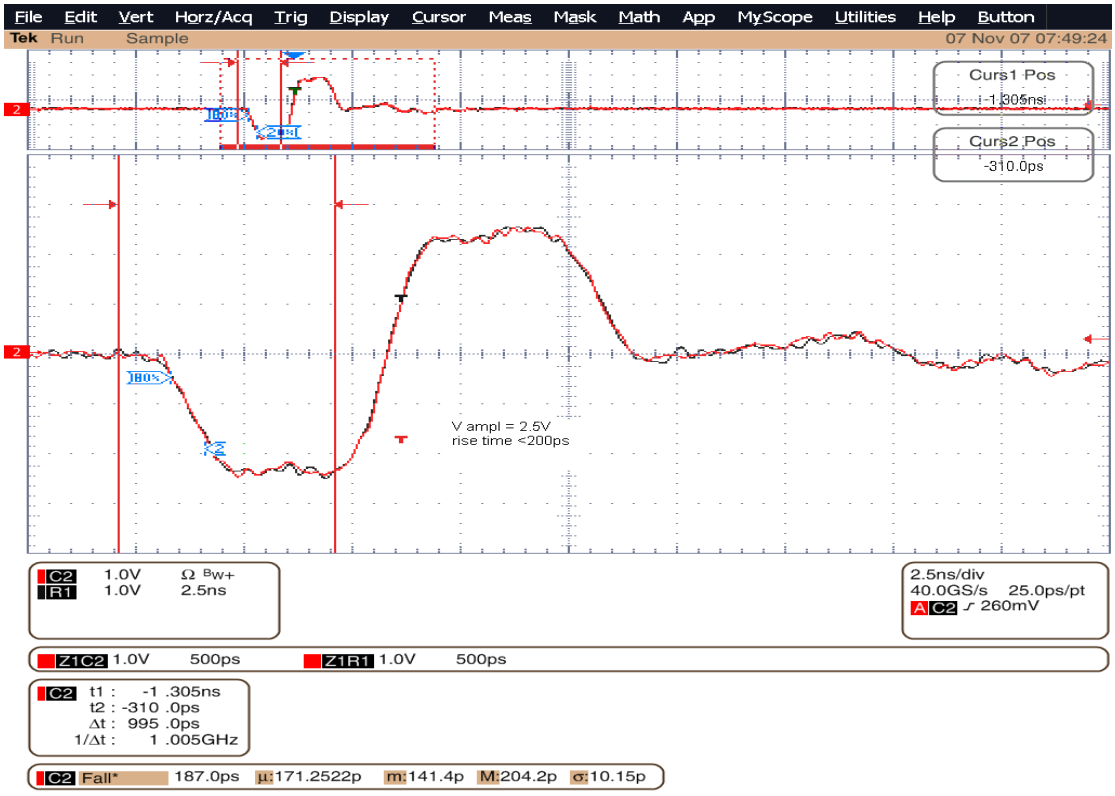

Fig.4. A SD CLOCK for in-time-multiplexing BPM.
The SD clock (amplified by one or another RF2360 amplifier) is shown red and black. The amplitude is 2.4V. The fall/rise time is <200ps.