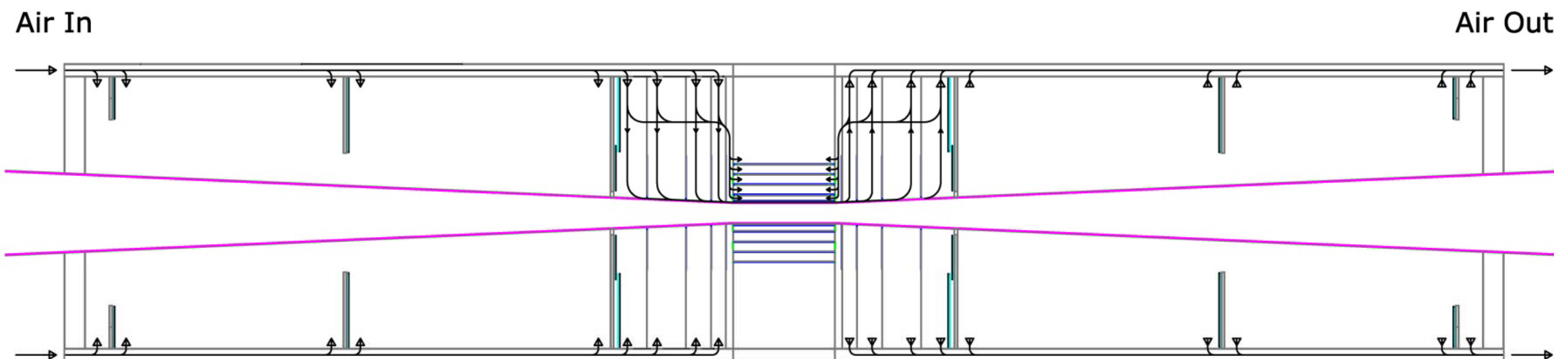
SiD Vertex Status and System Issues

Ronald Lipton (Fermilab)

Snapshot of current work and R&D

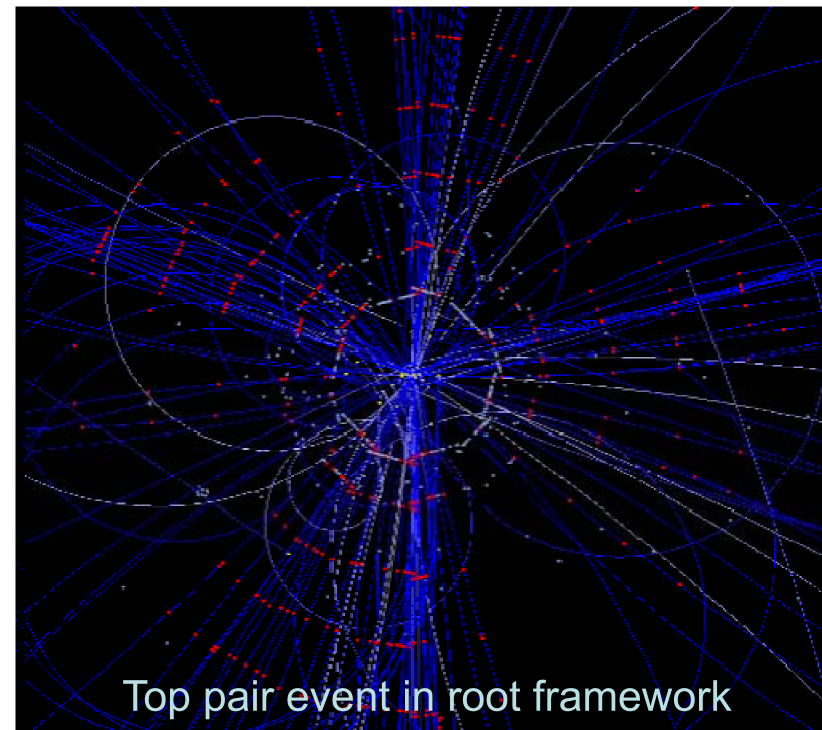
- Focus on work needed for a system design while continuing sensor R&D
  - Simulation
  - Mechanical Design
  - Cabling and Interconnect
  - Sensors



Simulation

Understand basic resolution parameters, especially in the forward direction.

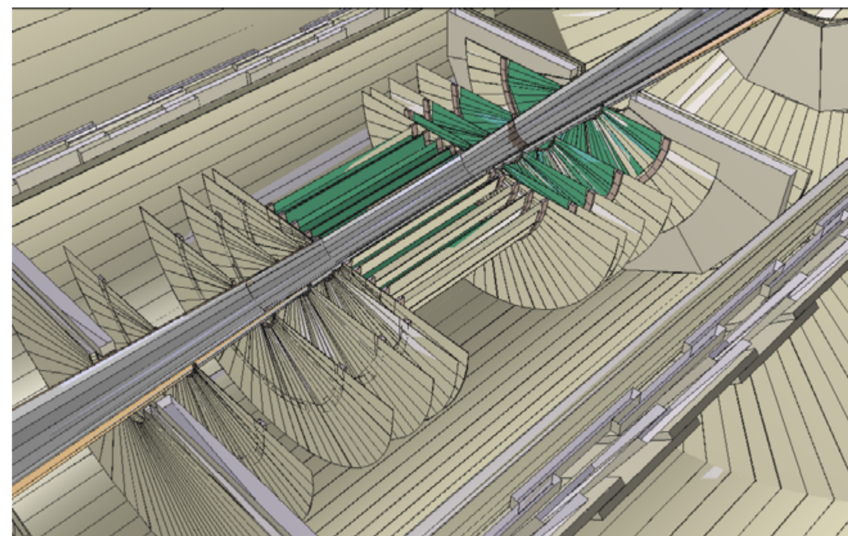
- Radial and angular dependence of backgrounds - how does this affect technology choices especially integration time?
- Resolution and pattern recognition in the forward direction


Top pair event in root framework

- Position resolution of barrels not too dependent on sensor technology other variables include:
  - Integration time - differs among sensor technologies
  - Thick (50 micron silicon) vs thin (10 micron) sensitive layers - effect on high angle tracks.
  - Depleted and undepleted detectors differ in diffusion, layer thickness, Lorentz forces.

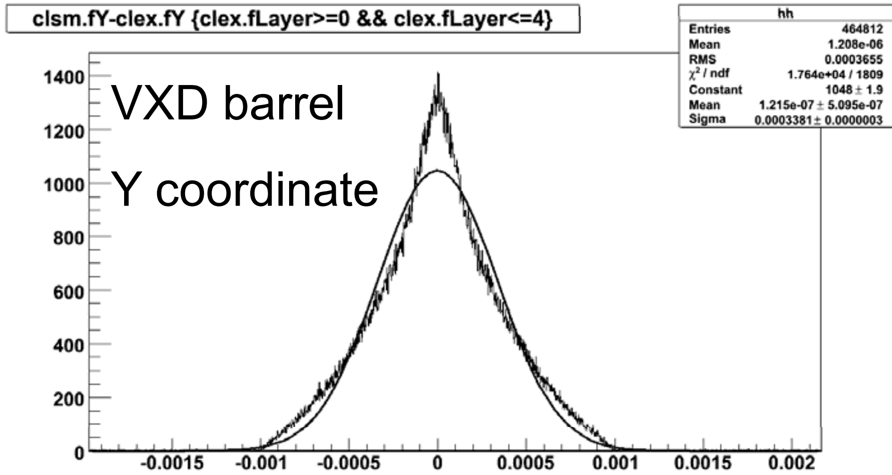
Simulation Framework

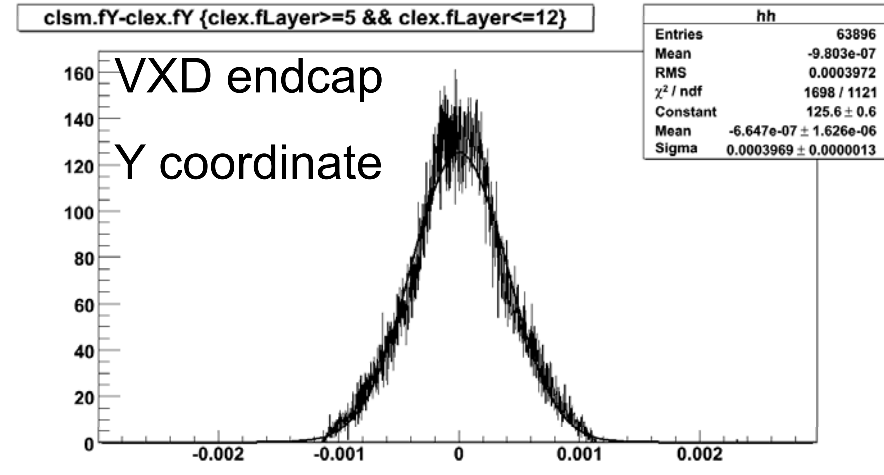
- Work by Nelson, McCormick, Sinev reported in tracking meetings
  - Basic framework for tracking in place - needs to be extended to vertex
  - Detailed physical simulation of several detector types will be available.
- Work by Gatto group on Root-based simulation
  - Full simulation available
  - Beam backgrounds included
- MPI group beginning to work on forward disk simulation.
- I assume that SiD will use the non-Root framework for further work

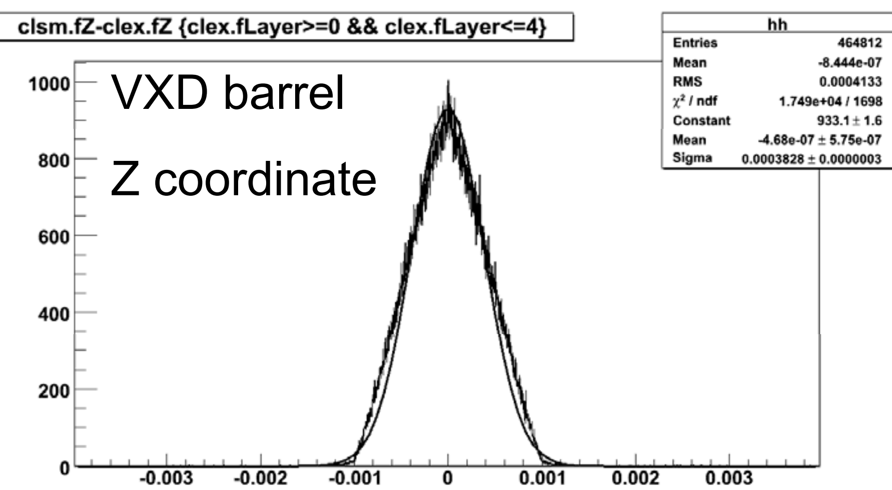


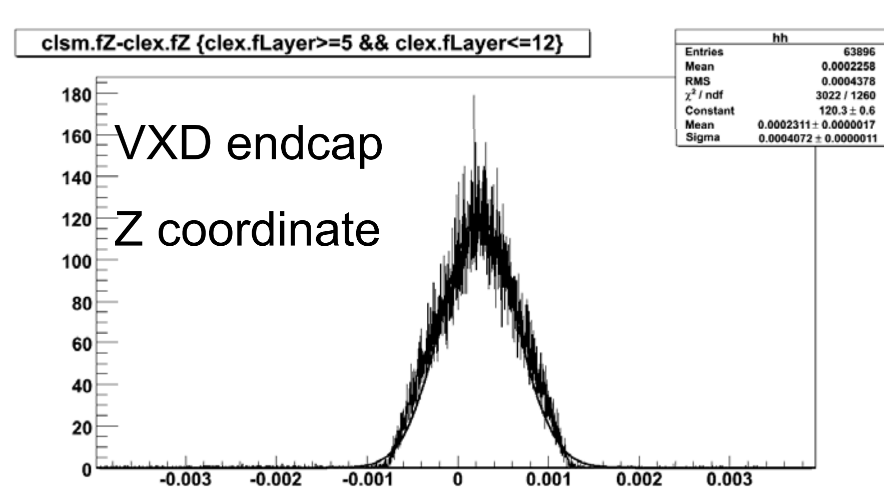
Ronald Lipton

D. Barbareschi Simulation



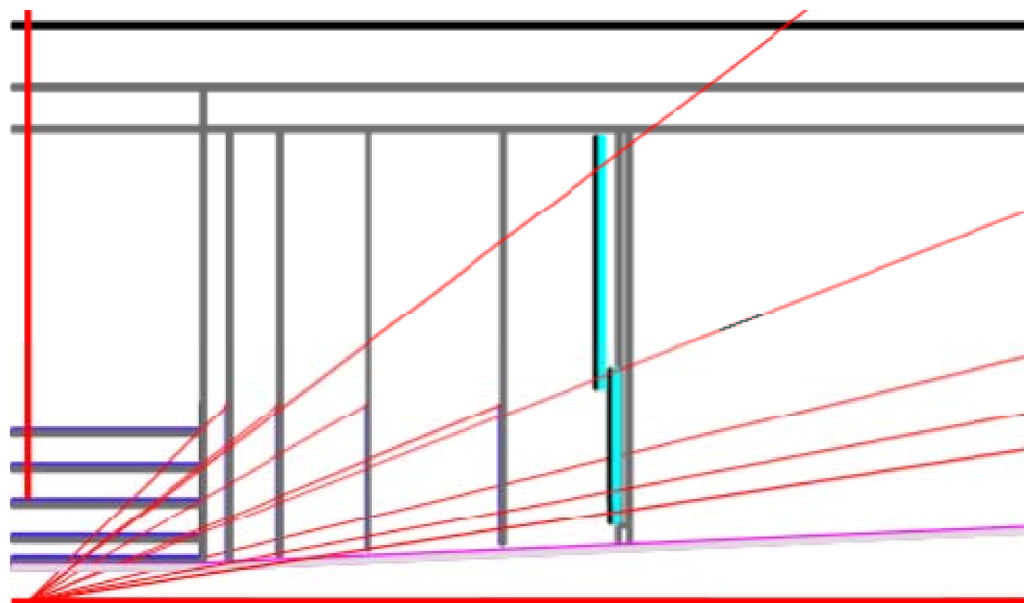






Forward Pixel Disks

- What pixel size is needed in the forward disks?
  - Tracks will pass through at least one barrel layer
    - IP resolution dominated by barrel hit(s)?
    - How are barrel hit resolutions degraded at large angle?
  - Impact of beam pipe, cables routed along pipe
  - Geometry probably requires outward routing of disk cables
  - What is needed for pattern recognition
    - resolution/power tradeoff
    - Beam background occupancy

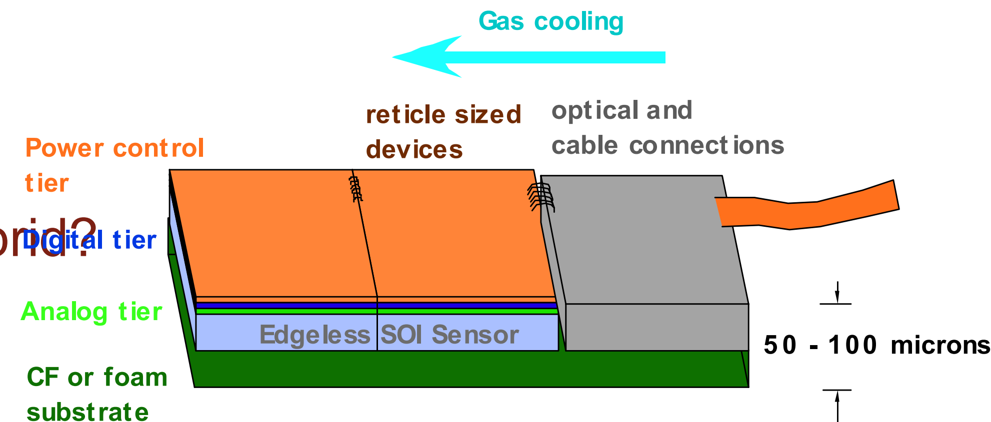


Simulation - Needs

- Understand pattern recognition tracking performance
  - Include beam backgrounds in simulation
  - Include full tracking
  - Study varying sensor integration times
  - Study varying sensor performance
  - Study varying material
- In parallel understand physics performance
  - Use simulation on physics benchmarks
  - Study forward tracking options – SiD could have a significant advantage over a TPC-based experiment

Cabling and Interconnect

- Power delivery design
  - Cable character and geometry
    - Routing - along beam pipe or radially outward?
    - Power cable mass and number
  - Generate “bottoms up” estimate of cable mass and locations
  - Optical interconnect - power required, location of electrical-optical interface
- Sensor/cable interface design.
  - Integrated on ladder?
  - Separate driver/interface hybrid?
- Lorentz forces.
  - Serial schemes can lead to unbalanced currents
- Pulsed power R&D.
  - Initial demonstration in a moderate system
  - Forces and stresses on components
  - Control systems



Cabling and Interconnect

- Serial Powering or DC-DC Conversion
  - Deliver power at increased voltage - can reduce current by a large factor (10?)
  - Reduce cable mass
- FNAL is developing rad hard serial power chip in collaboration with RAL/ATLAS
  - Control interface to set voltages
  - ADC to read out currents
  - Features to recover from failed modules - reduce shunt voltage
  - Bump bonded chip

  This should allow groups to develop integrated serially powered designs and study power cycling in complex systems

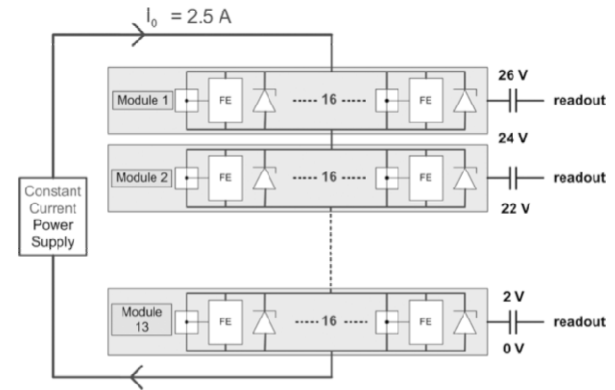
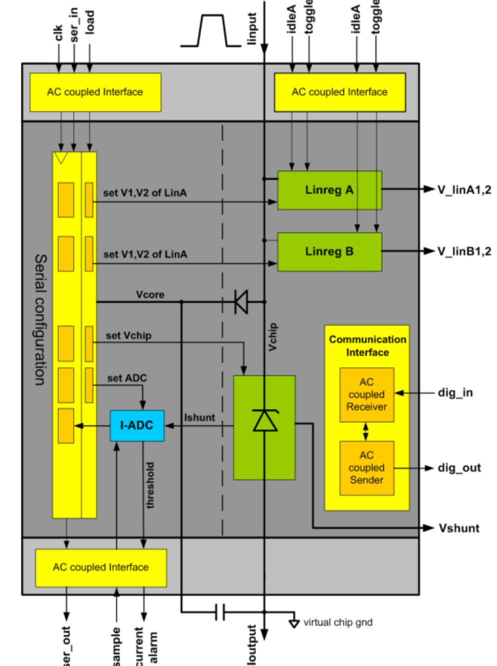


Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.



FNAL serial powering chip concept

Power Tradeoffs

$$ENC^2 = (C_{det} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

$$g_m \propto \frac{I_d}{nV_t}$$

$$P \propto freq \times C_{int} \times \Delta V^2$$

- Power vs time resolution
  - Front end preamp power
  - Clock frequency for rolling shutter
  - Power to drive readout interconnects
- Power vs pixel size
  - FE power directly proportional to number of pixels?
    - Depends on how capacitance scales
  - Vary size as a function of position and/or radius?
- Power vs technology
  - CCD - power dominated by clock
  - DEPFET - low per pixel power - dominated by edge readout
  - Time stamping - power dominated by in-pixel amp
    - More complex readout
    - If noise-related power is dominant pixel size scaling depends on detailed design - capacitance vs pixel size

Sensors

- To what extent do we want a sensor-independent design?
  - It is clearly too early to make a decision of any sort on sensor technology. How do we proceed in other areas given the uncertainty in sensor characteristics? What R&D should be done to establish specifications?
- Rolling shutter vs time stamp model
  - What time resolution is really needed?
  - What are the tradeoffs?
    - In some technologies time is directly related to power
    - Signal/noise related to power
    - Resolution related to power
  - Different schemes in inner and outer layers?
    - Su Dong has made a good case for selecting the optimal technology mix based on differing requirements for the sensors as a function of radius

Sensors

- How does sensitive layer thickness affect large angle track resolution?
  - Charge sharing model
    - fully depleted vs diffusion charge collection
    - signal/noise expected
- Disk sensors
  - Type
  - Pixel size
  - segmentation

Thinned Sensors

- MPI has demonstated thinning to 50 microns based on oxide bonding and rim thinning techniques

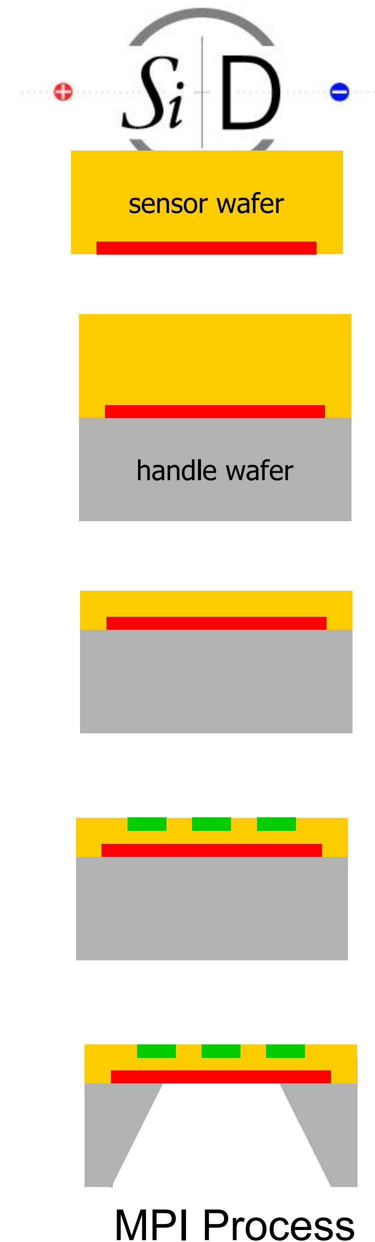
1) Process backside of thick detector wafer (structured) implant.

2) Bond detector wafer on handle wafer.

3) Thin detector wafer to desired thickness (grinding & etching).

4) Process front side of the detector wafer in a standard (single sided) process line.

5) Etch handle wafer.
If necessary: add Al-contacts
Leave frame for stiffening and handling, if wanted

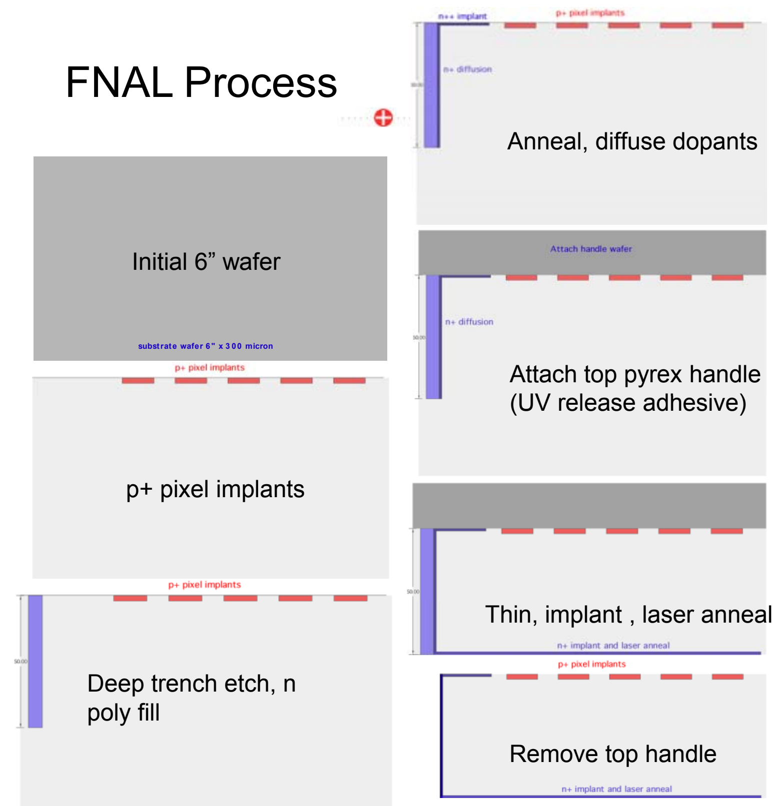


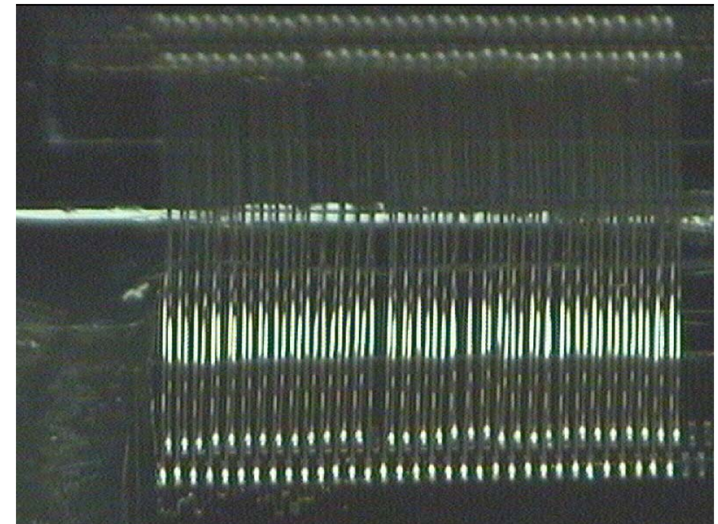
MPI Process

FNAL Thinning Process

FNAL is working on thinning and laser annealing techniques to enable thinning and formation of backside contacts on complex devices

- FNAL flow for thinning MIT-LL and OKI SOI detectors
  - Fabricate device, attach to handle
  - Thin, polish
  - Implant backside
  - Laser anneal
  - Detach to dicing tape
  - Dice
  - Remove from tape, glue on support
- Done for 50 micron thick MIT-LL test wafer
  - Can dice, handle, and wirebond to thinned device



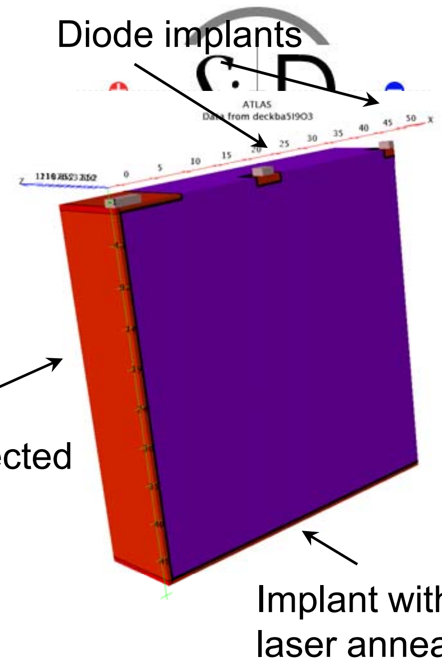


Ronald Lipton

SID Workshop Jan 28, 2007

Edgeless Thinned Detector Concept

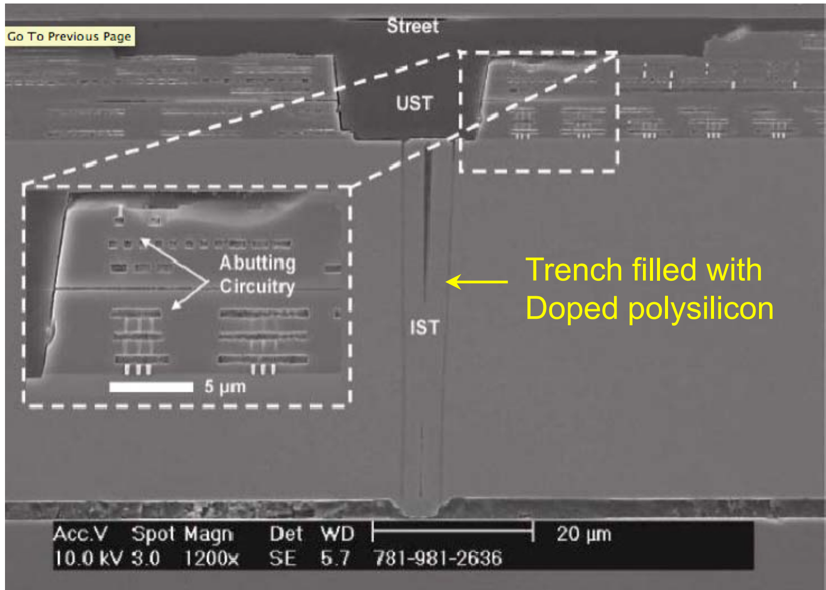
- Deep trench etching used in 3D vias can be used as a high quality detector edge (same as 3D detectors)
- This edge can be used as a detector electrode - eliminating edge losses in tiling reticle-sized detectors
  - We have produced a set of detectors at MIT-LL thinned to 50 and100 microns
  - Validate and develop thinning process
  - Understand performance in test beam
  - Develop handling and bonding techniques



Trench on detector edge filled with poly and connected to bottom implant

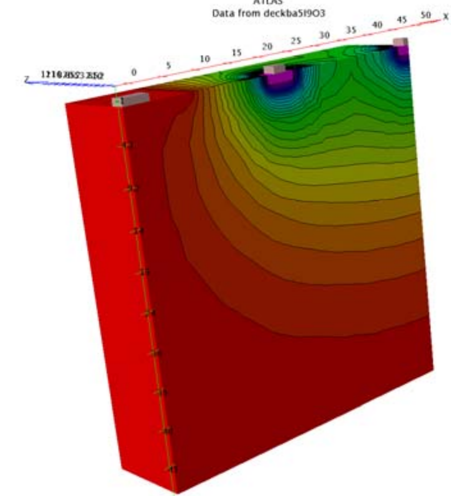
Implant with laser annealing

Detector Cross section near one detector edge



Trenched 3D sensor

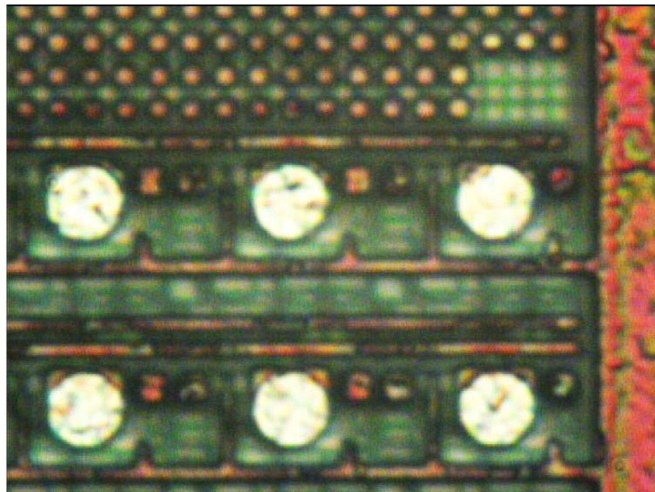
From MIT-LL

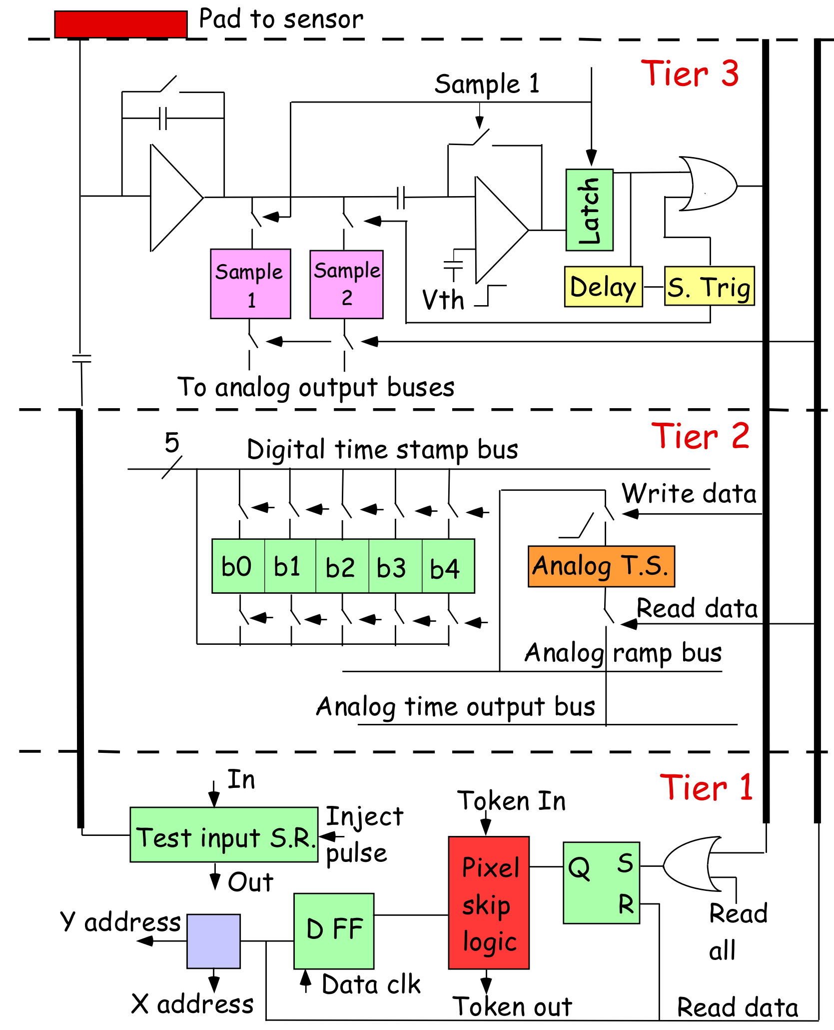


Equipotential lines in detector near one detector edge

FNAL 3D Chip

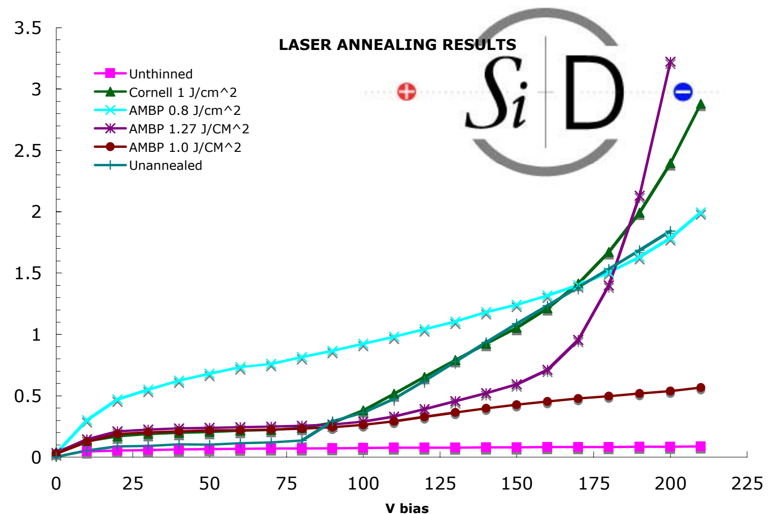
- Received from MIT-LL end of November
  - Error in test structure layout - repaired by FIB for 2 chips
  - Analog test structures look good, rise time, noise similar to models
  - Can download through full chain.
  - Full testing now underway



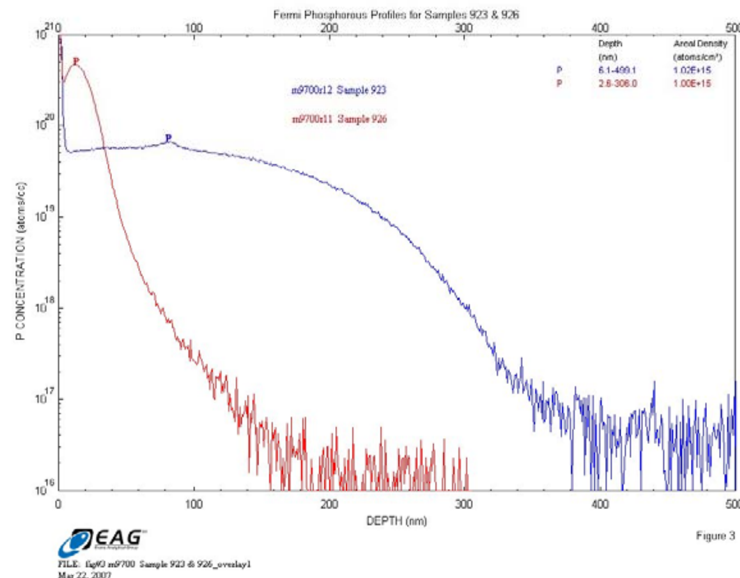


Laser Annealing

- We need to provide a backside ohmic contact to thinned active wafers.
  - Normally done using furnace anneal at ~1000 deg C.
  - But the topside had been fully processed and we need to keep the top below ~500 deg C to protect topside metalization
- Use a raster scanned eximer laser to melt the silicon locally – this activates the ohmic implant a repairs the implantation damage
- To study and qualify this process we took a samp of Run2b HPK, 4x10 cm, strip detectors and reprocessed them
  - Backgrind by ~50 microns to remove back implant and aluminization, polish
  - Re-implant detector
  - Laser anneal at AMBP, Cornell and measure CV and IV characteristics
- Qualifying final process with Micron wafer
  - Then thin and anneal 2 MIT sensors
  - Thin and anneal OKI SOI wafer



VI plots for several thinned and laser annealed sensors



–samples, before and after 1.2 J/cm^2 248 nm laser anneal

– Goal was ~>2x10^{19} concentration

– Melt depth ~300 nm

Ronald Lipton

Mask Design

- Masks designed at FNAL
  - Strip detectors (12.5 cm and ~2 cm)
  - BTeV FPiX2 pixel detectors (beam tests)
  - Detectors to mate to 3D chip
  - Pinned and unpinned surfaces
  - Test structures

BTeV Pixels

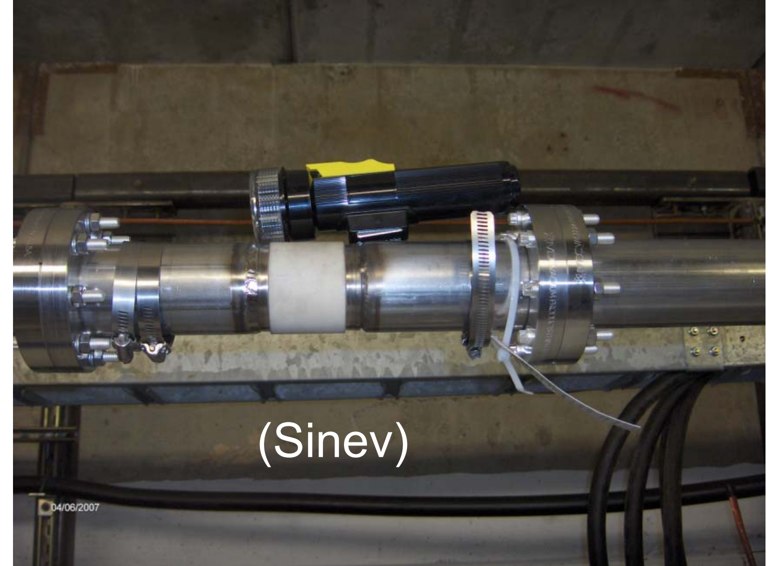
Mini strips

VIP sensors

Strip sensors

Test structures

EMI Studies



SLD saw significant electromagnetic interference associated with the SLC beam crossings

- amplifiers saturate, PLL lost lock
- This can have a major effect on vertex (and all electronics) design
  - Better to read out between bunches
  - Avoid active electronics during train

End Station A study of beam-induced EMI

- Antennas placed near (~1 m) gaps observed pulses of EMI in the high MHz range with strengths up to ~20 V/m.
- The pulse amplitudes varied in proportion to the bunch charge, independent of the bunch length.

Top trace: VXD board phase-lock loop signal\Other traces: the two EMI antennas. Time offsets are due to cable length differences.

- A single layer of 5mil aluminum foil placed over the ceramic gap and clamped at both ends reduced the signal amplitude by >x10 (eliminated?)
- A 1 cm hole in the al was enough to cause the PLL to fail, failures stopped at .6 cm

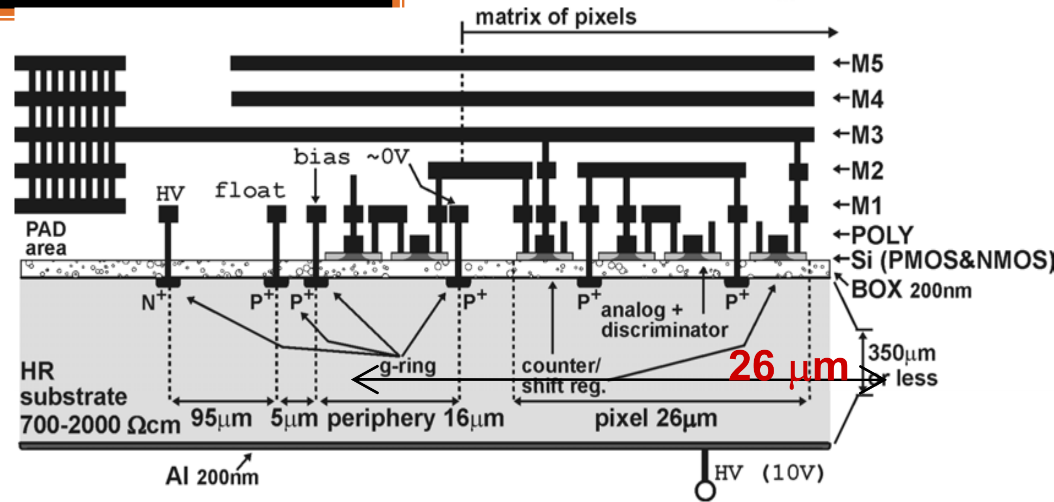
Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at three different foundries:OKI in Japan (via KEK), and American Semiconductor Inc. (ASI) and MIT Lincoln Labs in the US.

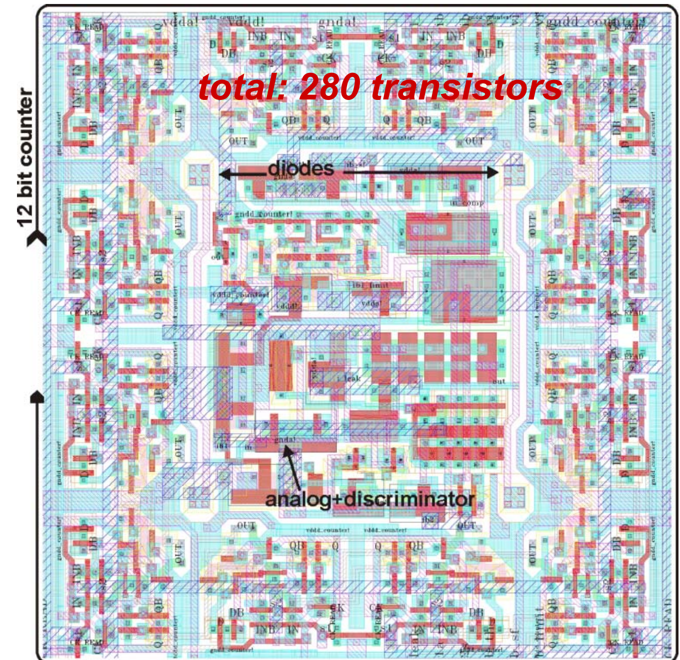
	OKI	MIT-LL	ASI
Feature size (μm)	0.15 0.2	0.18 0.15	0.18
Wafer Diameter	150mm	150mm	200mm
Transistor type	Fully depleted	Fully depleted	Partially depleted dual gate
Buried Oxide	200 nm	400 nm	200 nm
Work underway	Test Structures Mambo chip Laser anneal Mambo II	Test Structures 3D chip 3D RunII 3D Dedicated	SBIR design Simulation Test Structures Sensor SBIR

MAMBO - Monolithic Active pixel Matrix with Binary cOunters in SOI Technology OKI 0.15μm

- Mambo I tested
  - Analog/digital sections functional at different backside voltages
- Mambo II with increased BG tolerance submitted to the KEK sponsored multiproject run at OKI.

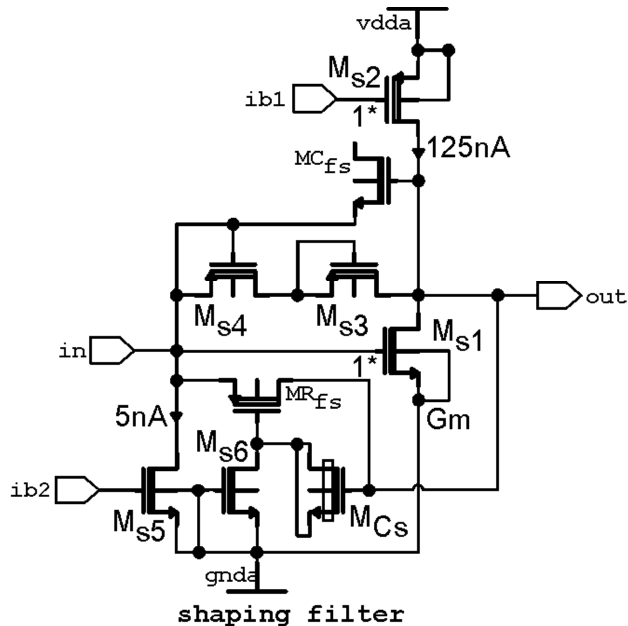


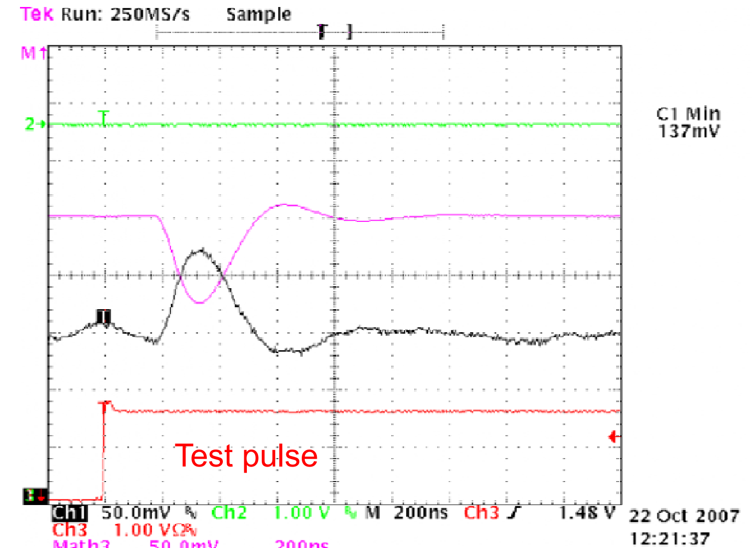
Counting pixel detector plus readout circuit
- Maximum counting rate ~ 1 MHz
- Each pixel: CSA, CR-RC2 shaper, discriminator + 12 bit binary counter
- Reconfigurable counter/shift register
- Peripheral circuitry limited to digital drivers (RO clock distribution, I/O signals, configuration switch) and bias generator
- 350 micron detector thickness
- Max 13 m implant pitch (4/pixel) is determined by the "back gate" effect where the topside transistors thresholds are shifted by handle potential

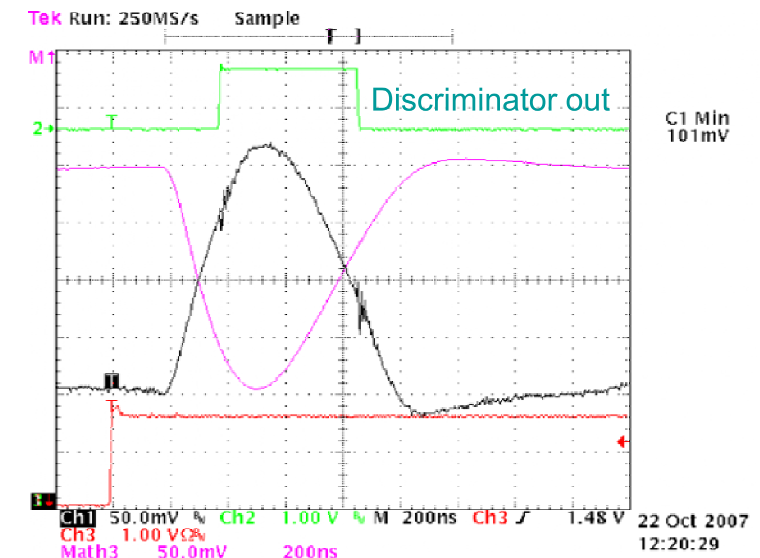


Analog Performance

- Original specs almost recovered with good shaping time and almost correct gain when applying -0.07V bias on feedback resistance (transistor) in the shaper (Vdet=5V):
- input charge ~1250 e-,
- 80e-<ENC<100e-



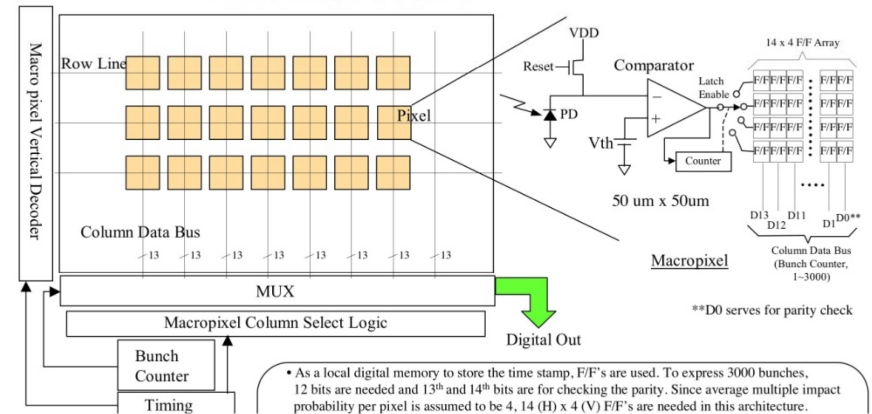


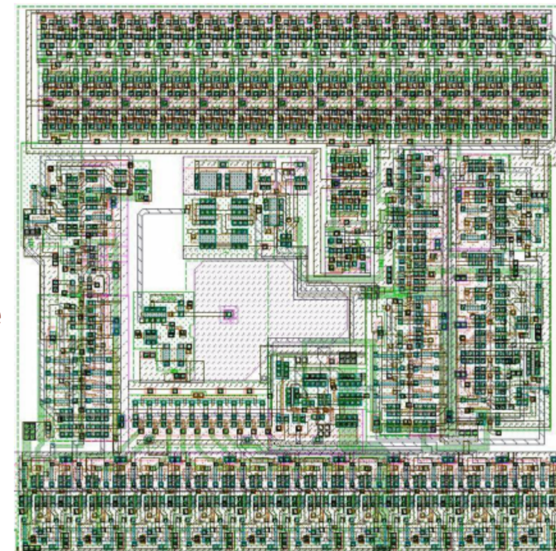


Chronopixel

Yale/Oregon/Sarnoff

- Completed Macropixel design last year
  - Key feature – stored hit times
  - 645 transistors
  - Spice simulation verified design
  - TSMC 0.18 mm => ~50 mm pixel
  - Epi-layer only 7 µm
  - 90 nm => 20-25 µm pixel
- January, 2007
  - Completed Chronopixel design
  - 2 buffers, with calibration
  - Deliverable – tape for foundry
- This year
  - Fab 50 µm Chronopixel array due June
  - Demonstrate performance



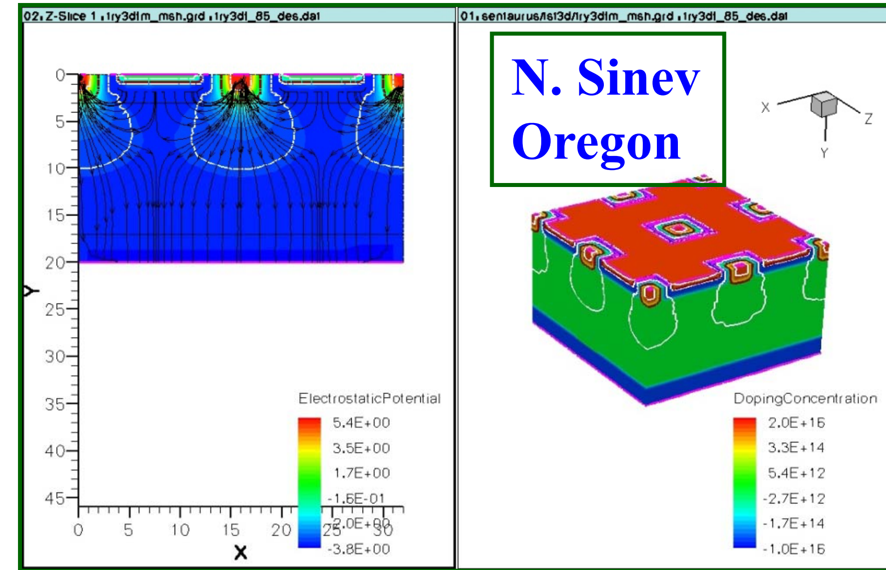


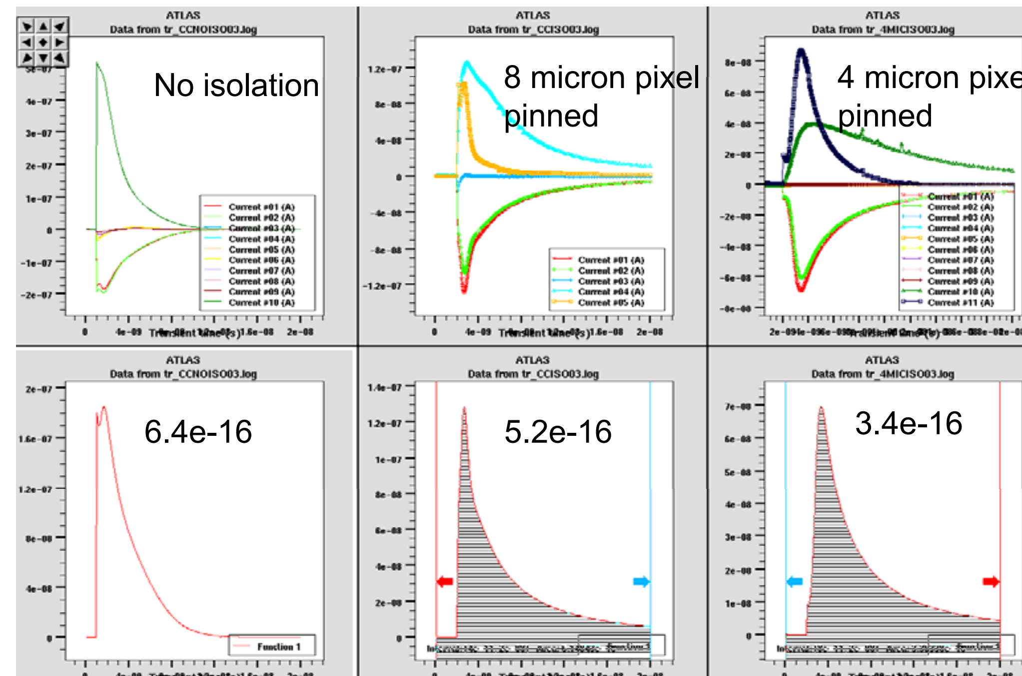
563 Transistors (2 buffers +calibration)

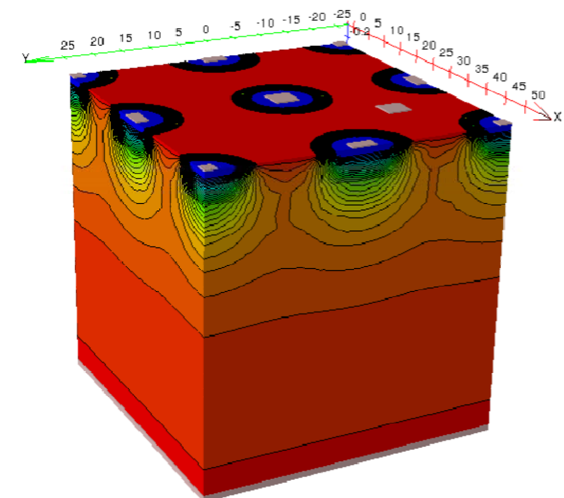
50 µm x 50 µm

TCAD Device Simulation

- Powerful tool in detector design - physics-based simulation of solid state devices
- Study charge collection, coupling, and diffusion as a function of device type and geometry
- Understand internal fields, effects of procssing variants
  - Studies of Chronopixel depletion
  - SOI detector configurations



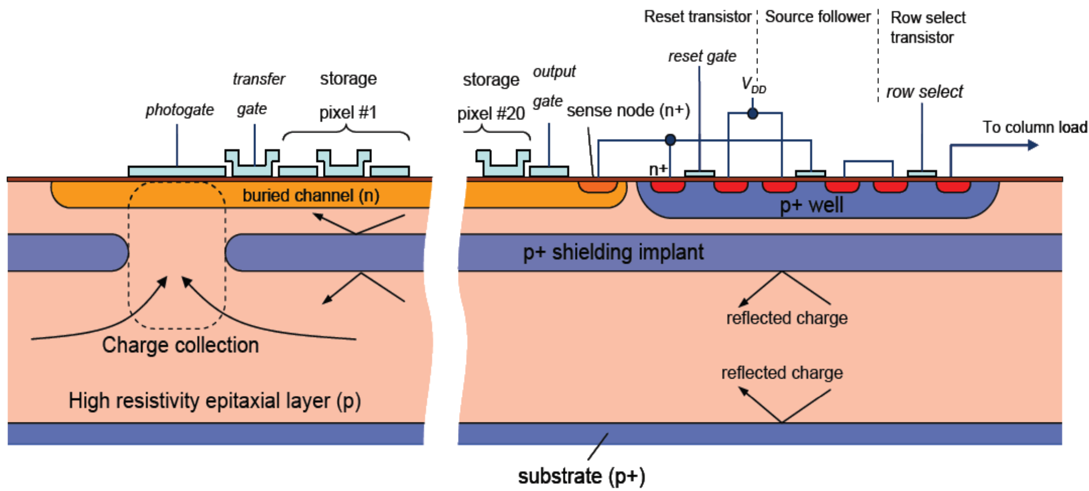




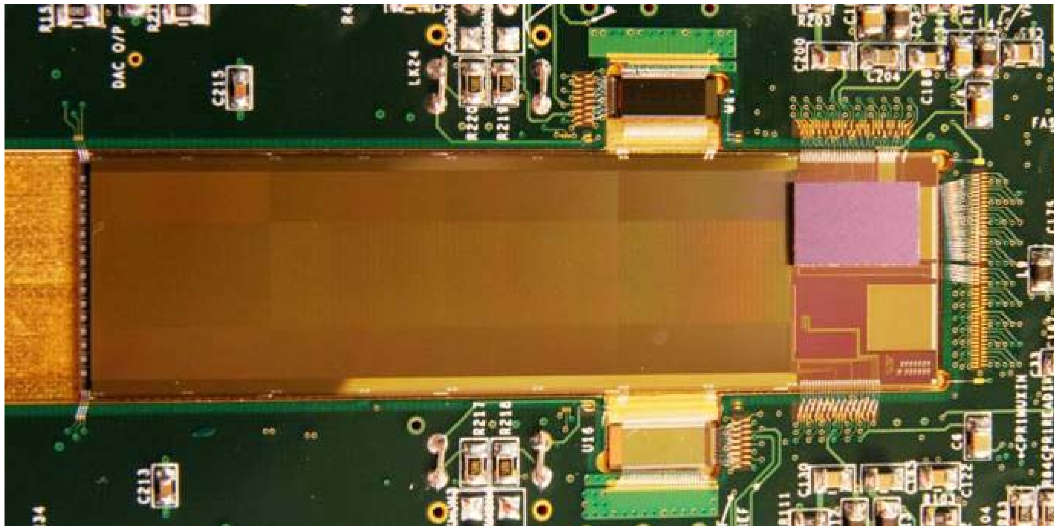
n+ pinning 10V Bias
8 micron pixels

LCFI Sensors, Mechanical, and Physics

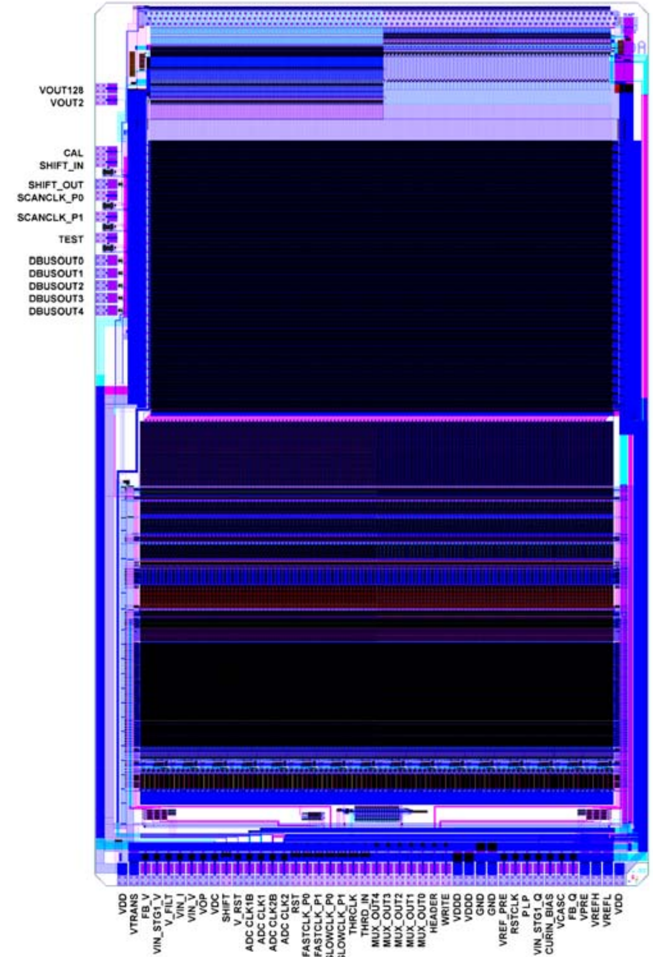
- Image Sensor with In-situ Storage (ISIS)
  - Design of CMOS-based ISIS started
  - Using modified 0.18 μm CMOS processes (1.8V/5V), custom epi
  - Fab to incorporate CCD buried channel implant and the deep p+ implant
  - Targeting submission for April multiproject run
- CCD sensors and readout
  - Test structure with many new column-parallel CCD designs due back soon
  - 12 wafers produced and tested, 29 design variants being packaged
  - Expect significant improvement (reduction) in capacitance and improved drive
  - New readout chip submitted and in fab (pad-compatible but much updated)
  - Will have *many* new devices to test!
- Mechanical
  - New results w/ foams & fibre, new fixturing in development
  - *See Bill's talk for update*
- Software/Analysis:
  - Final debugging for mass production in *ILD(!)* framework
  - LCFI Vertex Package and SiD… *see Andrei's talk*



ISIS concept with CCD storage, APS readout



CPC2-40+CPR2 and two CPD1 in MB5.0



CPR2A readout chip

Ronald Lipton

Effects of Budget Cuts

- FNAL
  - Cancelled plans for “direct bond interconnect” prototype using MIT-LL wafers and BTeV readout at Ziptronix
  - Simulation effort diverted
  - Can probably finish thinning and laser annealing of two other MIT-LL wafers (orders already placed)
  - Serial power chip probably can be funded with CMS/ATLAS help
  - Increased pressure to devote engineering and technical resources to other priorities
  - DARPA funded 3D runs at MIT-LL and Tezzaron (designs to include?)
- LCFI?
- MPI/DEPFET - Unaffected - will continue to work on forward region
- Chronopixel - due from Fab in June.
- Pressure to work on other things…