Electronics Systems Discussion

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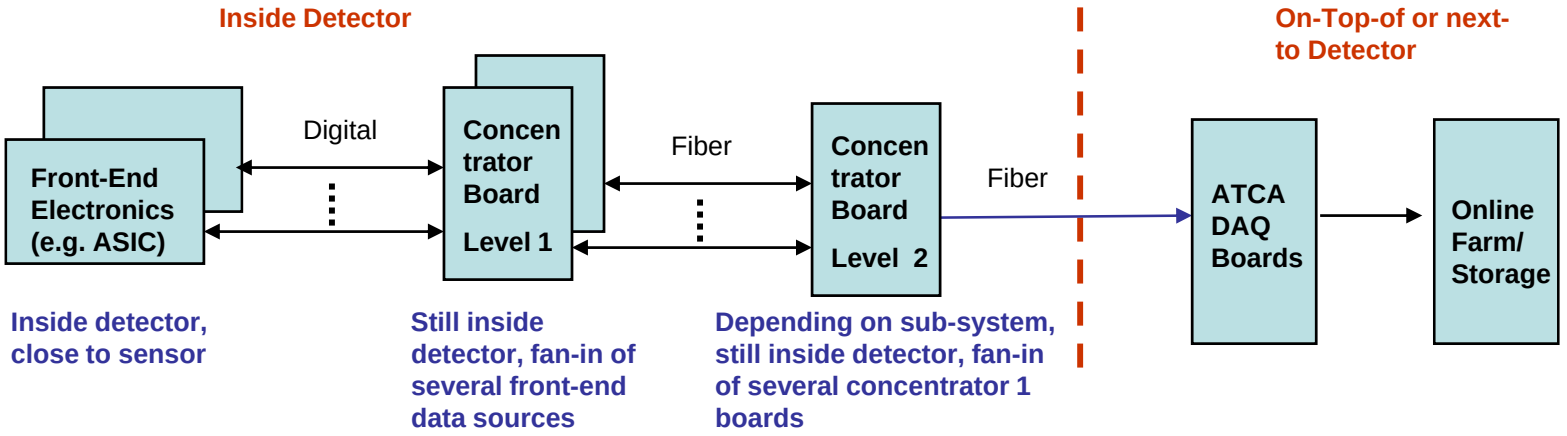
Overview

- Electronics Architecture
- Cold-Machine Readout
- Warm-Machine, focusing here on KPIX readout
- DAQ Hardware

Electronics Architecture



- Total data rate from each front-end relatively small, thus can combine data from several front-ends to reduce number of connections to the outside of the detector
- Front-End ASICs/electronics transmit event data to concentrator 1 boards
  - Digital interface (optical or electrical, e.g. LVDS)
  - Concentrator 1 boards close to front-end, combining data-streams from several front-end ASICs
  - Zero-suppression either at front-end or on concentrator 1 boards
    - No additional processing needed at this stage
- Event data from concentrator 1 boards are combined in concentrator 2 boards
  - Multiplexing of concentrator 1 board event data onto fewer fibers
- Event data is transmitted to top or side of detector
  - ATCA crate (see later) to process and switch data packets
  - Online farm for filtering (if necessary)

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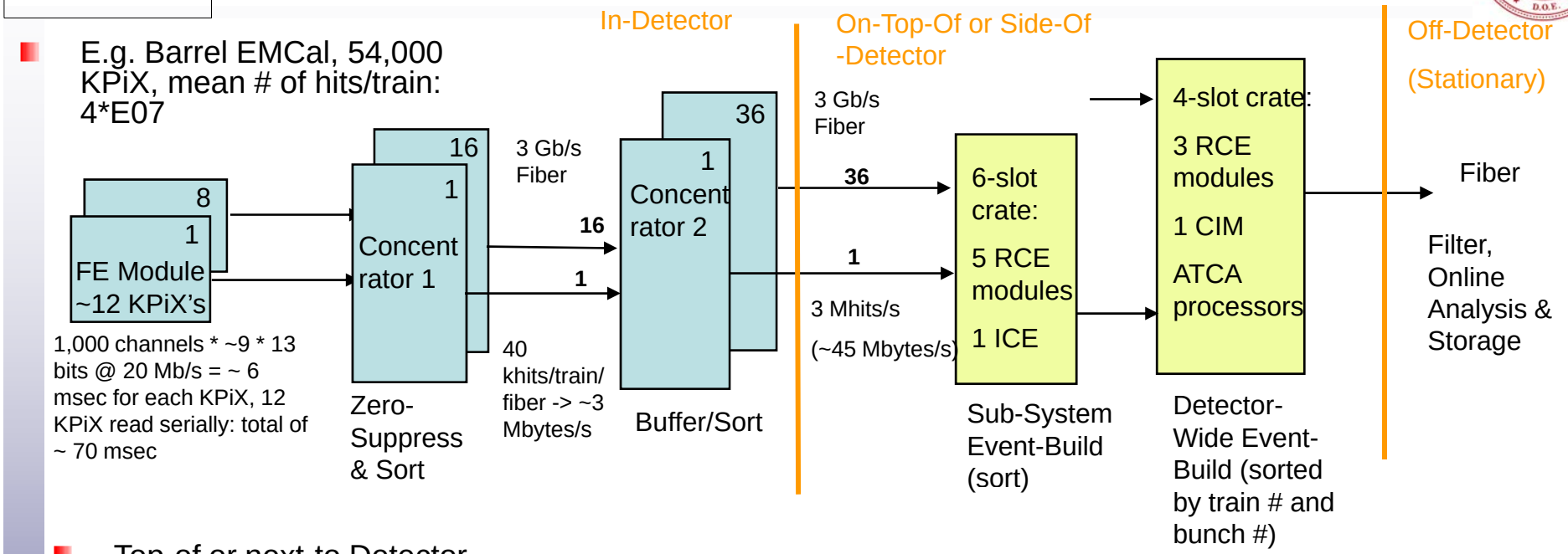
EM Barrel Example (Cold)



- Top-of or next-to Detector
  - Readout to outside-Detector crates via 3 Gbit/s fibers
    - Single 6-slot crate to receive 36 fibers: 5 RCE modules + 1 Cluster Interconnect Module (CIM)
  - Total out of EM Barrel partition: 1.6 Gbytes/s
    - Available bandwidth: > 80 Gbit/s (and is scalable)
  - Sorting, data reduction
- Can be switched into ATCA processors for data-filtering/reduction or online farm
  - A few 10-G Ethernet fibers off detector

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Warm-Machine Assumptions

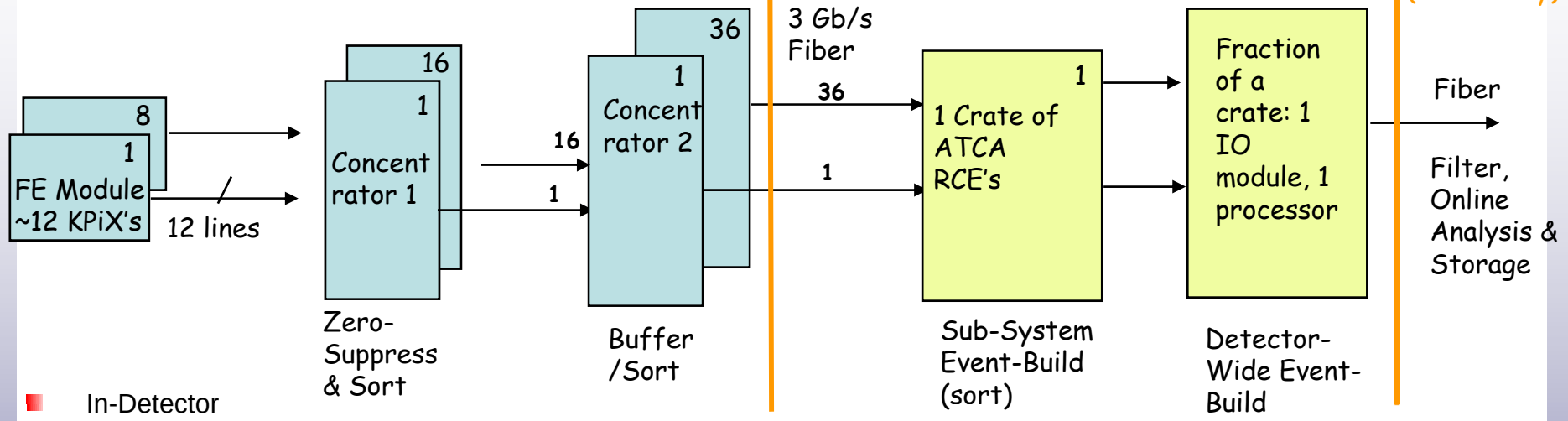
- 100 ns to 1000 ns train length
- 100 Hz to 1KHz train spacing
- Hits: depends on sub-system.
  - look here at calorimeter, assume for now 1 hit per train
    - get 50 nsec granularity when hit occurred in train

EM Barrel Example

- 1000 channels for each KPIX
  - Still don't need zero-suppression on KPIX
    - Settle + digitize: 400 usec
  - Readout: 1024 channels x 2 words x 14 bits x 50 nsec = 573 nsec
  - Requires some modification to optimize data in the readout structure

EM Barrel Example

- E.g. Barrel EMCal, 54,000 KPiX



- In-Detector
  - KPiX Readout via two levels of concentrator boards (FPGA-based, reconfigurable)
  - L1 concentrator: zero-suppress. Sort total 20 hits/train/Kpix -> 20 hits * (2 words of 14 bits + 26 bit total system address) * 1 KHz * 96 KPIX;s = 12 Mbytes/sec
  - To L2 concentrator:
    - Out of L2 concentrator: 12 Mbytes/sec * 16 = 192 Mbytes/sec
  - Readout to On-Top-Of-Detector crates via 3 Gbit/s fibers
    - Only need 1 fiber, assume 2
- On-Top-Of-Detector
  - Event-Builder for sub-system
- Off-Detector (Stationary)
  - Filter, Online-Analysis, Storage

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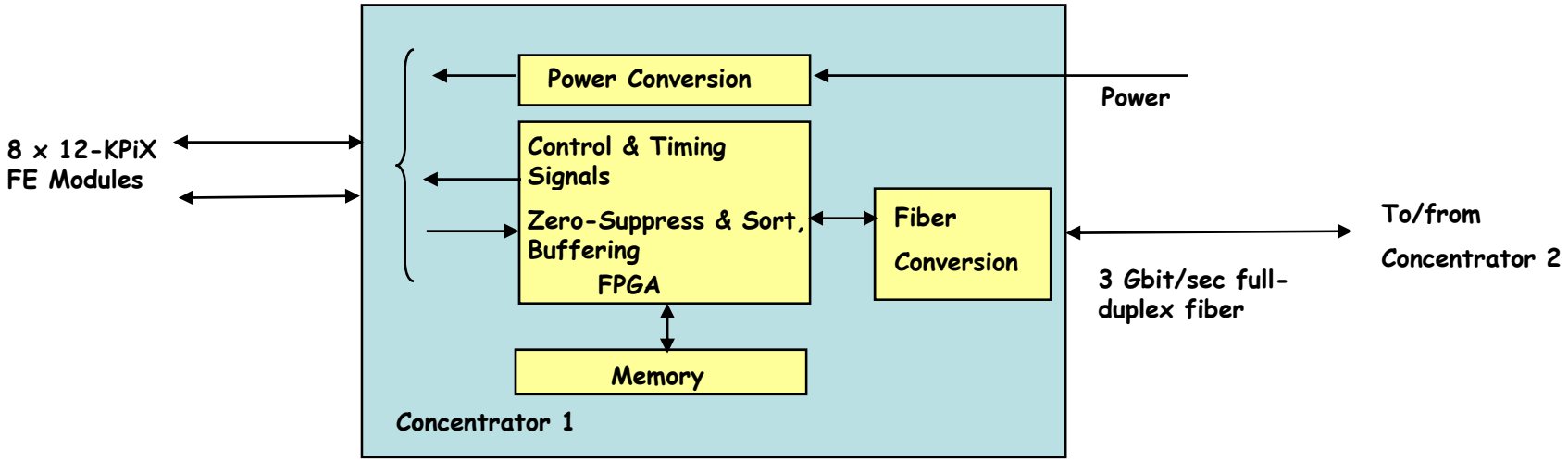
Concentrator-1



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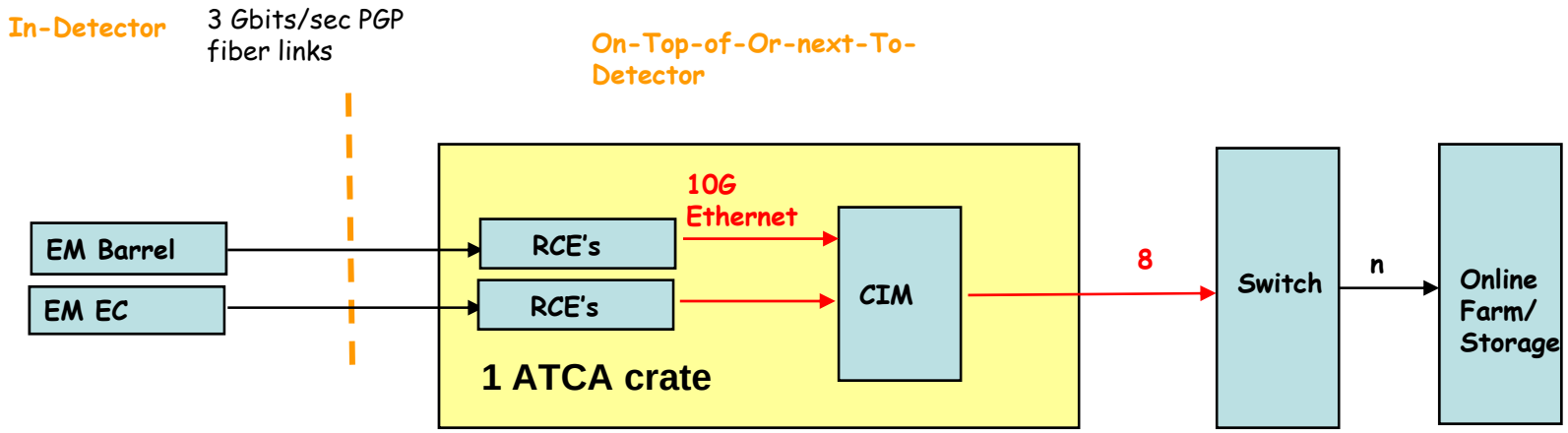
DAQ Architecture



- 1 ATCA crate for each sub-system for partitioning reasons
  - Two custom modules
    - RCE: Reconfigurable Cluster Element
    - CIM: Cluster Interconnect Module

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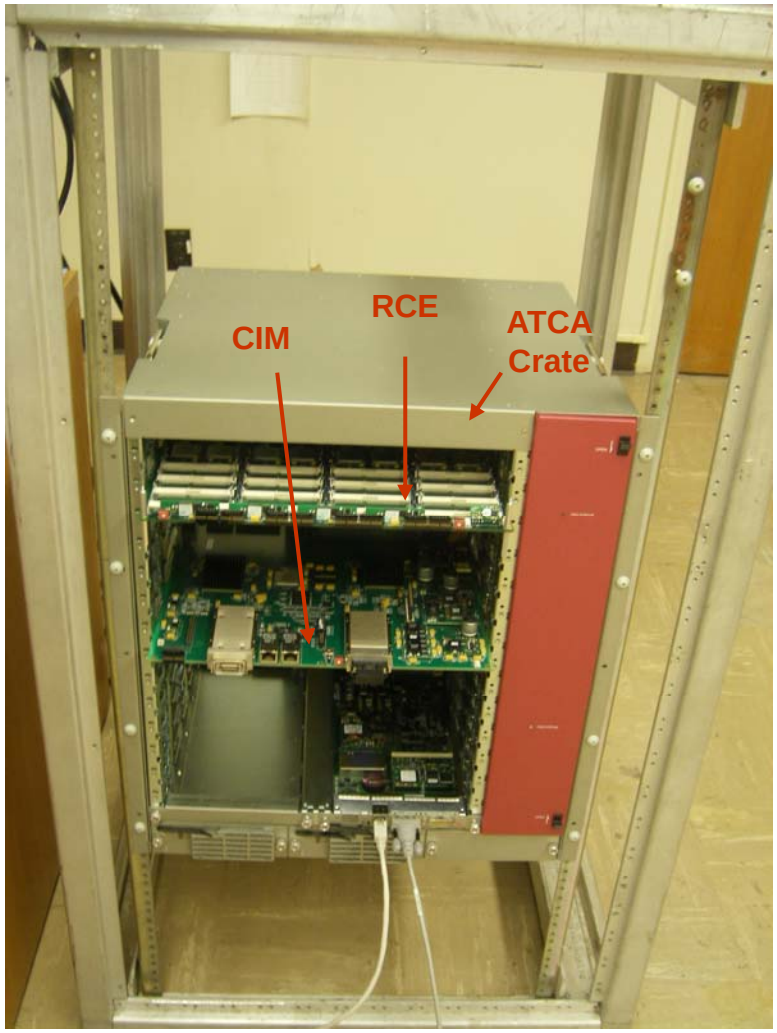
DAQ Sub-System

- Based on ATCA (Advanced Telecommunications Computing Architecture)
  - Next generation of “carrier grade” communication equipment
  - Driven by telecom industry
  - Incorporates latest trends in high speed interconnect, next generation processors and improved Reliability, Availability, and Serviceability (RAS)
  - Essentially instead of parallel bus backplanes, uses high-speed serial communication and advanced switch technology within and between modules, plus redundant power, etc

ATCA Crate

- ATCA used for e.g. SLAC LUSI (LCLS Ultra-fast Science Instruments) detector readout for Linac Coherent Light Source hard X-ray laser project
  - Based on 10-Gigabit Ethernet backplane serial communication fabric
- 2 custom boards
  - Reconfigurable Cluster Element (RCE) Module
    - Interface to detector
    - Up to 8 x 2.5 Gbit/sec links to detector modules
  - Cluster Interconnect Module (CIM)
    - Managed 24-port 10-G Ethernet switching
- One ATCA crate can hold up to 14 RCE's & 2 CIM's
  - Essentially 480 Gbit/sec switch capacity
  - SiD needs only ~ 320 Gbit/sec including factor of 4 margin
  - Plus would use more than one crate (partitioning)



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Reconfigurable Cluster Element (RCE) Boards

- Addresses performance issues with off-shelf hardware
  - Processing/switching limited by CPU-memory sub-system and not # of MIPS of CPU
  - Scalability
  - Cost
  - Networking architecture
- Reconfigurable Cluster Element module with 2 each of following
  - Virtex-4 FPGA
    - 2 PowerPC processors IP cores
  - 512 Mbyte RLDRAM
  - 8 Gbytes/sec cpu-data memory interface
  - 10-G Ethernet event data interface
  - 1-G Ethernet control interface
  - RTEMS operating system
  - EPICS
  - up to 512 Gbyte of FLASH memory

Cluster Interconnect Module

- Network card
  - 2 x 24-port 10-G Ethernet Fulcrum switch ASICs
  - Managed via Virtex-4 FPGA
- Network card interconnects up to 14 in-crate RCE boards
- Network card interconnects multiple crates or farm machines

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Summary

- KPIX system can also be used for warm machine with some modest mods within KPIX
- Event data rate for SiD can be handled by current technology, e.g. ATCA system being built for LCLS
  - SiD data rate dominated by noise & background hits
  - Can use standard ATCA crate technology with e.g. existing SLAC custom cluster elements and switch/network modules
- No filtering required in DAQ. Could move event data to online farm/off-line for further filtering/analysis
  - Still: investigate filtering in ATCA processors

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