

The MAPS ECAL

**SID Workshop
SLAC January 2008**

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University of Birmingham

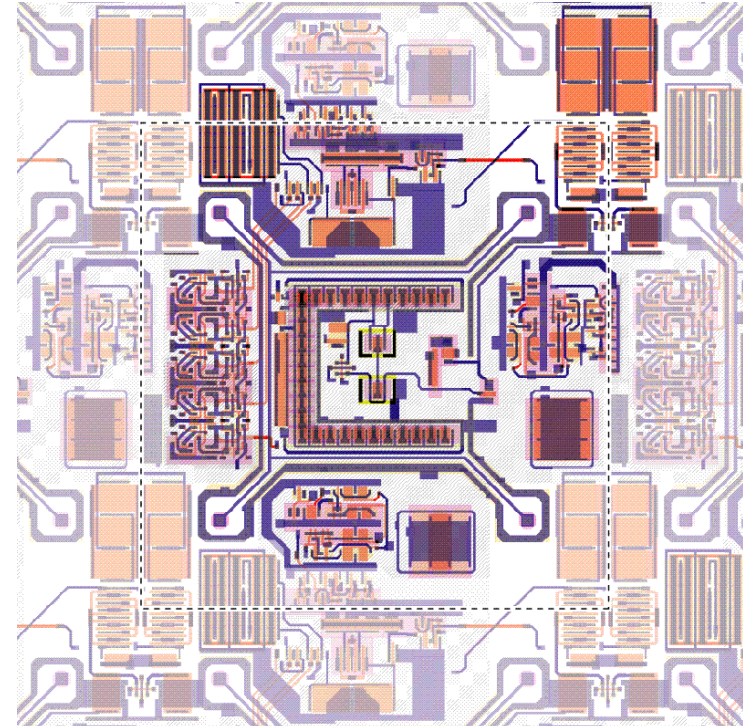
J.A. Ballin, P.D. Dauncey, A.-M. Magnan, M. Noy
Imperial College London

J.P. Crooks, M. Stanitzki, K.D. Stefanov, R. Turchetta, M. Tyndel, E.G. Villani
STFC-Rutherford Appleton Laboratory

Sensor specifications



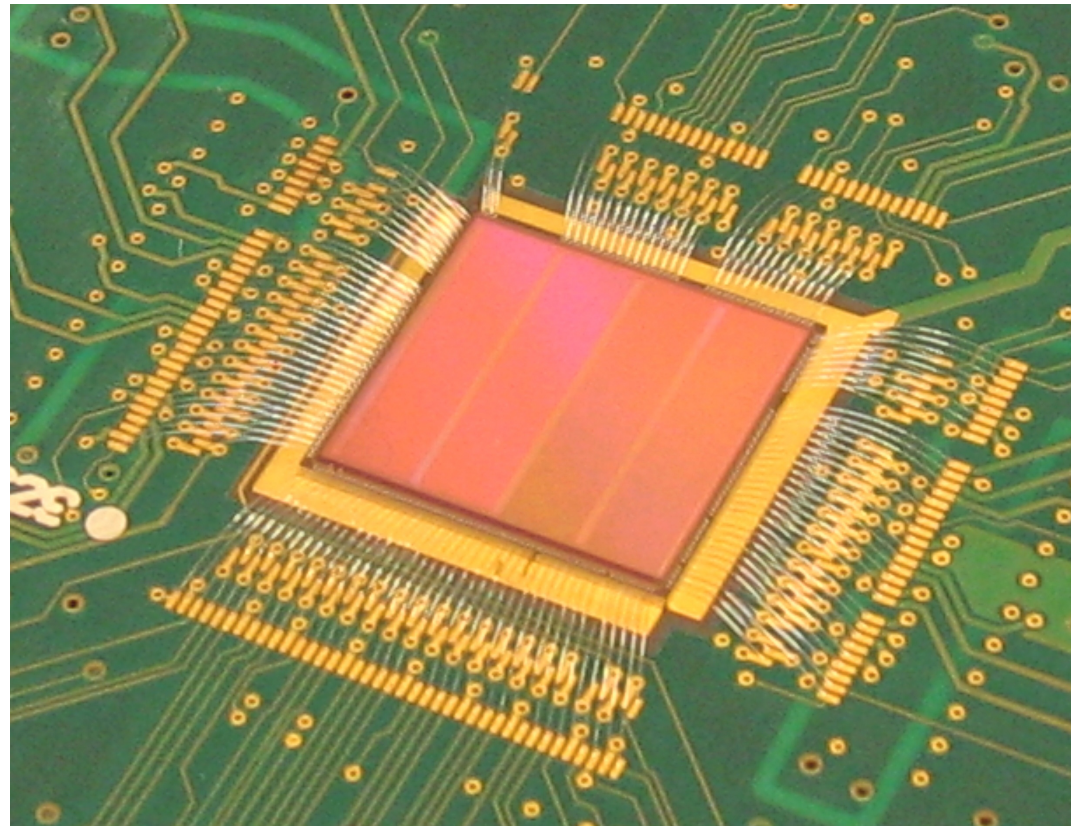
- 50x50 micron cell size
 - Binary Readout (Comparator)
 - 4 Diodes for Charge Collection
 - Time Stamping with 13 bits (8192 bunches)
 - Hit buffering for entire bunch train
 - Capability to mask individual pixels
 - Threshold adjustment for each pixel
- ⇒ Usage of INMAPS (deep-p well) process



The ASIC1 sensor



- Received in late July
- 0.18 microns CMOS INMAPS Process
- 168x168 Pixels
- 8.2 million transistors
- Test structures
- A lot of bond pads



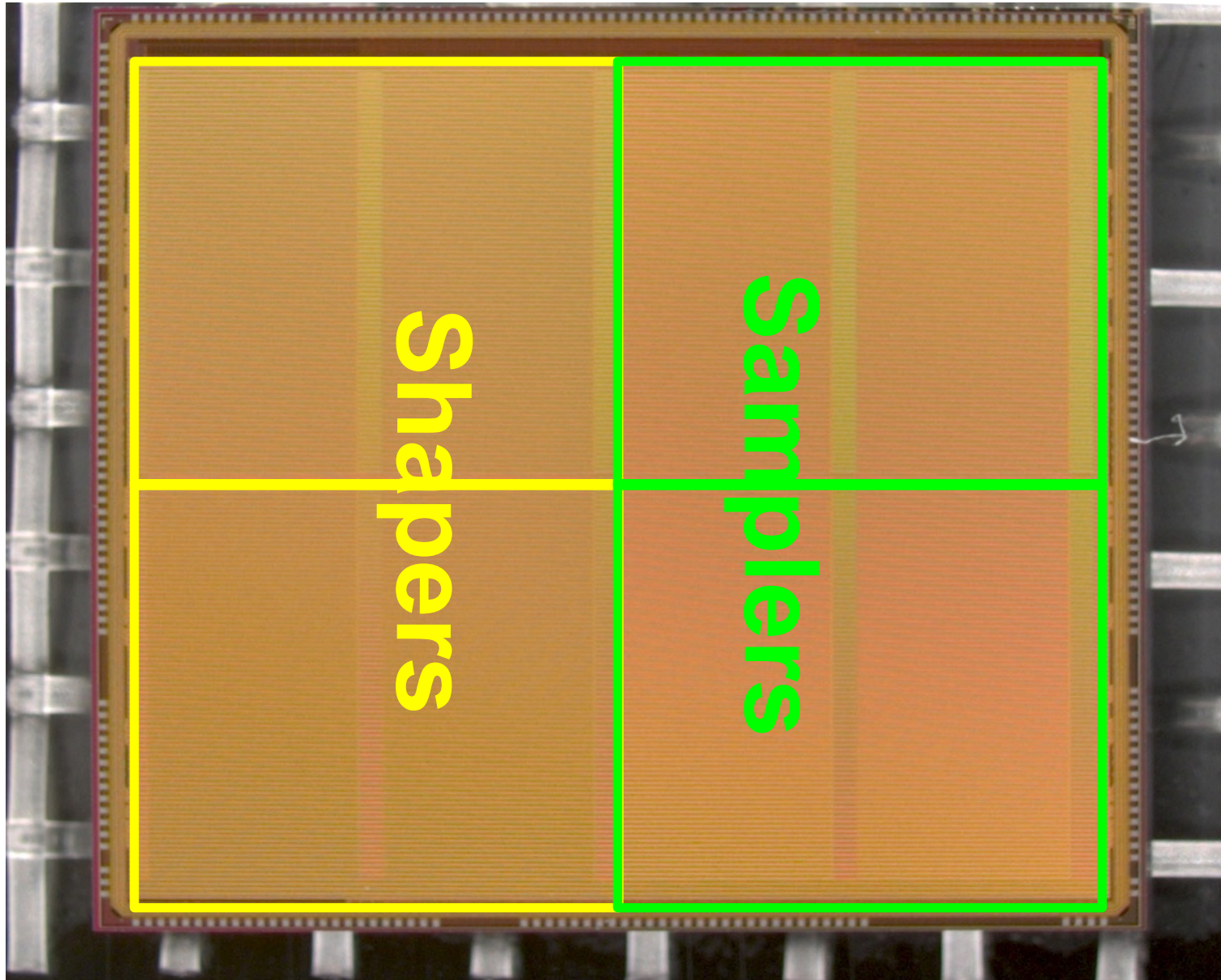
ASIC1 cont'd



- Two pixel architectures
 - Pre-Sampler
 - Pre-Shaper
- And for two capacitor configurations
 - As there were some issues with the circuit simulation
- 4 flavors of pixels
- 4 different processes
 - INMAPS 0.18 micron with 5/12 micron Epi
 - INMAPS 0.18 micron no deep p-well with 5/12 micron Epi
- Have about 300 chips



Illustrating ...



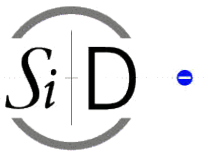
Sensor testing



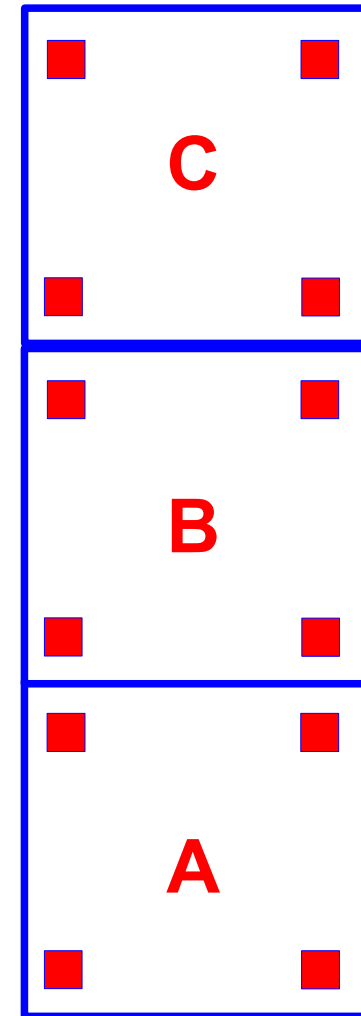
- Started testing program using several set-ups
 - Laser setup
 - analog characteristics
 - Pixel tests
 - Source runs with ^{55}Fe and ^{90}Sr
 - Test beam



The pixel test structures



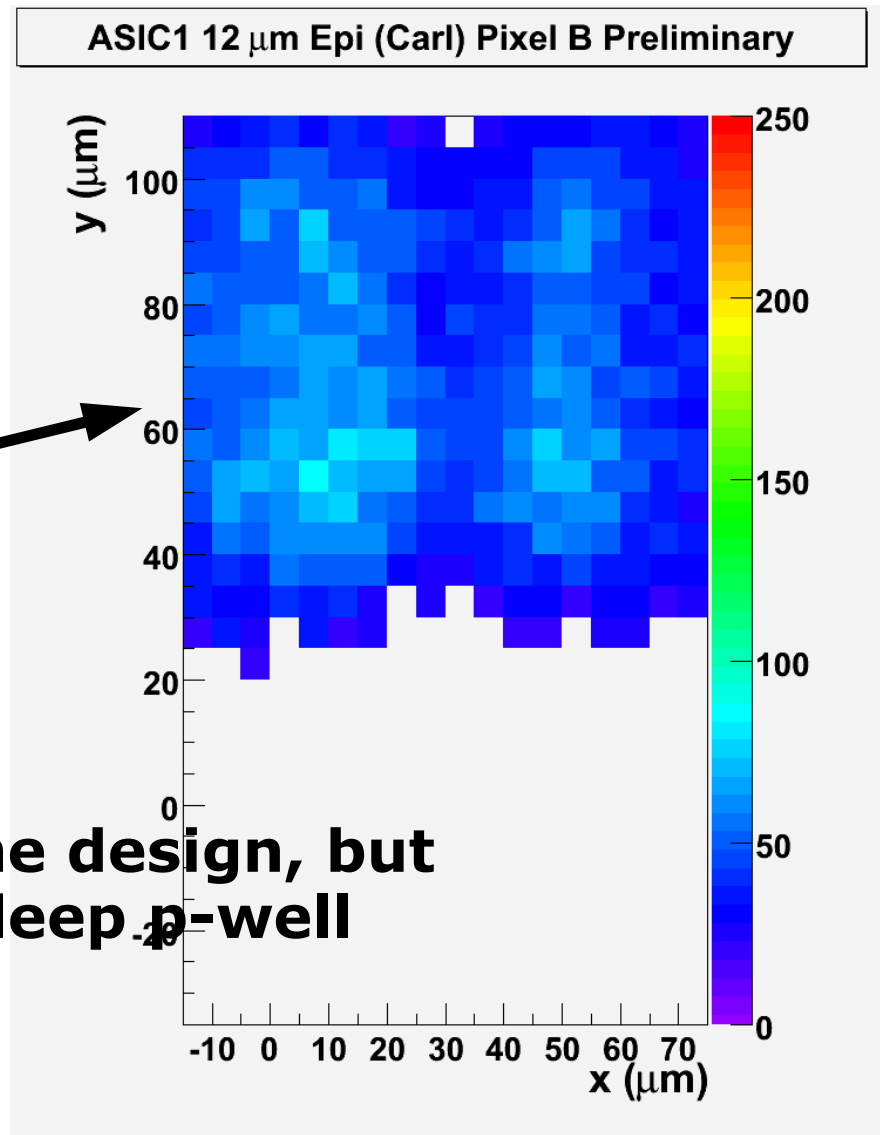
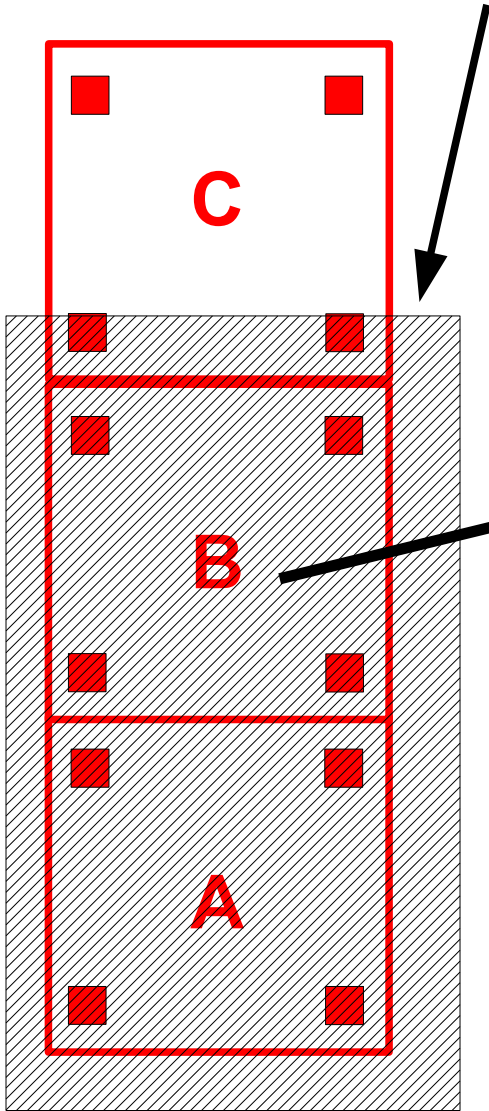
- 2 pixels with analog output (A & B)
- 1 Pixel not active & read out (C)
- Used for
 - Measurement of charge spread
 - Cross-check device simulations
 - Analog front-end testing
 - Gain calibration (to be done)
- All results are **PRELIMINARY**



No deep p-well ...

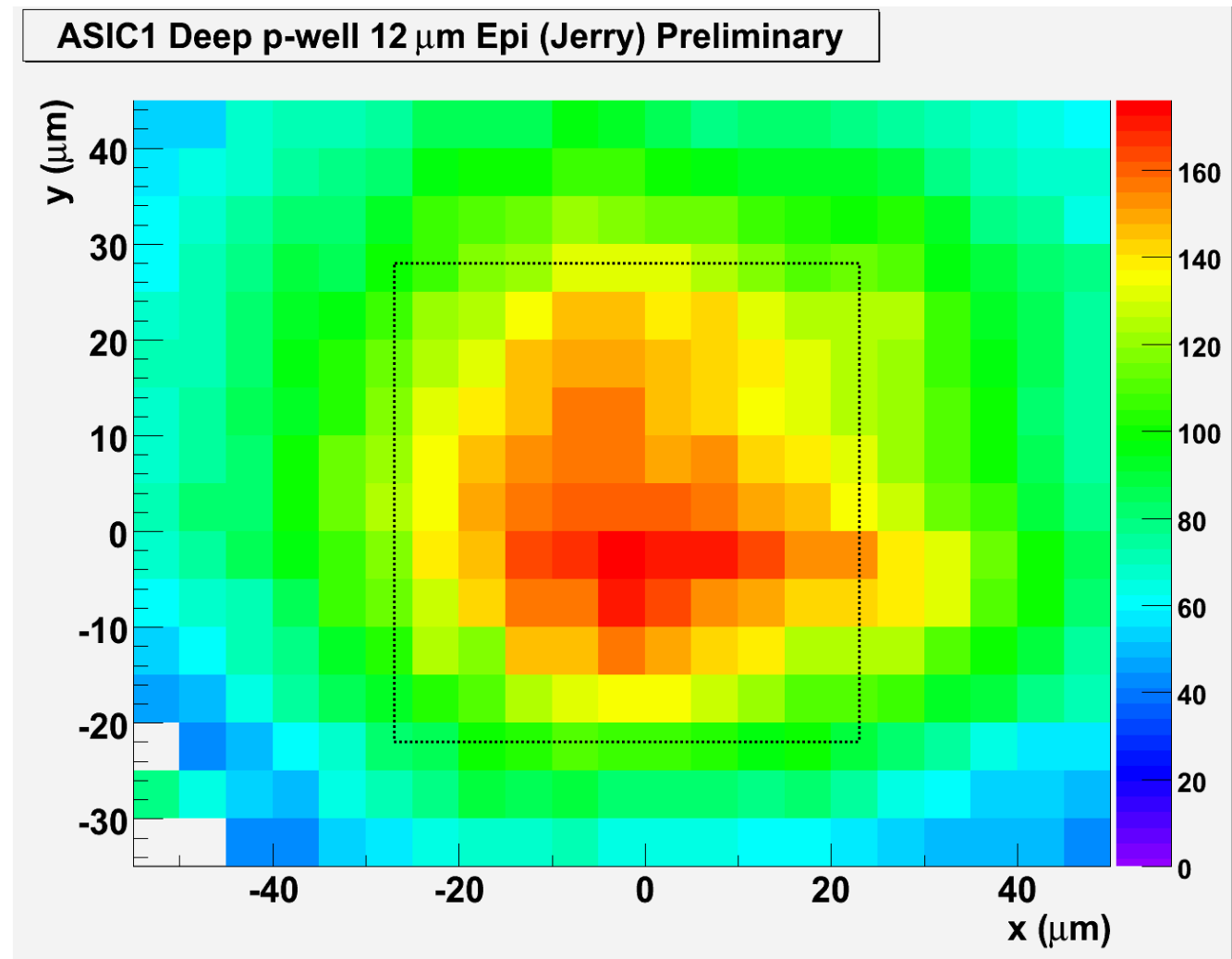
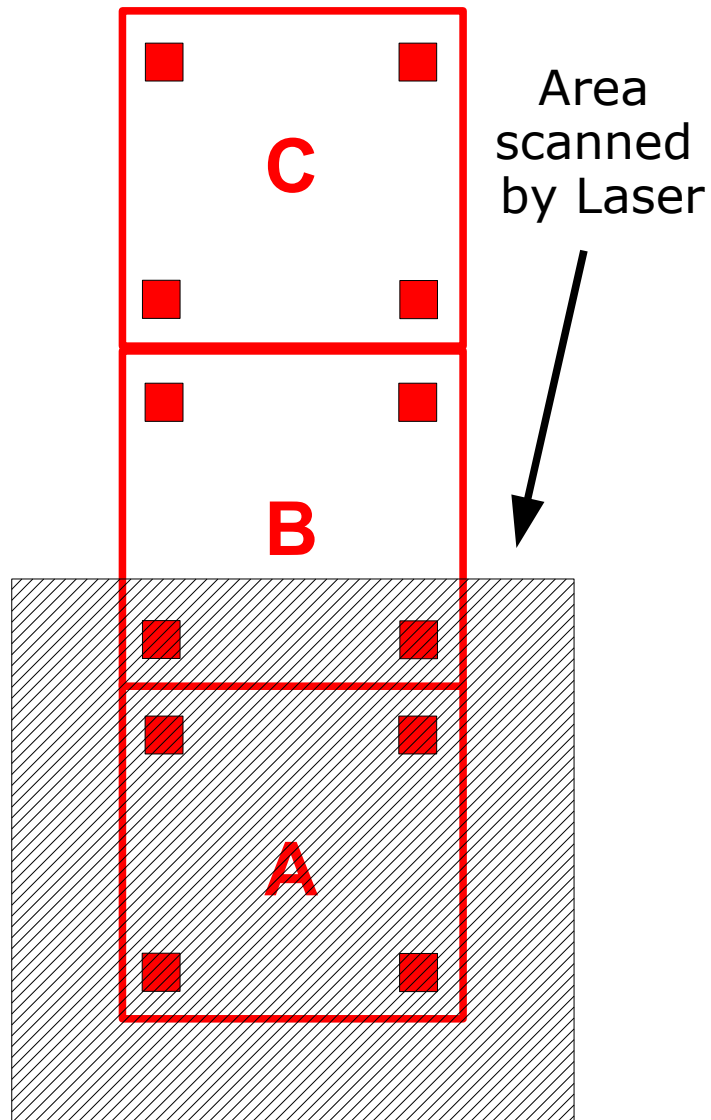


Area scanned by Laser



**Same design, but
no deep p-well**

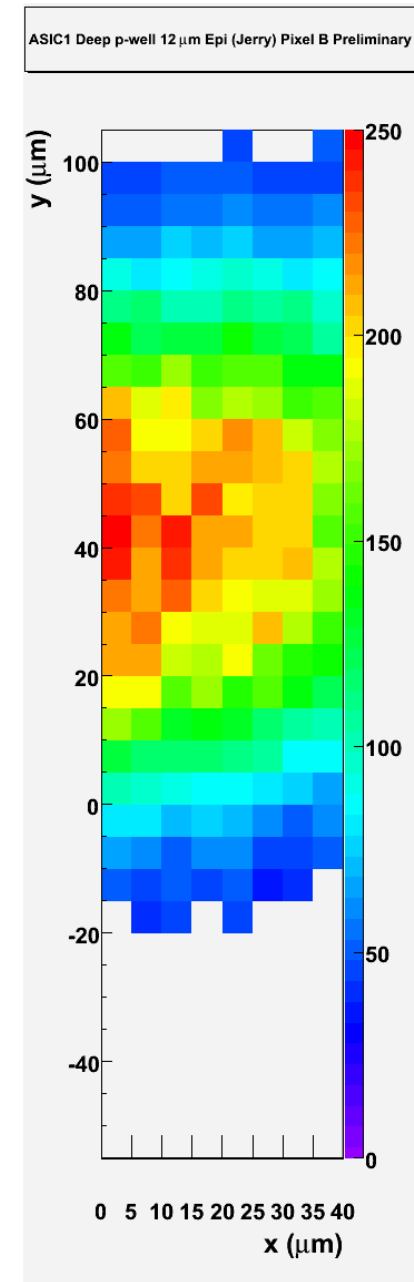
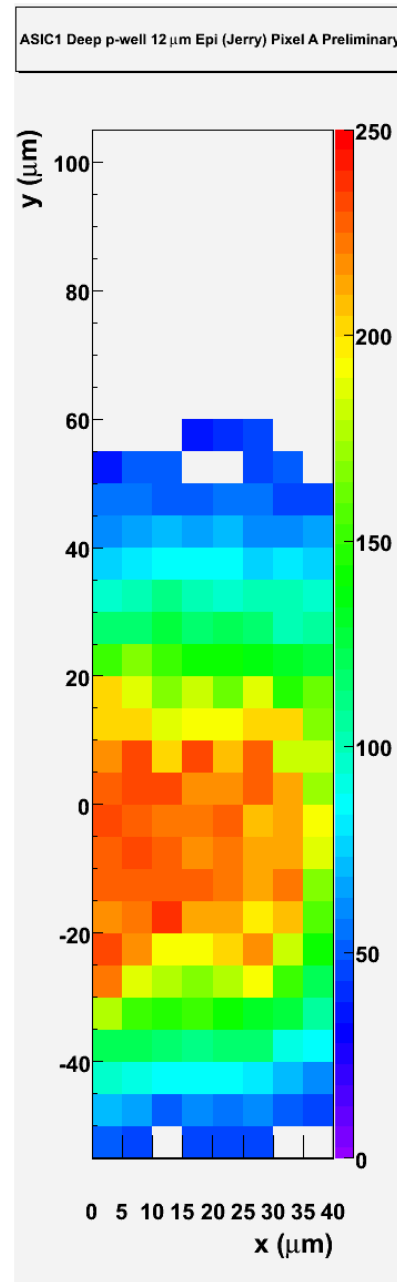
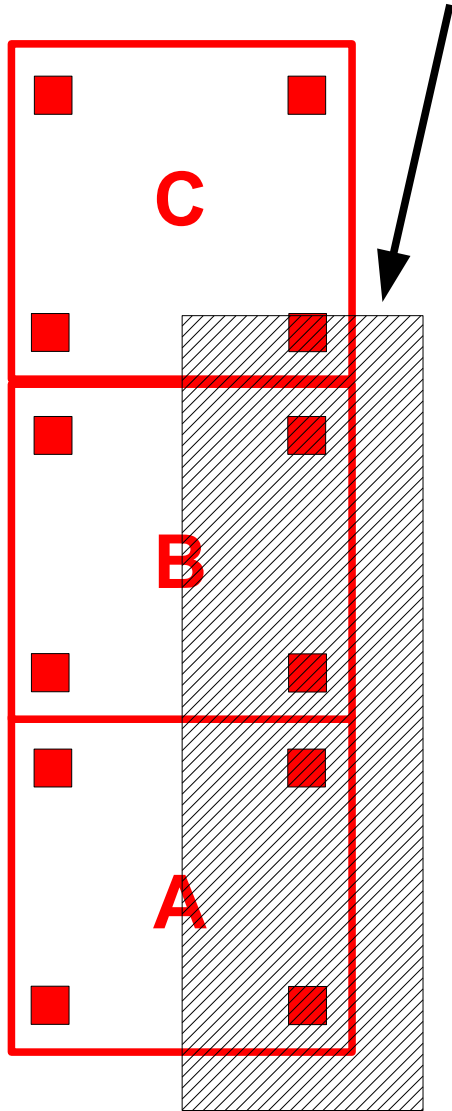
Deep p-well results (I)



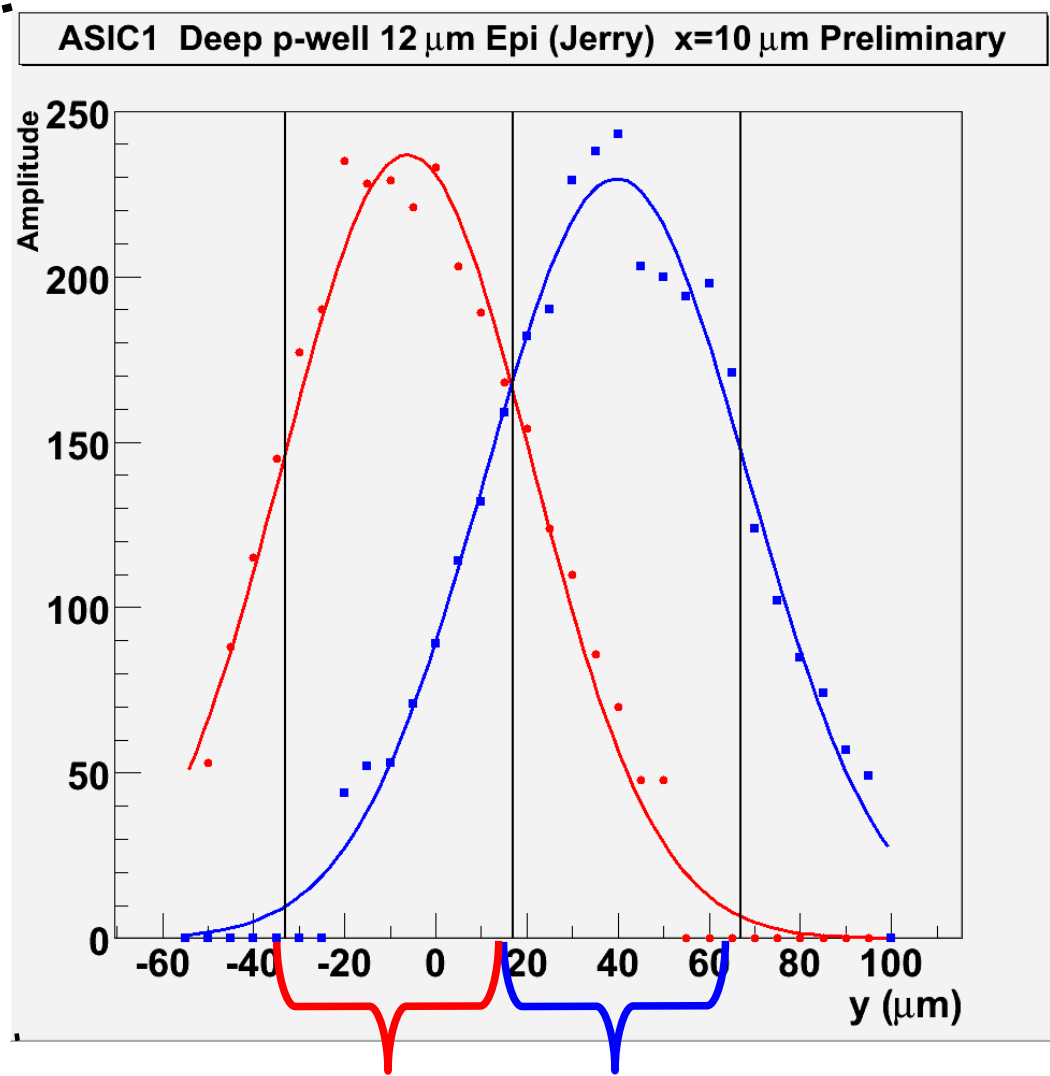
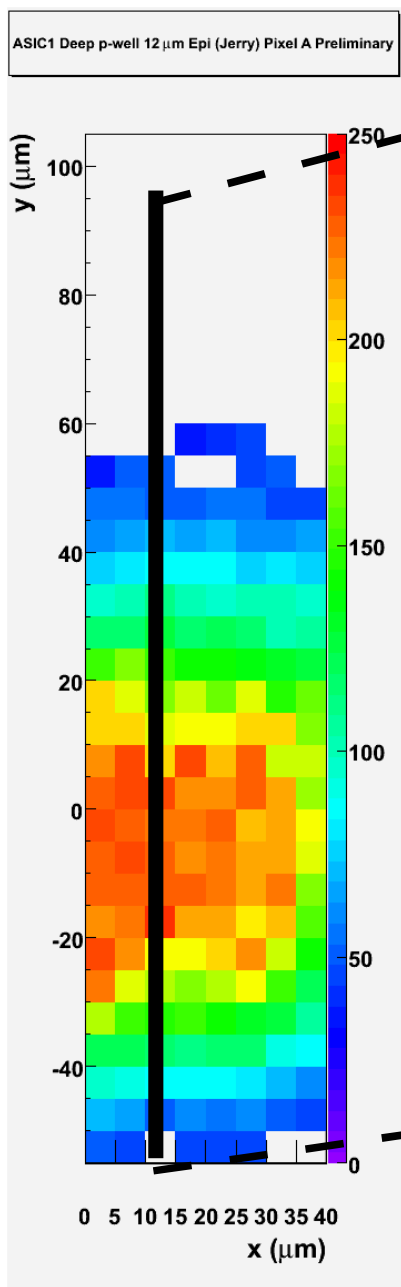
Deep p-well results (II)



Area scanned by Laser



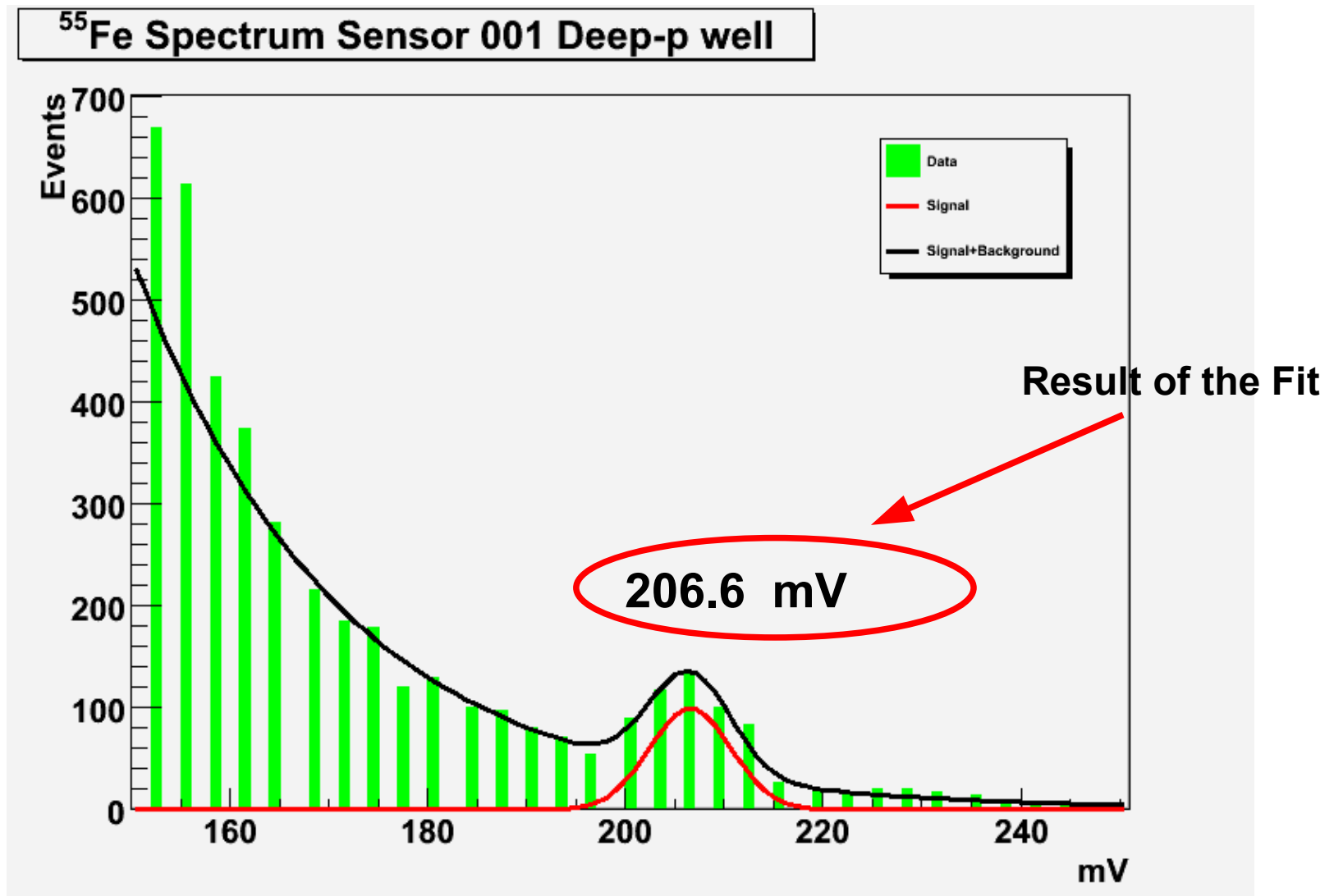
Deep p-well results (III)



Pixel A Pixel B



^{55}Fe Spectrum



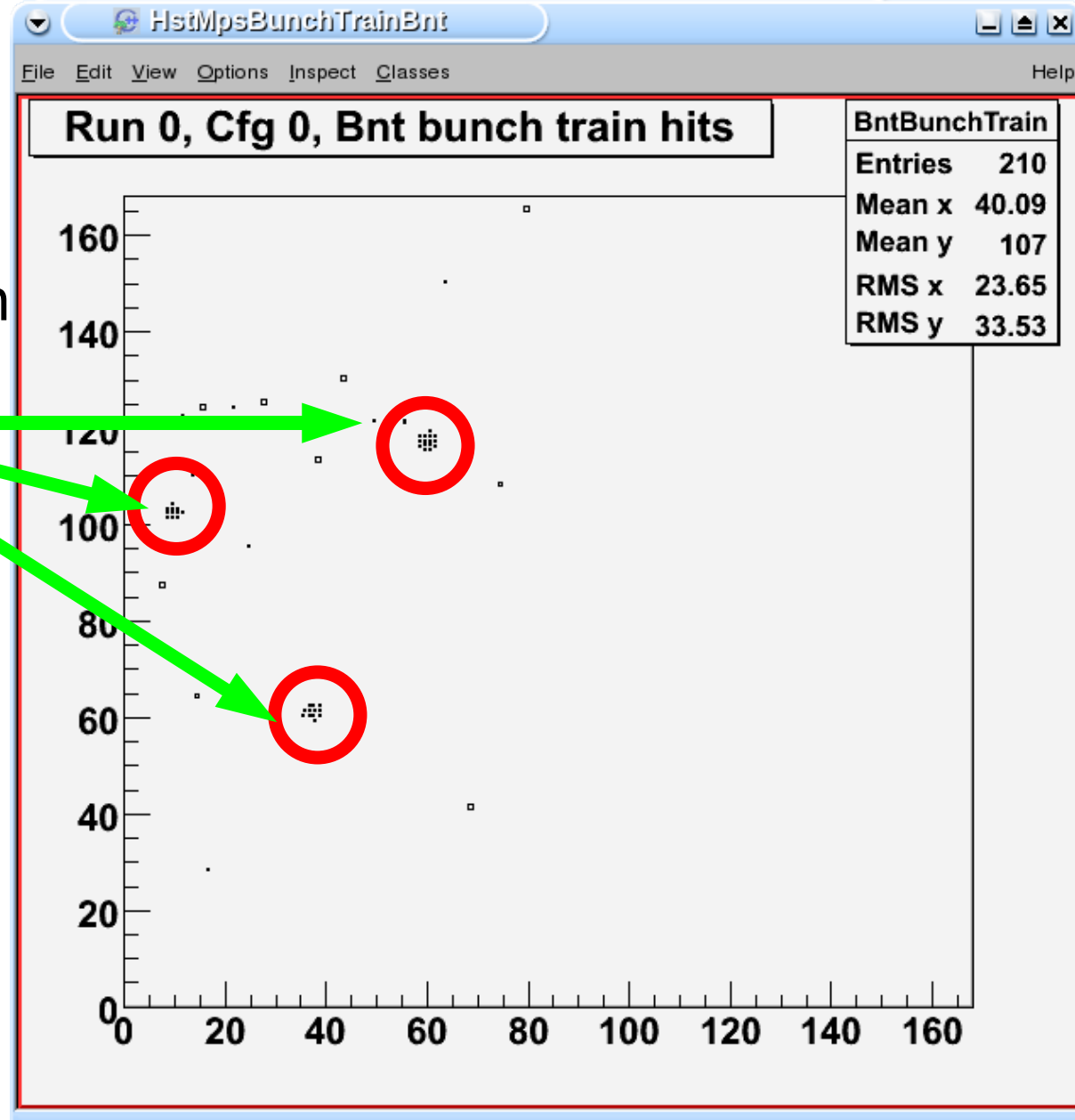
^{55}Fe gammas (5.7 KeV) :1620 electrons signal
Done using the analog test pixels: Gain $\sim 127 \mu\text{V}/\text{e}$



Results from Source runs



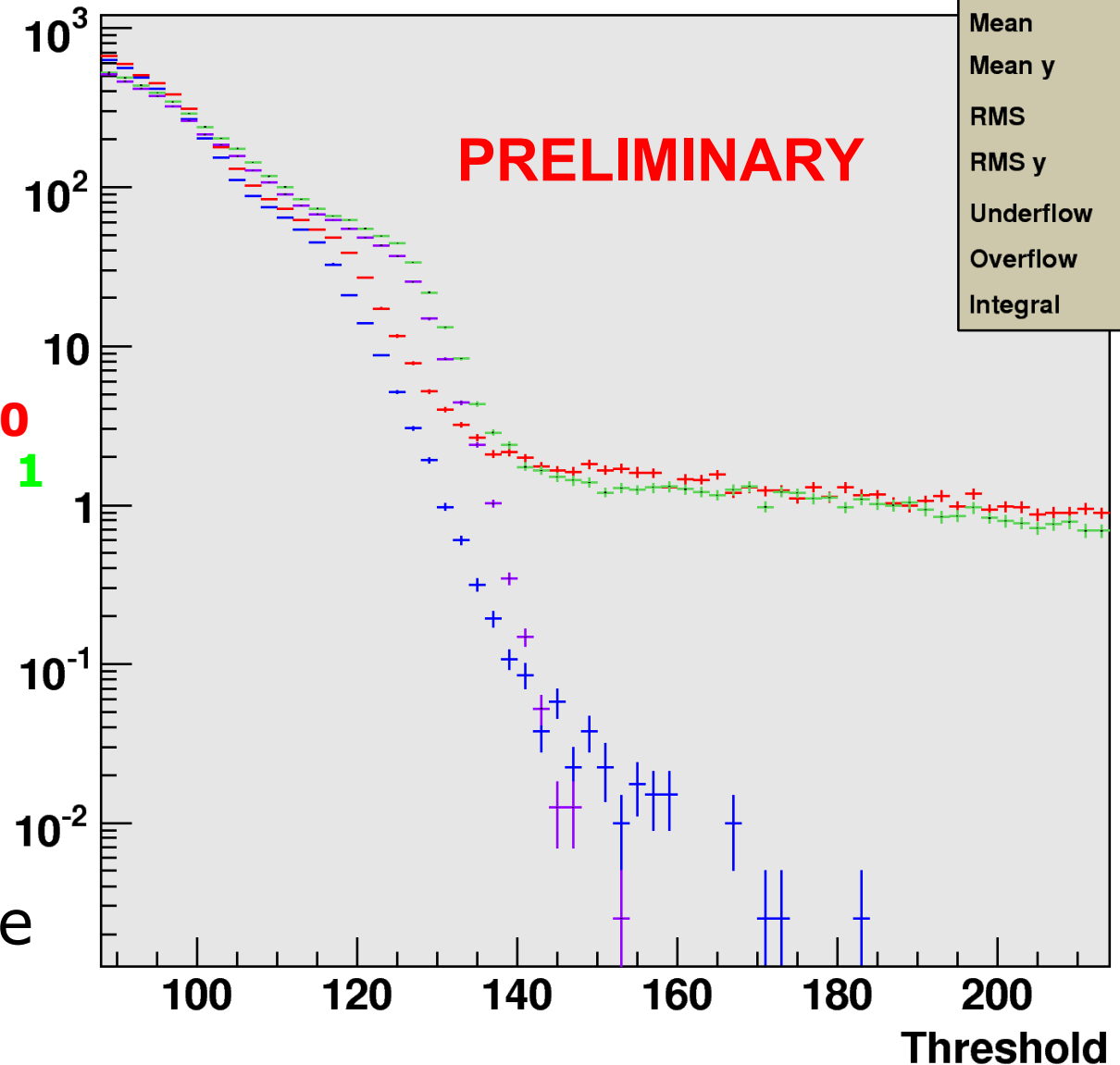
Clusters from ^{241}Am



Cont'd



Hits by region



red - with source, region 0
green - with source, region 1
blue - no source, region 0
purple - no source, region 1

Made using a β source

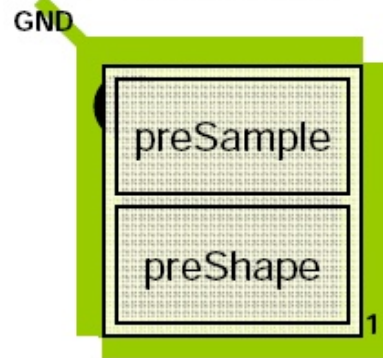
Thermal Properties



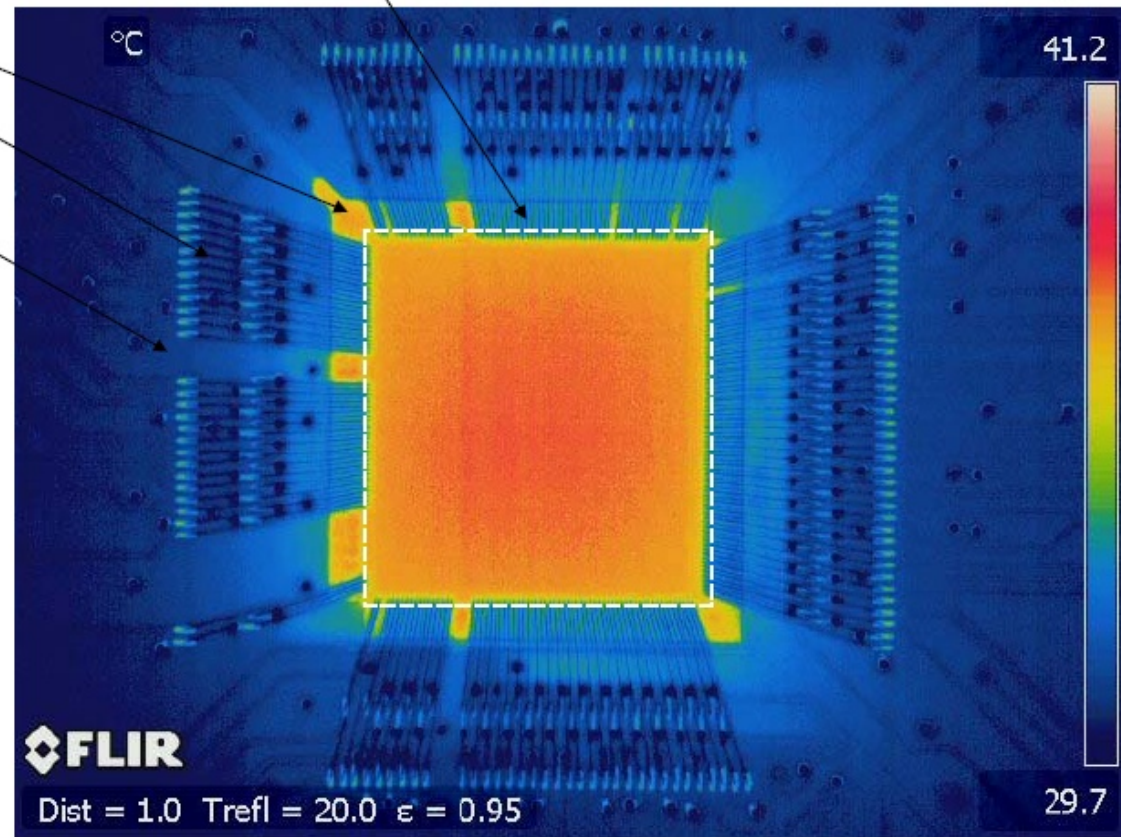
Orientation: Chip top view

- Temp scale
- Chip outline
- Ground pad
- Bond wires
- PCB

- Orientation



IR_0018.jpg



Testbeam Setup



- TestBeam at DESY
 - 3-6 GeV electrons
- 4 Sensors
 - mounted in mechanical structure
 - 1 DAQ board per Sensor
 - Readout via USB 2.0
- Comment:
 - Got an window of opportunity : *Do it next week or in 9 month*



The DAQ



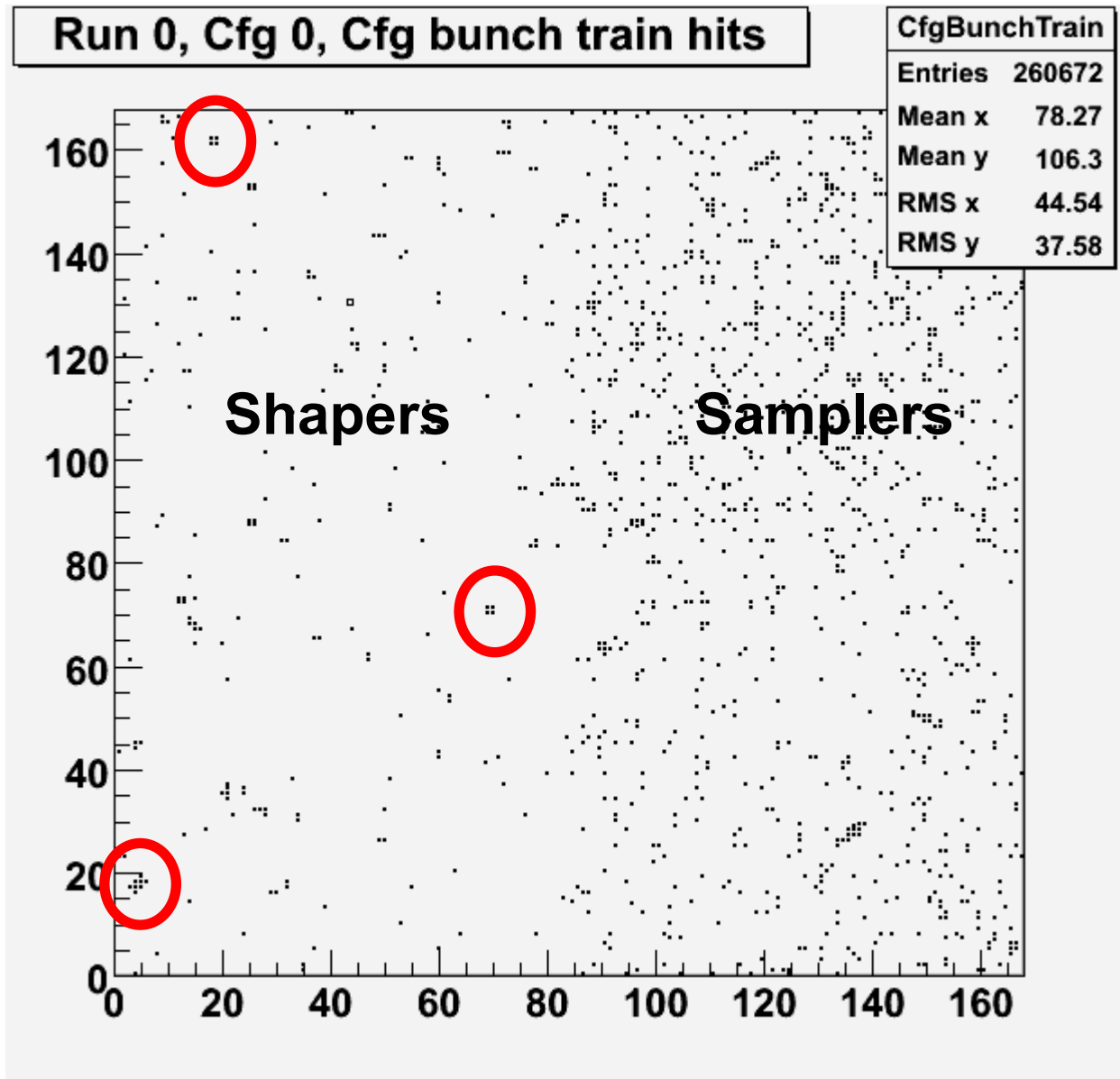
TestBeam Area 21



BEAM



First Hits



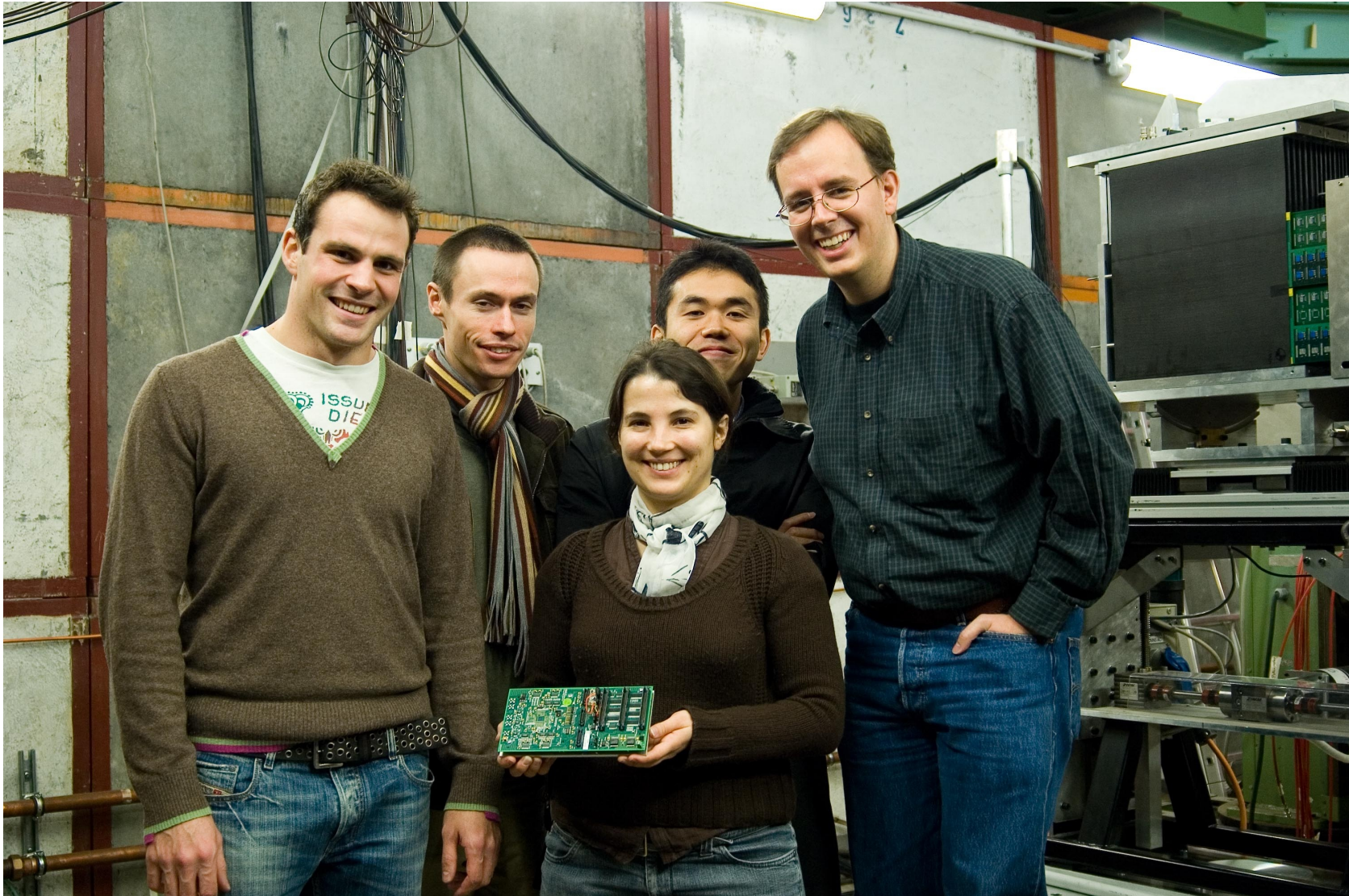
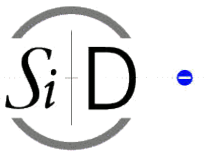
Some Comments



- The CHIP
 - worked stable and reliable
 - We are still analyzing the data (~100 GB)
 - So no quantitative statements yet
- DAQ
 - Smooth
 - basically no downtime
- We can qualitatively say
 - The chip works



The Testbeam Crew



The Future...



- Given the STFC's statements on the ILC ...
 - It is fair to say, that the future of the UK-ILC program isn't bright
 - *"We expect to put in a new proposal next year to continue the MAPS programme despite the recent UK announcement"*
 - Everything else is not clear yet

