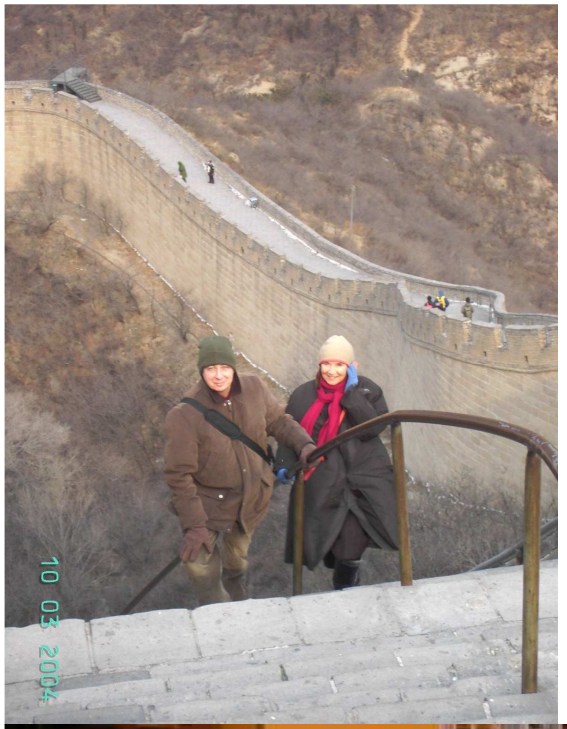
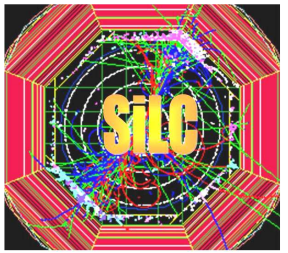


SiLC: What's new???

on behalf of SiLC Collaboration



Latest Advances on:

- R&D sensors
- R&D Electronics
- Mechanics
- Tests

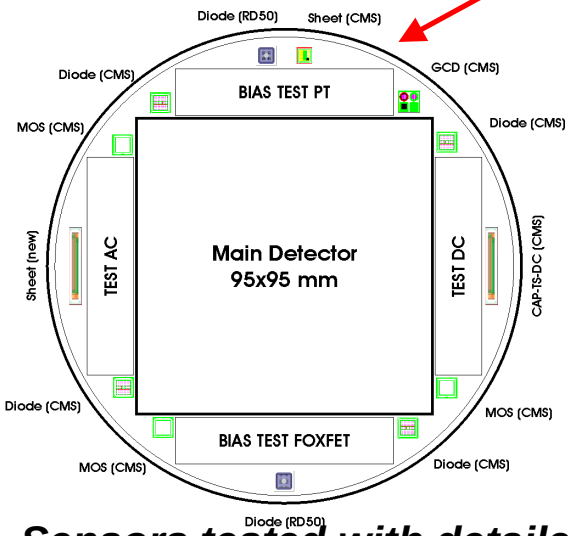
Perspectives 08-09

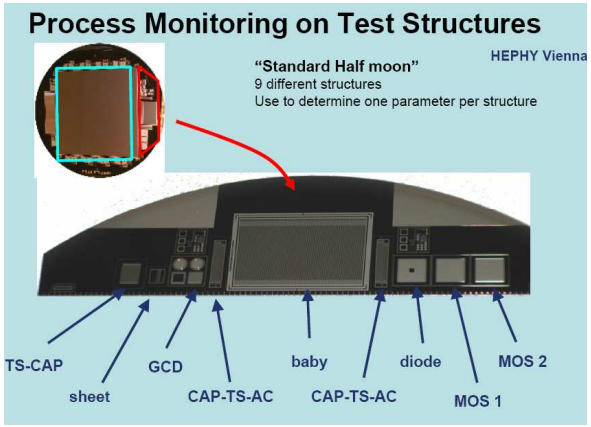
Progress made by SiLC since:
BILCW'07 review &
Update by A. Ruiz's at ALCPG-FNAL Oct 07

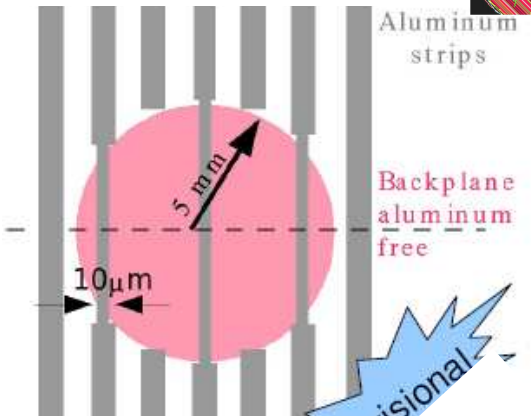
Aurore Savoy-Navarro, LPNHE/CNRS-IN2P3

- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beam

Presently new: HPK µstrips, **6'' wafer, but:**
pitch=50µm; thickness: 320µm; Length: 9.15cm,





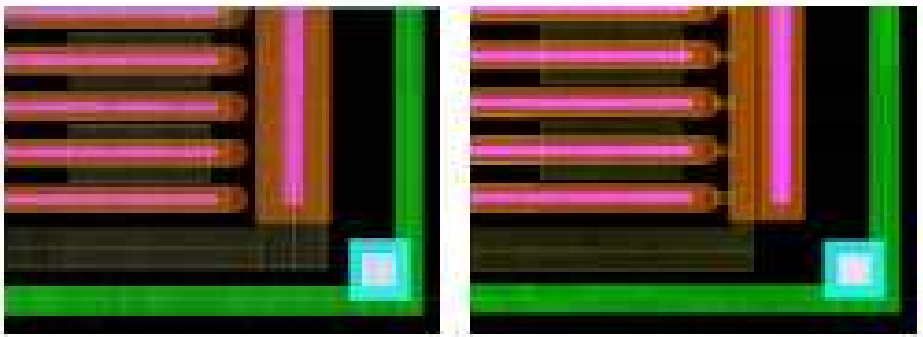


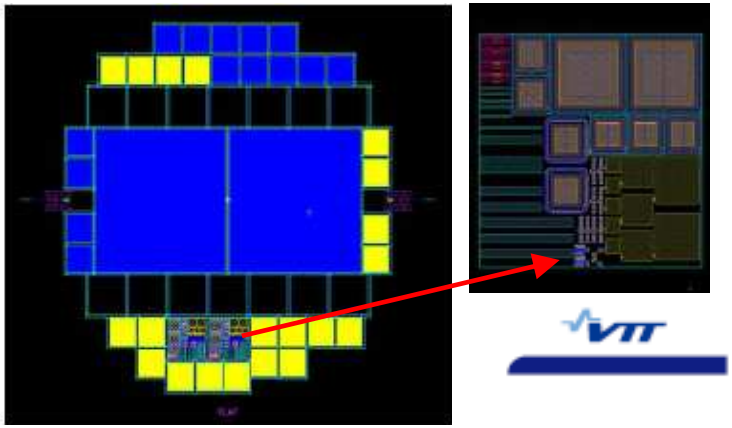
Test structures

5 sensors specially treated for laser alignment

Sensors tested with detailed QA control (HEPHY+IEKP)

New technological approach: 3D Planar µstrips:
Edgeless (hermetic), Low V, Lower Thickness, Faster, Rad hard, expected 03/08





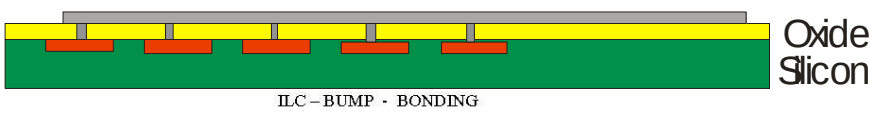
The biaising schemes for the ILC tracker's edge active strip Detector (left) punch through, and (right) FOXFET The detector Is biaised from one corner of the active edge (green)

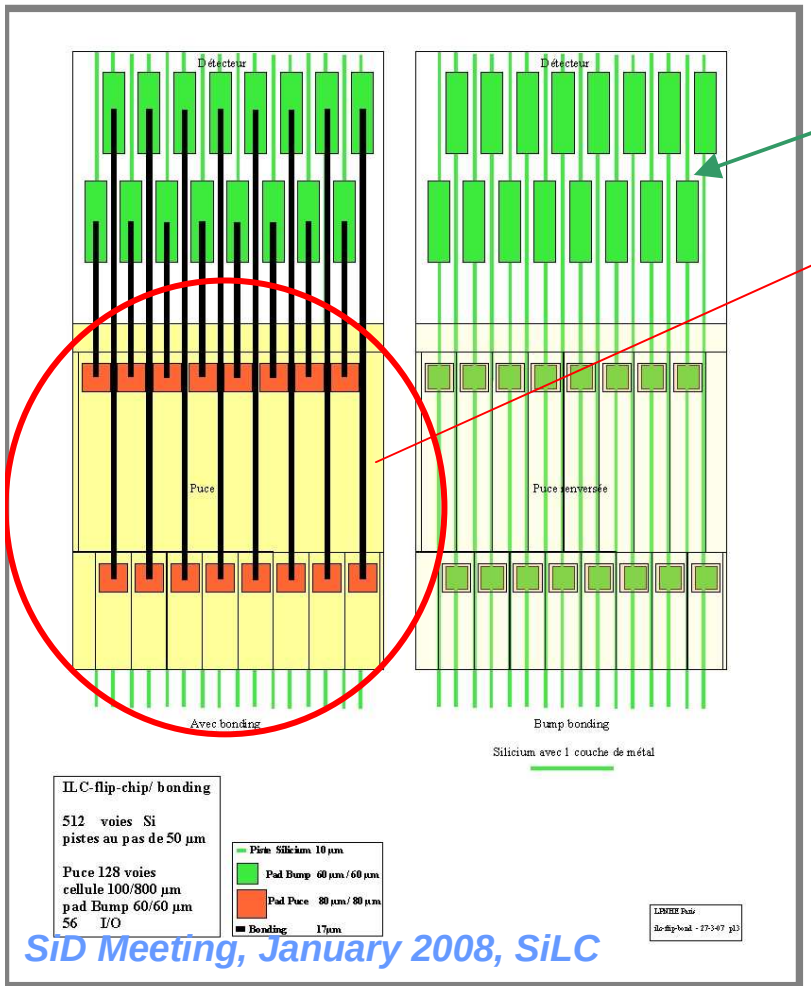
And a lot more also on pixels R&D

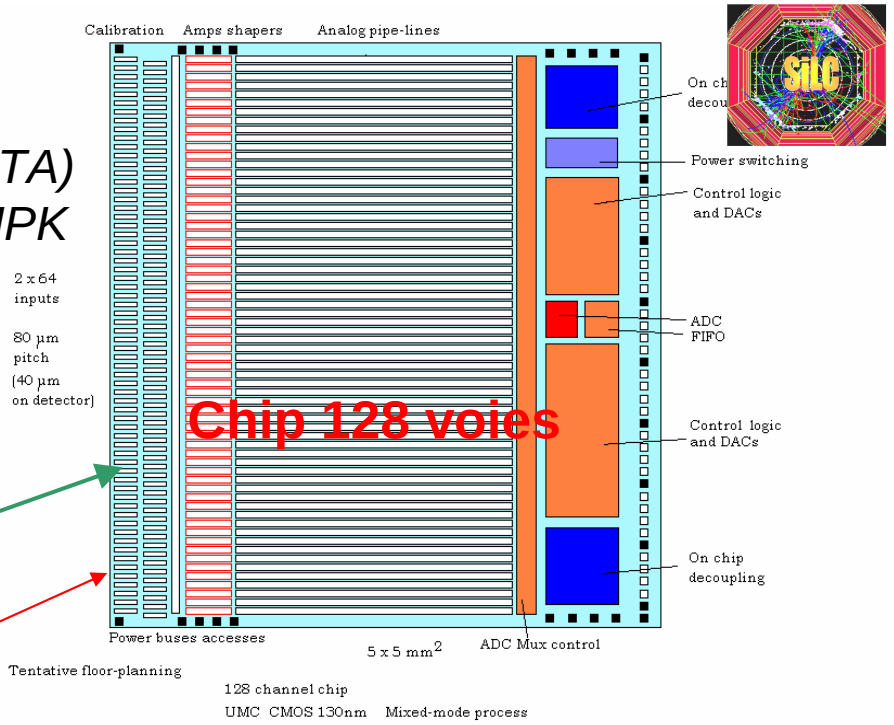
COLLABORATION HPK/LPNHE-IN2P3

Goal: develping new routing and inline pitch Technology for FE chip onto the strips(NdA + MTA)

1st try: SiTR_130-128 chip and presently new HPK sensors







Decrease %X_0: NO hybride & pitch adpater

1st approach (2008-2009):

Chip directly routed onto the strips by bump bonding

HPK: sensor + bonding of the chip

IN2P3: chip 128 voies

performance tests comparing new connection wrt hybride

Demonstrator: 2008, production 2009

Chip bonded sensors at the price of usual sensors

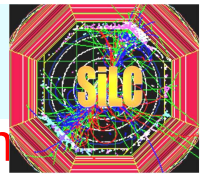
Futur: Technologie 3D pour µstrips & connection chip/µstrips

- R&D on sensors
- R&D on electronics:

HEAD ON THE SiTR-130_128

- Mechanics developments
- Test beams

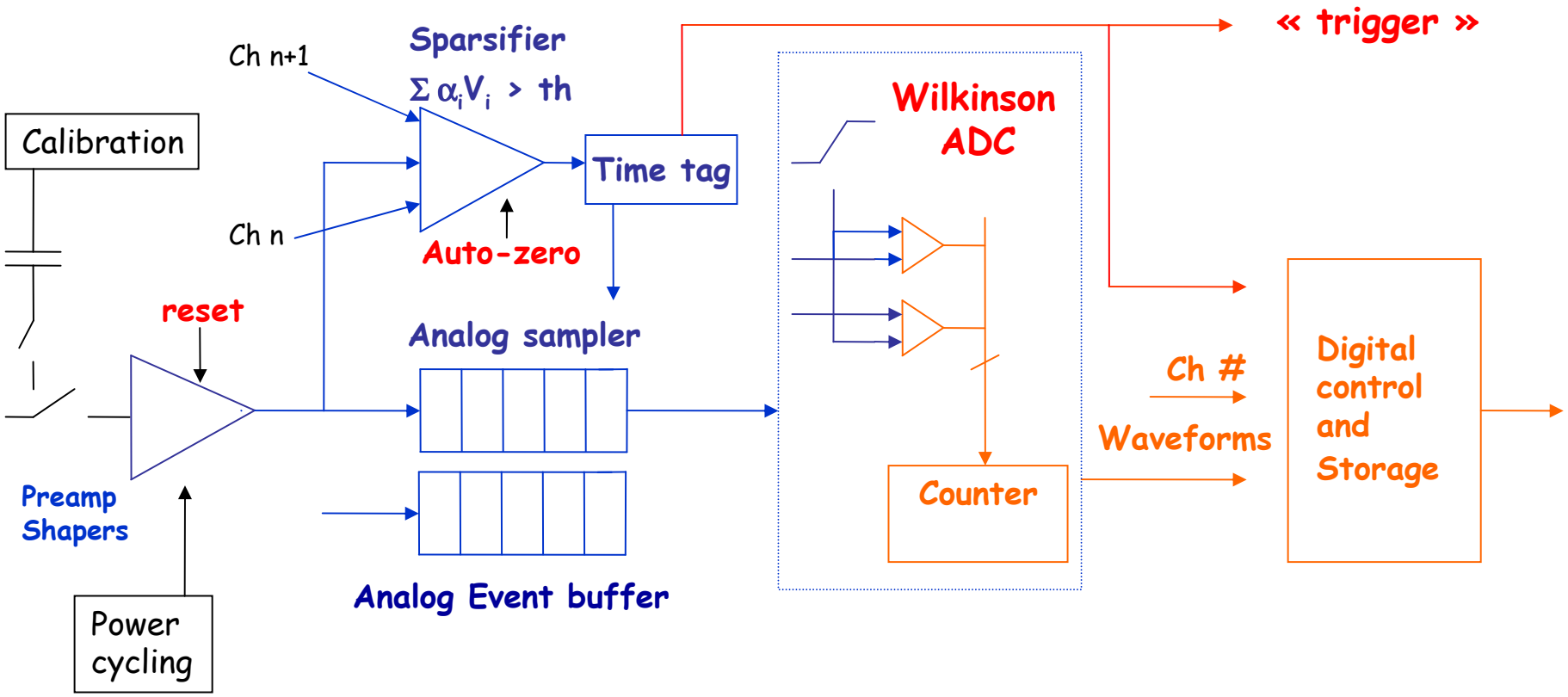
Functionalities to be integrated



- Full readout chain integration in a single chip, 512 or 1024 ch in 90nm
  - Preamp-shaper
  - Sparsification — Trigger decision on analog sums
  - Sampling — 8-deep sampling analog pipe-line
  - Analog event buffering: — Occupancy: 8-16 deep event buffer
  - On-chip digitization — 10-bit ADC
  - Buffering and pre-processing: Centroids, χ2 fits, lossless compression&error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

Amplifiers: - 30 mV/MIP over 30 MIP range
Shapers: - Two ranges: 500ns–1μs, 1μs-3μs
Sparsifier: - Threshold the sum of 3-5 adjacent channels
Samplers: - 8 samples at 80ns sampling clock period
- Event buffer 8 deep
Noise baseline: Measured with 180nm CMOS:
375 + 10.5 e-/pF @ 3 μs shaping, 210μW power dissipation
ADC: - 10 bits
Buffering, digital pre-processing
Calibration
Power switching can save a factor up to about 100

Front-end architecture



Charge 1-30 MIP, Time resolution: BC tagging 150-300ns
80ns analog pulse sampling

Technology: Deep Sub-Micron CMOS 130-90nm

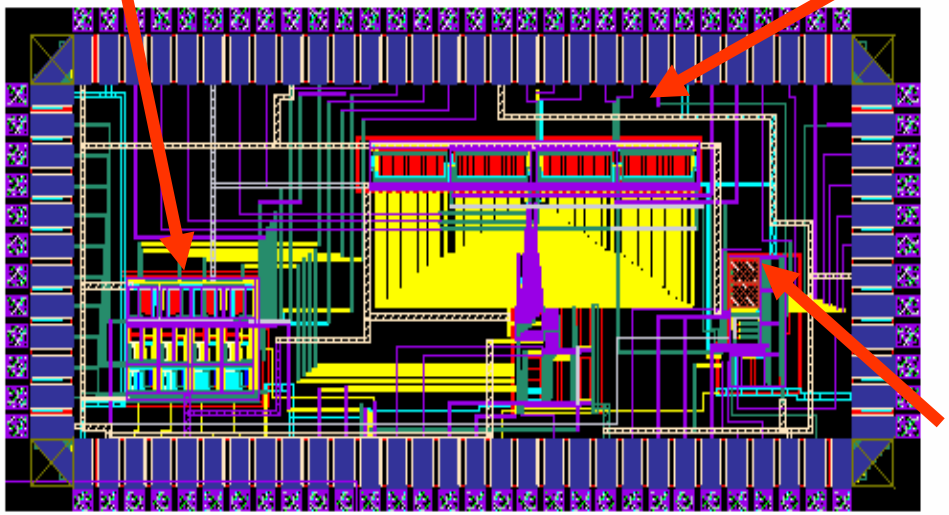
1 step: the 4-channel chip,SiTR-130_V1&2

(LPNHE-LAPP)

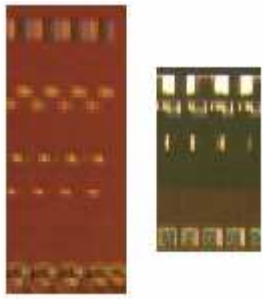
Amplifier, Shaper, Sparsifier 90*350 µm²

Analog sampler 250*100 µm²

layout



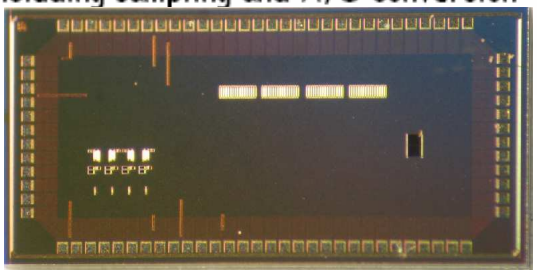
A/D 90*200 µm²



180nm 130nm

Layout of the 130nm chip including sampling and A/D conversion

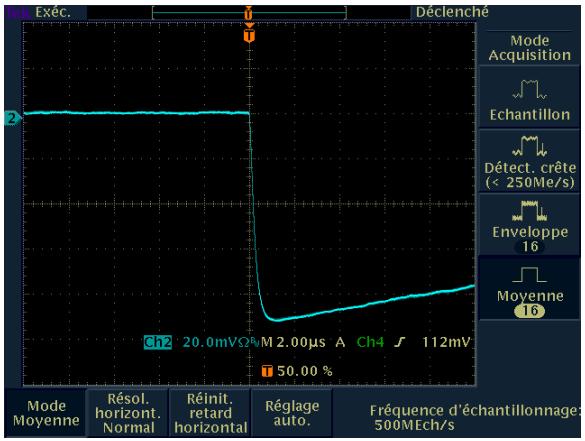
Photo



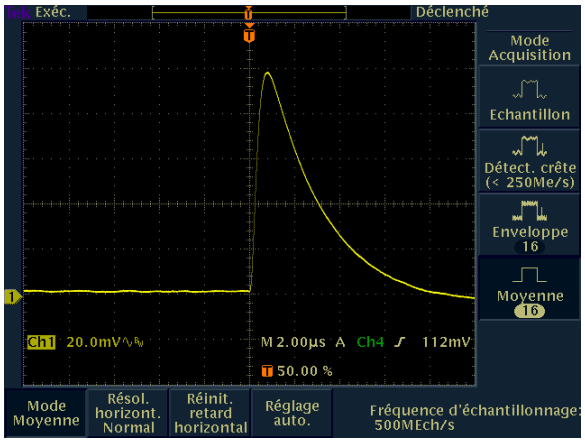
Preamplifier-shaper performances

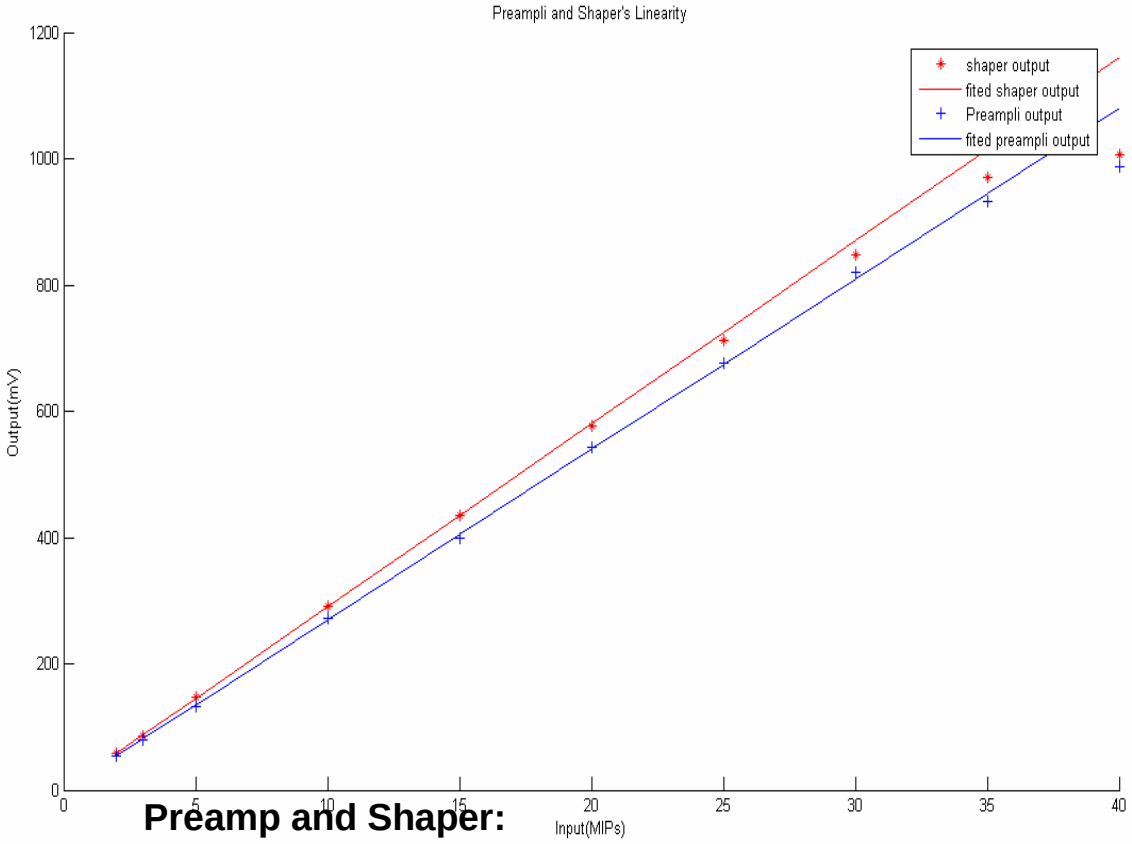
Measured gain - linearities

Preamp output



Shaper output





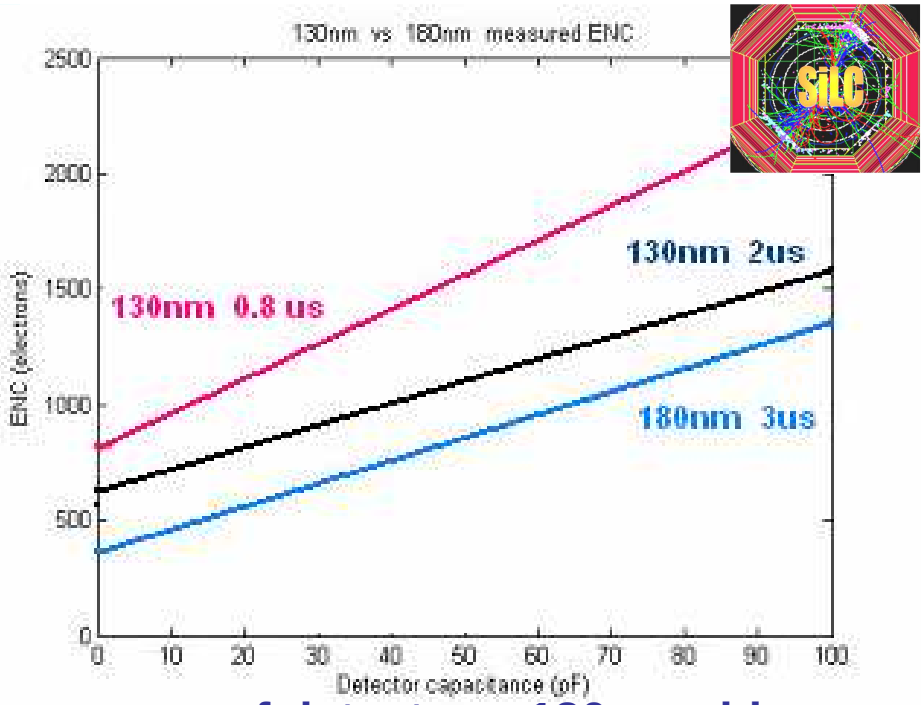
Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

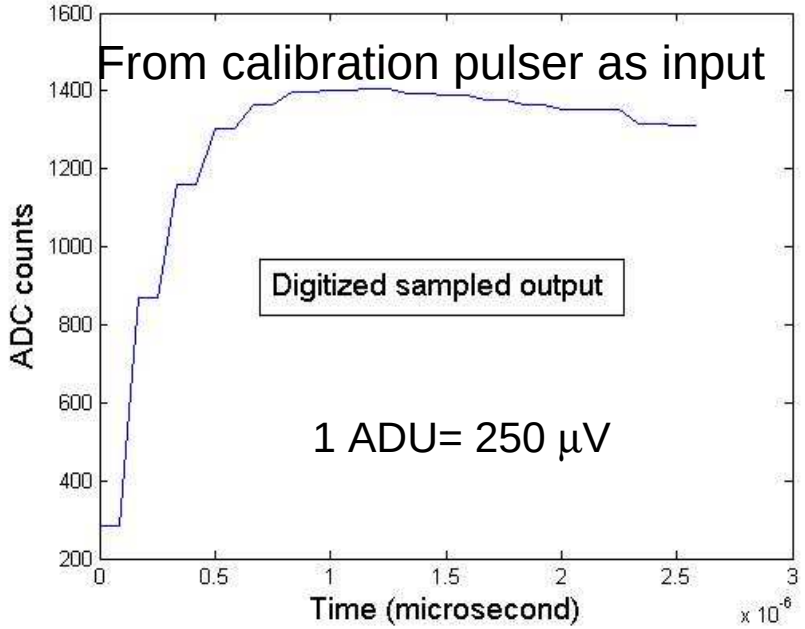
Measured Performances

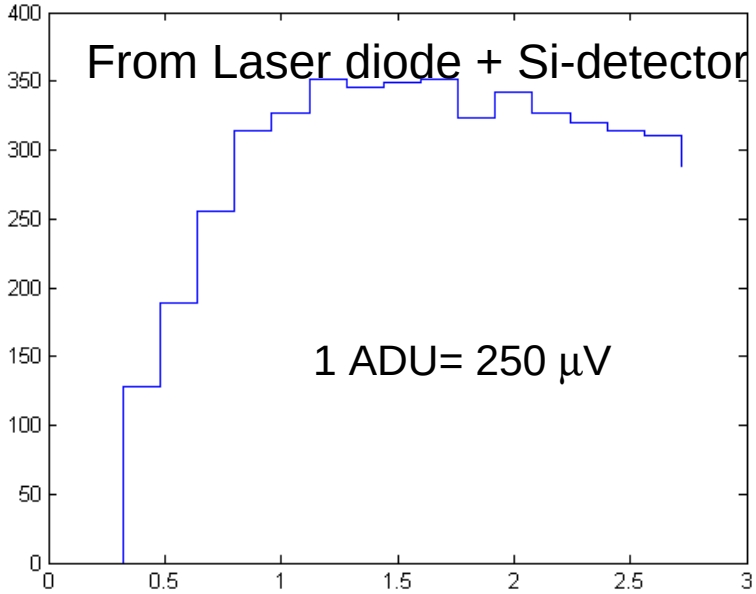
Noise:
130nm @ 0.8 µs: 850 + 14 e-/pF
130nm @ 2 µs : 625 + 9 e-/pF
180nm @ 3 µs : 375 + 10.5 e-/pF

Power (Preamp+ Shaper)
130 nm: 150+90= 245 µW
180 nm: 70+140= 210 **µW**

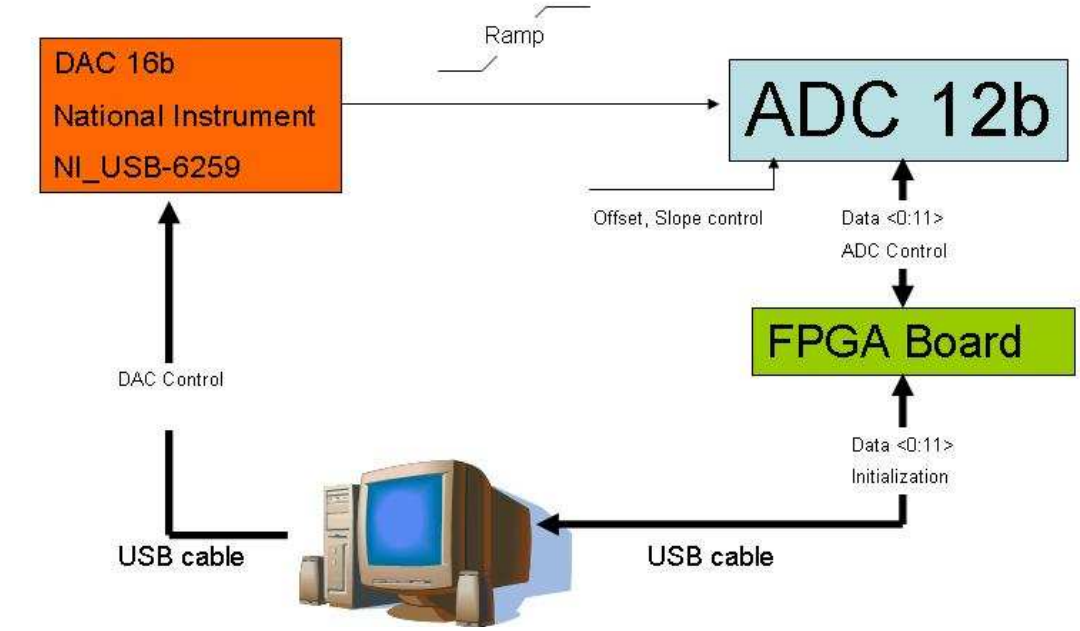


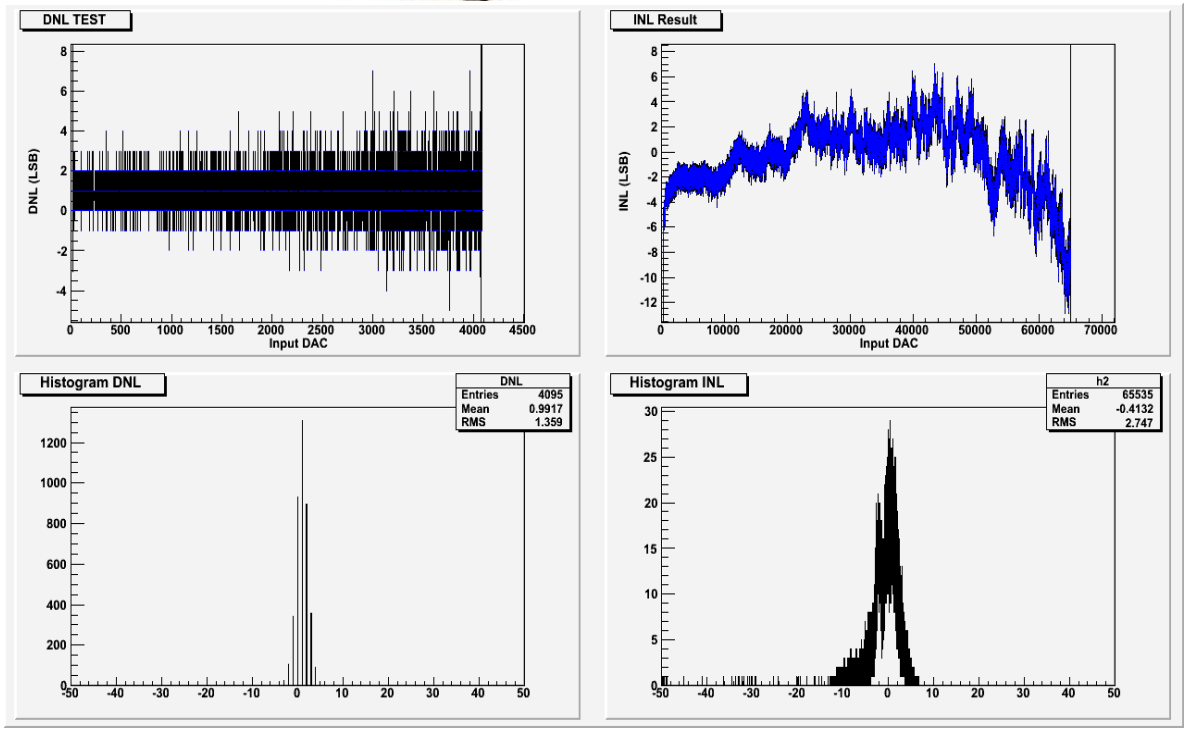
Digitized analog pipeline output Laser response of detector + 130nm chip





Sampling rate = 12 MHz; Readout rate = 10 KHz





ADC TEST

DAC Input :

Dynamic : 0 – 1V

Offset : ~1V

ADC Output :

From 50 bin to 3780 bin:

+INLmax = 7 LSB

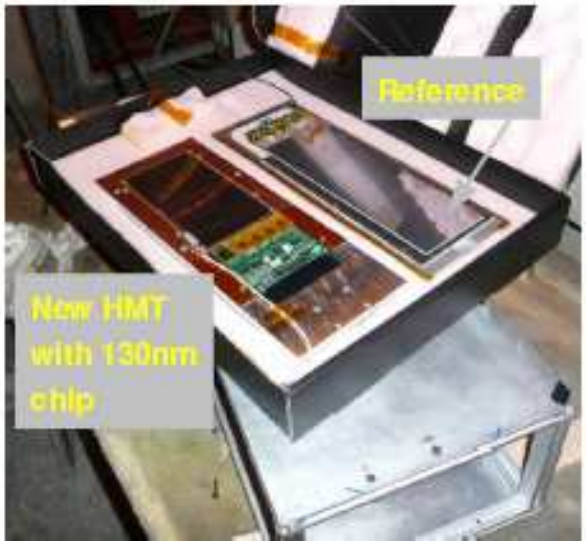
+INLrms = 2.74 LSB

+DNLmax = 7 LSB

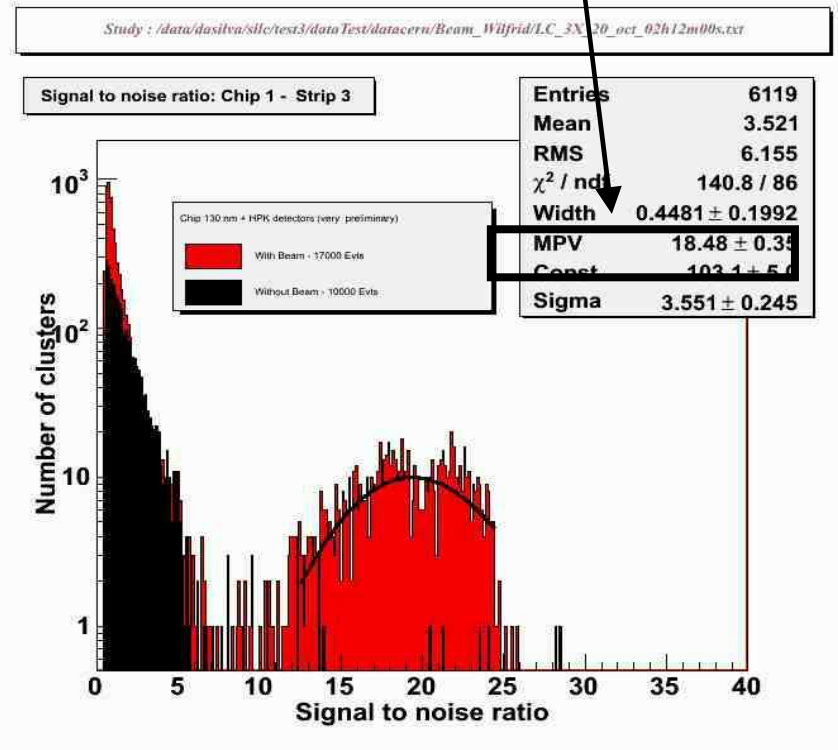
+DNLrms = 1.36 LSB

→ ~ 9b effective in the worst case

SiTR-130_V1 test-beam response



Signal to Noise ratio from beam-tests

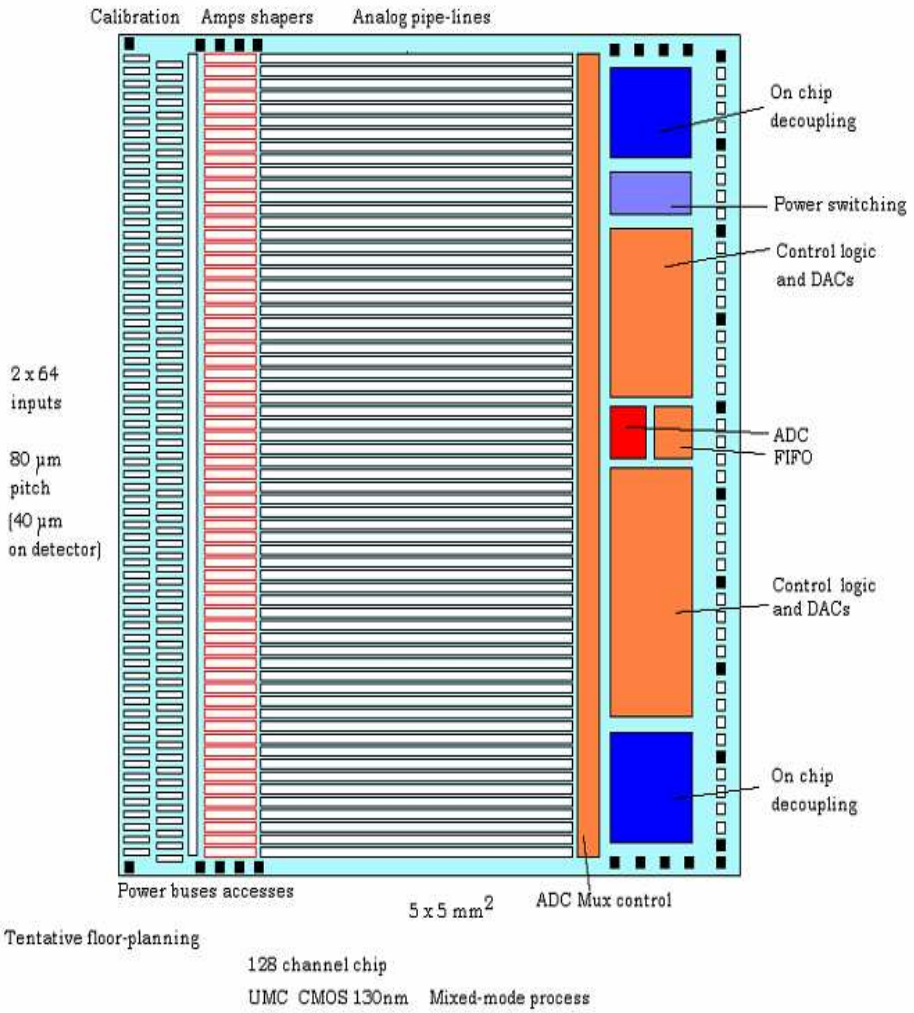


This CMOS 130nm design and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels) with

- DC power under 600μW/ch
- Silicon area under 100 x 500 μ²/ch

New version: SiTR-130_128

Floorplan



- 128 channels in 130nm CMOS
  - Improved shaper (reduced noise)
  - Improved pipeline
  - Chip control
  - Digital buffer
  - Processing for :
    - Calibrations
    - Amplitude,time χ2 estimate, centroids
    - Raw data lossless compression
  - Power cycling using DACs controlled current sources

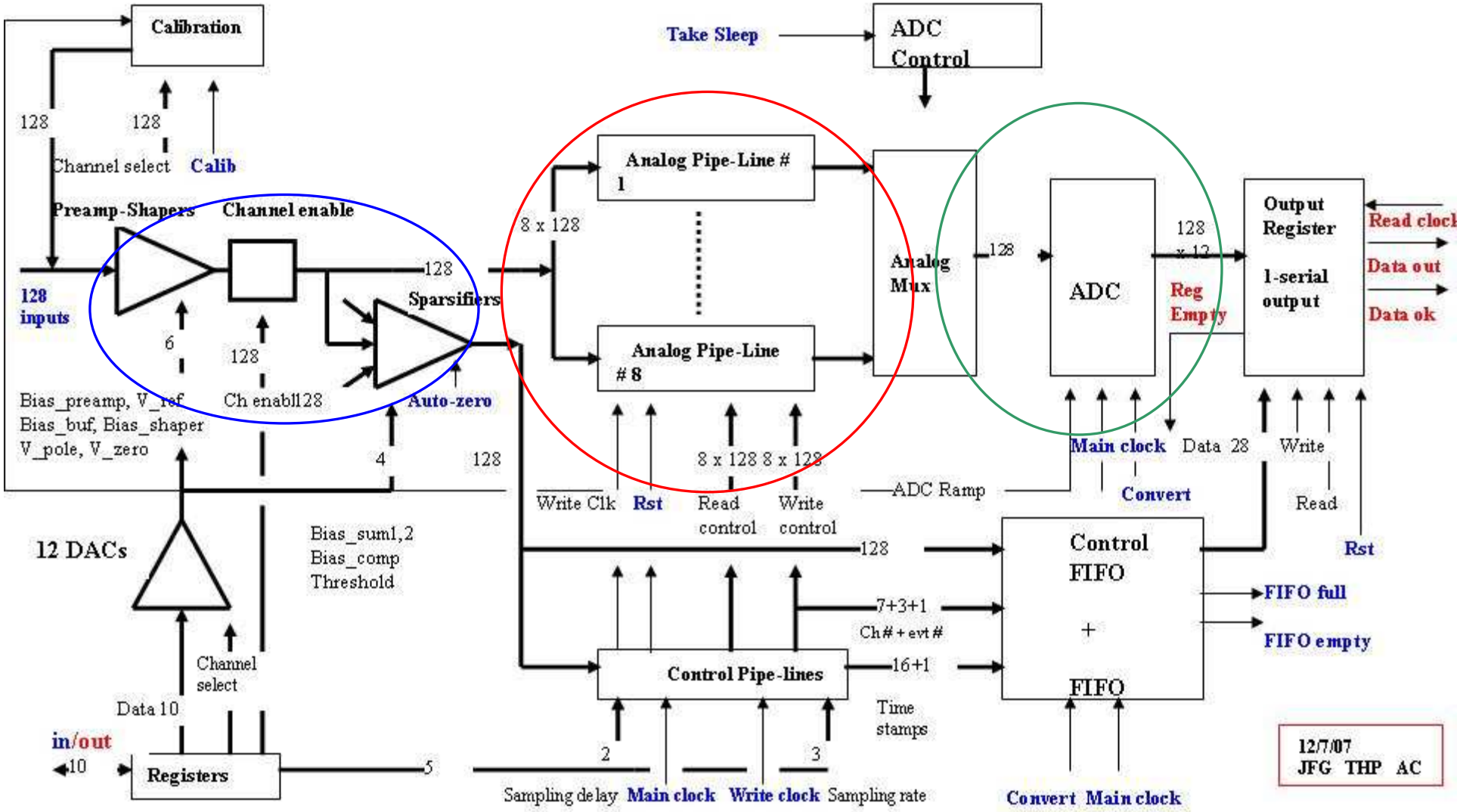
Tools

- Cadence DSM Place and Route tool
- Digital libraries in 130nm CMOS available
- Synthesis from VHDL/Verilog
- SRAM
- Some IPs: PLLs

Needs for a mixed-mode simulator
AMS designer under installation at LPNHE

SiTR-130_128 block diagram

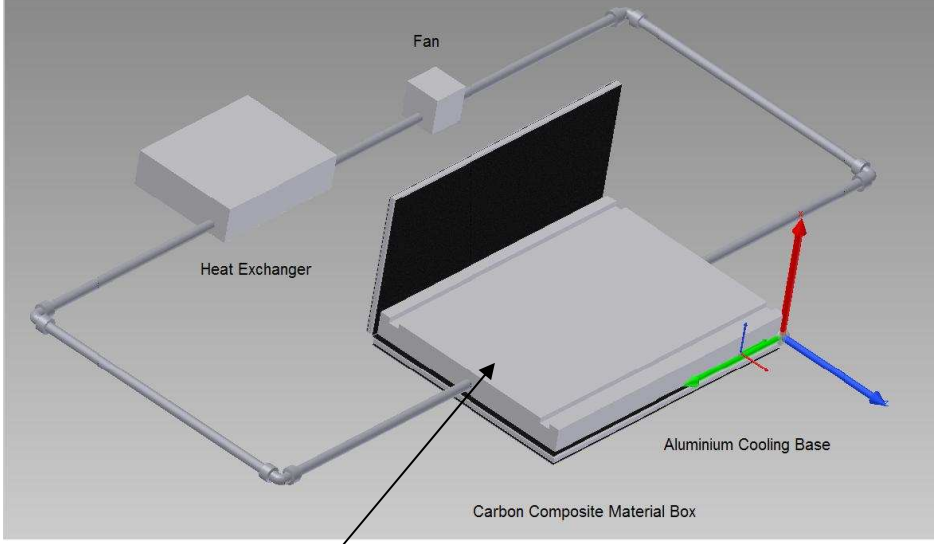
(*B.U., LPNHE, LAPP)*

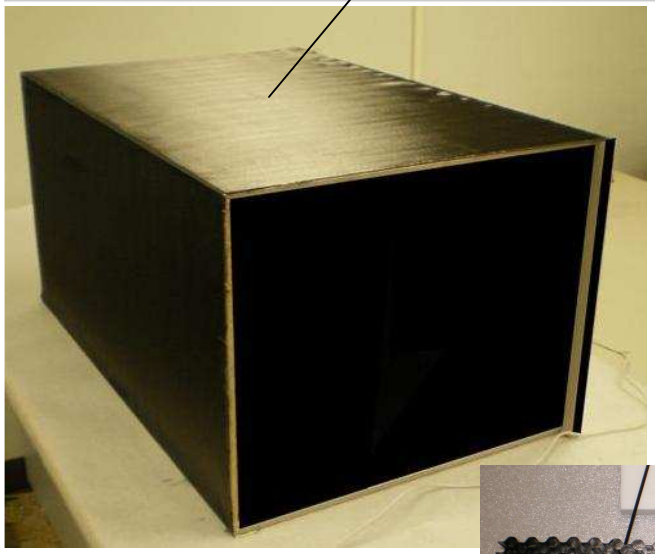


Expected to be sent to foundry April 15

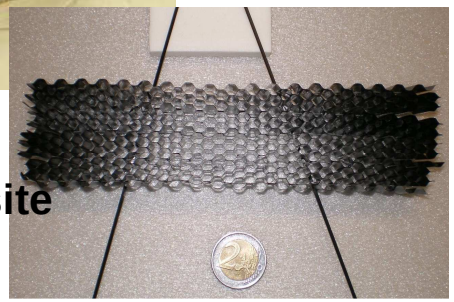
- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beams

Air dry cooling system (OSU) or just an insulating frame





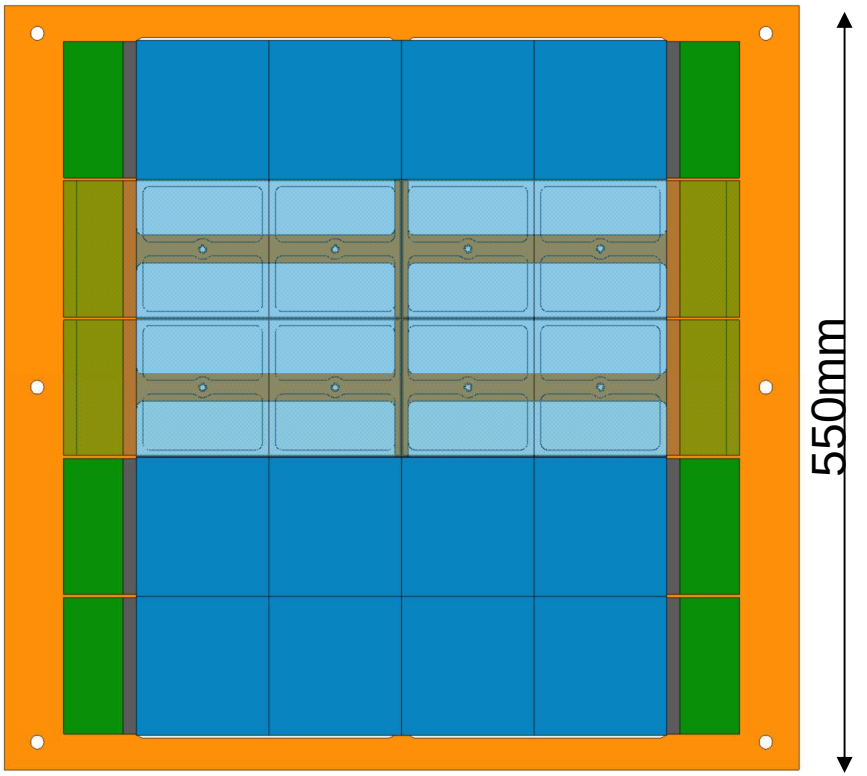
C composite material insulating box



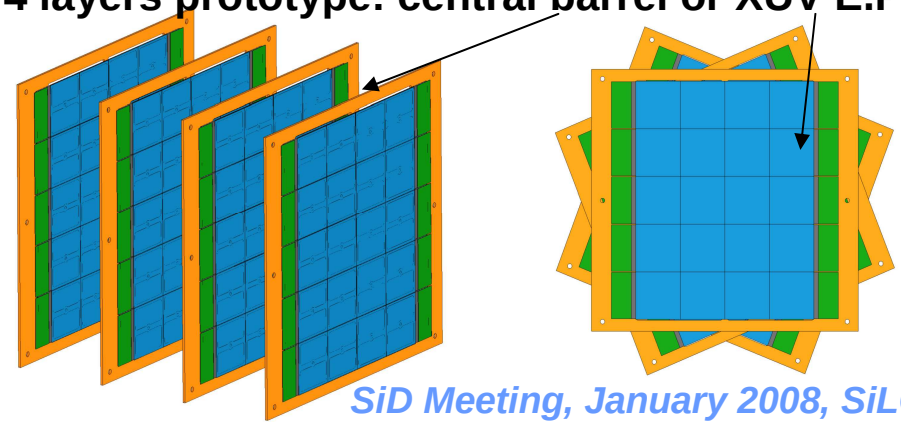
Double-sided honey-comb Carbon composite material

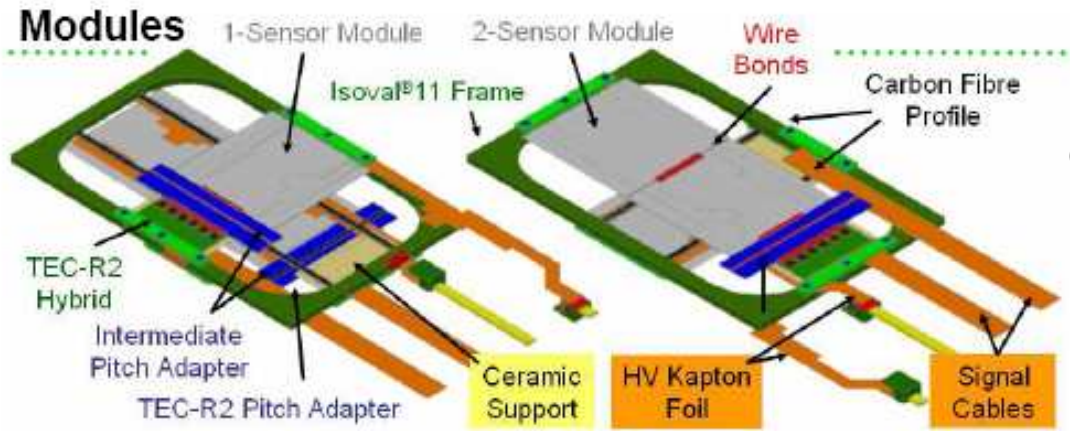
Prototypes for test beams:

- Large size support structure

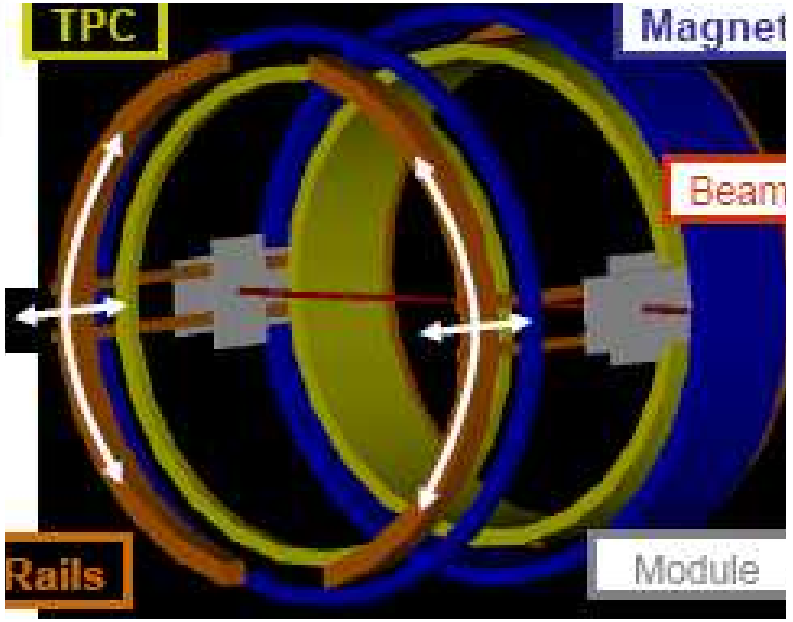


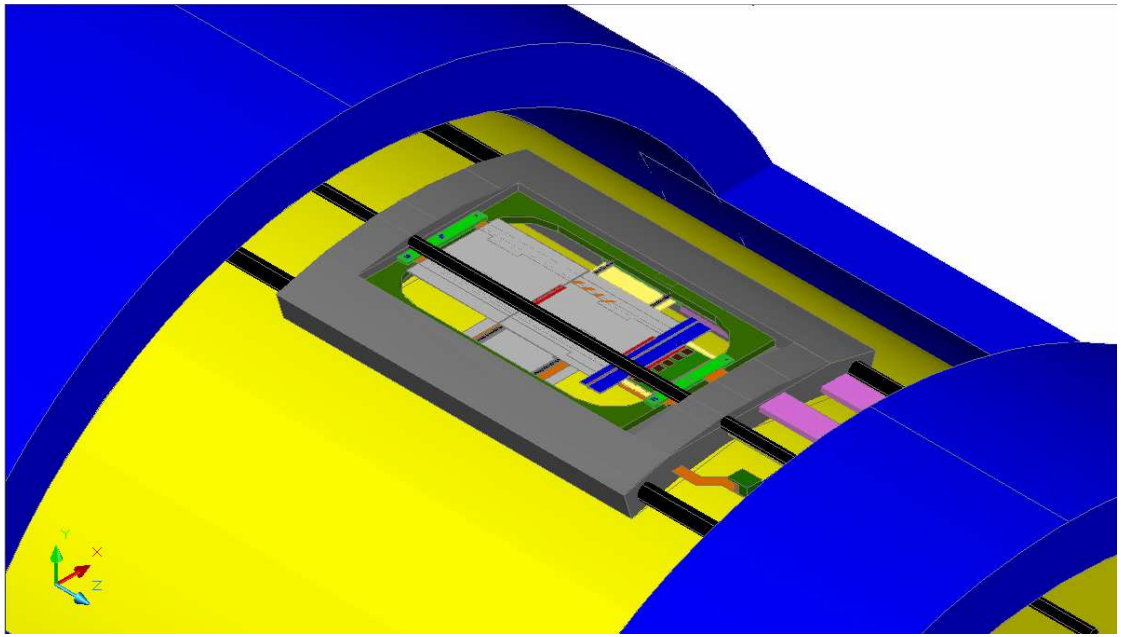
4 layers prototype: central barrel or XUV E.P.





Both prototypes include working on new modules starting with lighter module structure at first .





Test with of the Silicon Envelope with LCTPC in 2008 at DESY: Modules(HEPHY), structures(IEKP) final electronics (LPNHE)

Alignment: 2-fold approach

and CNM/CSIC

AMS-like approach:

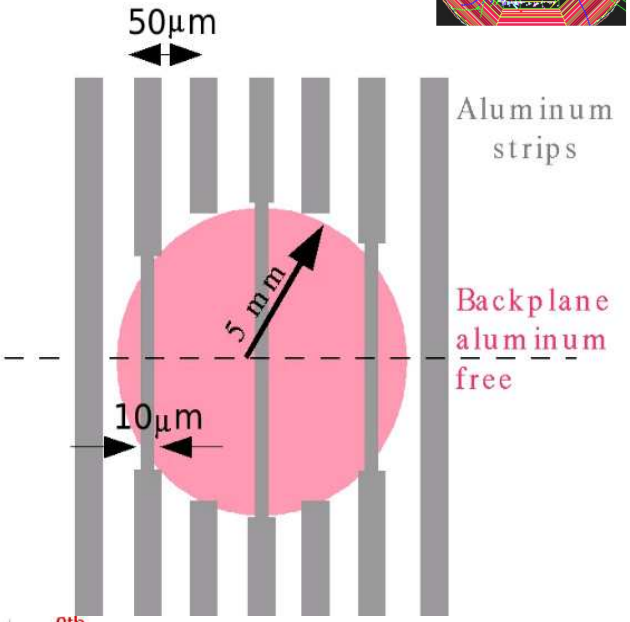
baseline version: Minimum set of changes for any SiLC sensors
For instance, for the new HPK sensors

Implemented:

- ∅~10 mm window where Al back-metalization has been removed

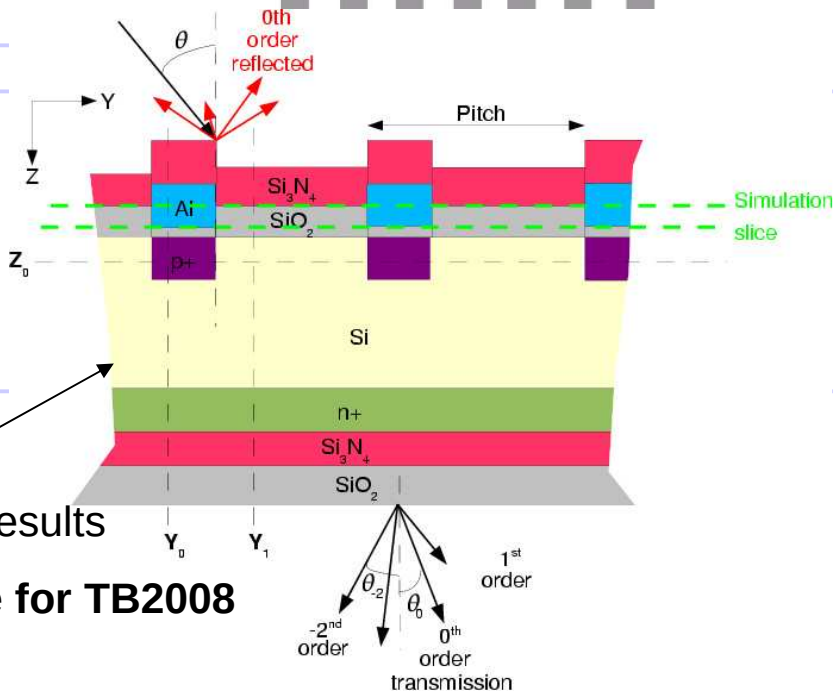
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)



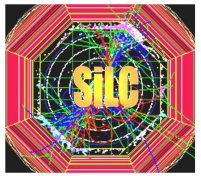
R&D on transparent Silicon µstrip sensors:

- Together with IMB-CNM (Barcelona) design, build and test new IR-transparent Silicon microstrip detectors.
- Consider option of aluminum electrodes or transparent electrodes



Realistic sensor simulations: very interesting studies/results

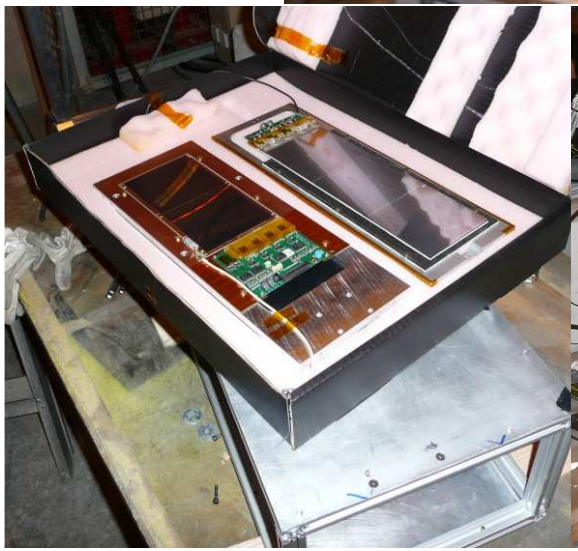
Test bench in development and alignment prototype for TB2008

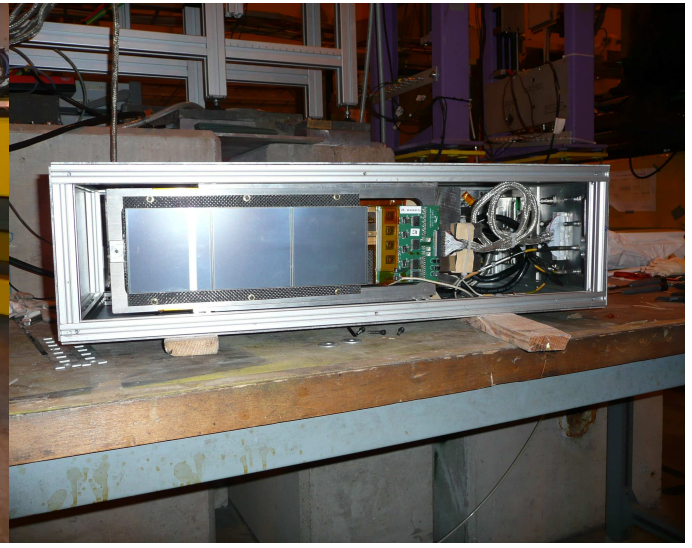


- R&D on sensors
- R&D on electronics
- Mechanics developments
- Test beams

SiLC: IEKP Karlsruhe, LPNHE Paris, CU Prague, IFCA Santander, Torino INFN & Uni, and collaboration with Maps telescope: DESY & Geneva U. and CERN support (Silicon Lab)

Arrival and setting up of the test at SPS West area, October 10-22, 2007

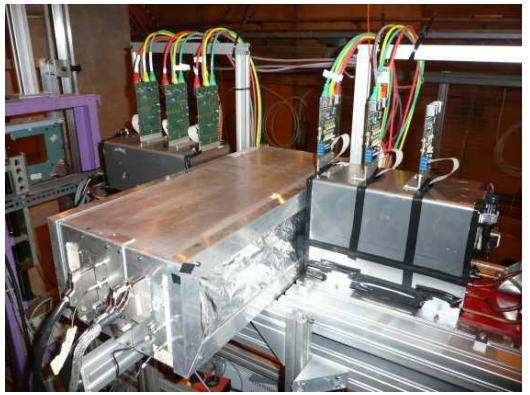


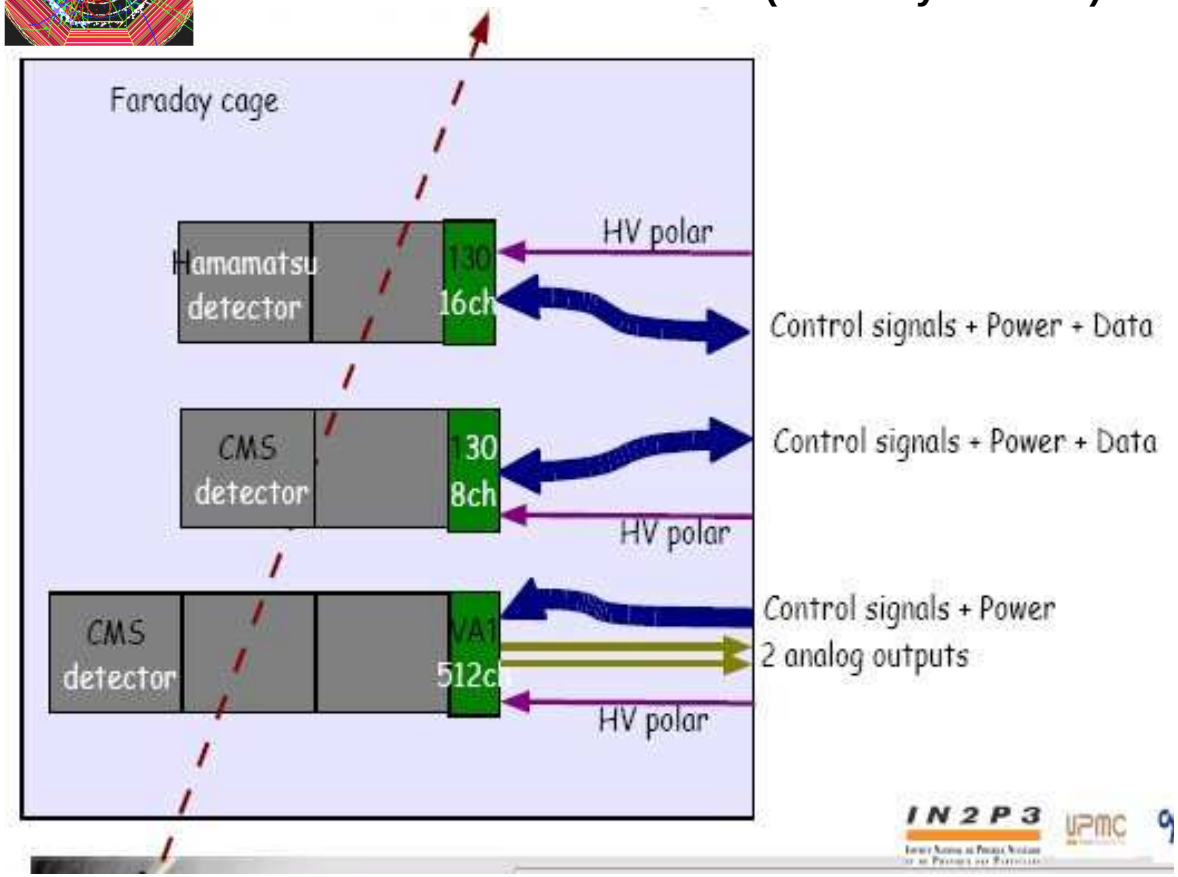


Photographs by F. Kapusta

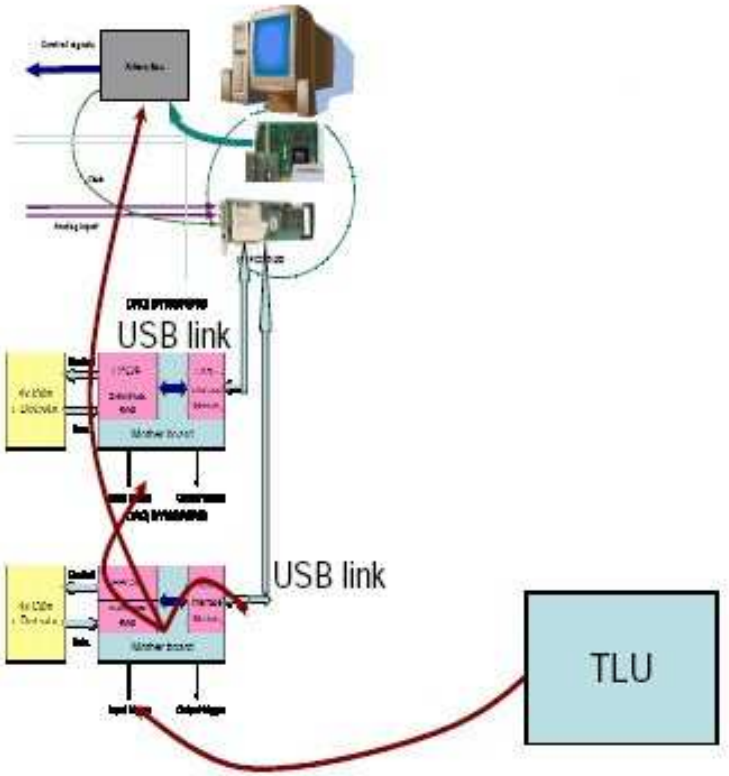
Inside the Faraday cage

(slides by J. David)

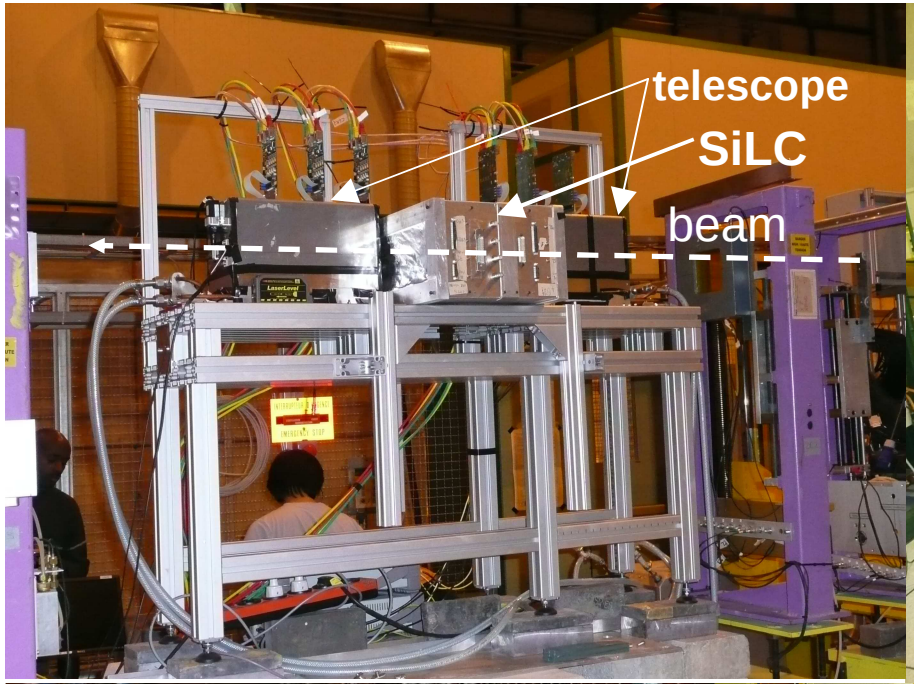


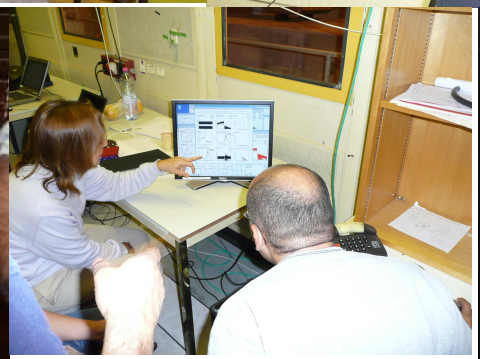


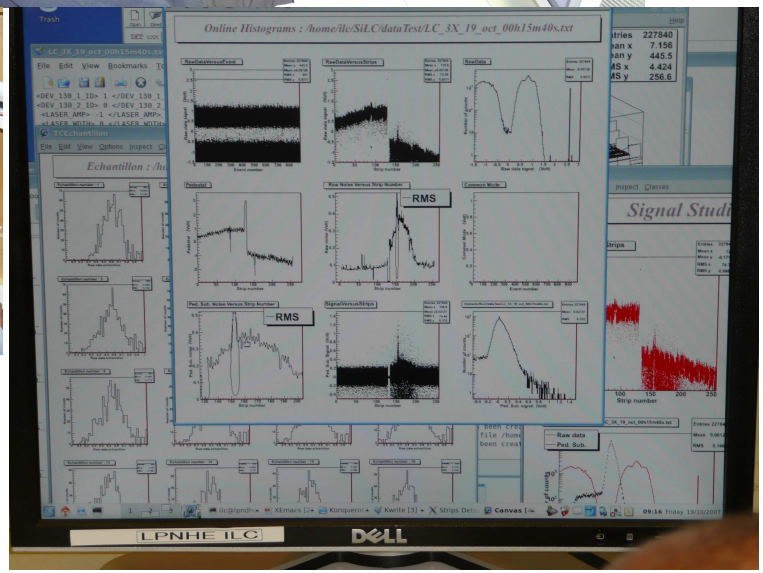
The trigger: TLU



Test running and data taking

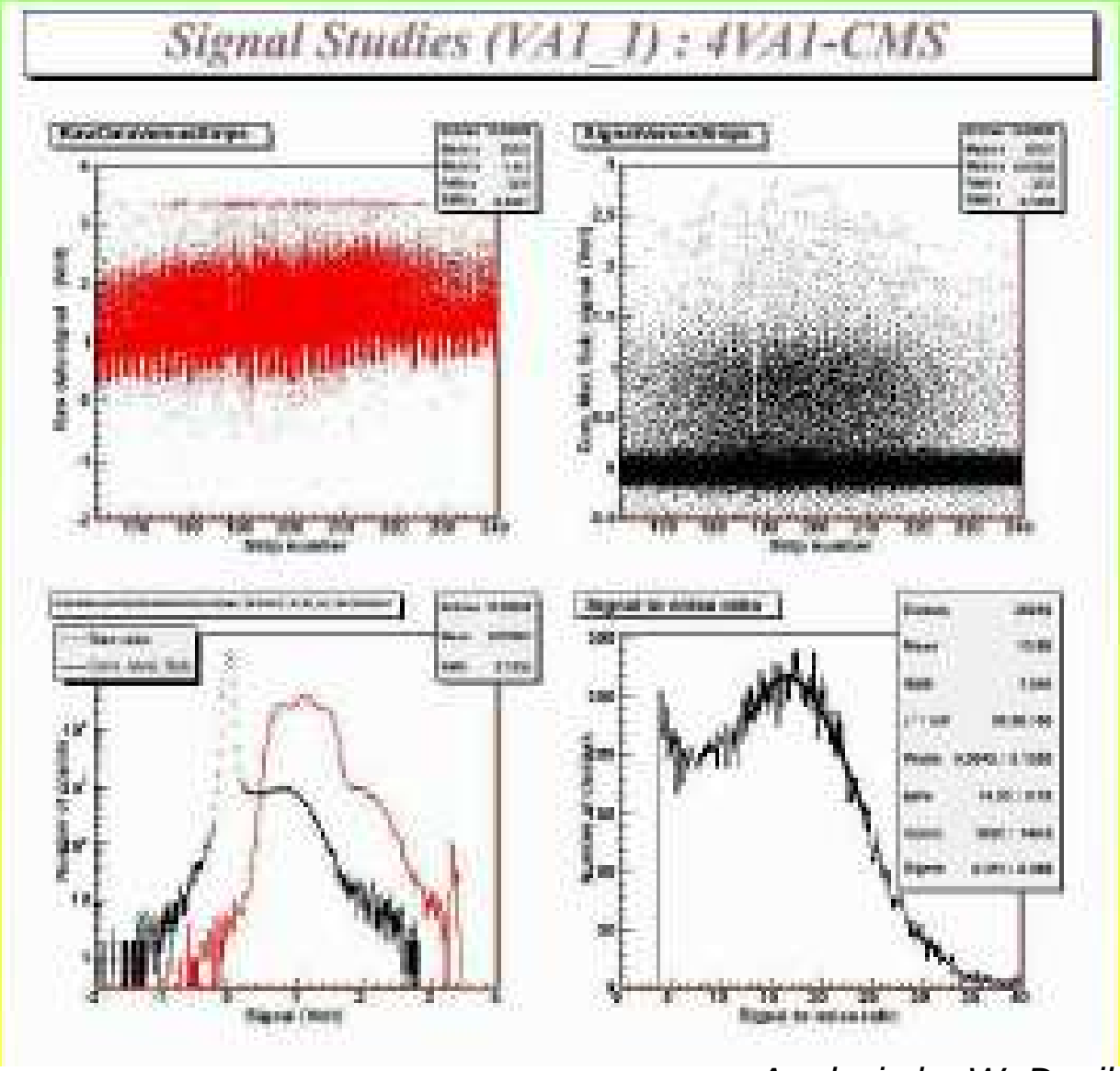






Photographs by F. Kapusta

The beam is on : the VA1-3CMS is responding S/N $\simeq$ 15

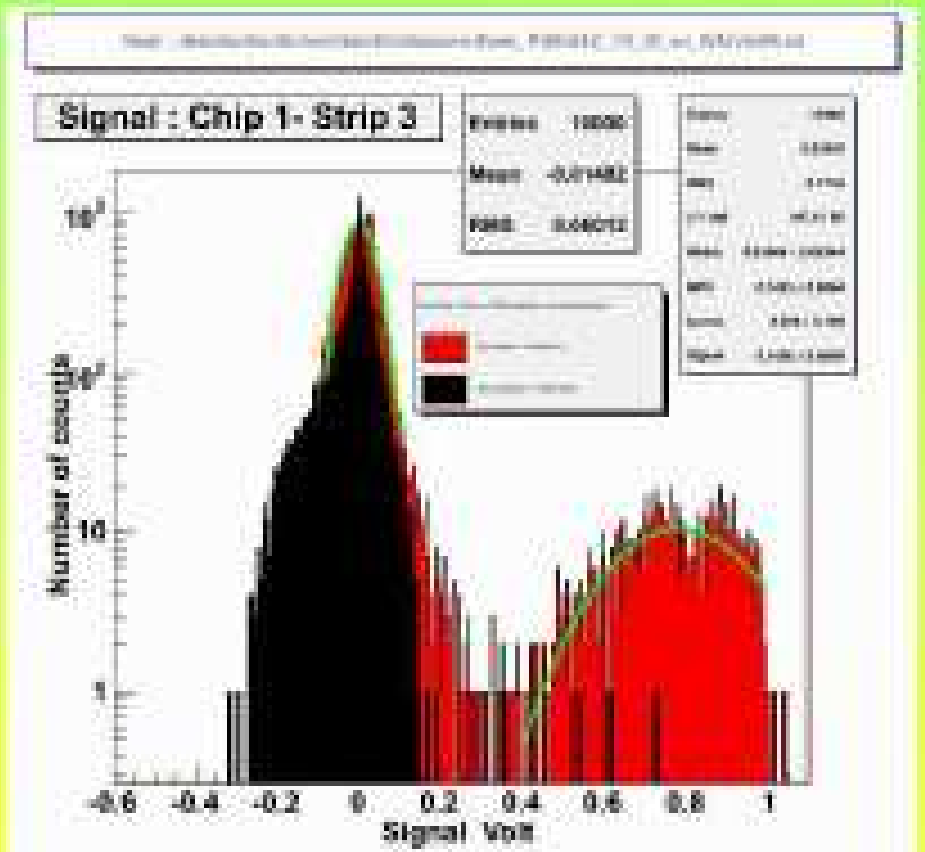


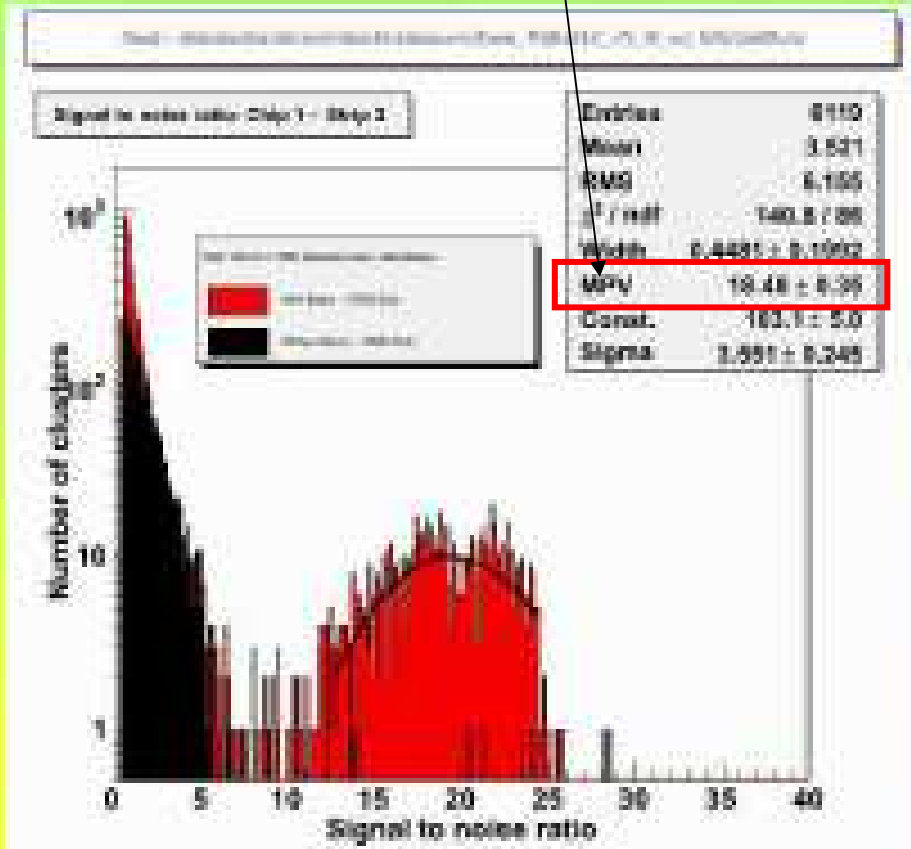
Analysis by W. Dasilva and F. Kapusta

Results with the new HPK + SiTR-130

HPK 130 nm procedure results for a good responding strip

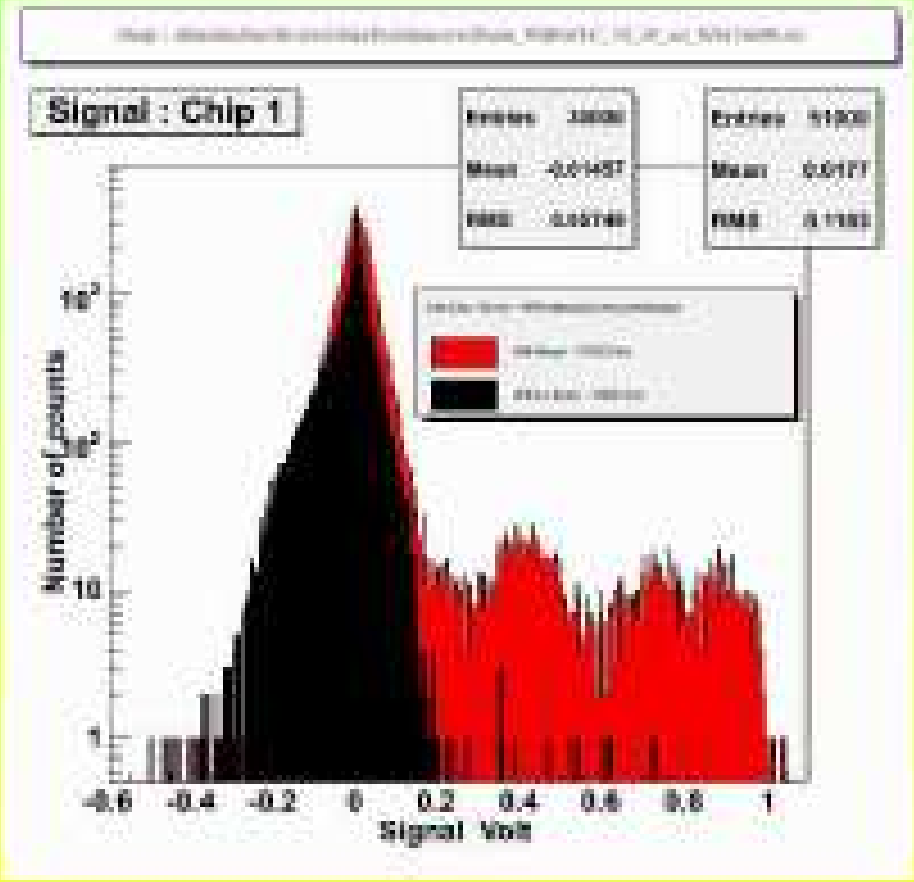
Black : Beam Off - Red : Beam On - S/N ~ 18

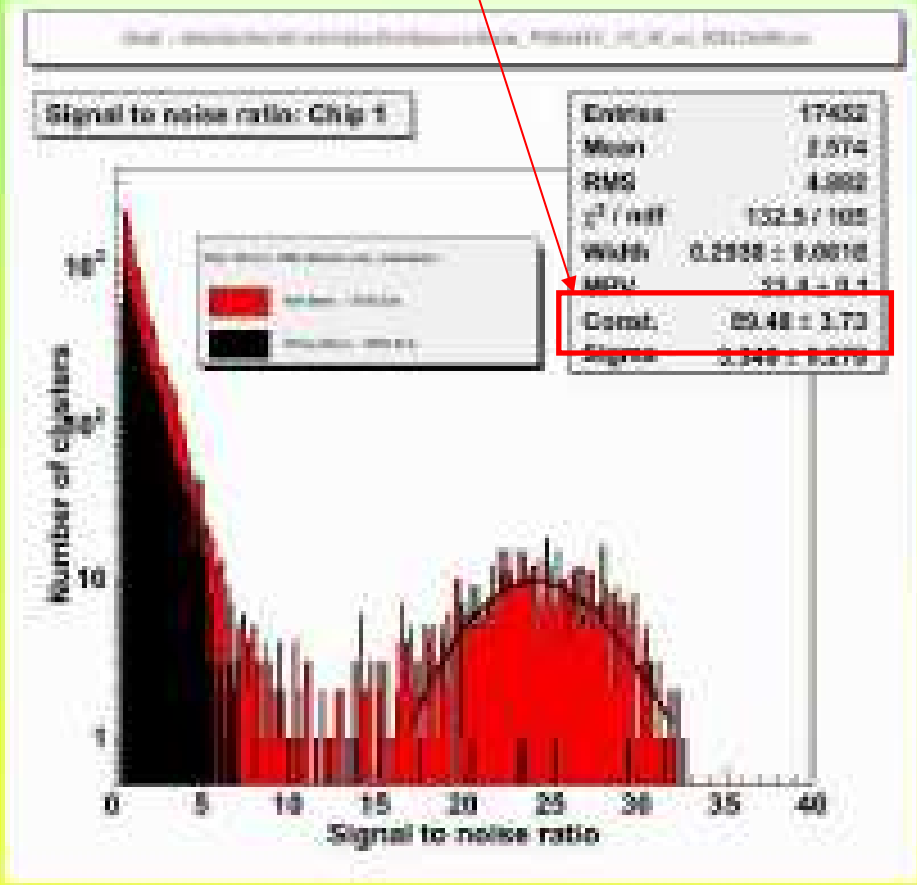




Results with the new HPK + SiTR-130

HPK 130 nm : 2 strip clustering - S/N ~ 23





Perspectives

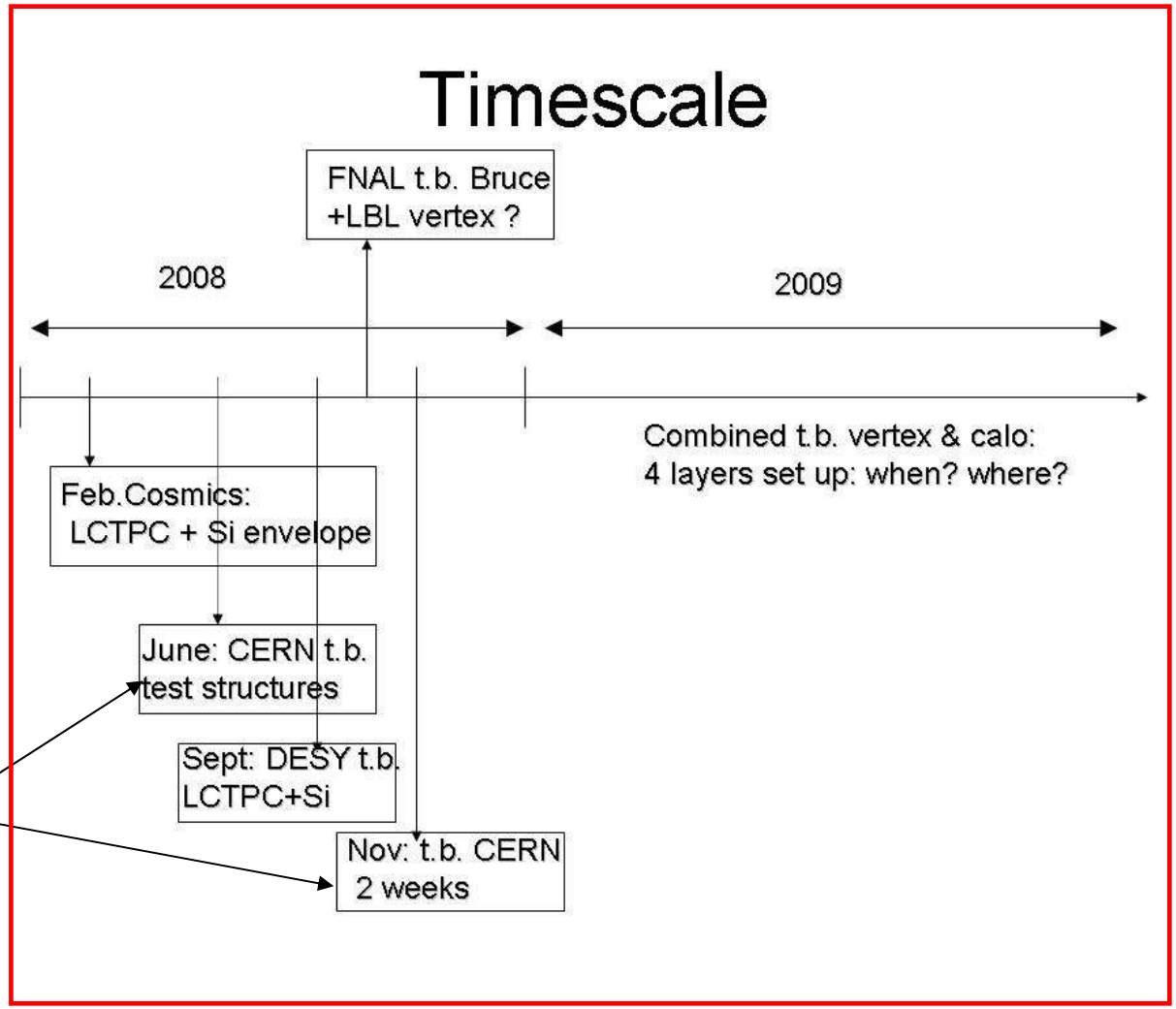
Proposal submitted to the CERN SPS Committee for
A beam test at the CERN-SPS in 2008 by:
SiLC R&D Collaboration

Abstract: The SiLC R&D collaboration is requesting a total of three weeks beam test at the SPS at CERN in 2008, in order to pursue the work started at the beam test H6 at CERN SPS, from October 16 to October 22, 2007. This collaboration is aiming to develop the new generation of large area Silicon systems in synergy with the work achieved for constructing the present LHC Silicon trackers and also in view of their upgrades for sLHC and the future trackers for the Future Linear Collider. It is also part of the EUDET JP-P6 European Project.*

**Members of the SiLC R&D collaboration are: University of Michigan-Ann Arbor (USA), LAPP-Annecy (France), University of Barcelona and University Ramon Llull in Barcelona (Spain), IMB/CNM-CSIC in Bellatera (Spain) Helsinki Institute of Physics (Finland) and VTT Technical Research Center of Finland-Helsinki (Finland), IEKP Karlsruhe (Germany), Liverpool University in Liverpool (UK), Moscow State University-Moscow Russia), Obninsk State University – Obninsk (Russia), LPNHE-University Pierre et Marie Curie/CNRS-IN2P3 (France), Charles University in Prague (Czech Republic), SCIPP and University of California in Santa Cruz (USA), IFCA-University of Cantabria and CSIC-Santander (Spain), Tomsk University, Seoul National University and SungKyunKwan University all in Seoul, and Kyungpook National University in Daegu (Korea), INFN-Torino and University of Torino in Torino (Italy), IFIC, University of Valencia and CSIC- Valencia (Spain), HEPHY, Austrian Academy of Sciences in Vienna (Austria), Hamamatsu Photonics in Hamamatsu City (Japan)*

SiLC test beam coordinator: Aurore Savoy-Navarro
aurore@lpnhe.in2p3.fr
SiLC contact person at CERN: Marcos Fernandez Garcia
Marcos.fernandez@cern.ch

Proposal submitted to the SPSC-CERN Nov 16,2008



SiLC R&D Collaboration

U.S.A

Michigan U.
SCIPP-UCSC

Connections with:

- FNAL (DOE prop 05 funded)UCSC, FNAL, LPNHE
- SLAC (DOE prop 03: funded): UCSC, SLAC Michigan U, LPNHE and meetings SiD
- CERN (collab of bonding Lab+TB infrastructures)

Europe

IMB-CNM/CSIC, Barcelone (SP)
(eudet ass.)
U.Barcelona (SP)
Helsinki U.(Fi) *(eudet)*
VTT-Finland (Fi)
IEKP, Karlsuhe U. (D)
Liverpool U.
Moscow St. U. , Moscou(Ru)
(eudet ass.)
Obninsk St. U., Obninsk (Ru)
(eudet ass.)
LPNHE, Paris (Fr) *(eudet)*
Charles U. , Prague (CZ) *(eudet)*
IFCA/CSIC, Santander(Sp) *(eudet)*
Torino U., INFN-Torino (It)
IFIC-CSIC Valencia (Sp) *(eudet ass.)*
HEPHY, Academy Sci., Vienna (Au)

Asia

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

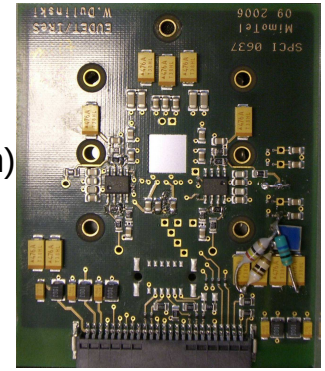
Launched January 2002, Proposal to the PRC May 2003, Report Status May 2005, ILC tracking R&D Panel at BILCW07 February 2007, next PRC Status report April 08

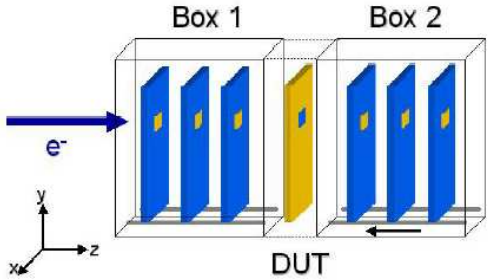
This brief review is an attempt to present all the SiLC collaborators hard work results: Many thanks to all of them!

Backup Slides

Eudet's telescope: what we had...

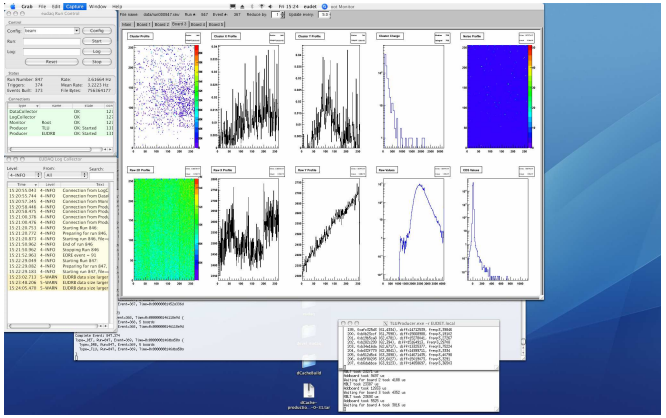
We had an analogue telescope (demonstrator version)
Chip size 7x7 mm^2
256x256 pixels, 30 µm pitch





Replacement mechanics
to position sensors precisely

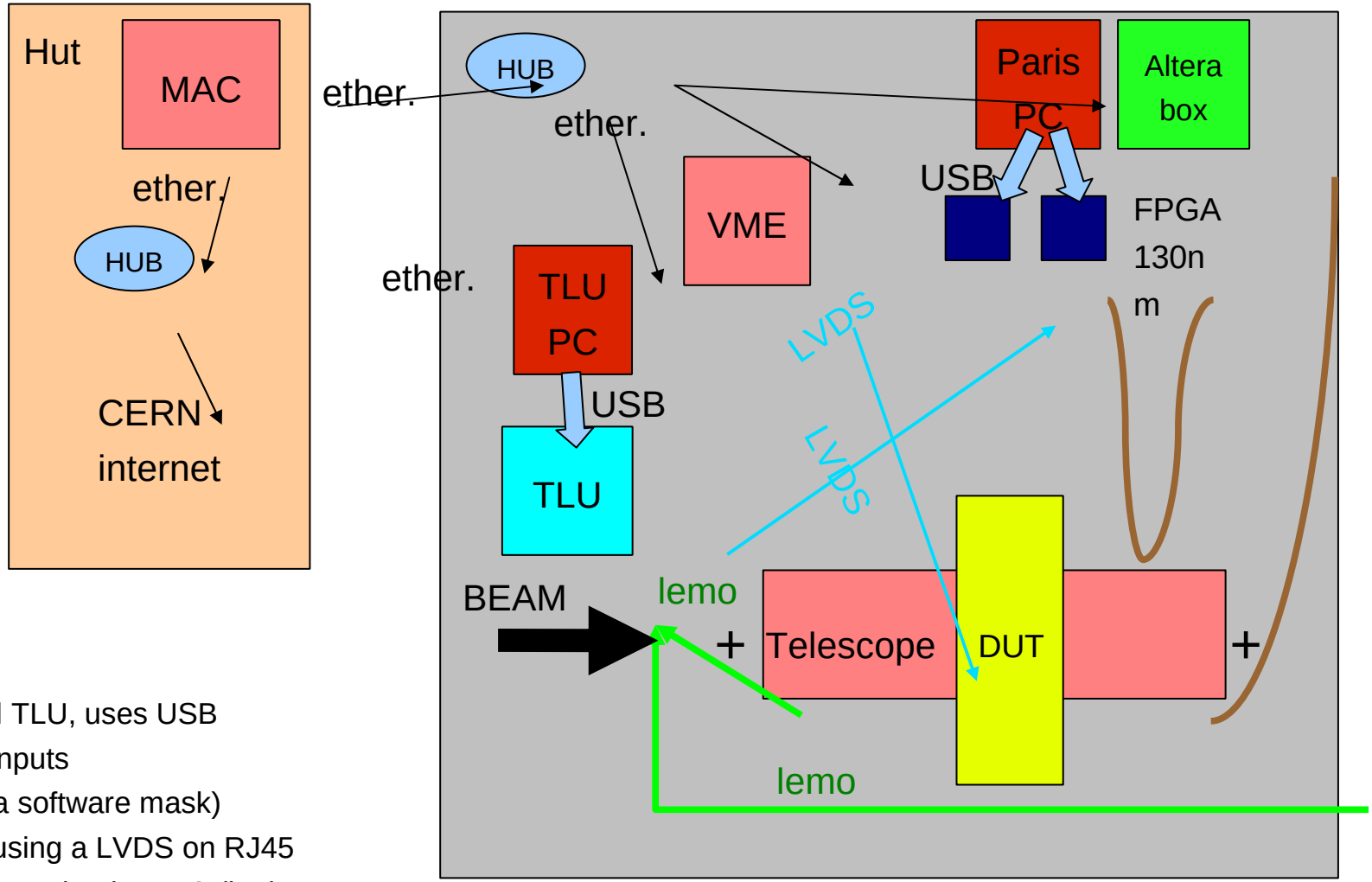
EUDRB (INFN):
online pedestal&noise calc
cluster finding
FPGA remote config
ADC
RO modes:
- Full frame
- Zero suppression



Trigger Logic Unit (TLU)
Simple integration of DUT into telescope
Event number and time stamps from events
Provides handshake between scin. Trigger, and DUT using trigger/busy signals

Custom telescope DAQ
Data collected in custom format, converted to LCIO/Marlin format
Analysis using grid

HW SETUP



- Linux PC to control TLU, uses USB
- TLU accepts NIM inputs

(trigger logic set by a software mask)

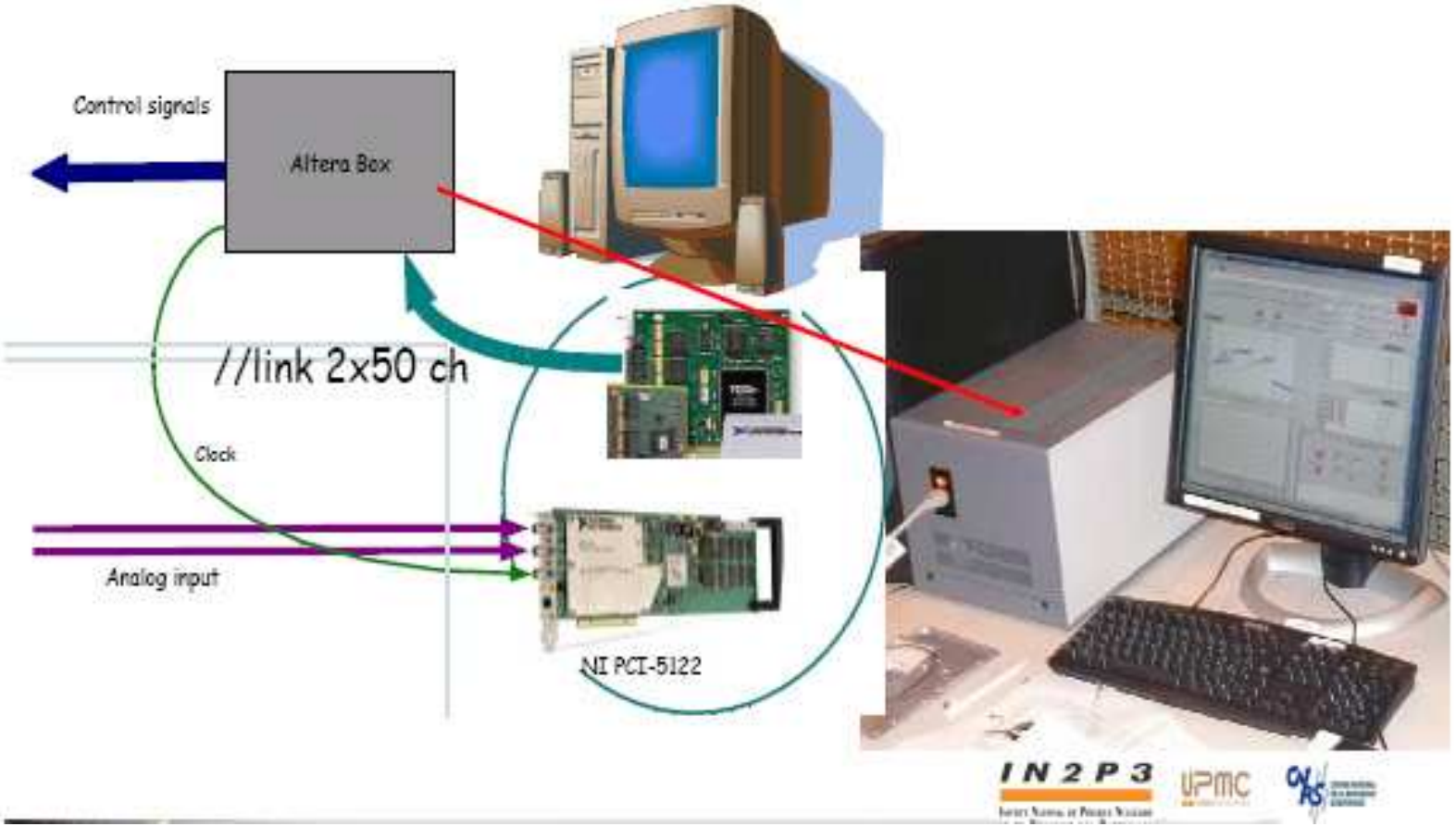
- TLU talks to SiLC using a LVDS on RJ45
- TSCOPE software running in MAC (hut).
- Ethernet communication with VME (hall), running LynX. VME houses EuRDB
- Paris win-pc for SiLC RO and FPGA programming
- Gigabit HUB in experimental area
- Gigabit HUB in the hut, connected to CERN ethernet

TB Menu

- Approx. 228k events: 77k ped, 99k SiLC+TLU, 53k SiLC+TLU+Telescope
- 47 SiLC files, 77 telescope files (limited to 890 entries each)
- 25 files with SiLC + TLU+telescope
- 22 files with SiLC alone (TLU in internal trigger mode)
- Hadrons=120 GeV pions
- Runs with different collimator settings to reduce hit multiplicity (detector occupancy)
- Logbook available as an excel worksheet under google docs

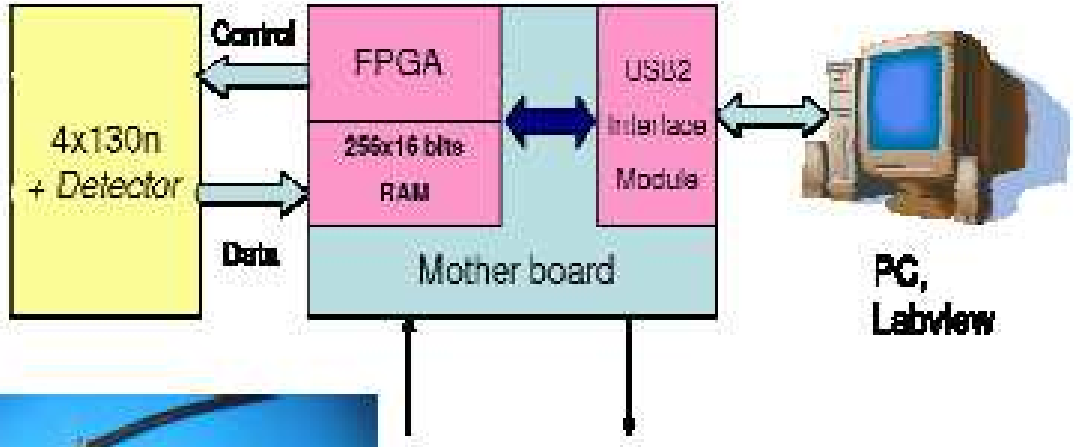
The DAQ for the VA1

(slides by J. David)



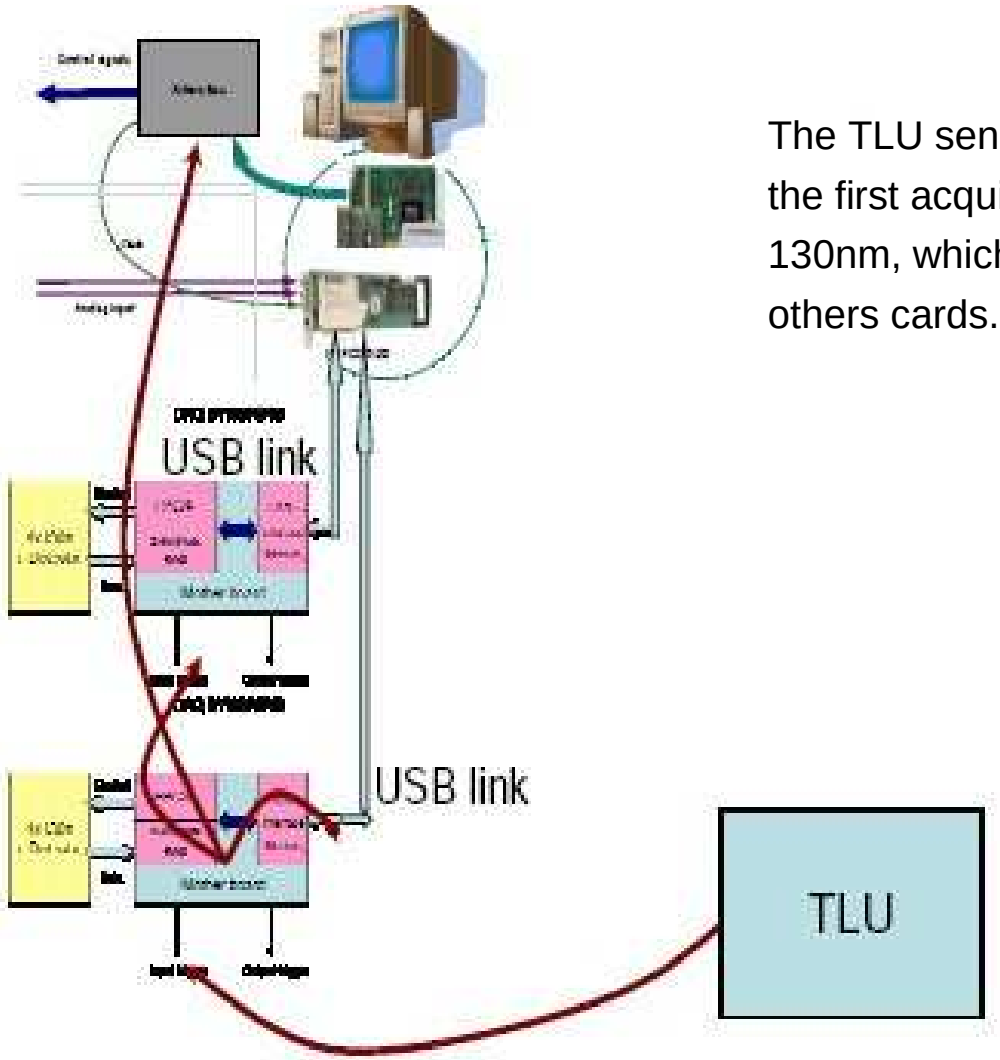
The DAQ for the 130 nm

(slides by J. David)



This card was duplicated
for the two 130 nm modules

The trigger



The TLU sends a simple trigger to the first acquisition board of the 130nm, which transmits it to the 2 others cards.