FNAL Pixel R&D Status

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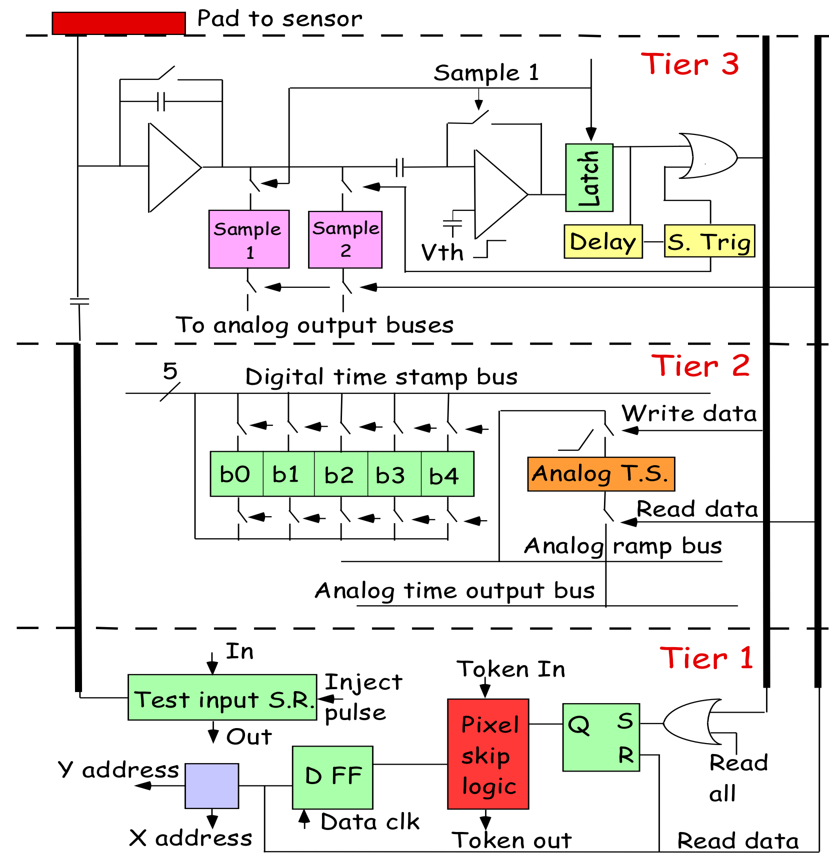
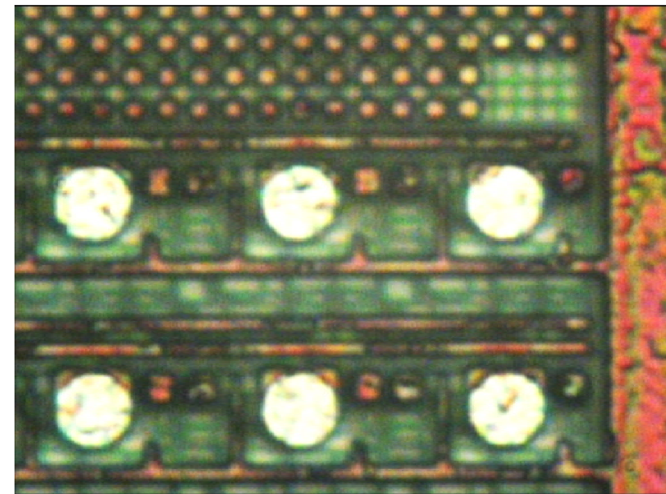
Brief overview due to 3 failed MS Powerpoint versions

- 3D electronics
  - New technologies for vertical integration of electronics and sensors
- Detector thinning after topside processing
  - Thinning processes
  - Laser annealing
  - Handling and assembly
- Silicon-on-Insulator
  - Monolithic pixel detectors
  - Technology R&D

VIP 3D Chip

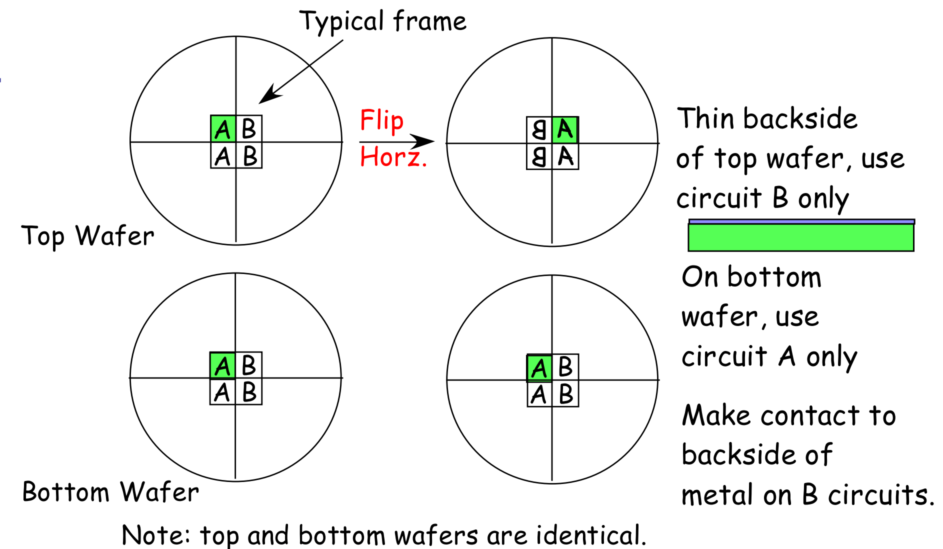
- Chip received in November
  - Needed FIB repair to bias analog test structures
  - These structures look good - gain, noise similar to simulation
  - Some work on one chip and not another – yield issue?
- Beginning to work on full chip readout.
- Plan for 2nd DARPA run





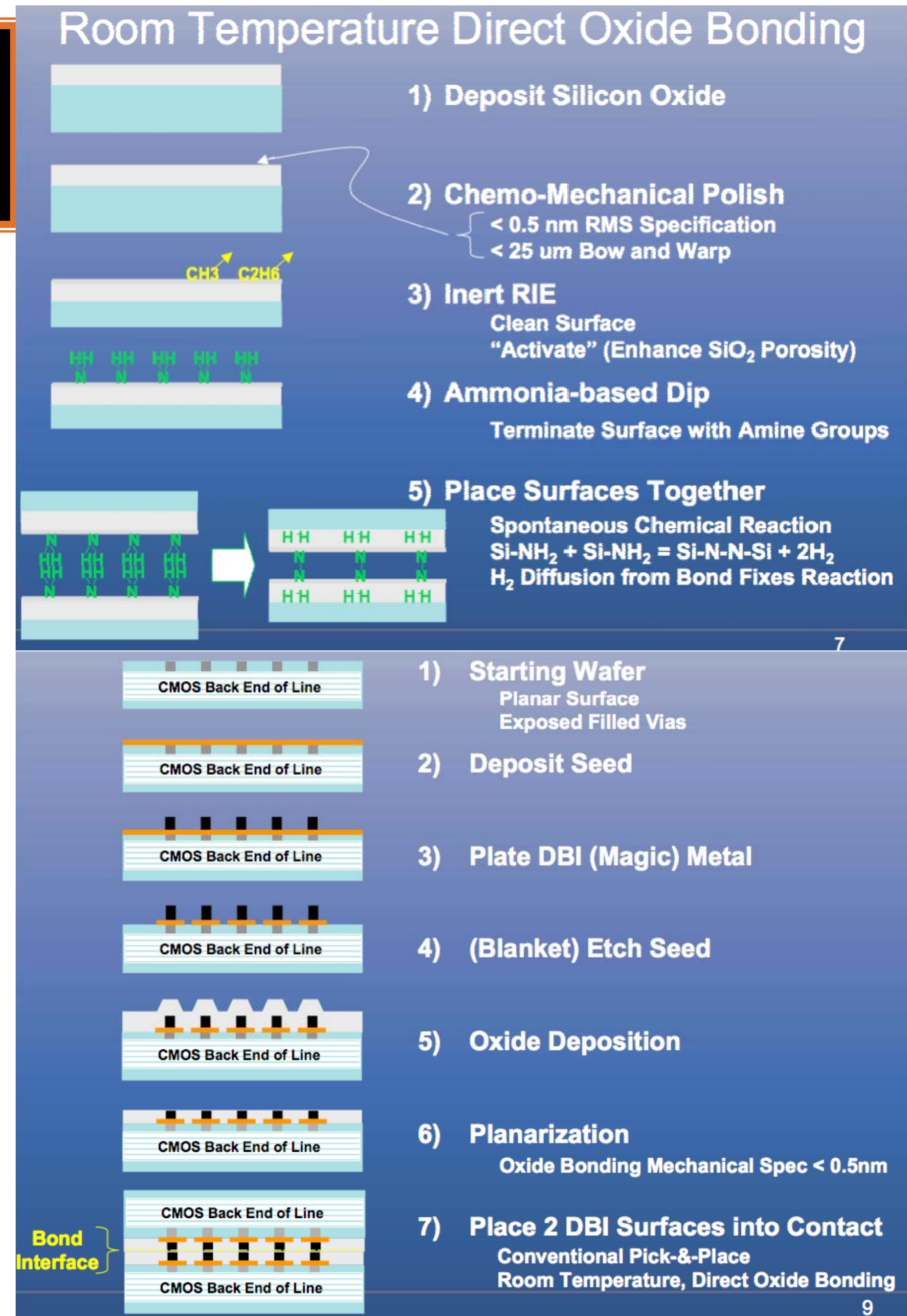
Future and Current 3D Work

- 3rd DARPA run expected next year
- Considering dedicated HEP MIT-LL multiproject run
  - Exploring interest, funding and technical options
  - Radiation hard BOX available (receiving test structures)
- Reduce costs for R&D
  - Two circuit tiers
  - Sensor on SOI handle
  - Use results from 2 DARPA runs and test structure measurements
- CuSn structures with RTI
- DBI demonstration with BTeV chips and MIT-LL sensors
  - Thin bonded chip-sensor pairs
  - Potentially most radiation hard process
- DARPA sponsored run with Tezzaron – 0.13 micron two tier commercial process



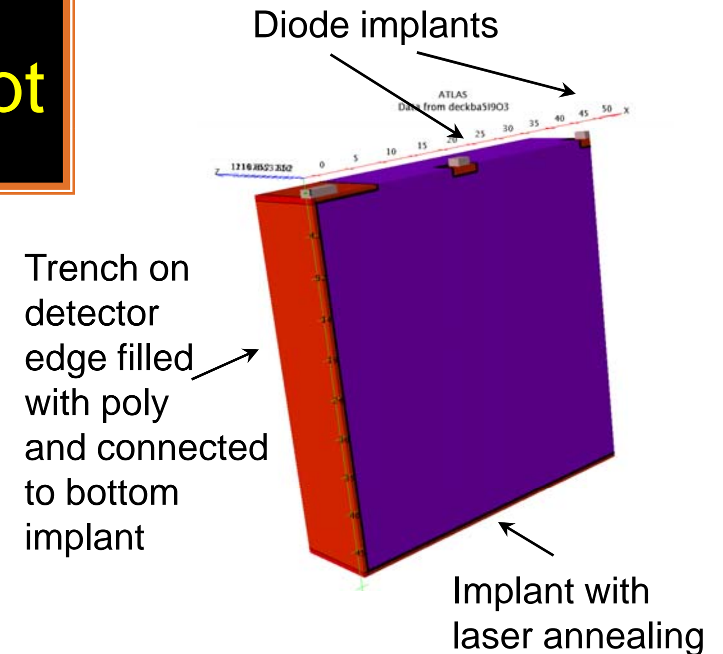
Direct Bond Interconnect (DBI)

- Particularly interesting as a replacement for bump bonding
  - Robust mechanical connection - can be ground and thinned
  - Achieved 8 micron pitch
- PO stalled due to budget cuts.

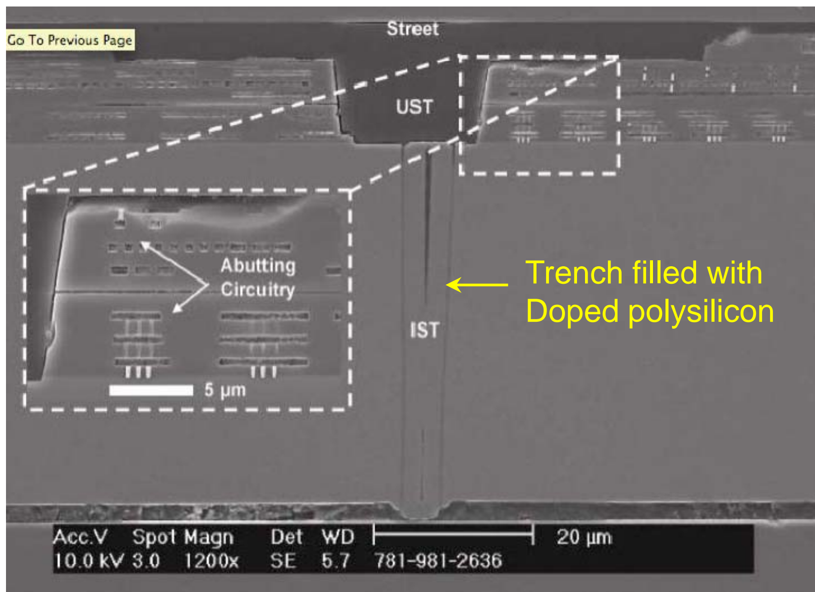


Edgeless Thinned Detector Concept

- Deep trench etching used in 3D vias can be used as a high quality detector edge (same as 3D detectors)
- This edge can be used as a detector electrode - eliminating edge losses in tiling reticle-sized detectors
  - We have produced a set of detectors at MIT-LL thinned to 50 and100 microns
  - Need to thin and backside process

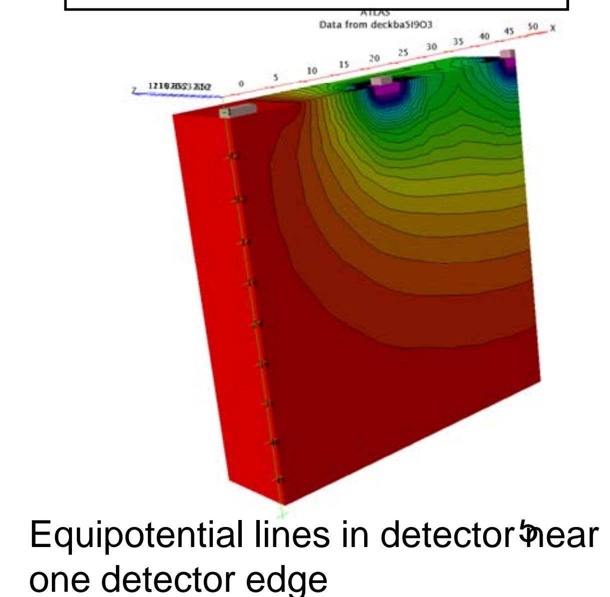


Detector Cross section near one detector edge



Trenched 3D sensor

From MIT-LL

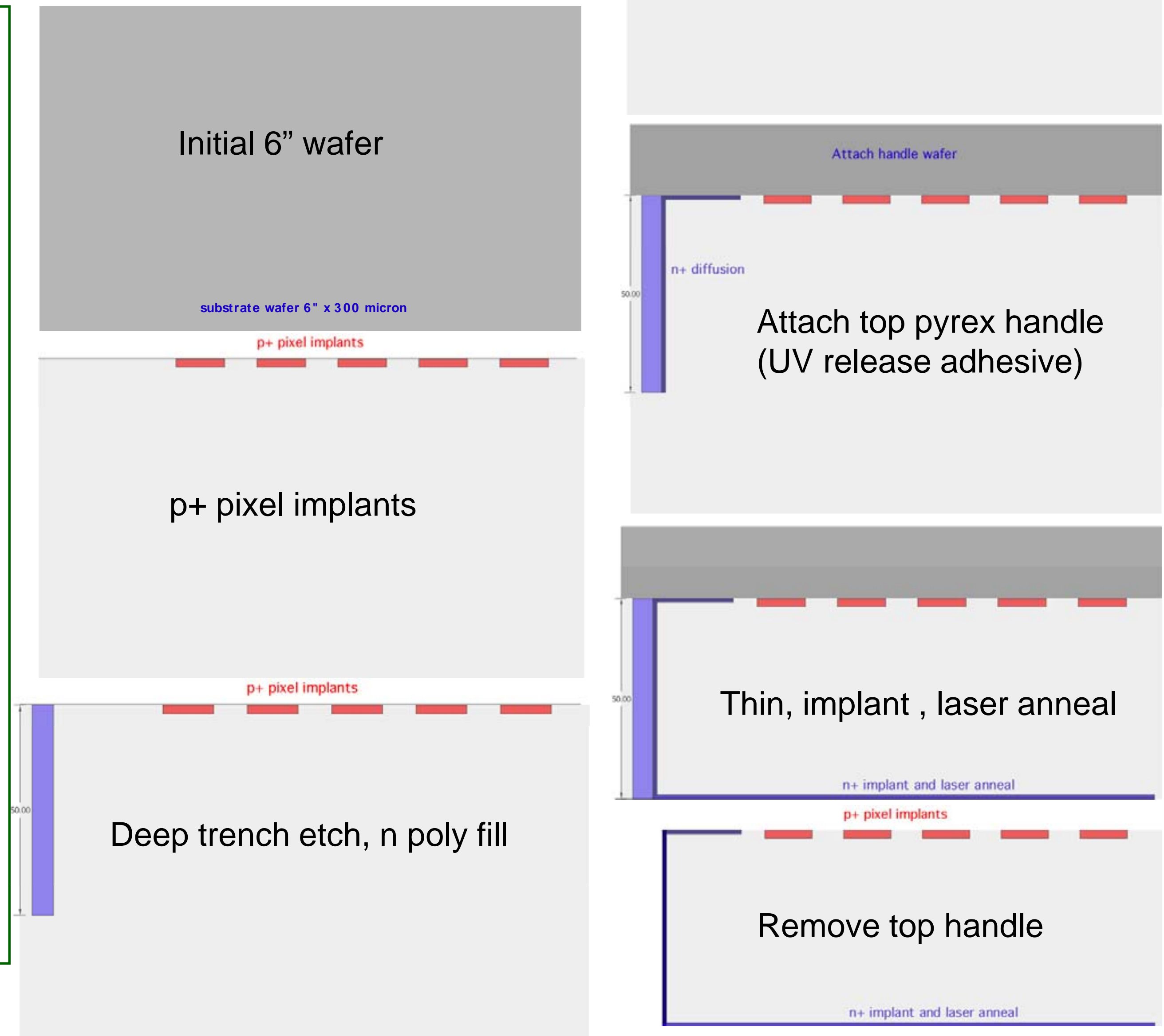


Equipotential lines in detector near one detector edge

Detector Process

Issues:
- How to hold wafer during backside thinning, implantation, anneal
- How to handle wafer once thinned to 50-100 microns

Commercial processes:
- Rim thinning
- Handle wafers
  - Silicon with epoxy
  - Thermal release adhesive
  - UV release adhesive with glass handle



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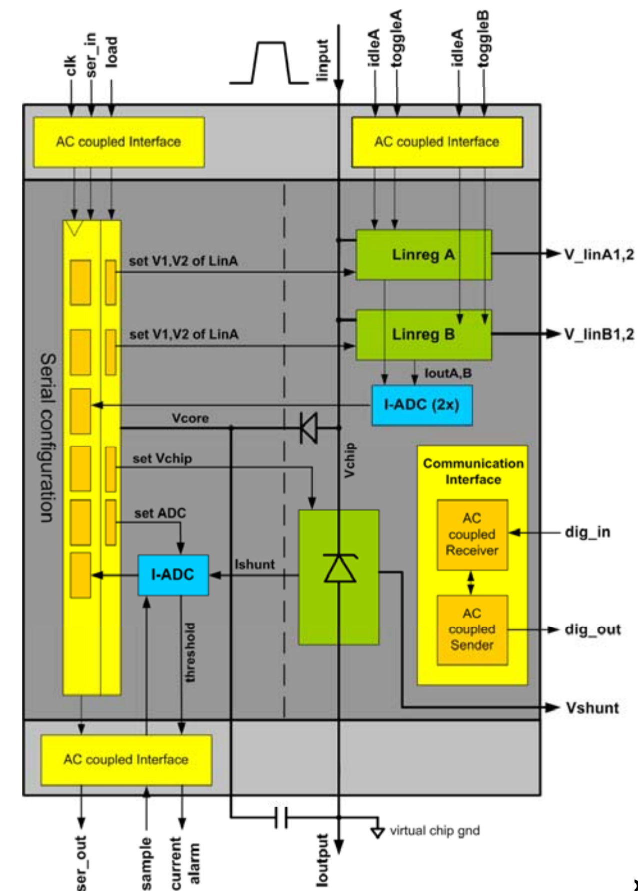
Thinning and Laser Annealing

- Initial thinning – designed to avoid contamination in MIT-LL implanter failed
  - 50 μm trenched dummy silicon wafer on pyrex cracked curing epoxy removal
  - Used shards to study handling.
    - We were able to removed the silicon from the pyrex to dicing tape, dice and then remove the diced detector
    - Use this to study bonding, gluing …
- New study using Micron 6” donated wafers
  - More standard process – no epoxy, implantation at commercal firm
  - Stuck at grinding vendor due to argument with CMP subcontractor
  - Verify process soon – MIT LL will laser anneal
- If this works we will thin the MIT-LL wafers, and also thin and anneal one OKI SOI detector wafer.
- Laser annealing study with thinned HPK strip detectors almost done
  - Generally good results but some variation in IV characteristics with “identical” processing
  - Cornell student completing dedicated study of annealing parameters

Serial Powering

- Chip designed in collaboration with RAL/ATLAS
  - Demonstration of rad rad chip with pulsed power features
  - Bump bonded interconnects
  - Hope to submit in ~ 2 months

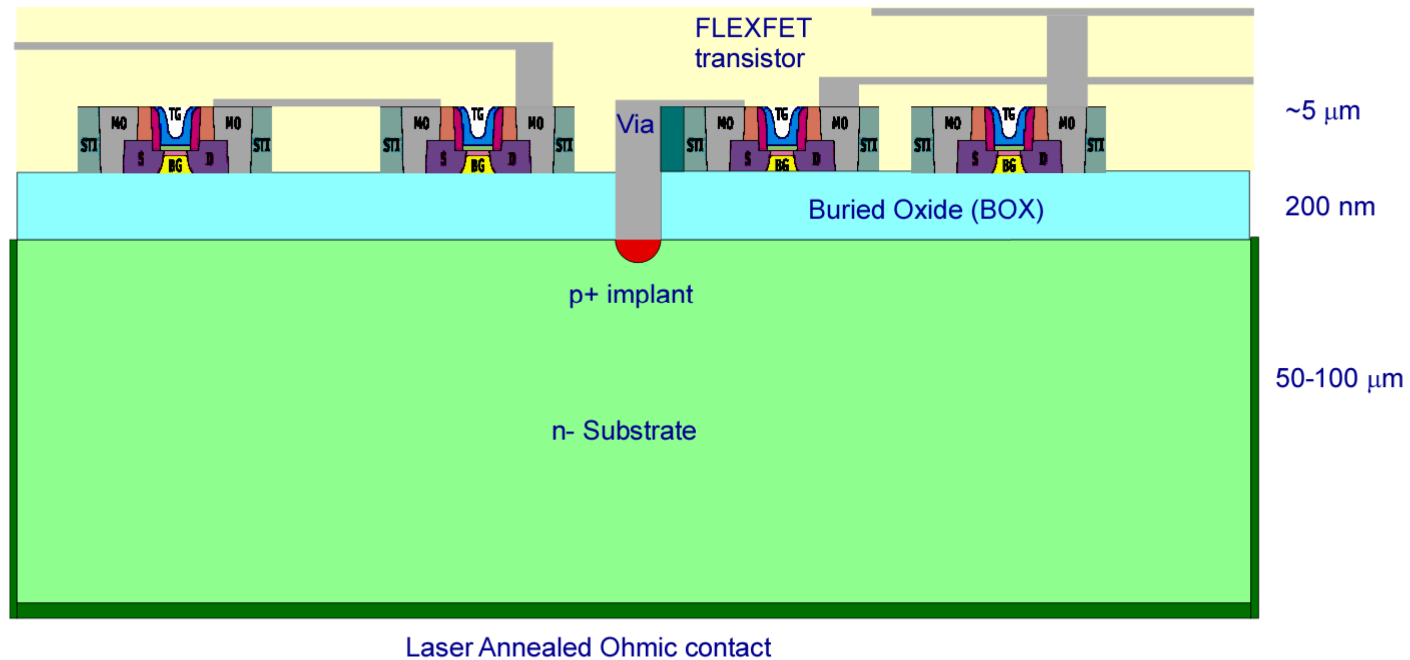
old design



SOI Detector for HEP

not to scale

Minimal interconnects,
low node capacitance



High resistivity
Silicon wafer,
Thinned to 50-100 microns

Active edge
processing

Backside implanted after thinning
Before frontside wafer processing
Or laser annealed after processing

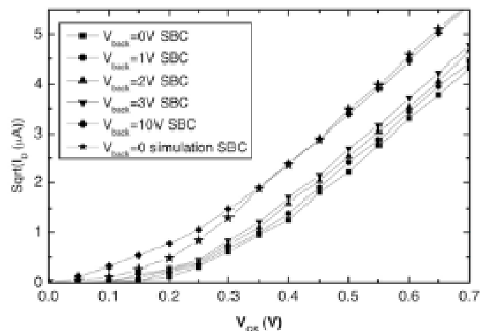
Fermilab SOI Detector Activities

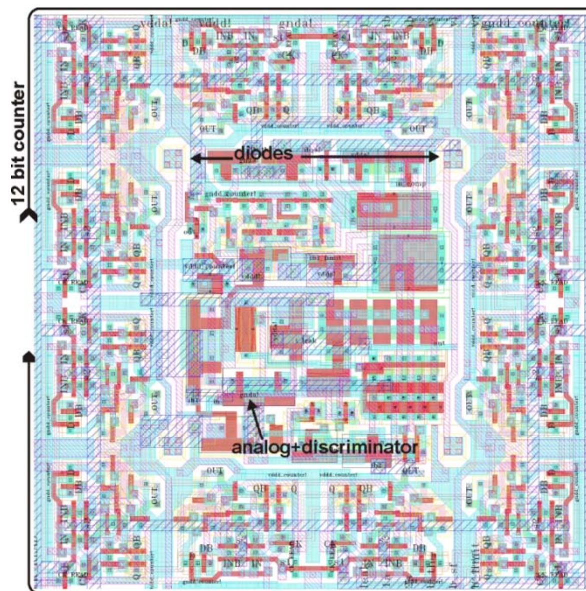
SOI detector development is being pursued by Fermilab at three different foundries:OKI in Japan (via KEK), and American Semiconductor Inc. (ASI) and MIT Lincoln Labs in the US.

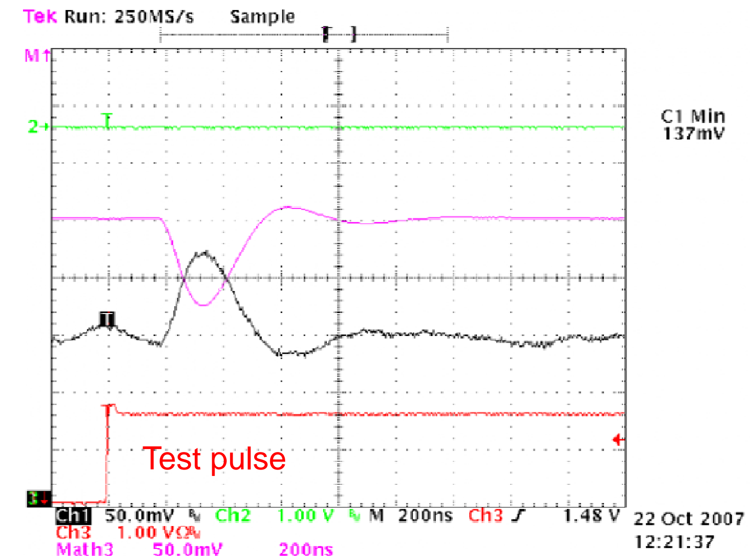
	OKI	MIT-LL	ASI
Feature size (μm)	0.15 0.2	0.18 0.15	0.18
Wafer Diameter	150mm	150mm	200mm
Transistor type	Fully depleted	Fully depleted	Partially depleted dual gate
Buried Oxide	200 nm	400 nm	200 nm
Work underway	Test Structures Mambo chip Laser anneal Mambo II	Test Structures 3D chip 3D RunII 3D Dedicated	SBIR design Simulation Test Structures Sensor SBIR

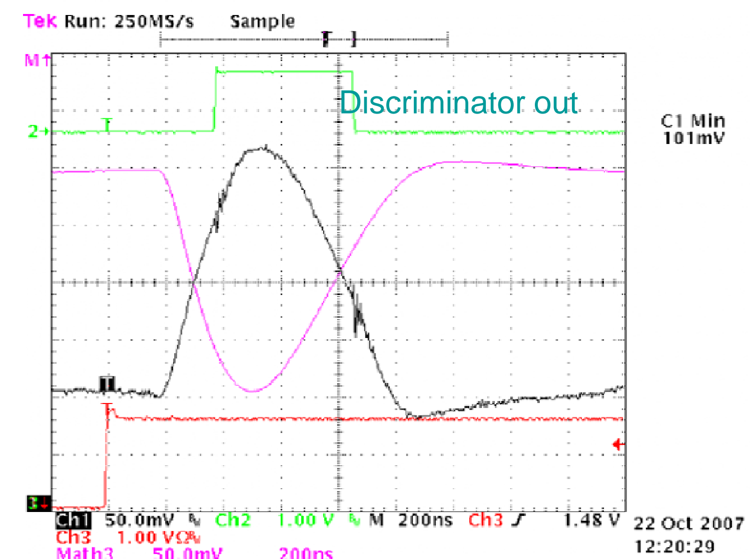
MAMBO - Monolithic Active pixel Matrix with Binary cOunters in SOI Technology OKI 0.15µm

- KEK sponsored multiproject run at OKI. 64 x 64 26 micron pitch 12 bit counter array for a high dynamic range x-ray or electron microscope
- input charge ~1250 e-,
- 80e-<ENC<100e-
- Back gate limited combined analog/digital performance
- MAMBO II to be submitted this week 0.2 micron









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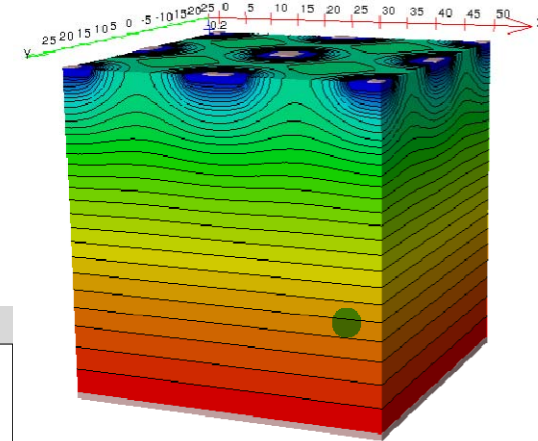
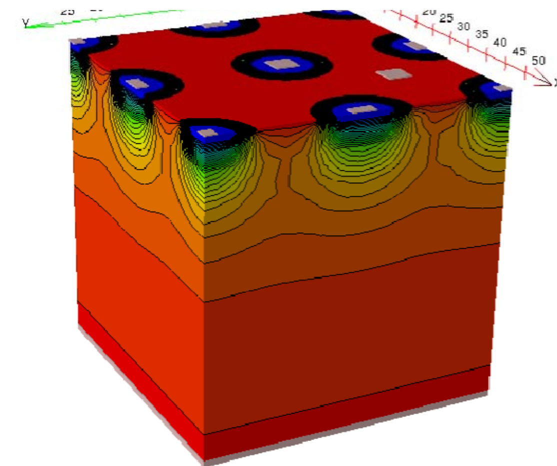
SOI Device Simulation

- Study charge collection, coupling, and diffusion as a function of pixel implant and pinning layer dimensions. Keep bias at 10 V to limit back gate effects. (Silvaco 3D TCAD simulations)

25 micron pitch
2 micron pixel - pinning gap



No pinning 10V Bias
8 micron pixels



n+ pinning 10V Bias
8 micron pixels