

# Omega

**FEV5 PCB design  
+ ECAL status**

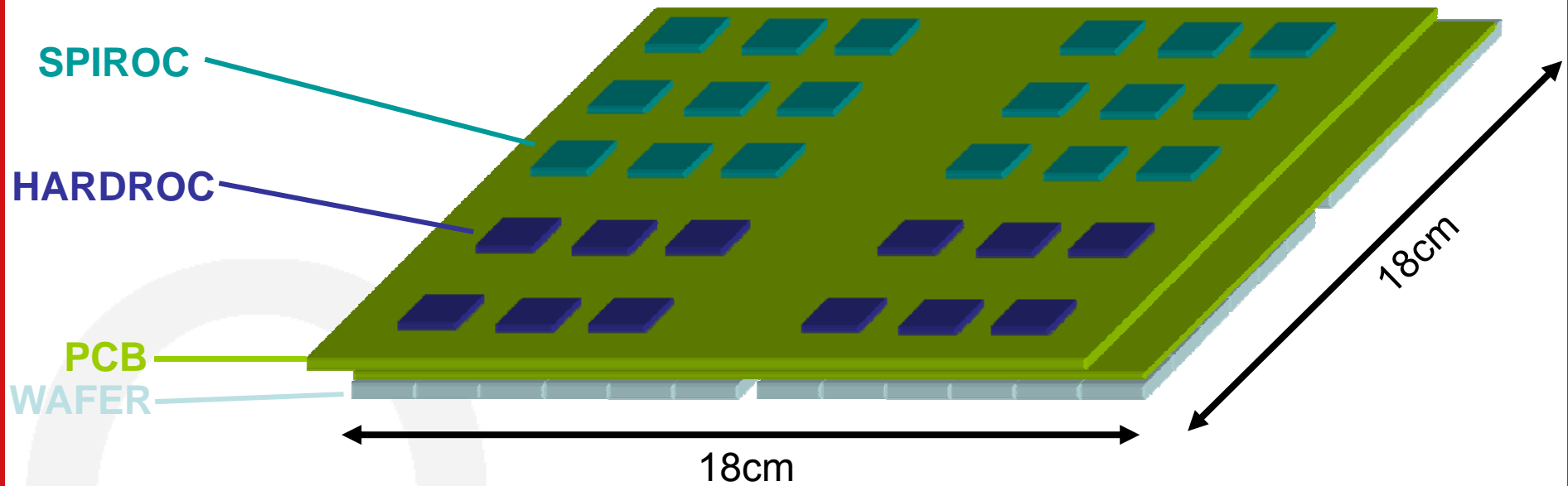
6 February, 2008

*Orsay MicroElectronics Group Associated*

- Designed for :
  - 6-inch wafers (4 wafers of 9\*9cm)
  - 0.5\*0.5cm<sup>2</sup> pads → 324 pads/wafer → 1296 channels/PCB
  - Only 512 equipped with 8 Hardroc Chips
- New stitching :
  - No step, solder pins on top layer
  - Exact solder procedure to be defined (Patrick, Maurice, etc.)
- In fab : expected end of January

# FEV5 : first thoughts

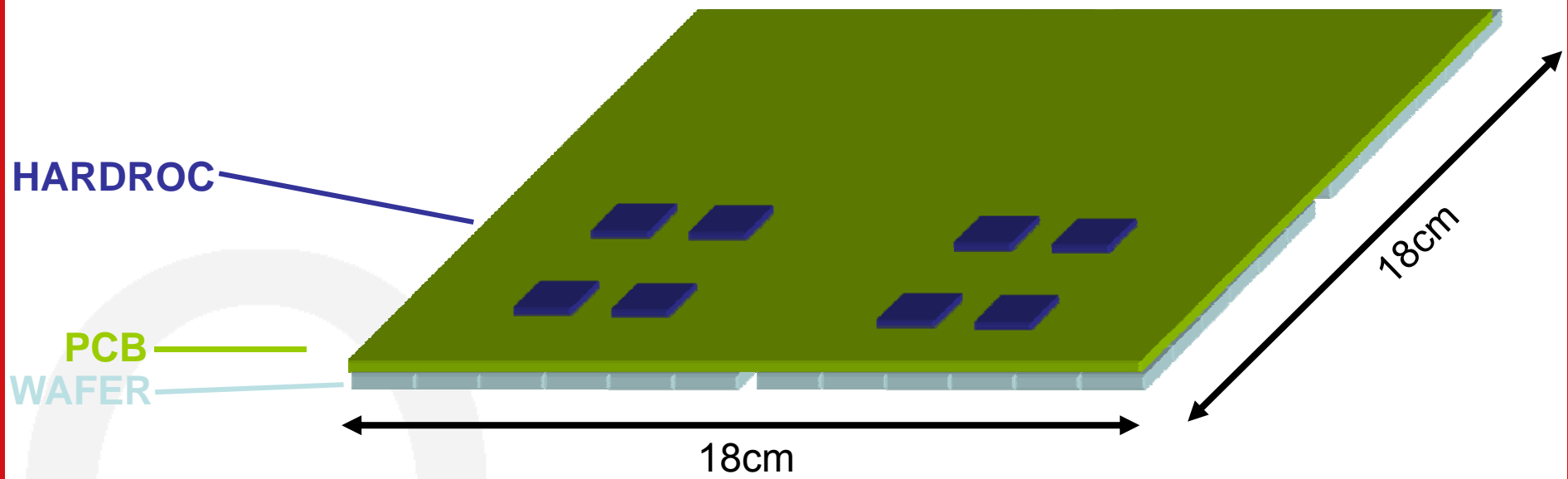
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1296 channels. Half SPIROC (18 chips) / half HARDROC (12 chips)

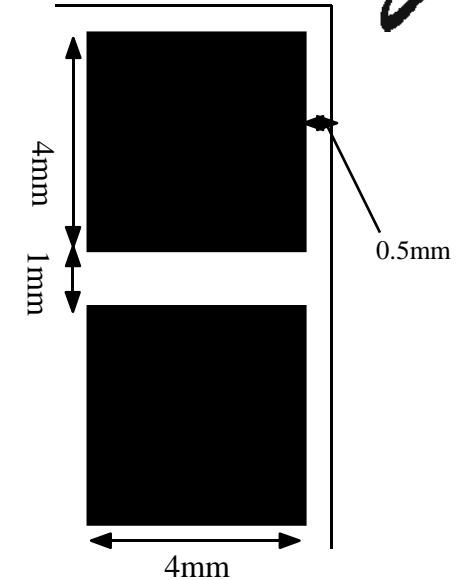
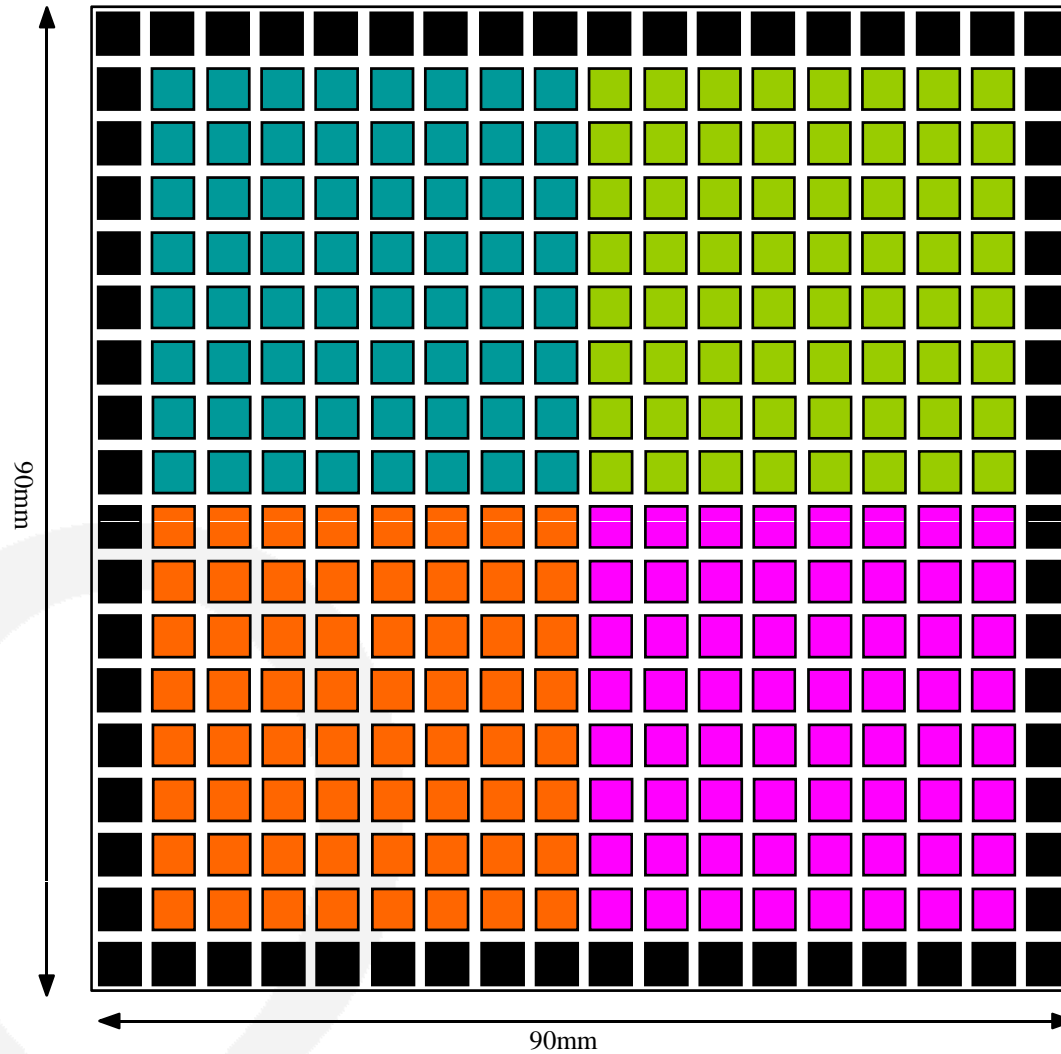
# FEV5 : designed

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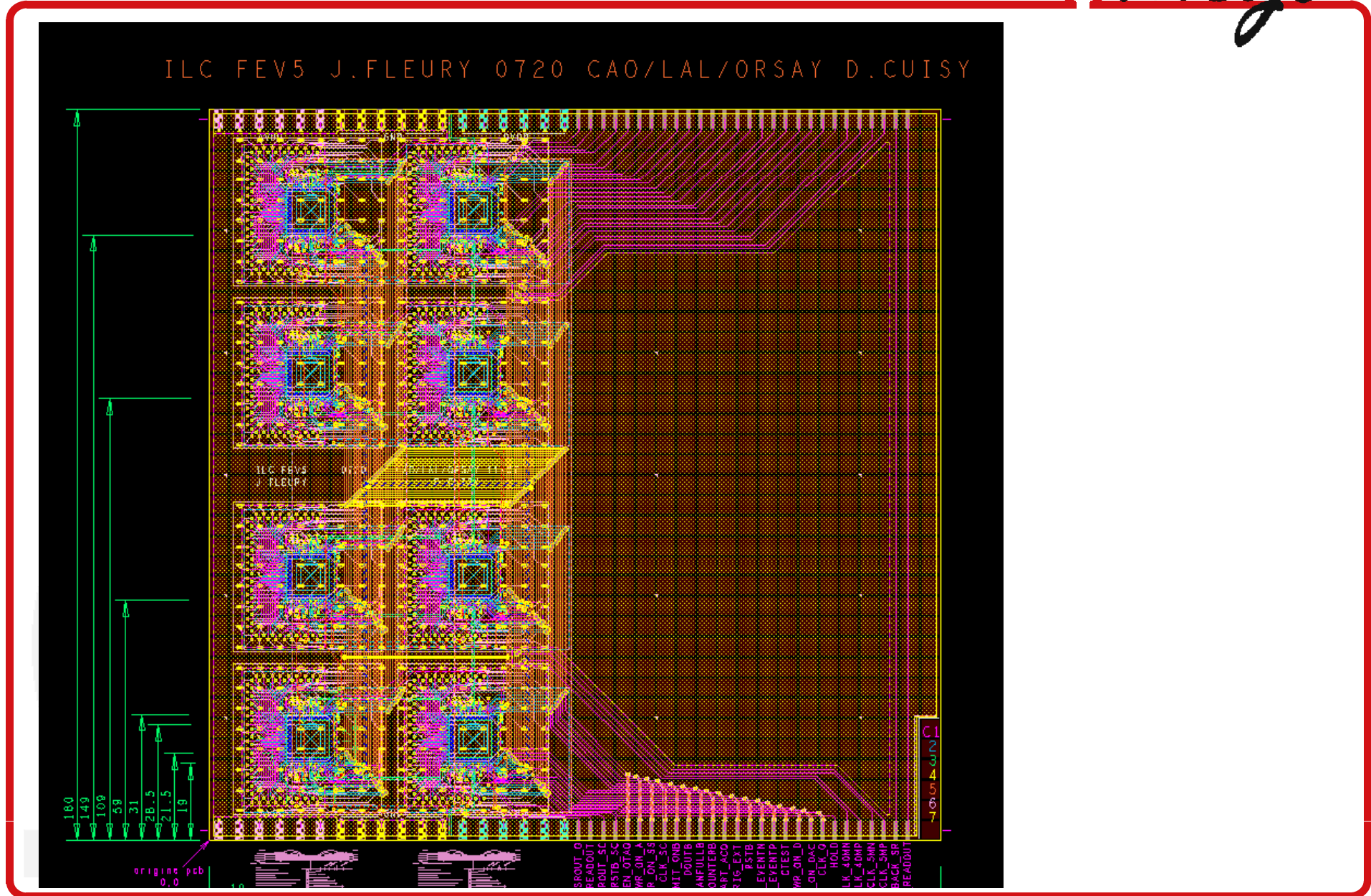
1296 channels. 8 HARDROC (512 channels equipped)

# Wafer : channel equipped



- Chip 1
- Chip 2
- Chip 3
- Chip 4
- NC

# Layout : general



# Chip Embedding + PCB Pile-up

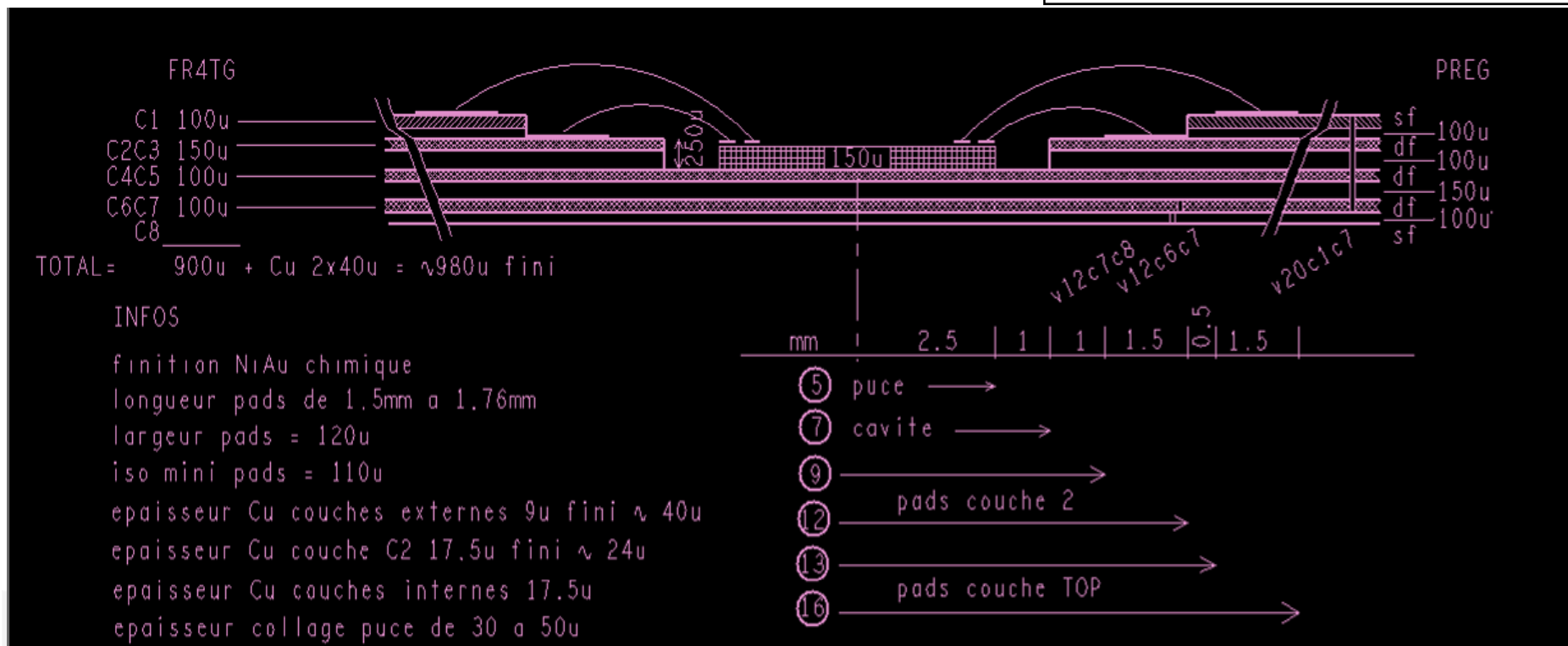


## Pile-up

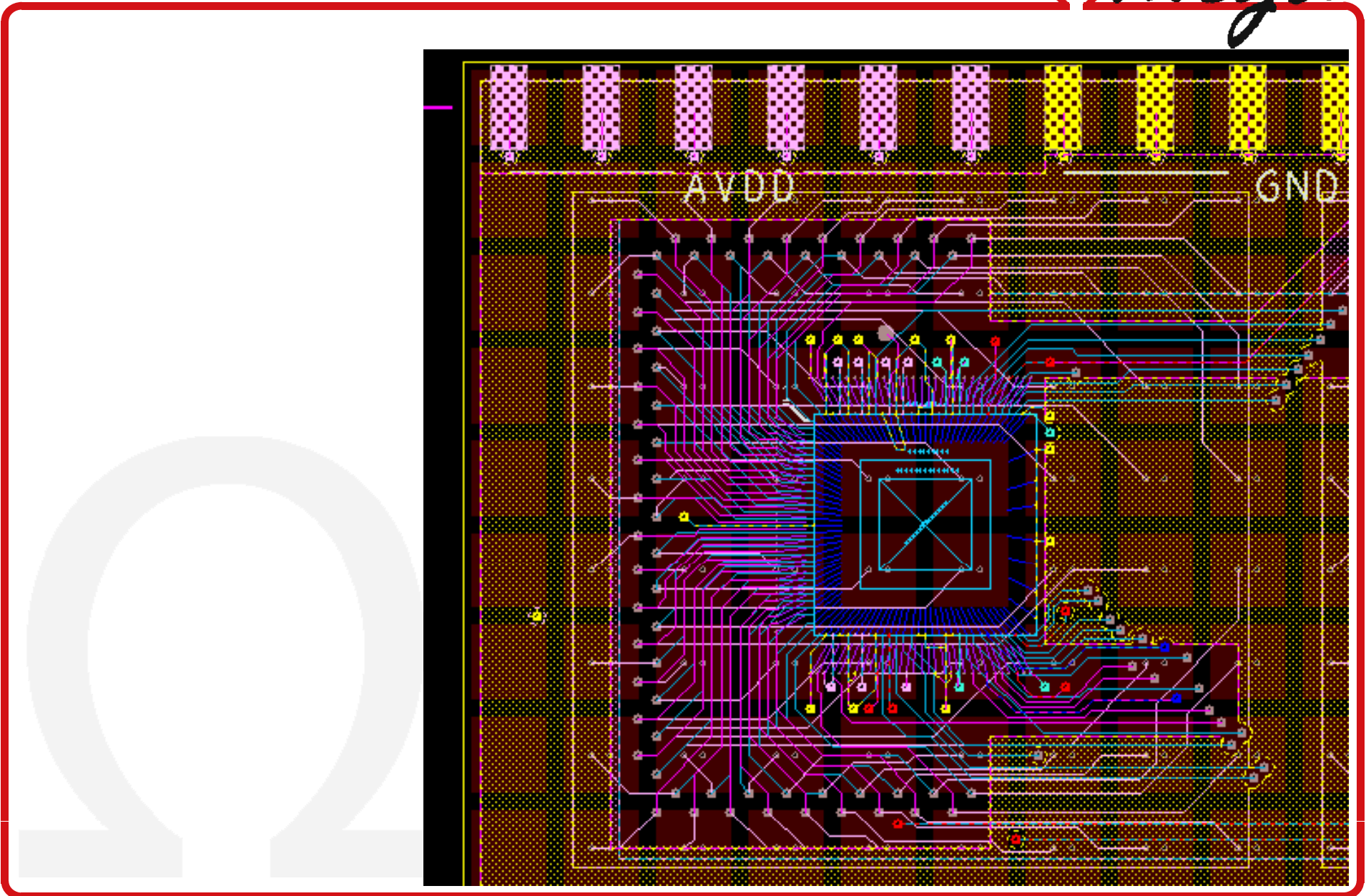
TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

## 3 drilling sequences :

- Laser C7-C8 120μ filled
- Laser C6-C7 120μ
- Mechanical C1-C7

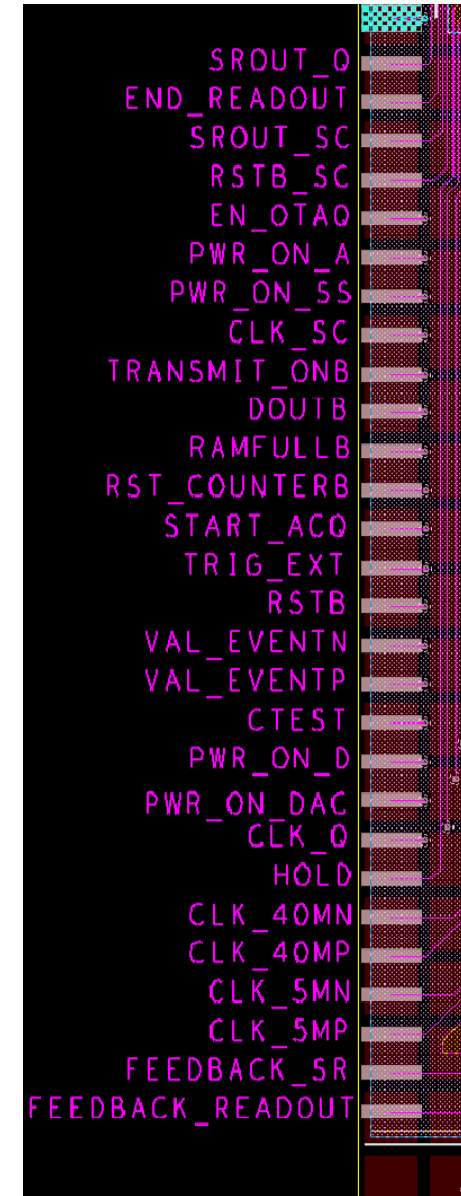
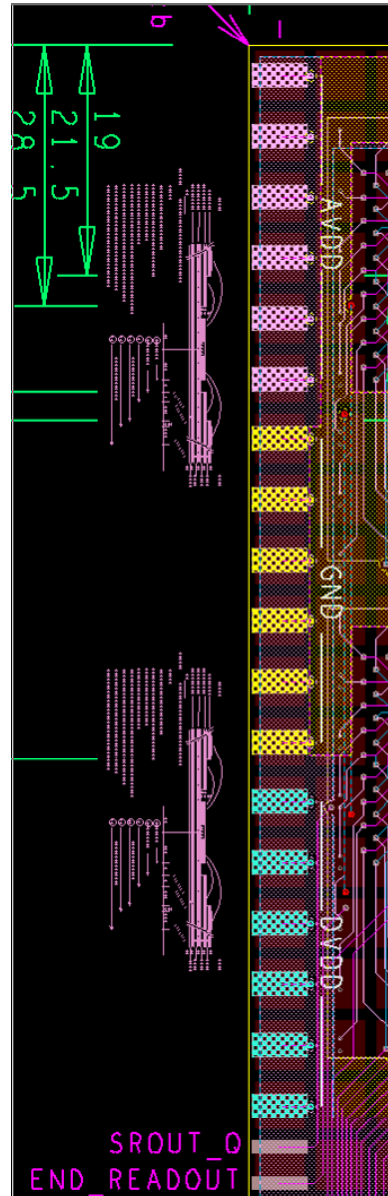


# Pads tu Hardroc connection





# I/O list



## Conclusion

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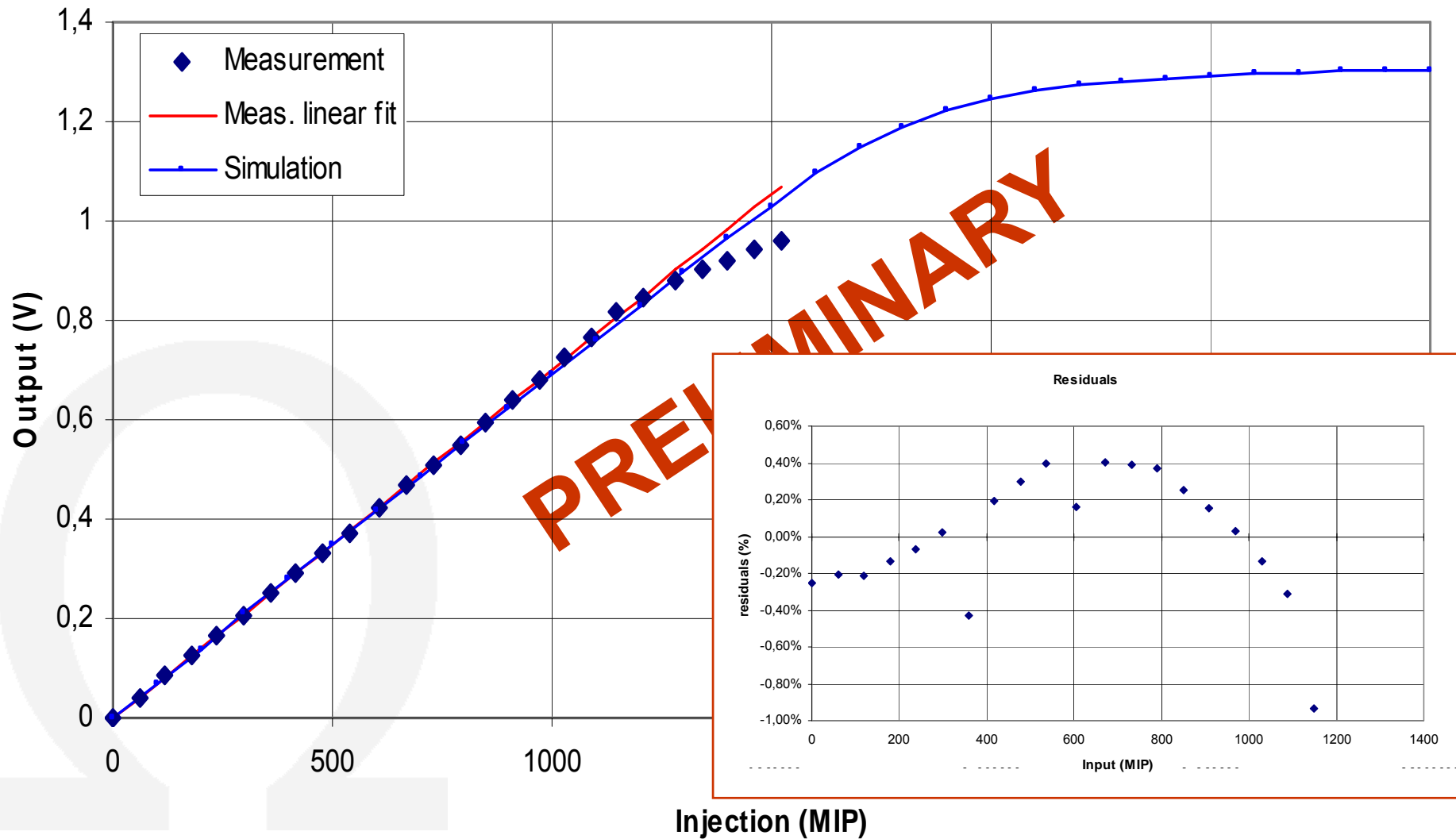
- Within 2 months : first ASU prototype available for collaboration
- Need a DIF to connect and test
  - No way to test without a DIF
  - First 8-hardroc chain
- Schedule ?



# SKIROC STATUS



### SKIROC linearity results



# Pedestal dispersion



The pedestal measurement is coherent with what we expect :  
-No pedestal pattern (random values according to statistical dispersion)  
-Statistical dispersion equivalent to what we get with that technology

## Standard deviation :

$$\sigma_{\text{Gain 1}} = 1.8\text{mV}$$

$$\sigma_{\text{Gain 10}} = 1.95\text{mV}$$

## Standard deviation ADC

$$\sigma_{\text{Gain 1}} = 1.84\text{mV}$$

$$\sigma_{\text{Gain 10}} = 2.1\text{mV}$$

