Status Report on ADC developments @ LPC Clermont-Ferrand

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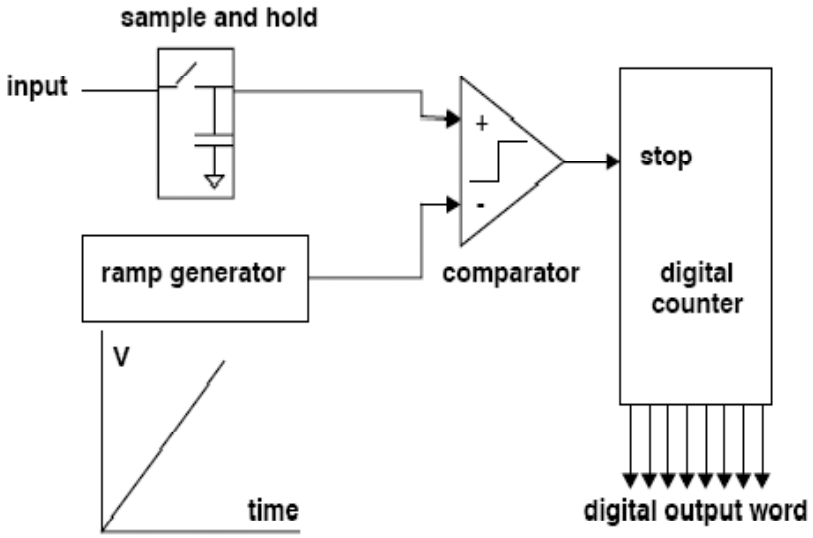
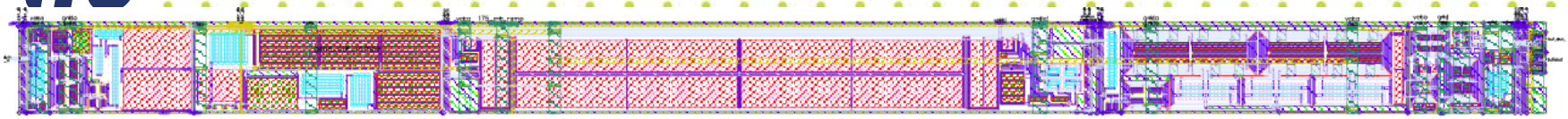
A 12-bit 3.5V Wilkinson ADC

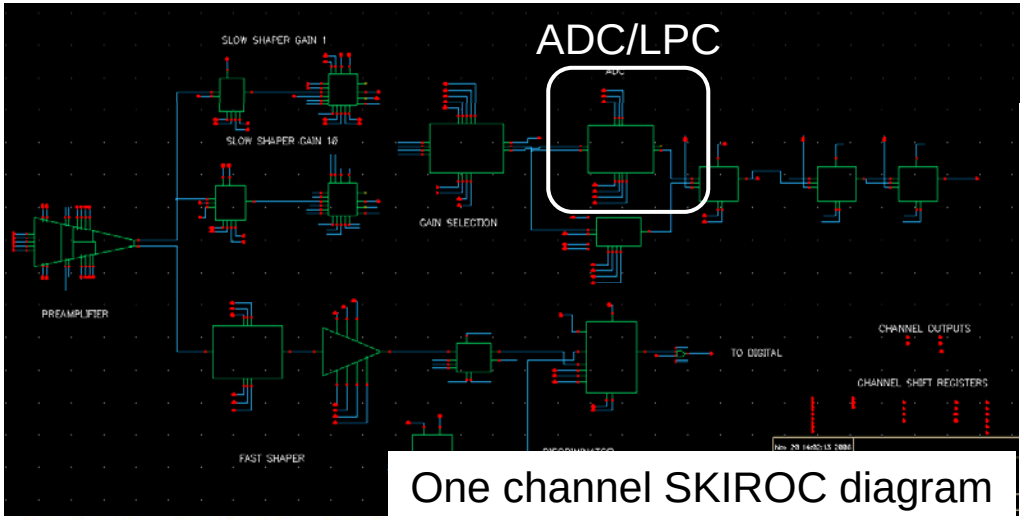


12-bit **Wilkinson** ADC in SKIROC



Layout of the ADC

- Characteristics:
  - **Techno: BiCMOS SiGe 0.35µm**
  - **Power consumption: 3 mW @ 3.5V**
  - **Power pulsing**
  - **Conversion time : 80µs @50MHz**
  - **Differential architecture**
  - **Open loop ramp generator**
  - **Die area: 0.12 mm²**

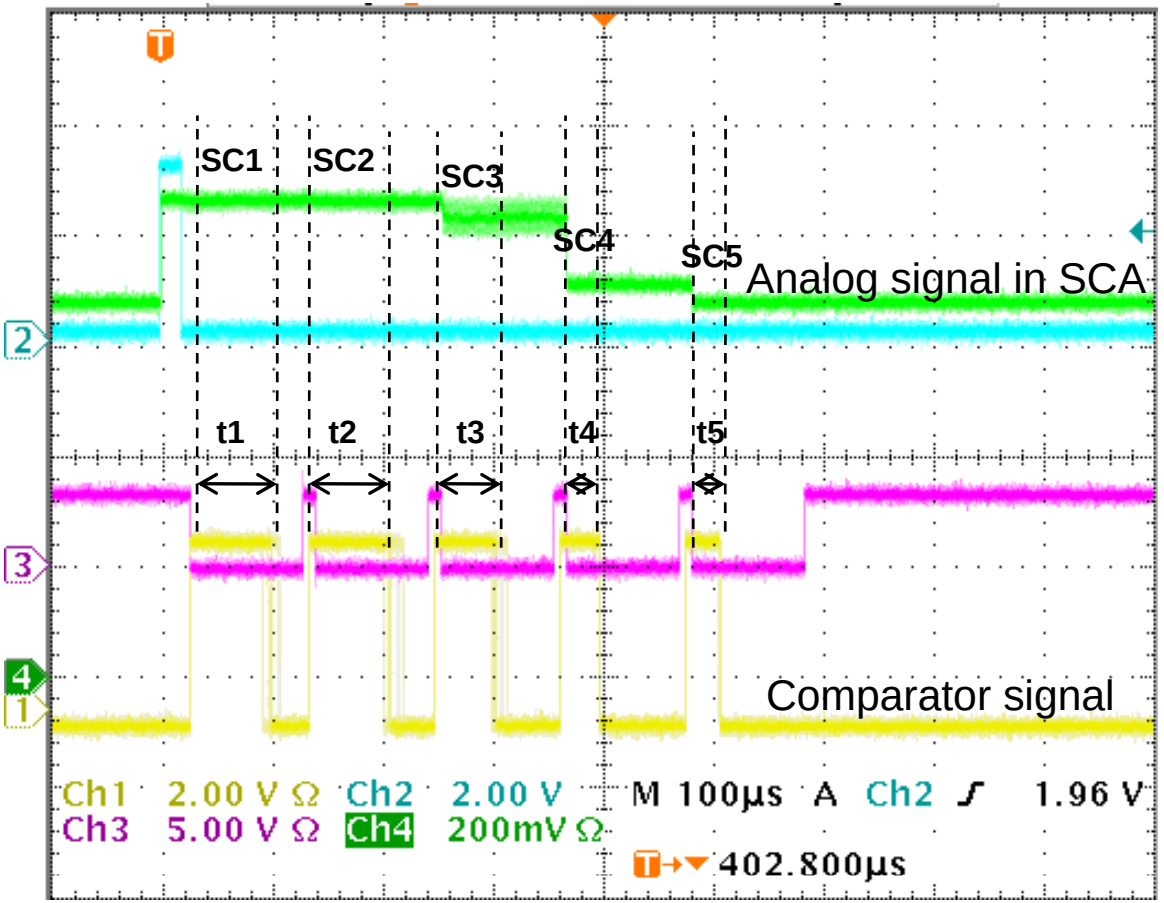


One channel SKIROC diagram

SKIROC measurements @ LPC

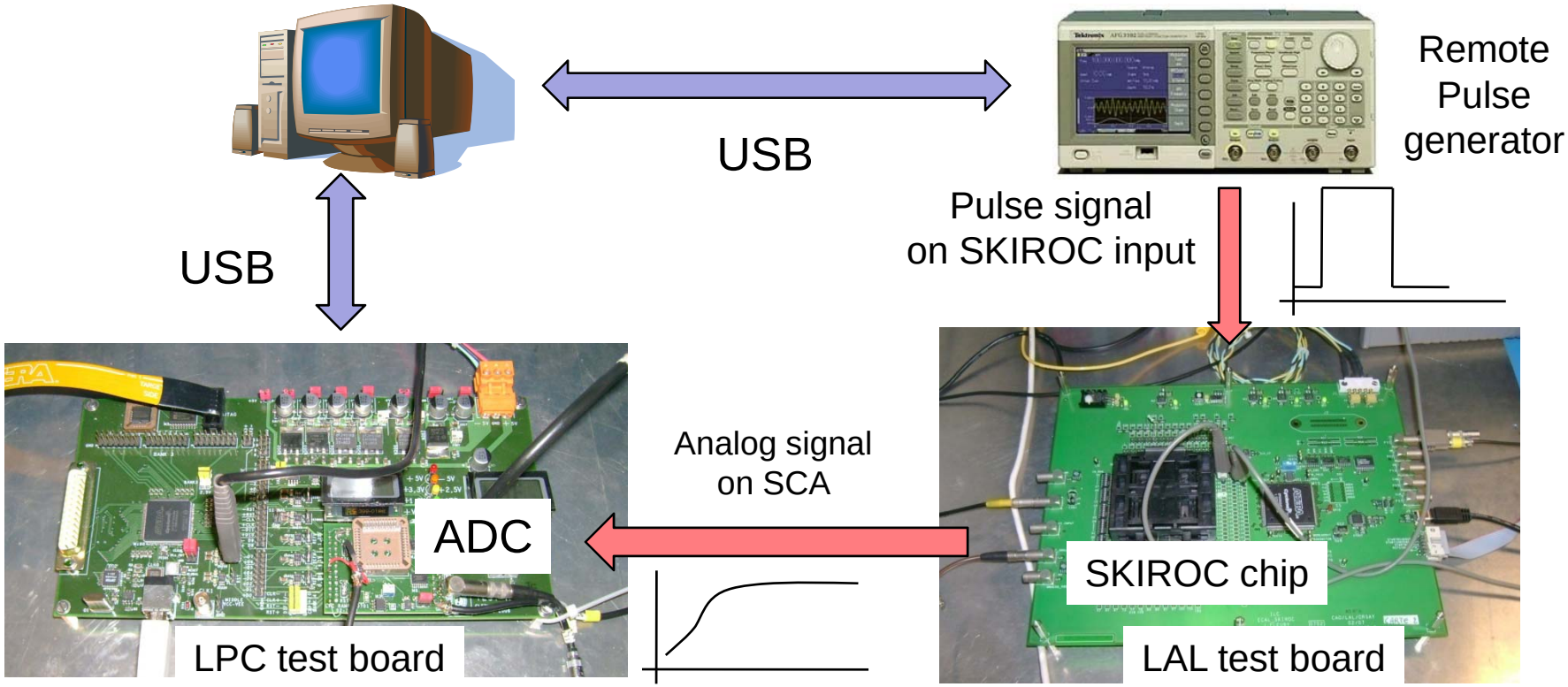
Status:

- One test board given by LAL @ LPC to test ADCs
- LabView Control program developed by LAL used to configure SKIROC through USB interface
- Several bugs found in the digital part (in FPGA)
  - Fixed by LAL
- ADC functionality checked with scope



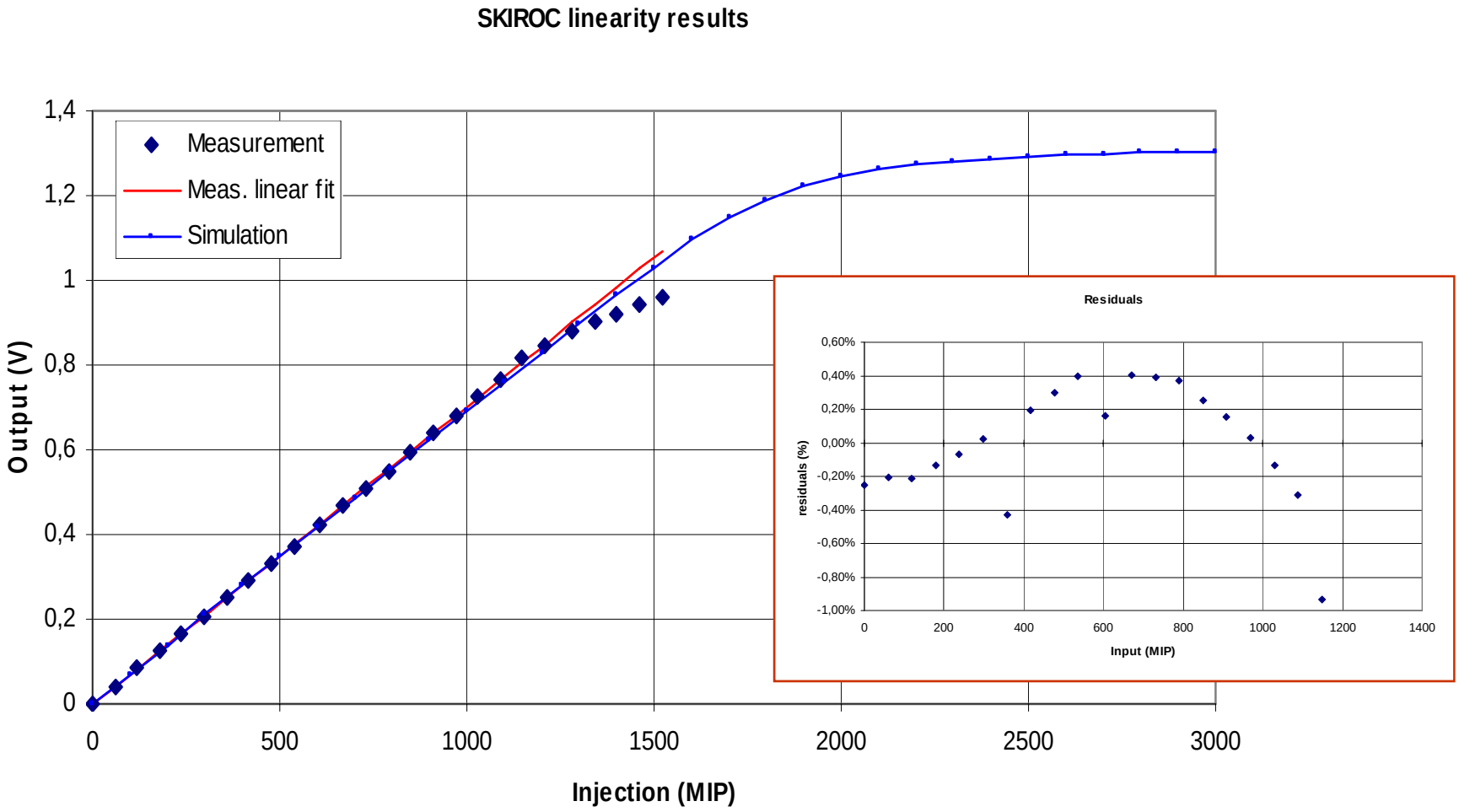
SKIROC measurements @ LPC

- To measure ADC performance, the automatic transfer of the ADC digital data from FPGA to PC via USB is required
  - under devpt @ LAL
- We have adapted the setup of the test bench @ LPC to measure linearity of the analog channel (preamp + shaper) and to compare results with those obtained @ LAL



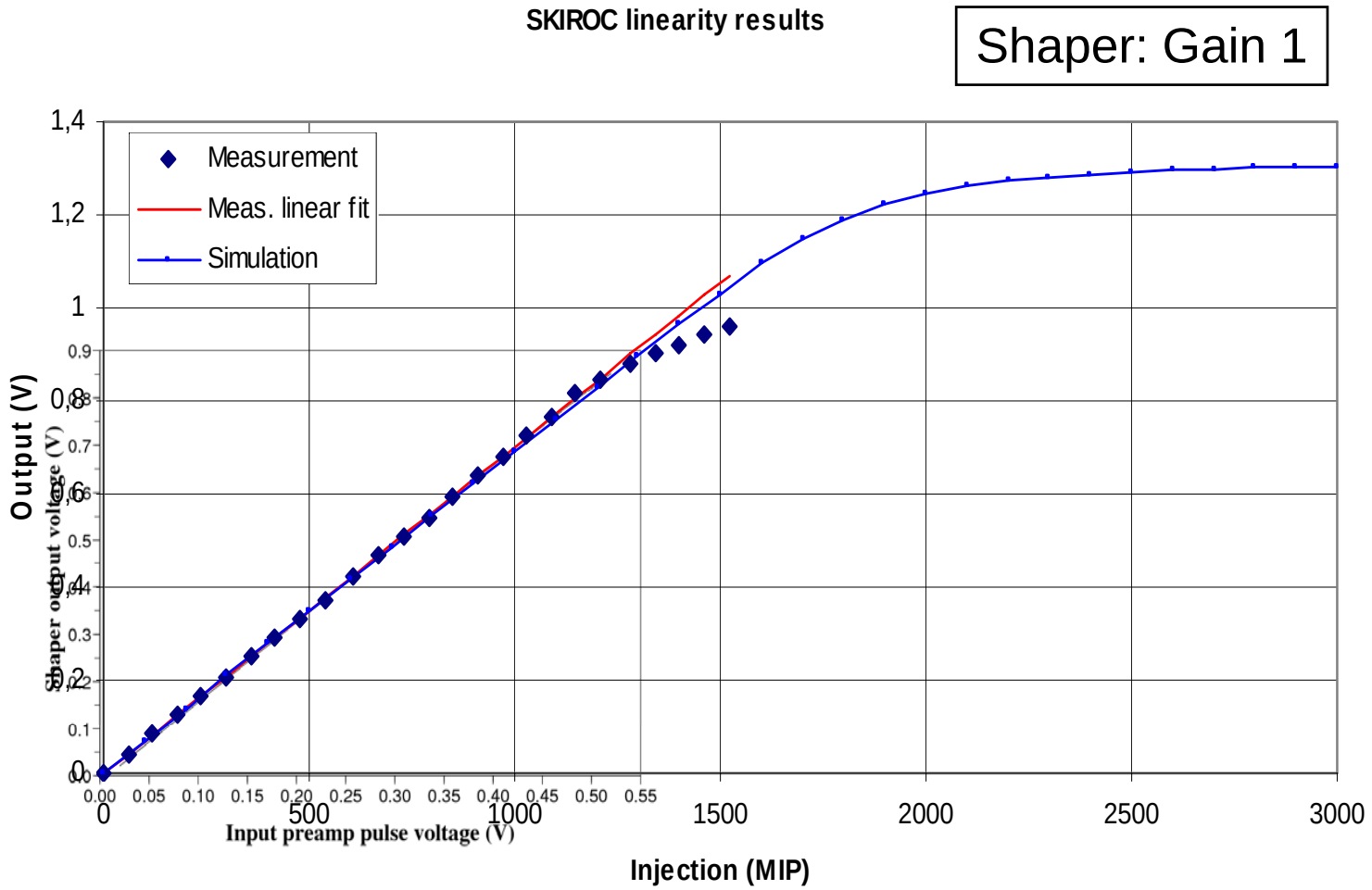
Setup to test the (preampli + shaper) linearity

Linearity measurements @ LAL

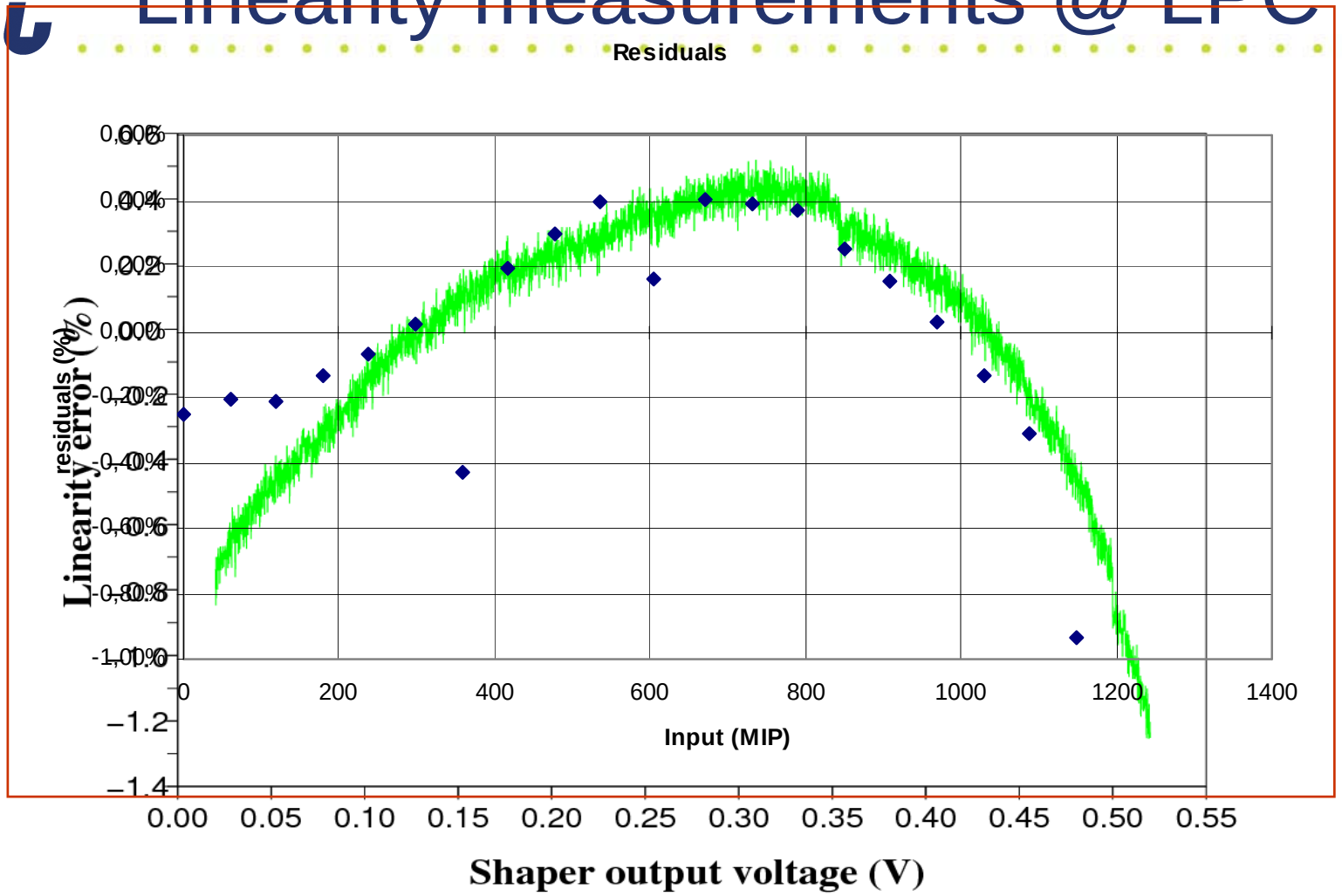


Not expected saturation observed @ 1200 MIPs

Linearity measurements @ LPC

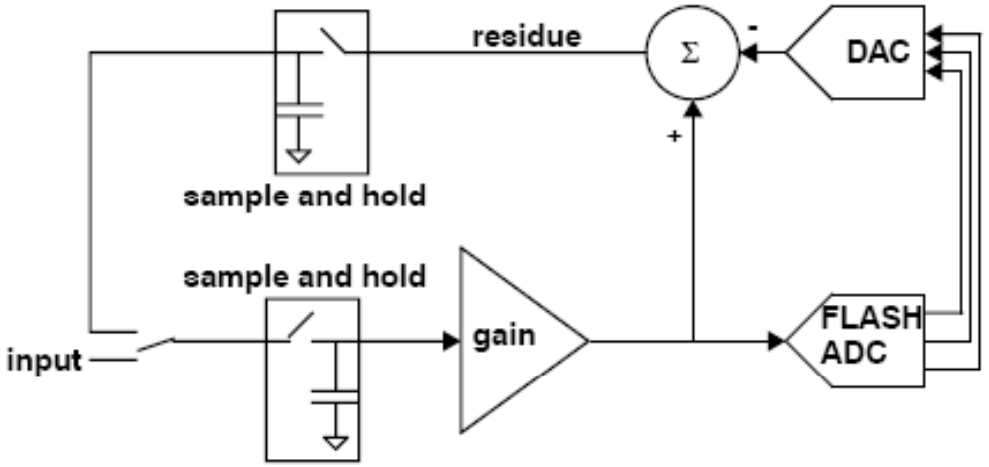


Linearity measurements @ LPC



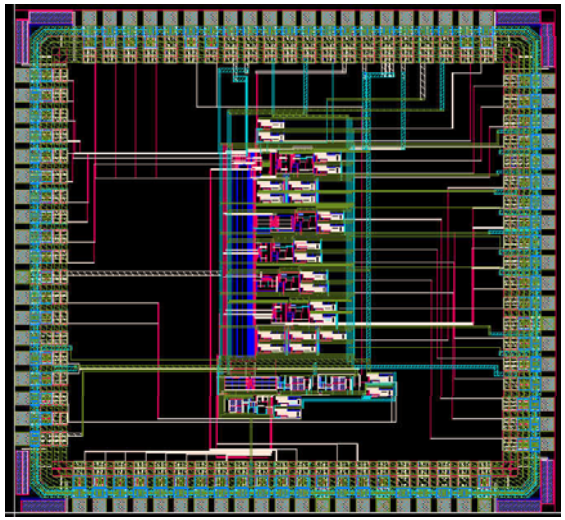
Same saturation observed @ LAL &LPC:
>>> not induced by the test bench

A 12-bit 3.5V Cyclic ADC



12 bits – 3.5V cyclic ADC

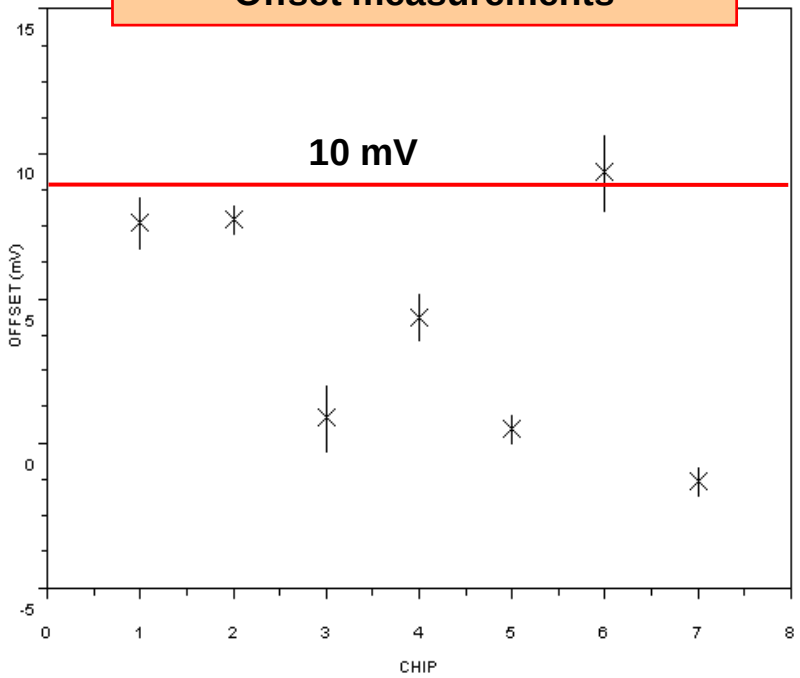
- **Objective :**
  - Design a 12-bit cyclic ADC with 3.5V power sup. based on the buildings blocks of the pipeline ADC but with a lower power supply (5V→ 3.5V)
  - Gain 2 accuracy required for a 12-bit ADC is multiplied by 4 compare to a 10-bit ADC
    - 10 bits ADC accuracy is 1/1000
    - 12 bits ADC accuracy is 1/4000
- **Two chips designed to characterize two main elements of 12-bit cyclic ADC**
  - Comparator (July 06)
  - Gain-2 amplifier (July 07)



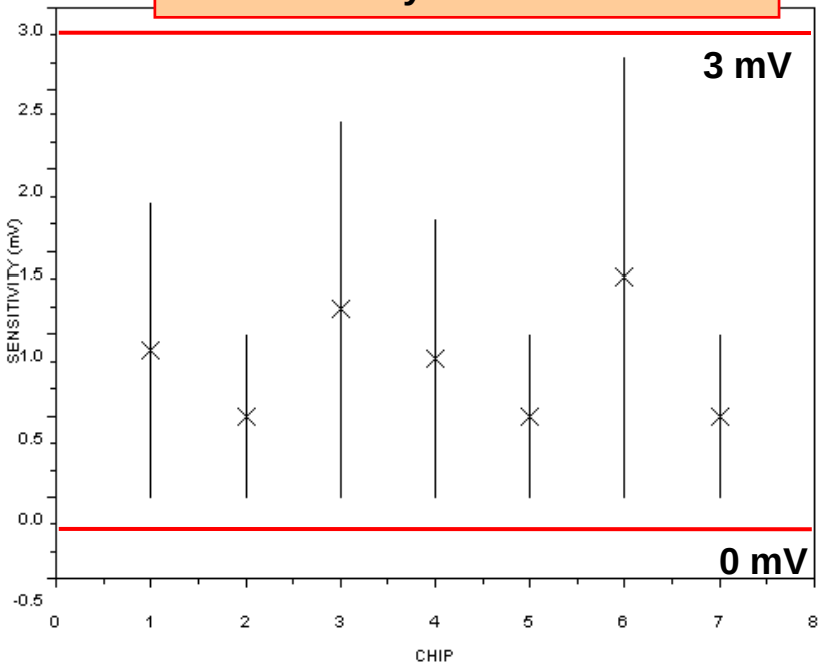
Comparator measurements

- **Characteristics:**
  - Technology: CMOS 0.35µm
  - Power supply: 3V
  - Clock frequency: 10 MHz
  - Differential architecture
  - Consumption: 68µA
  - 7 chips tested

Offset measurements



Sensitivity measurements



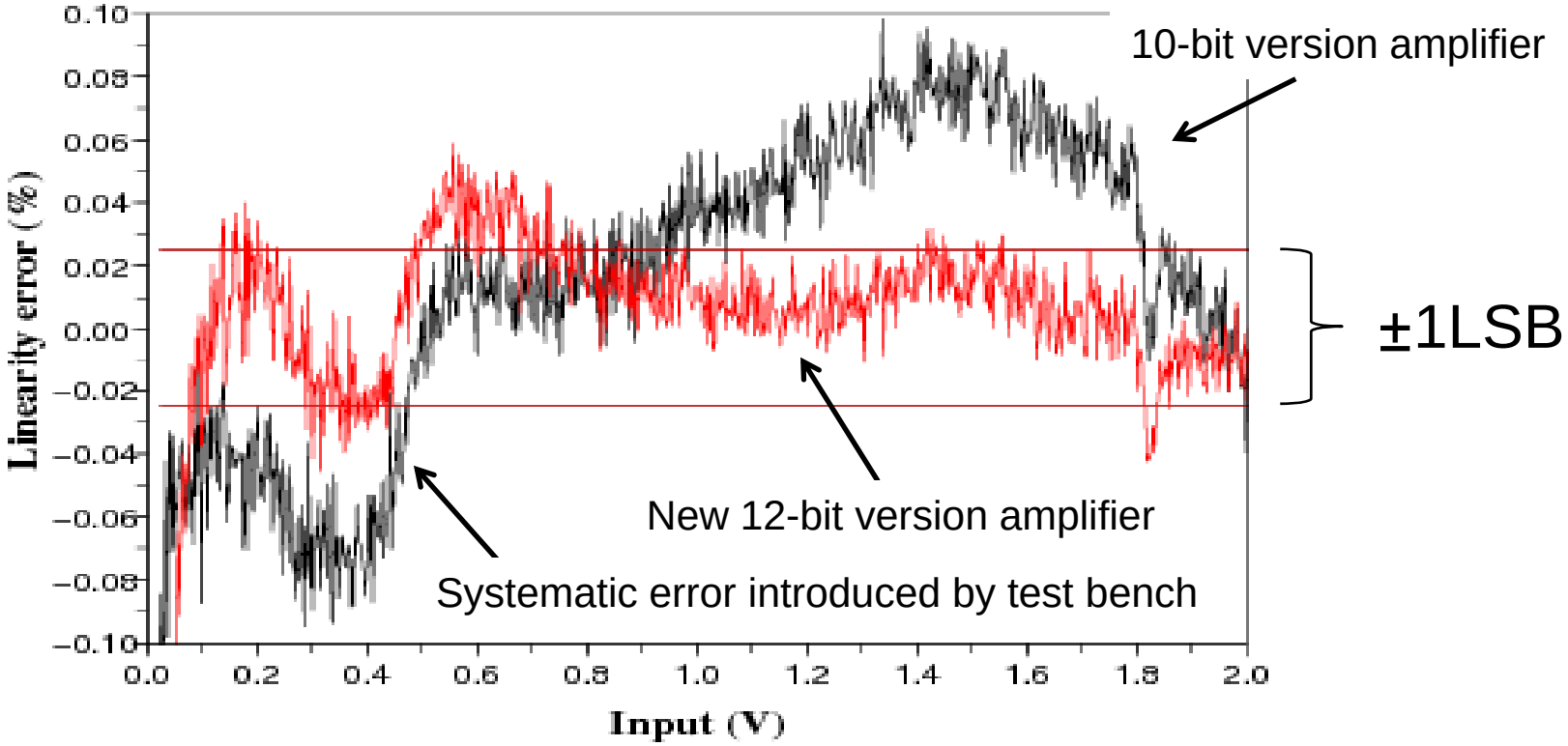
Max. Sensitivity: 3 mV @ ±3σ including setup noise
Max. Offset: 10 mV
→ Requirement: < ± 125 mV

Gain-2 amplifier: preliminary results

Characteristics & performance:

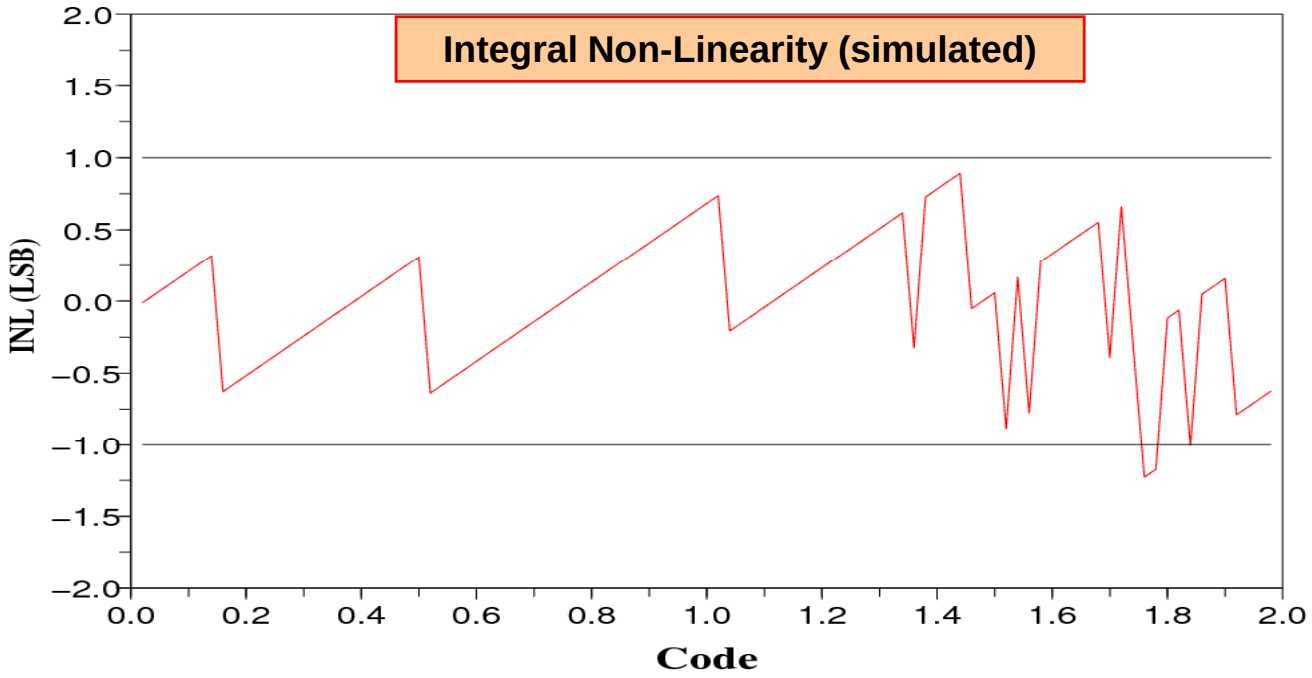
- Technology: CMOS 0.35µm
- Power supply: 3.5V
- Differential architecture
- Consumption: 2.8 mW

- Gain : 16 k
- Gain Band product: 50 MHz
- Linear, Stable
- Matching of capacitors optimized (precision of gain 2)



Simulation of the 12-bit cyclic ADC

- **An original architecture:**
  - One gain-2 amplifier and two comparators required
  - Only 6 periods of clock needed to achieve a conversion
- **Simulated performance:**
  - Integral Non-Linearity nearly within ±1 LSB
  - Conversion time (clock freq. of 1MHz) : 6 µs
  - Power consumption: 3.2 mW



Summary

	# bits	Precision	Integ. consum. per channel	Die area	Status
Pipeline	10	10 bits	0.22 µW (1%) 1 ADC/n channels	1.4mm^2	Tested & publicated
Wilkinson	12	12 bits @ low energy 10 bits @ high energy	6 µW (13%) 1 ADC/channel	0.12mm^2	in SKIROC Test in progress
Cyclic	*12*	*12 bits*	*≈0.5* µW (2%) 1 ADC/channel	*≈0.15 mm^2*	in develop^t Building blocks validated

- Our Wilkinson ADC is a candidate for the EUDET VFE chip… IF its performance is confirmed by measurements
- Our cyclic ADC, which is an evolution of the pipeline ADC, should be a good candidate to the final chip (accurated, low power, compact…)

→ Fabrication and test of prototypes foreseen in 2008