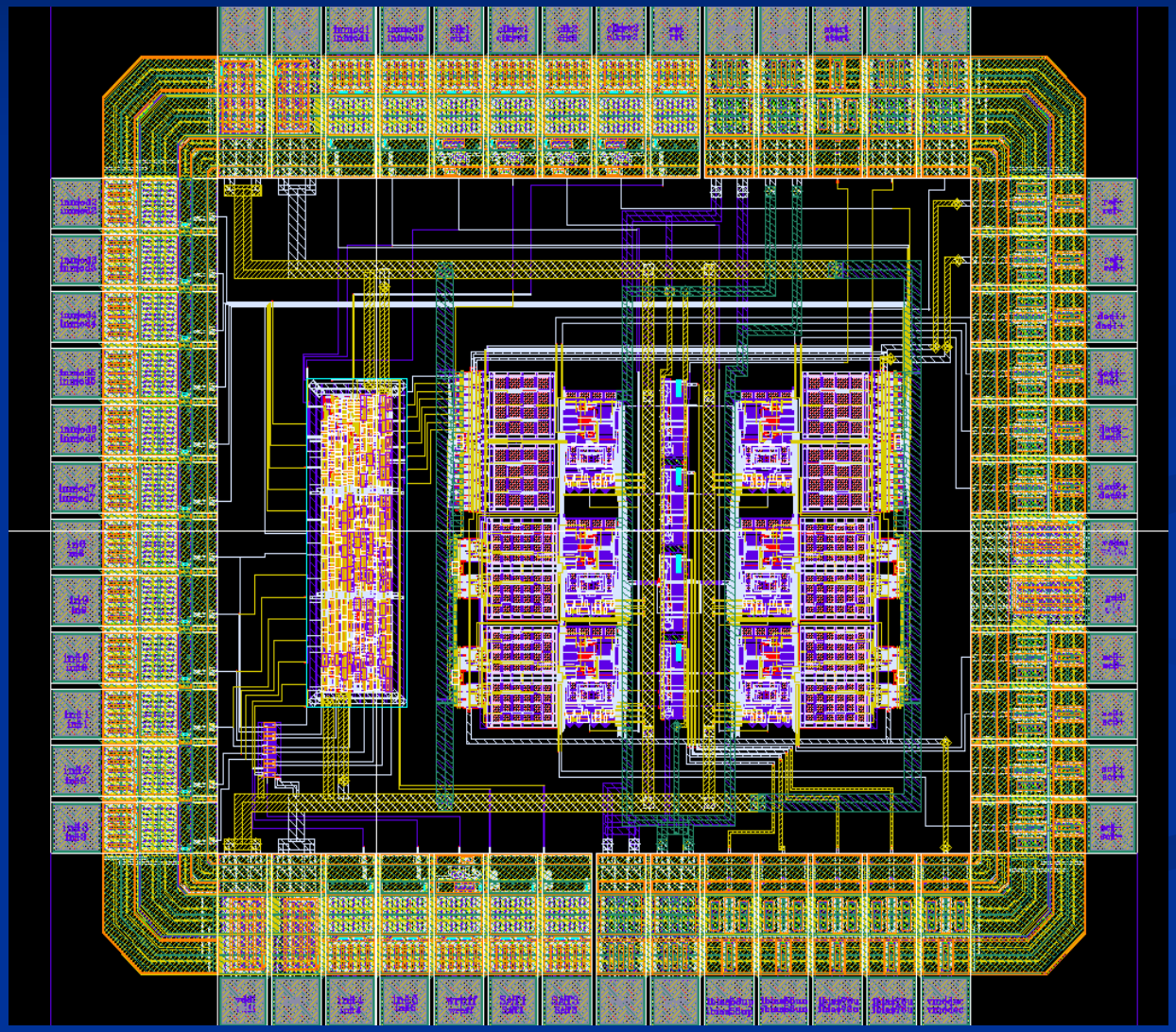
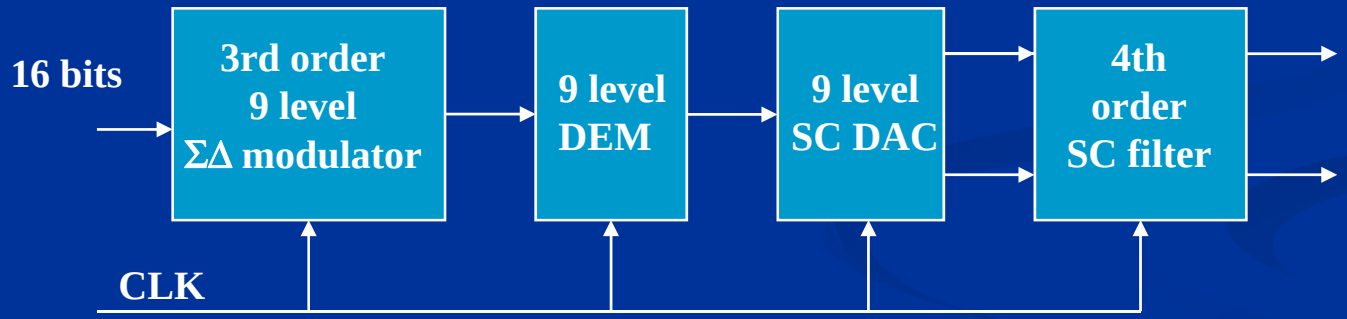
CALICE February 6th

LPSC Grenoble

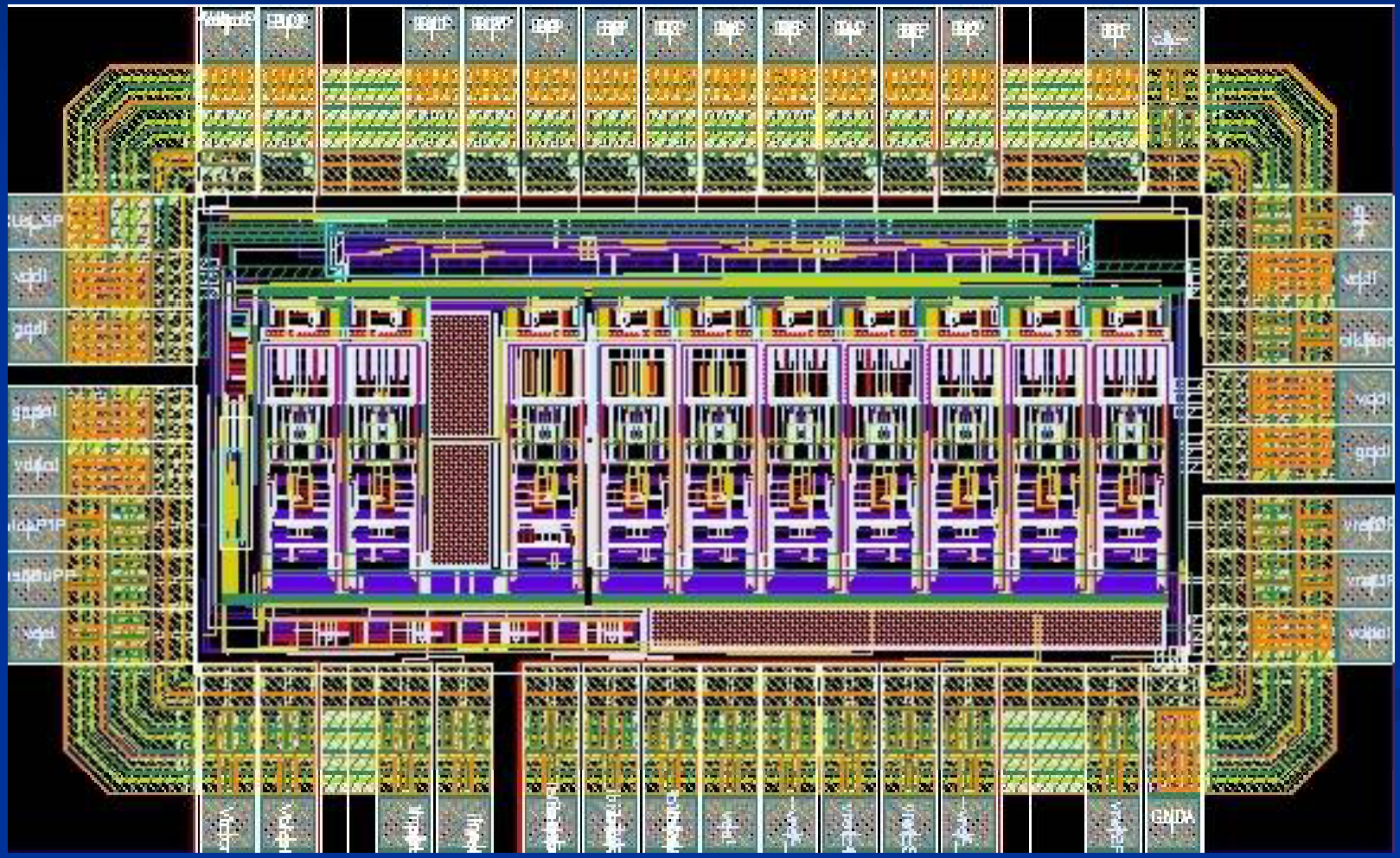
16 bits ΣΔ DAC (submitted January 21st)



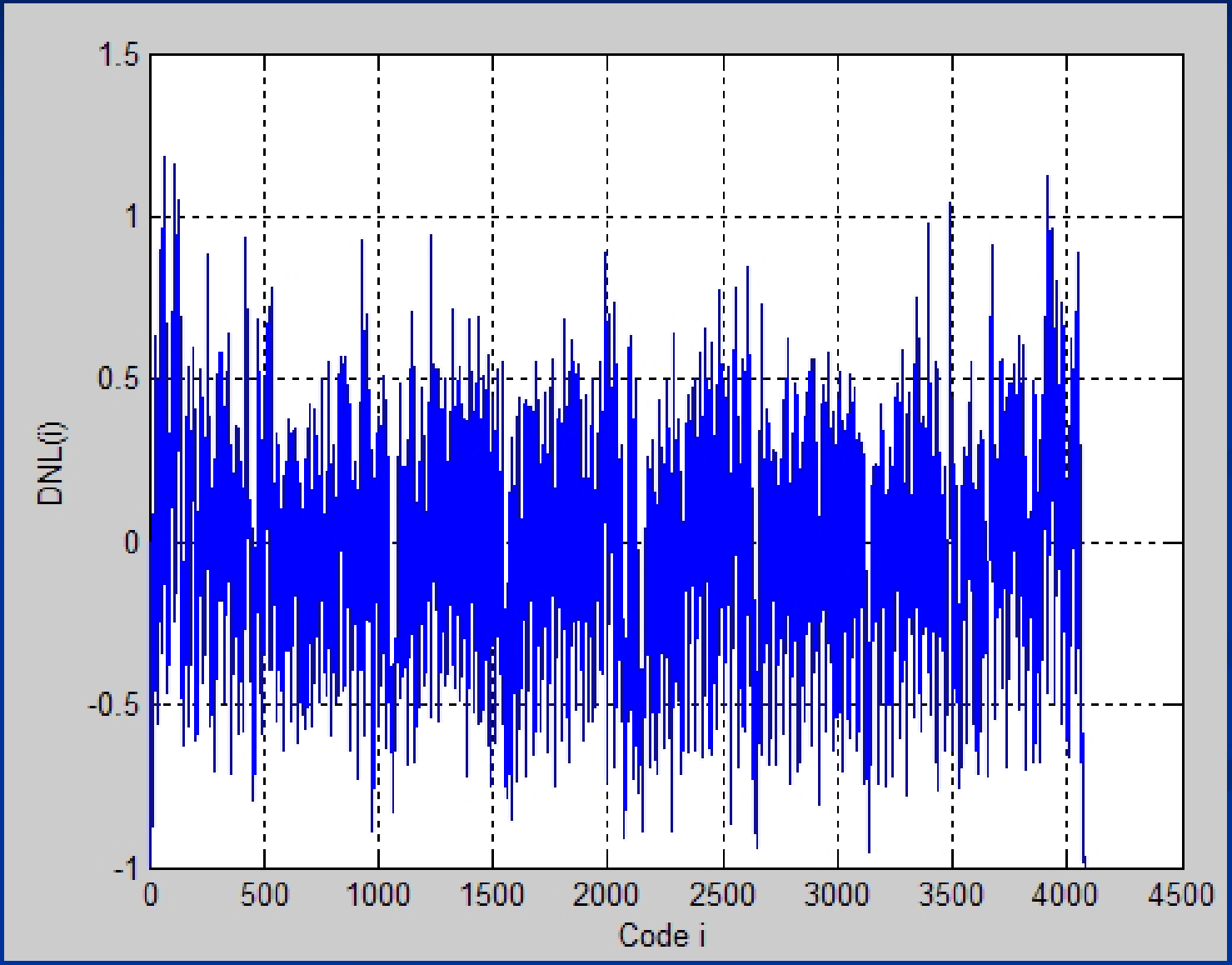
16 bits ΣΔ DAC Block diagram



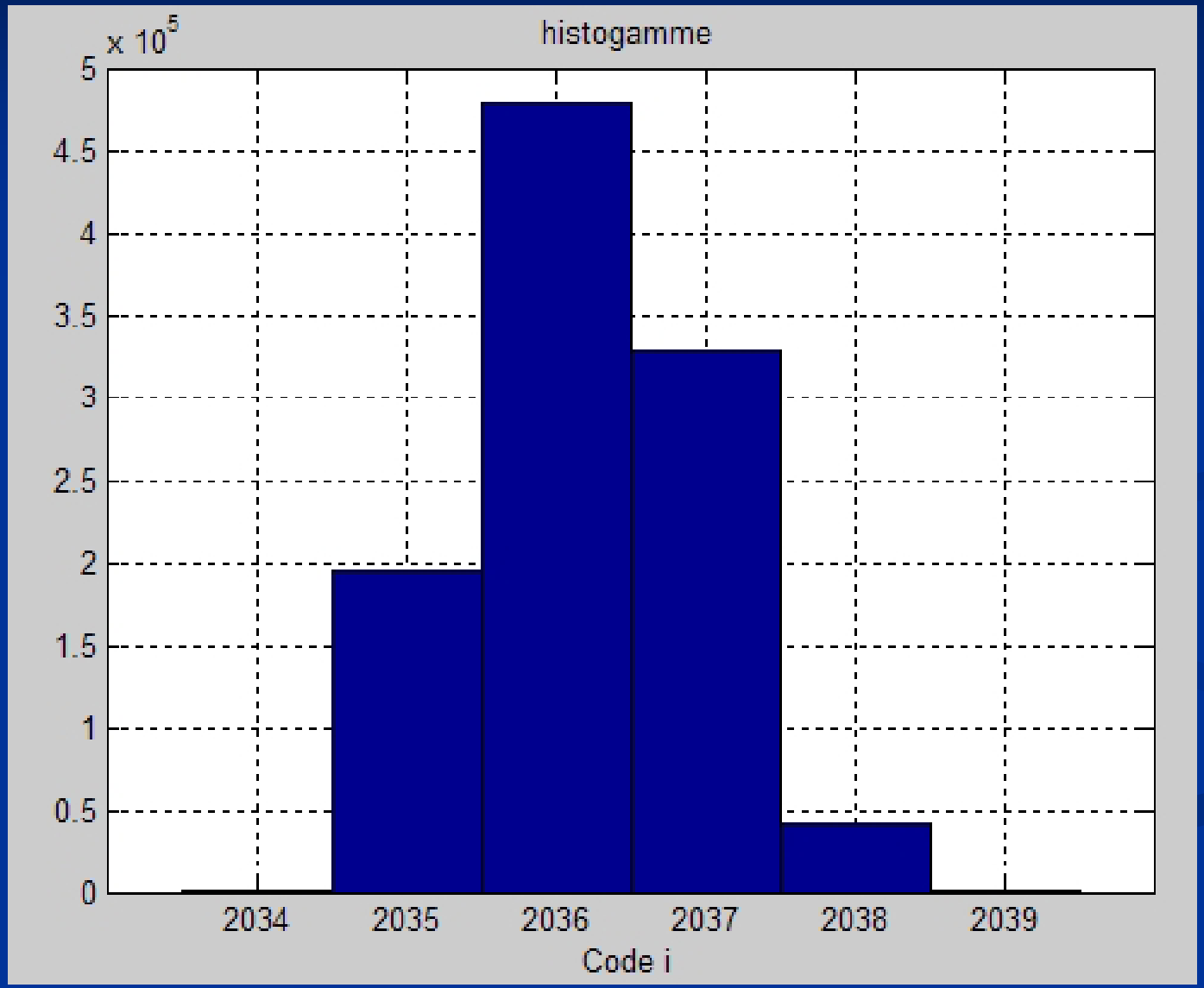
12 bits, 30 MHz ADC pipeline



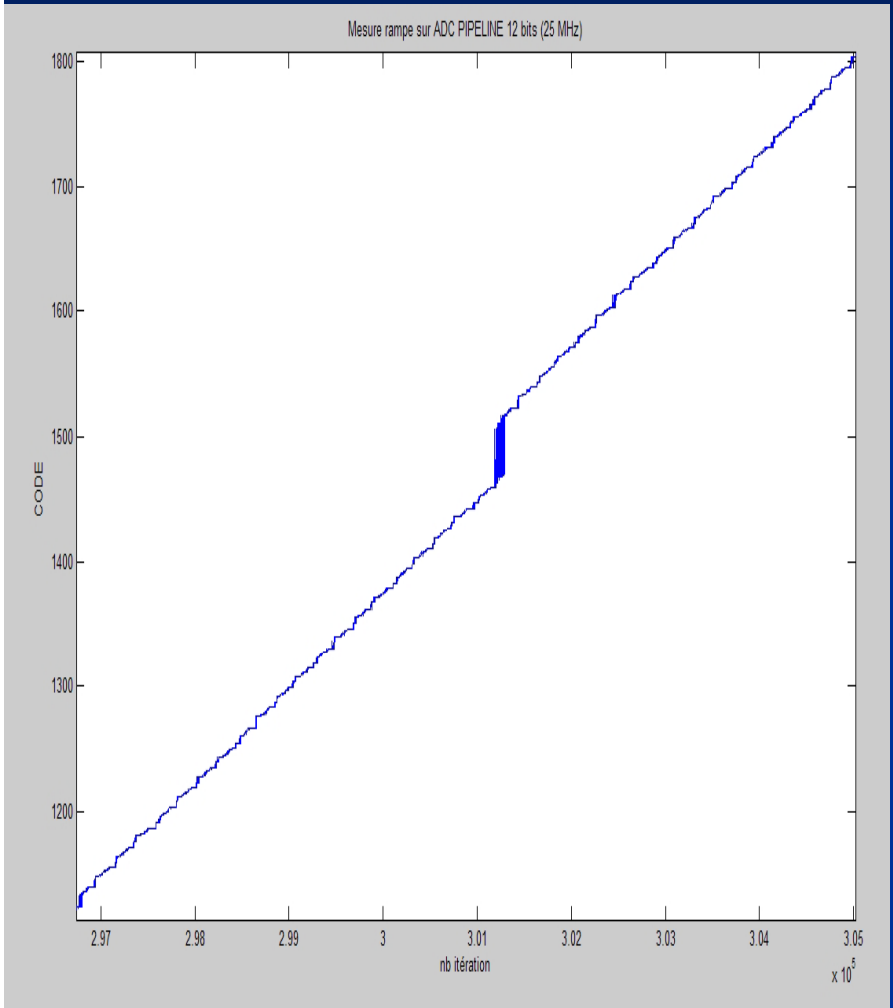
DNL testing result

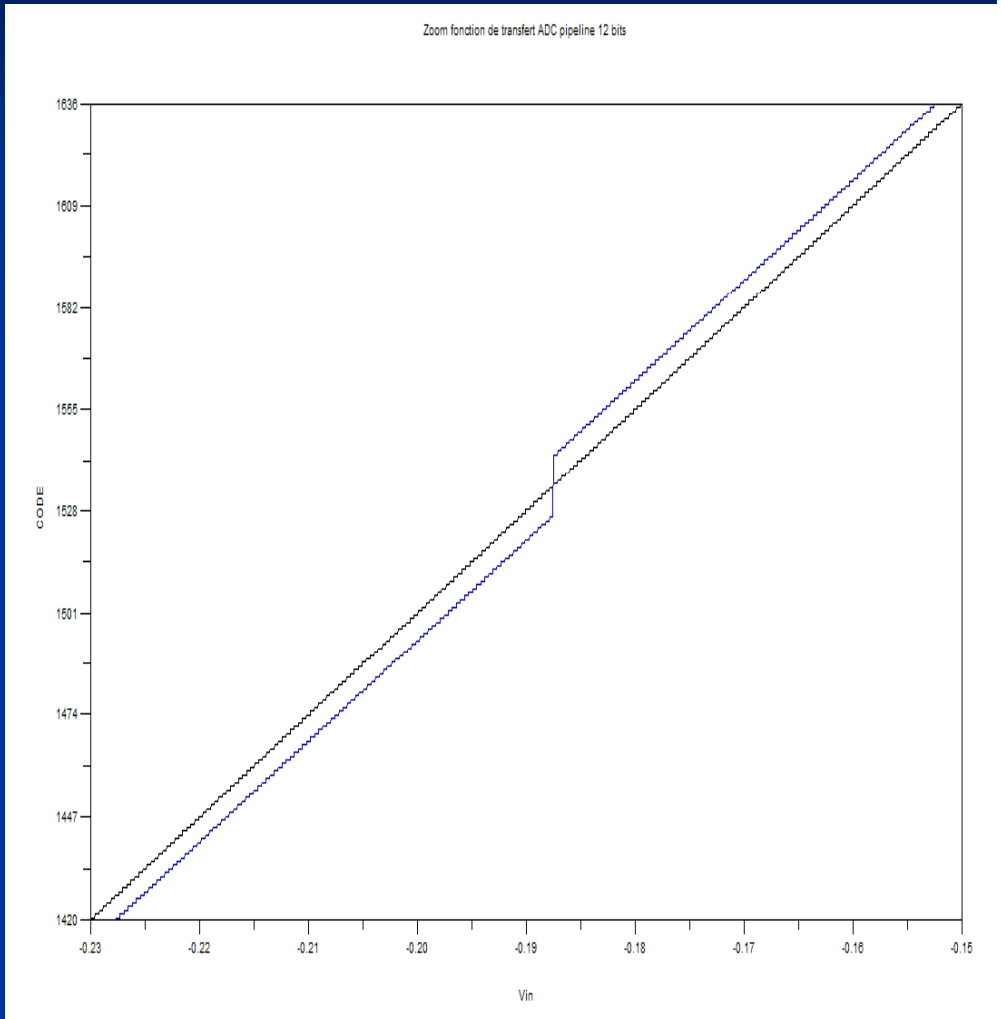


Noise : 0.8 LSB


histogamme
x 10^5
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
2034
2035
2036
2037
2038
2039
Code i

Ramp simulation and testing results





measurement

simulation

Capacitor layout : Matching problem in the first stage