US DHCAL Status

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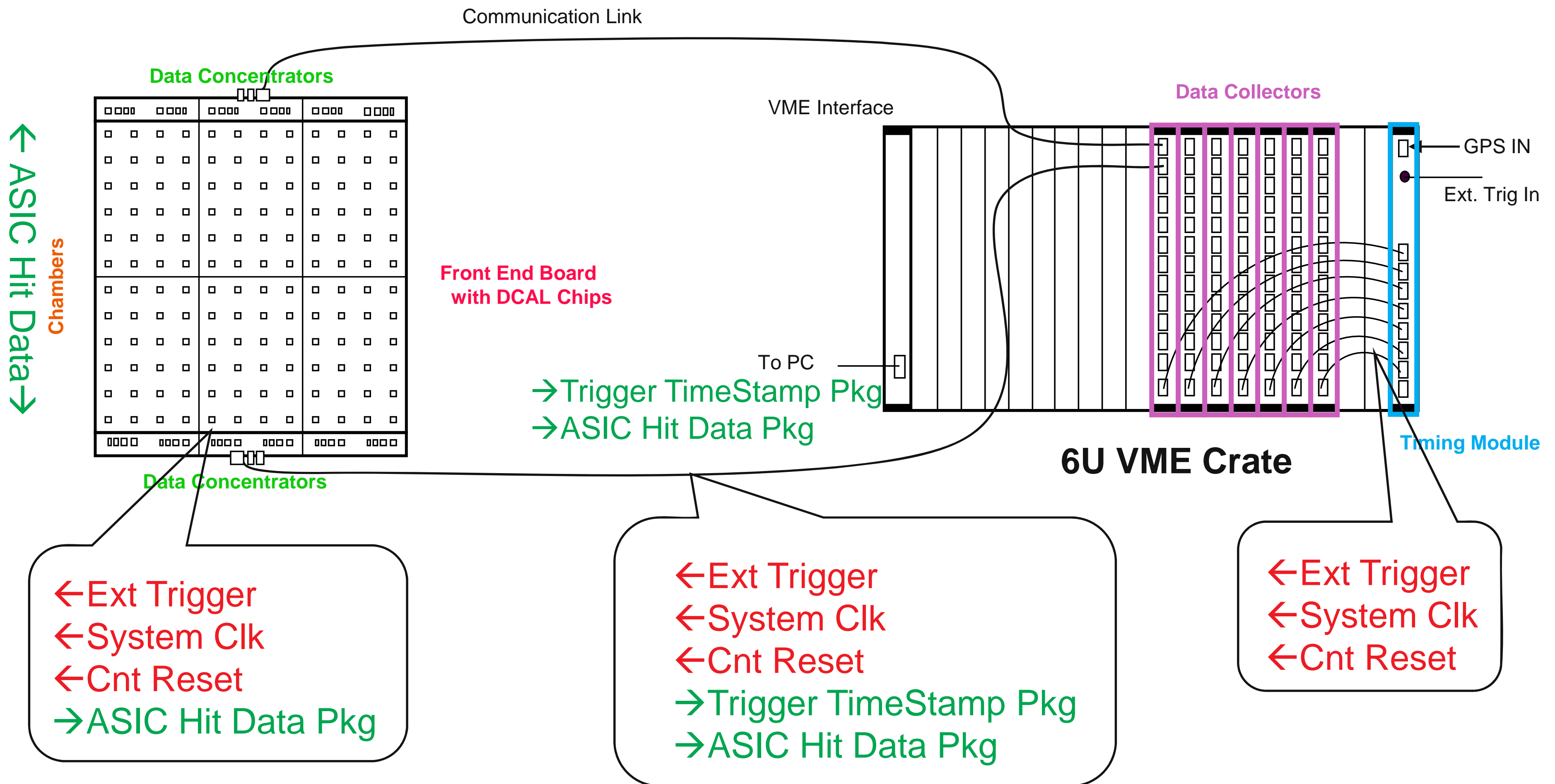
Outline

- US-DHCAL had a successful small scale beam test – Vertical Slice Test
  - A lot of data
  - Extremely valuable experience on this digital device: detector, electronics, DAQ, system integration, etc.
- Next steps:
  - 1m^3: factor of x200 bigger than VST
  - ILC HCal: factor of x50 bigger than 1m^3, x10000 the VST
- Towards a successful next step:
  - Complete data error analysis of current VST
    - *Found ~15 different modes of errors*
    - *Successfully removed ALL but 1 errors – the last one is in progress*
  - System improvement since VST
    - *ASIC*
    - *PAD + FE board*
    - *DAQ program (see Jim Schlereth's talk)*
    - *Large size RPC construction*
    - *HV and Gas distribution (new design exist, initial tests done)*

System Physical Implementation



Basic data block: 16-bite package (trigger timestamp OR hit data)

Data Error summary

- All data/system errors were thoroughly studied
- An event reconstruction program was developed to build events correctly out of data with errors
  - Used to re-run all test beam data
  - Identify events with know data errors
- Known data errors:

Fatal Errors (bit definition): original data can not be recovered
bit 0: x beginning of run (BOR) events (or junk data at the beginning of a run)
bit 1: x end of run event (due to DAQ program, last event of a run may have lost data packages)
bit 2: x additional junk byte(s) (DCON error bits 1, 2, out of bound time stamp, non-matching time stamp)
bit 3: x fake trigger (only a few DCON shows up, with or without hit pattern)
bit 4: x "0" data + leading bit error
bit 5: x check sum error + reserved bit set
bit 6: x "0" time stamp (but other bytes are non-zero)
bit 7: x wrong time stamp (in DCON or in individual chips, wrong T > correct T)
bit 8: x trigger bit error (trigger bit bit[14][7] = 1, but hit patter != all 1's) (always have check sum error as well)

Non-fatal Errors (bit definition): original data can be recovered
bit 0: - wrong time stamp (in DCON or in individual chips, wrong T must be < correct T)
bit 1: x missing (a few) DCON in trigger timestamps
bit 2: x duplicate 16-byte data package
bit 3: x late trigger package (after some data package appeared, or even appears in the next event)
bit 4: x late data package (appeared in the next event)

Other: (mostly in charge injection runs) fake counter reset

Data Error: system grounding related

- Non-optimal grounding scheme allowed noise to propagate to FE boards and Data Concentrators
  - Related to many of the errors
  - Also the reason for RPC inefficiency problems at the end of the VST
  - Caused various charge injection run issues
  - Caused mask registers to flip bits
- Related errors

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Data Error: detector noise related

- Detector noise (HV spark, etc) propagate into the FE system and mimic system signal
  - Reset timestamp counter
  - Fake trigger
  - Interrupt FE serial link
- Related errors

Fatal Errors (bit definition): original data can not be recovered
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Non-fatal Errors (bit definition): original data can be recovered
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Data Error: TTM/system clock related

- This is a recent finding, mostly affect charge injection runs
  - Found a vme-operation related clock jitter in TTM
  - Result in mis-interpretation of data bits
- Already fixed by new TTM firmware
- Related error

Other: (mostly in charge injection runs) fake counter reset

Data Error: current status

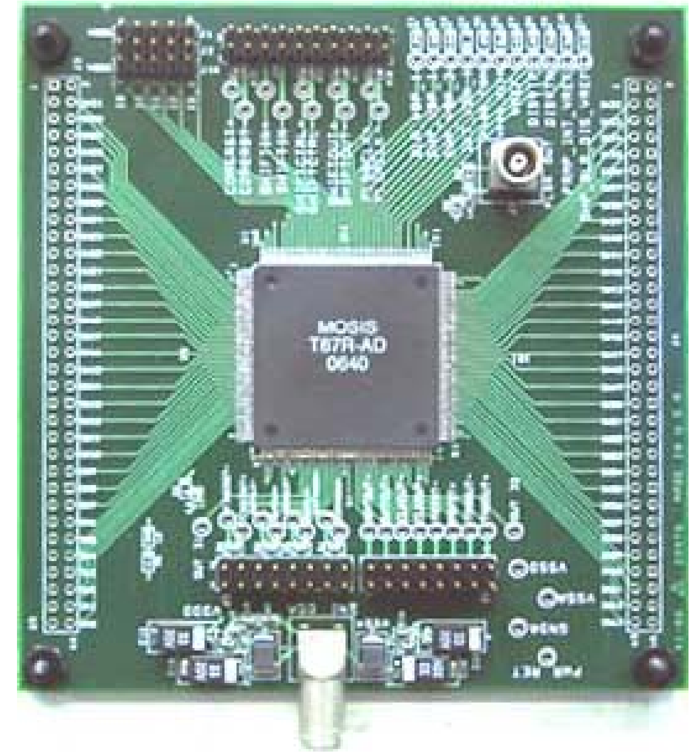
- Most errors have been successfully eliminated through system improvement
  - Improved grounding
  - Improved detector noise
  - New firmware
- Only one data error left – under study
  - Originally thought it was not harmful
  - Recent tests shows that system drop data packages (trigger timestamp AND hit data) at ~0.5% level
  - Extensive tests started recently
  - Expect to solve the problem in the near future – then we will have a PERFECT VST readout system

With a fully debugged VST readout, we are confident in building 1m^3

R&D towards a 1m^3 (since VST)

Last DCAL modifications before production

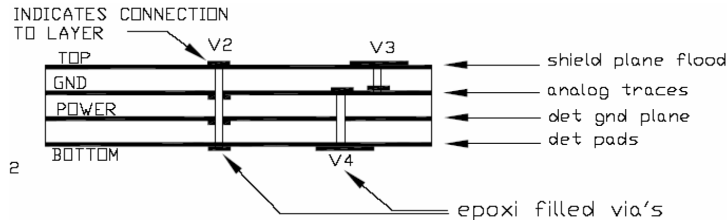
- 50% data lost when output buffer is empty
  - Not a problem in triggered running
  - Simple bug in ASIC logic: identified, corrected and simulated
- Noise introduced by internal test lines
  - OK for RPC, fixed for ASICs on GEM board
  - Simple fix in chip packaging
- Problem with mask register and CI-mask register
  - Original design use asynchronous clear -- more sensitive to noise
  - Improved detector to reduce noise
  - Modify ASIC: needs some design time (~1 week)
- Problem with slow control readout
  - A bug in the ASIC prevents daisy chaining slow control readout – addressed in FE board design
  - Trivial change already implemented

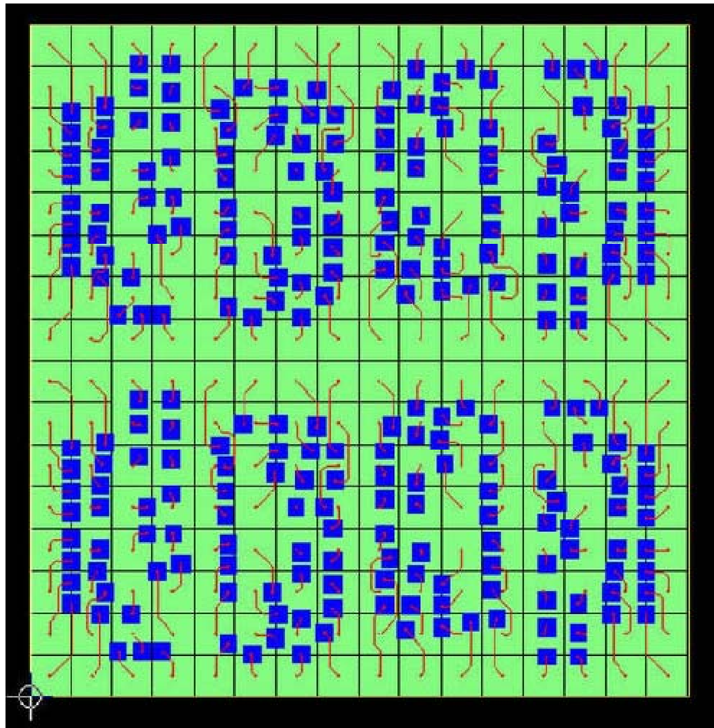


No more prototype run needed before chip production

Current Pad Board & Front End Board Design

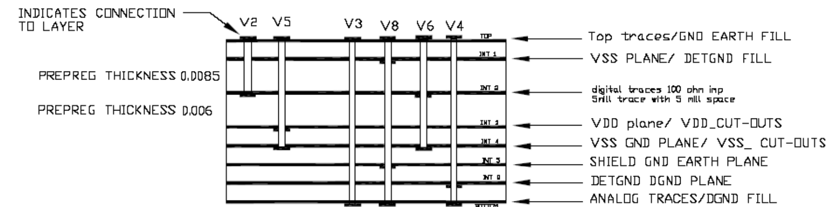
4-layer Pad-board (3 shown)

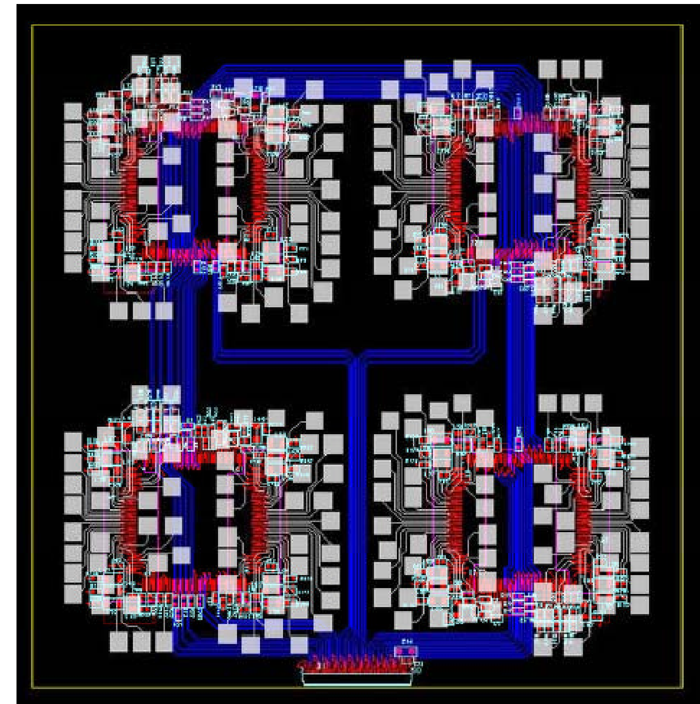




Blind vias to route sensitive signals to glue pads – needed to minimize contact with digital lines in FEB

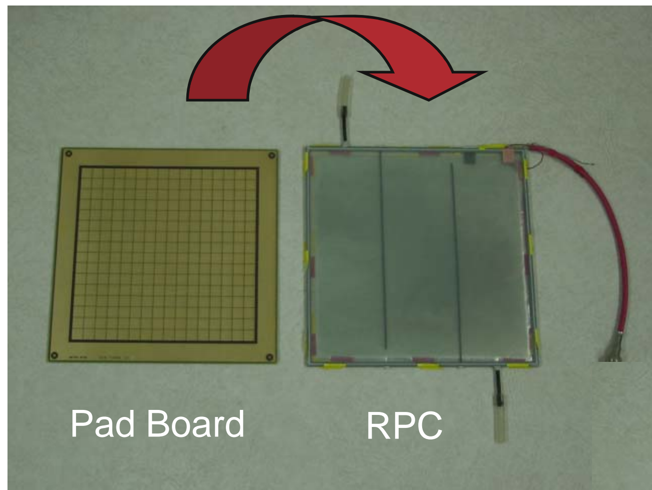
8-layer FE-board (3 layers shown)

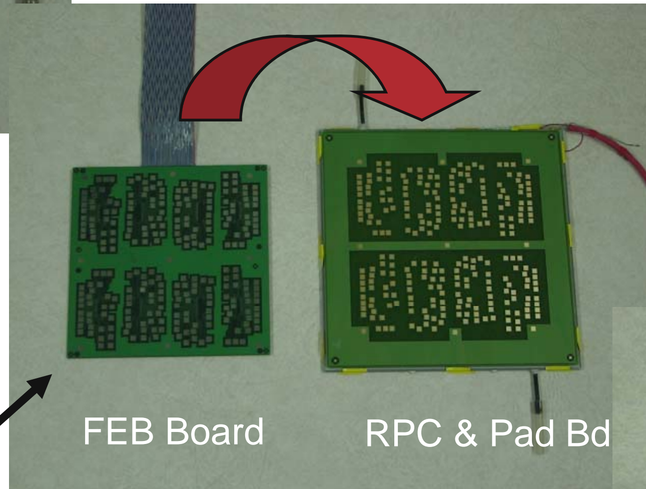


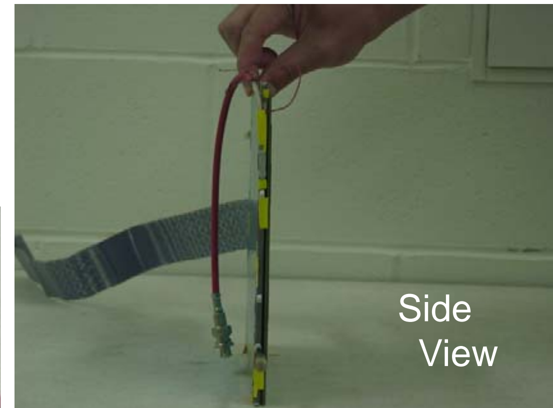


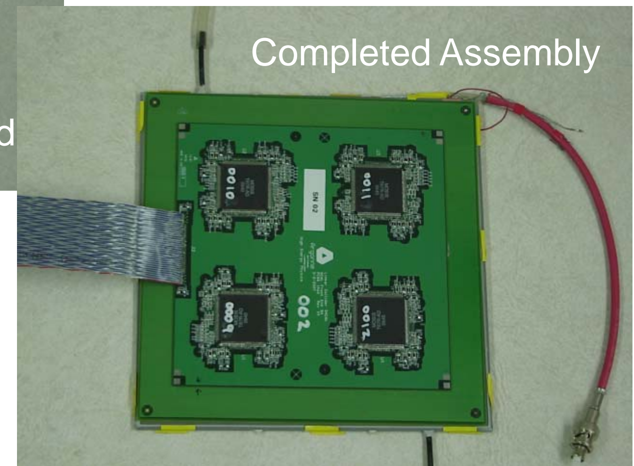
Also has blind vias
→ Very complex board design to minimize crosstalk & digital noise pickup

Vertical Slice Electronics Construction









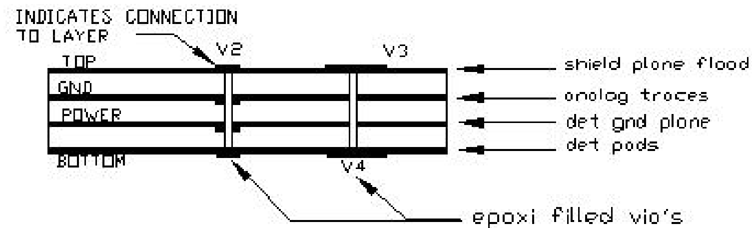
Assembled & Tested Beforehand
Use conductive epoxy to glue together

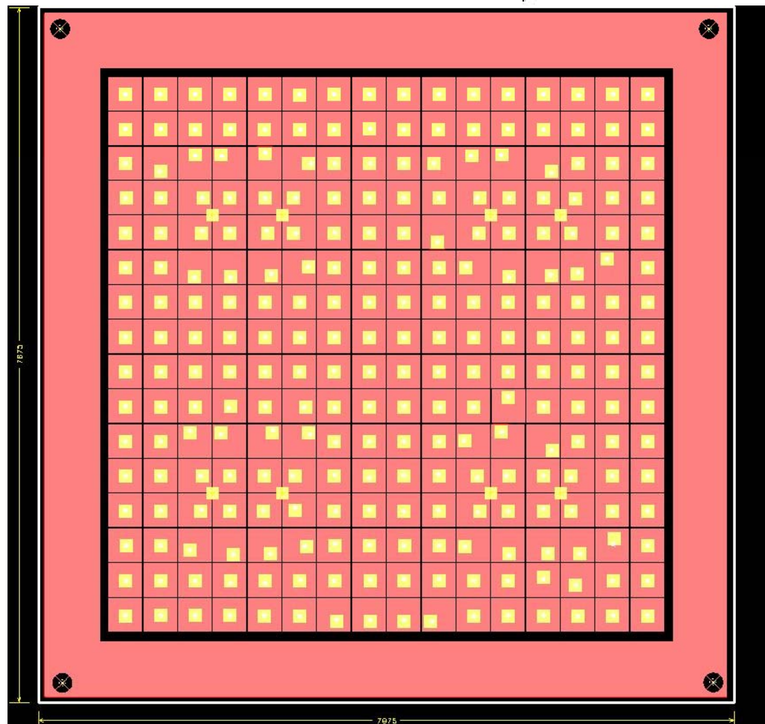
Front End Board - Work in Progress

- Current design has extremely good noise performance
  - Noise floor: only 10 – 15 ADC count (low gain)
  - System comfortably runs @ 30 ADC count or even lower (normal runs @110 ADC count)
  - Left a lot of head room for cost reduction
- Have designed new 16 cm x 16 cm FEB with ***NO*** blind vias
  - Still 8 layer
  - Still has ground shielding layers to protect charge signals
  - Primary change: now ALL vias come down to glue pad layer (bottom)
- Have designed ***Two*** new 16 cm x 16 cm Pad Boards also with ***NO*** blind vias
  - One is 2 layer, with no internal ground plane
  - One is 4 layer with 2 internal ground layers

New Pad Board & Front End Board Design

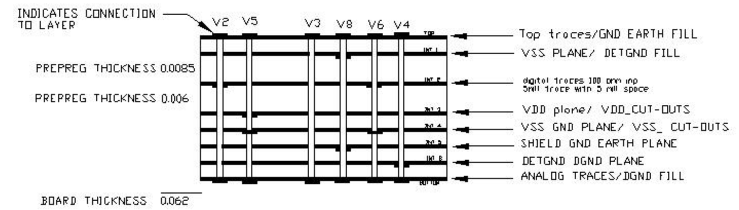
4-layer Pad-board (3 shown)

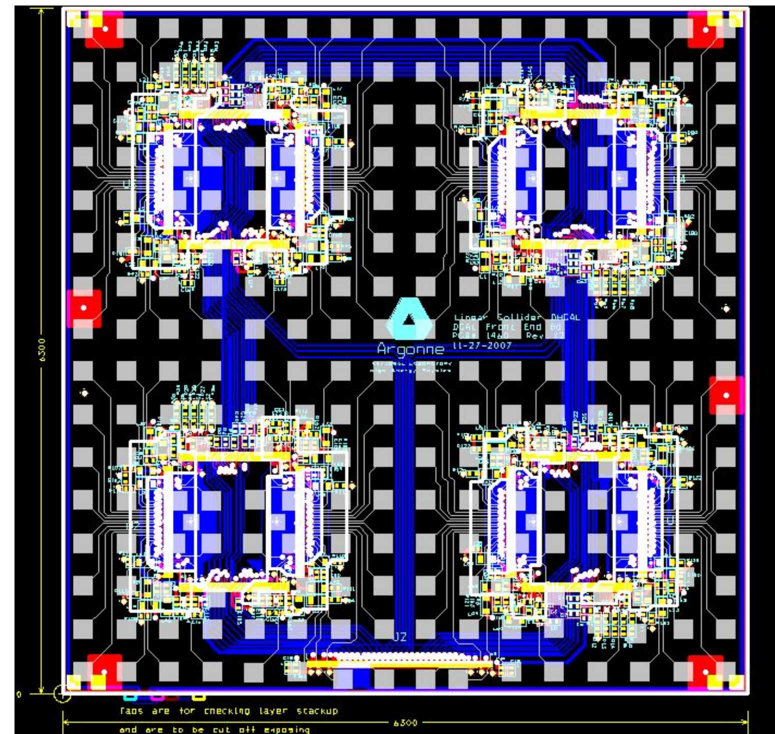




No blind vias

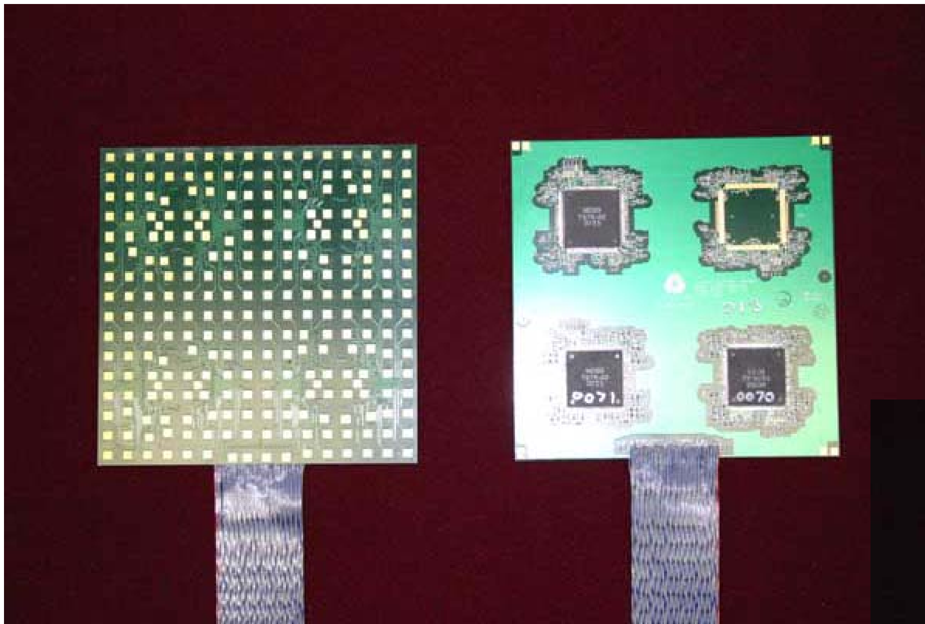
8-layer FE-board (3 layers shown)

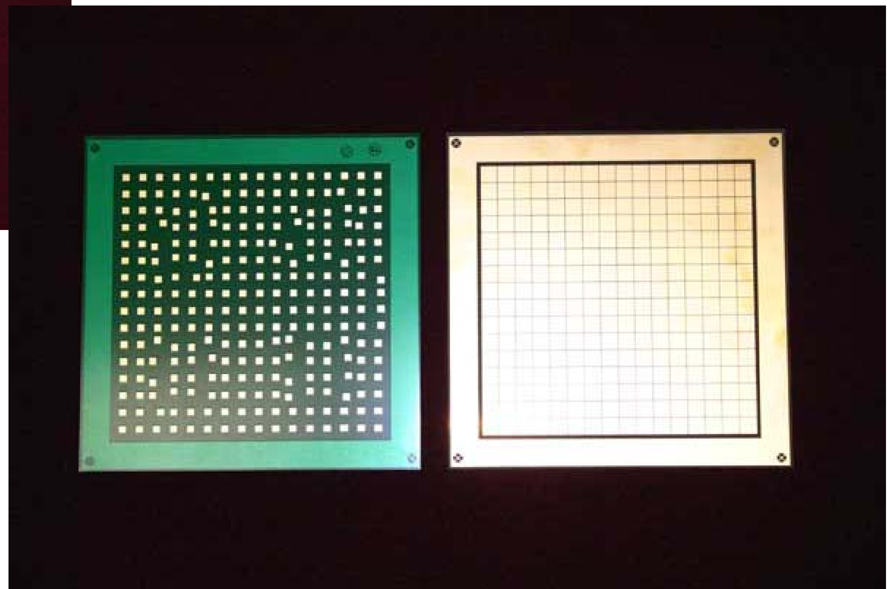




No blind vias

New Pad Board & Front End Board

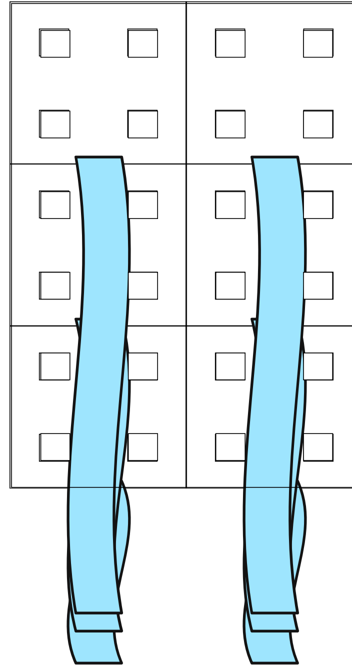




Boards are manufactured, being stuffed and tested

FEB – Current Thinking

- If the new design is successful, we can make larger boards:

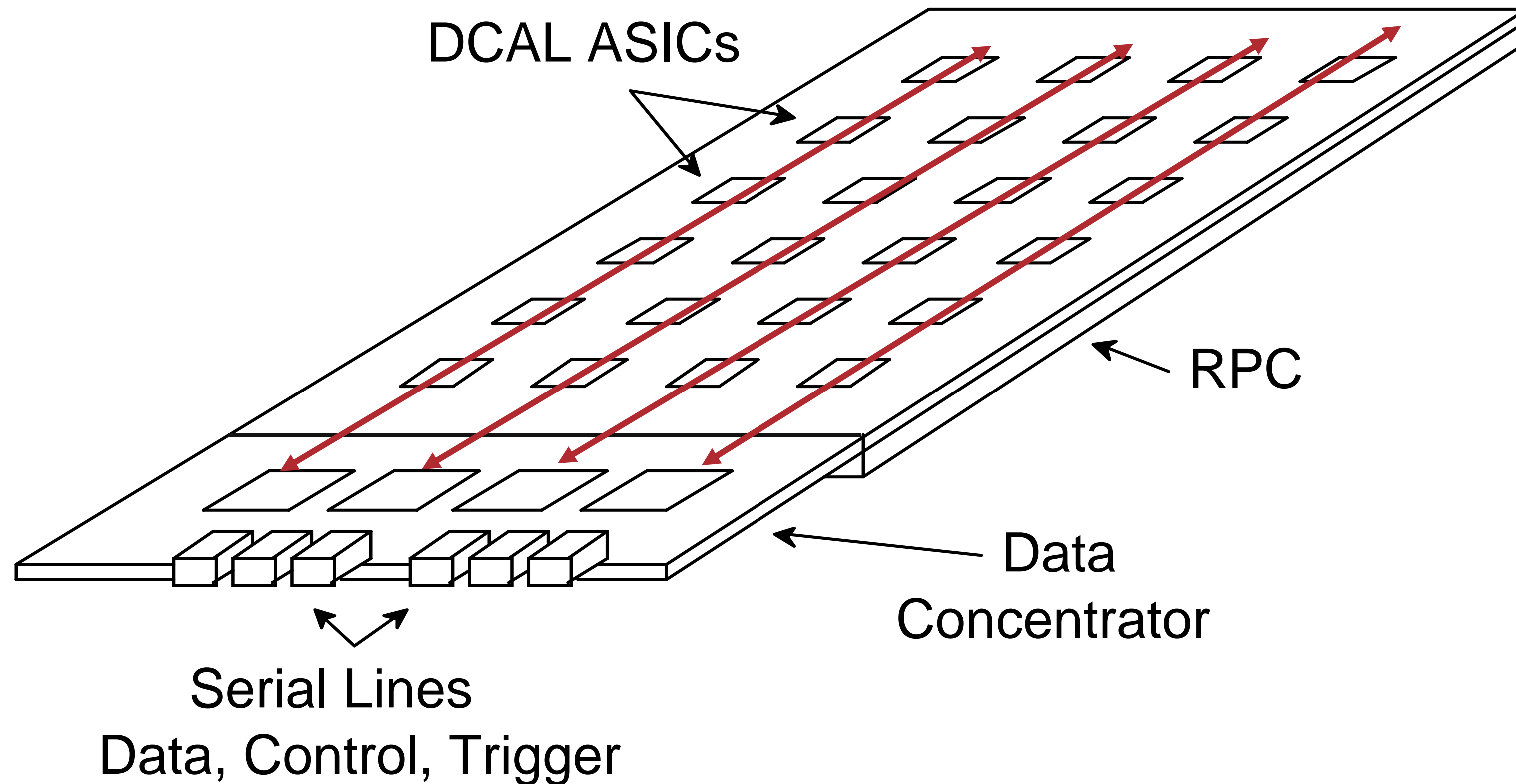


⇨ ***Could not make larger boards before with blind vias – Too Difficult***

⇨ ***Larger boards are cheaper, eliminates cables & connectors, reduces impedance mismatches, improves reliability, etc.***

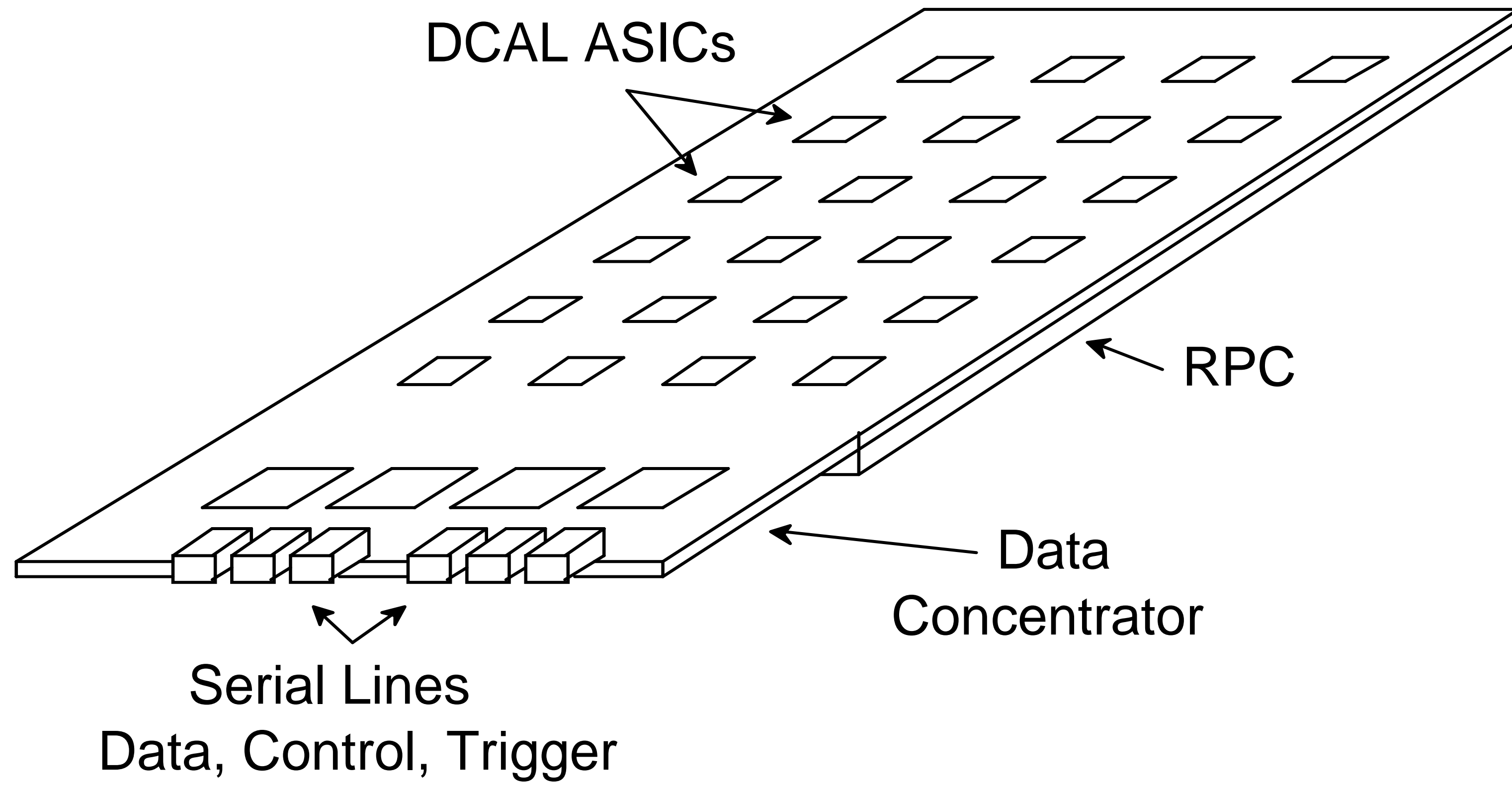
FEB & Data Concentrator – Work in Progress

- New Data Concentrators – One services 24 chips
  - Idea: Column Architecture



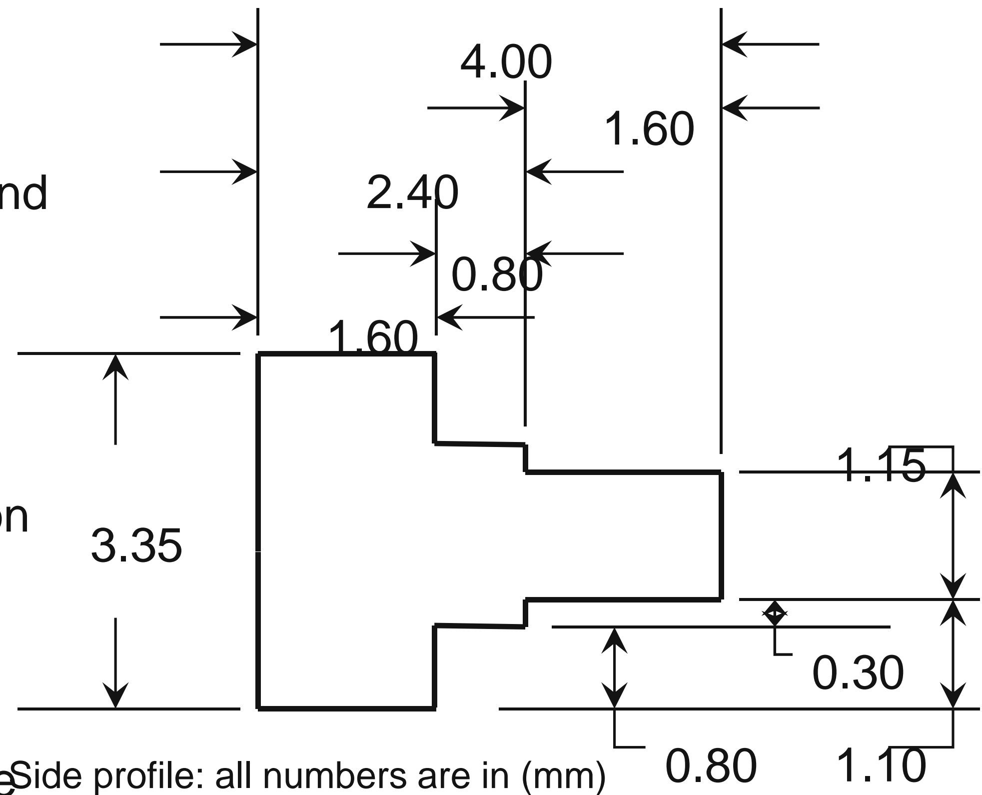
FEB & Data Concentrator – More Current Thinking

- Going a step further: Make FEB & Data Concentrator Monolithic...



Current RPC design and construction

- VST started using the current design
  - Chambers have flush surface
  - Frames are easier to machine, and can be extruded
  - Simplified chamber construction
- Assembly procedure developed and used for all VST chambers
  - Suitable for large scale production
  - Produced 12 RPCs for VST
  - All RPCs are gas tight from the very beginning
  - All RPCs have good performance and chamber to chamber variation is small



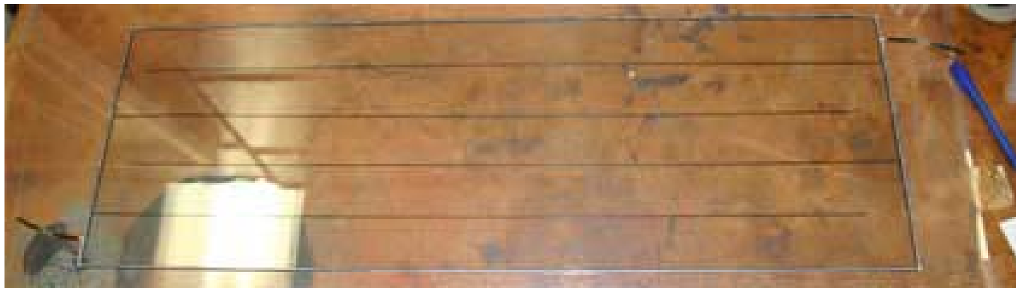
Side profile: all numbers are in (mm)

Large RPC production: frame extrusion

- VST chamber frames are all machined
  - Very time consuming and labor intensive (costly)
  - Critical dimension can be controlled to ~ 10% accuracy
- 1m^3 chamber frames will be extruded
  - Once setup, production is very cheap
  - Very good uniformity over long distance
  - Only need small amount of machining to cut into length/shape
- 1st prototype run: ~3 weeks ago
  - Critical dimension controlled to ~5% accuracy over several meters
  - One non-critical dimension was off by over 10%
  - Sample used to produce the 1st full size RPC for 1m^3
- 2nd prototype run: last week
  - All dimensions agree with spec
  - Will go for production (miles of them)

Large RPC production: 1st RPC (almost) done

- 1st full size RPC constructed for $1m^3$
  - Used 1.2mm glass, 96cm x 32cm (VST: 1.1mm glass, 20cm x 20cm)
- Slightly modified assembly procedure works for large chamber
  - Chamber is gas tight (~ 5 meters long glue trace!)
  - Chamber is relatively stiff, deformation doesn't affect gas tightness
  - Good for large scale production
- Chamber dead area: 4.7%
  - Frame: 3.3% (irreducible, unless go for larger chamber)
  - Fishing line: 1.4% (can be reduced, if use other spacer)



Summary

- Vertical Slice Test was extremely successful
- All problems in VST and cosmic ray runs were thoroughly studied
- The whole readout system is (almost) completely debugged
- Final R&D towards $1m^3$ is progressing smoothly
  - ASIC production: need trivial modification, no more prototyping
  - New FE and PAD board prototyped, and are being tested
  - RPC frame extrusion has been setup, ready for production
  - 1 full size RPC assembled
- The DCAL chip production is now defining the timeline of $1m^3$
- Extrapolation from VST to $1m^3$ (x200 VST) will be a successful one