Status of EUDET Prototype
An Attempt to give/get an Overview

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LAL Orsay

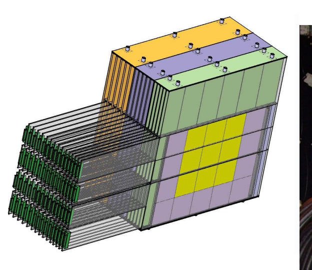
- Status of Mechanical Construction
- Status of Wafer Production and Electronics Development
- Interplay between different components (interleaved)
- Plans for 2008

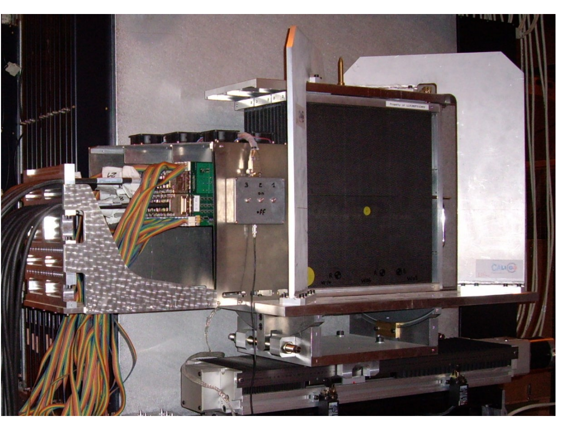
Material for this presentation courtesy of:

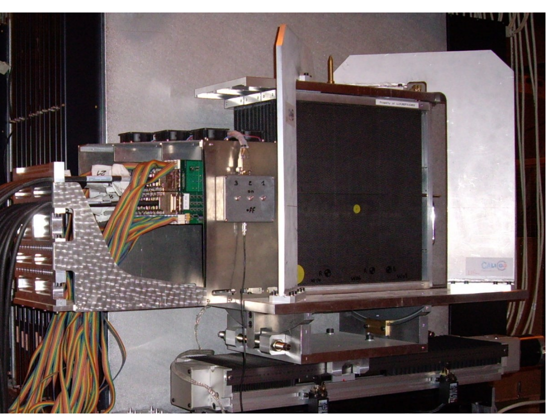
Marc Anduze, Denis Grodin, Ray Thomson, Julien Fleury
Maurice Goodrick, Laurent Royer

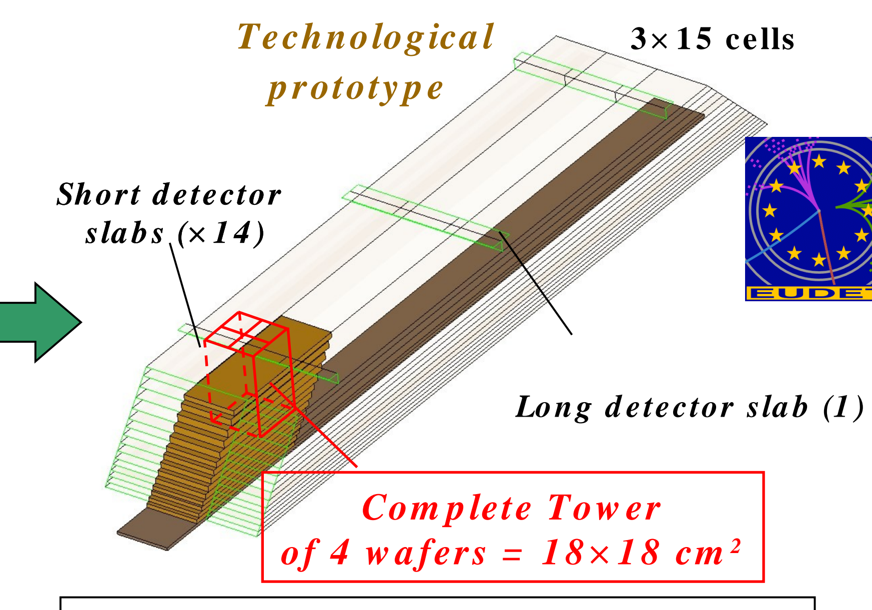
EUDET Prototype

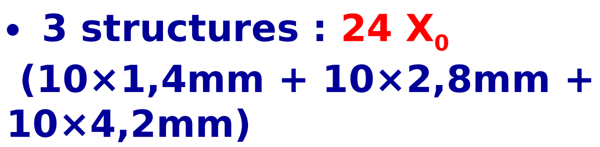
- Logical continuation to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of technological solutions wich could be used for the final detector (moulding process, cooling system, wide size structures,…)
- Taking into account industrialization aspect of process
- First cost estimation of one module









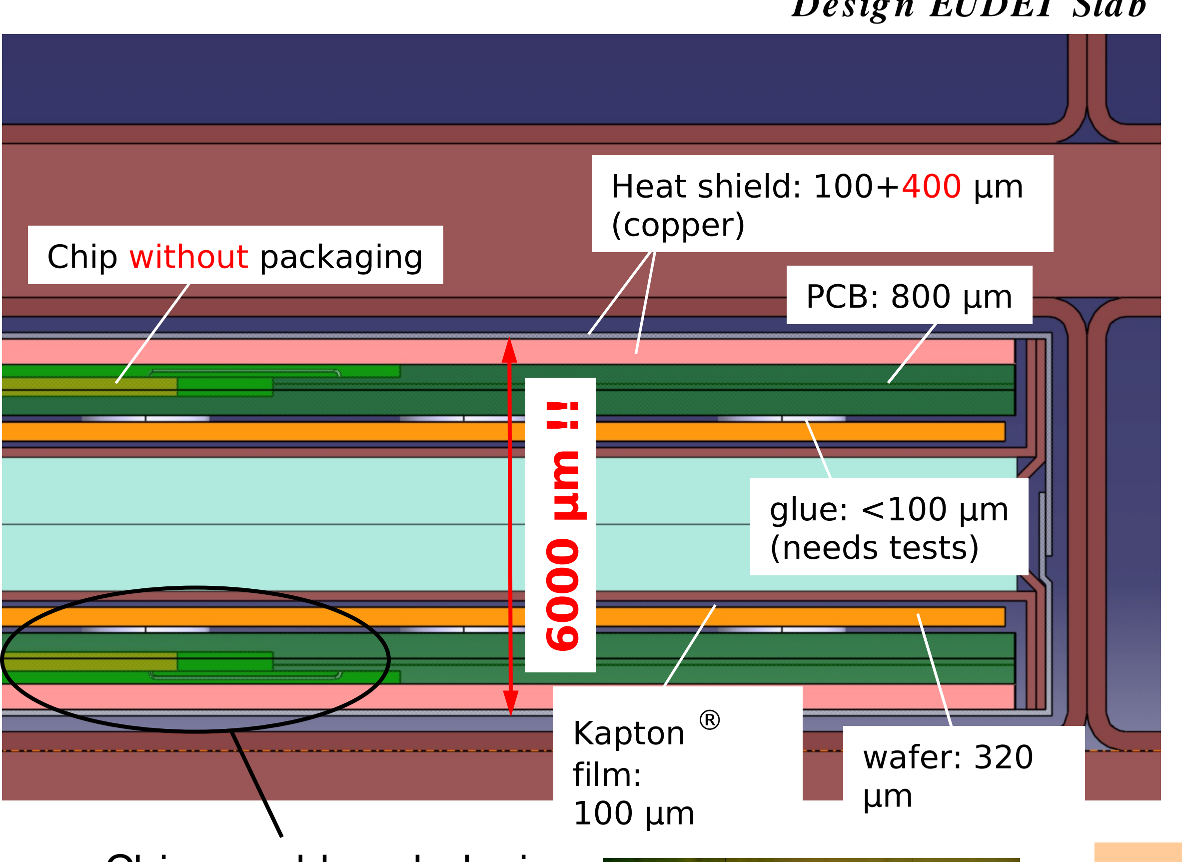


- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

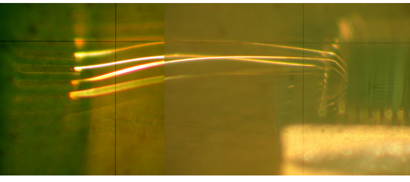
Design of Slab – Cross Section

The expected alveolar thickness is 6.5 mm **if** :



- ⇨ Gaps (slab integration) : 500 μm ?
- ⇨ Heat shield : 400 μm ?
  but real thermal dissipation ?
  (active cooling ?)
- ⇨ PCB : 800 μm (tolerances : ± ?)
  but chips embedded in PCB ?
- ⇨ Thickness of glue : < 100 μm ?
  study of the size of dots
- ⇨ Thickness of wafer : 320 μm – (± ?)
  30 matrix ordered (90×90 mm²)
- ⇨ Kapton® film HV feeding :
  100 μm - OK *(DC coupling)*
- ⇨ Thickness of W : 2100 μm (± 80 μm)

Chips and bonded wires inside the PCB



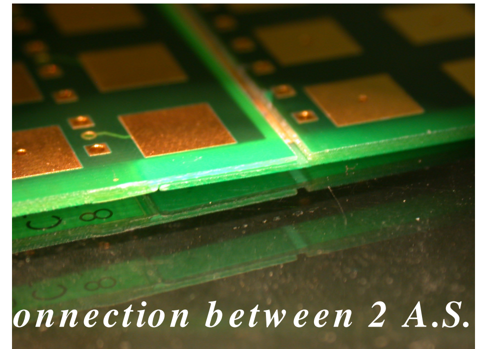
Several technological issues have to be studied and validated

Detector Slab Principle

Long slab is made by several short PCBs :

A.S.U. : Active Sensors Unit

- Design of one interconnection « **inside** » PCB
- Easier development : study, integration and tests of A.S.U in parallel with other components of the project
- The length of each long slab will be obtained from the size of one "final PCB"



3330 ± 20 4900 900 450 3330 ± 20 4900 89600 89960 ± 40 89960 ± 40 Back Side: Common Anode(All metalization) 780 ± 20 1230± 20 Guard Ring PIXEL Size (4000 x 4000) PIXEL Signal PAD 89600

wafer

180.5 180.5

Interconnection zone

ECAL SLAB Interconnect

DAQ Architecture – Overall view

~150 VFE ASICs on each side of SLAB

ODR

LDA

LDA

LDA

LDA

DIF

DIF

DIF

DIF

DIF

DIF

SLAB

SLAB

SLAB

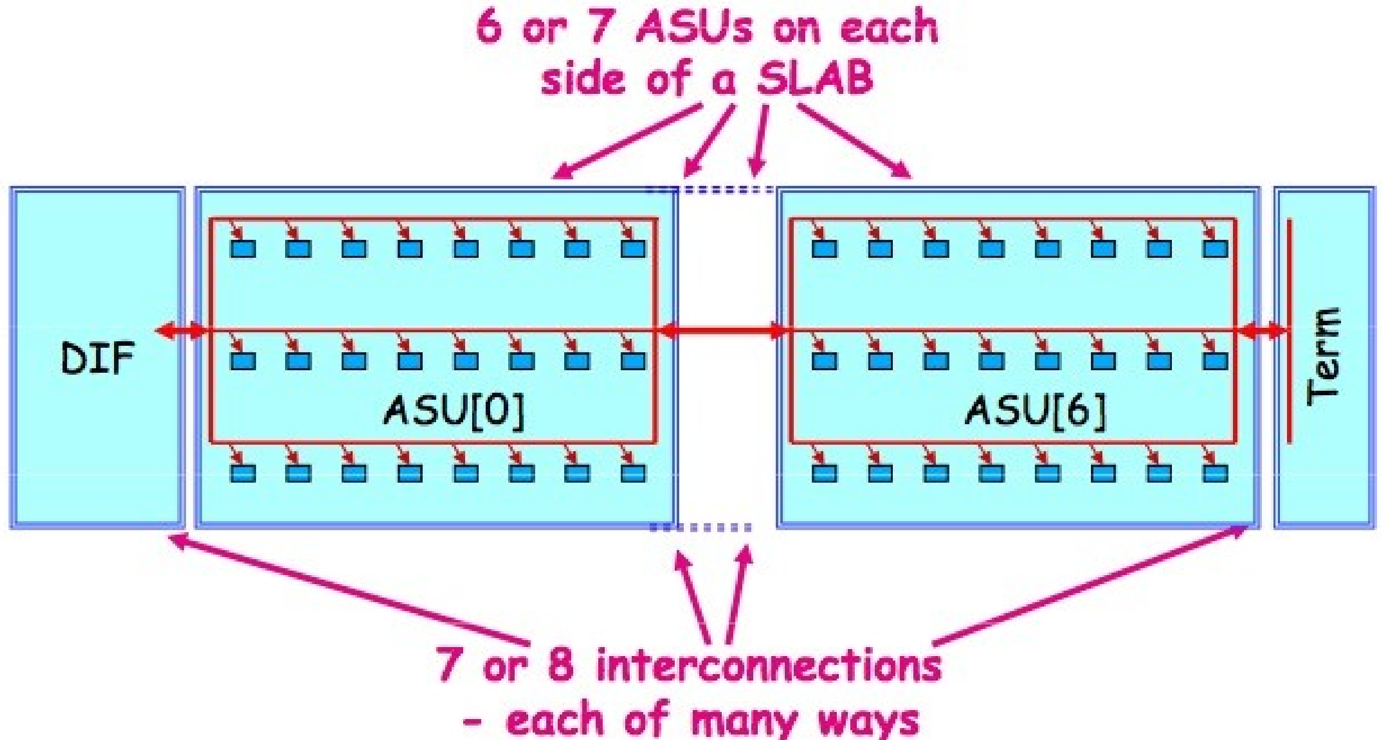
SLAB

SLAB

SLAB

Maurice Goodrick & Bart Hommels , University of Cambridge

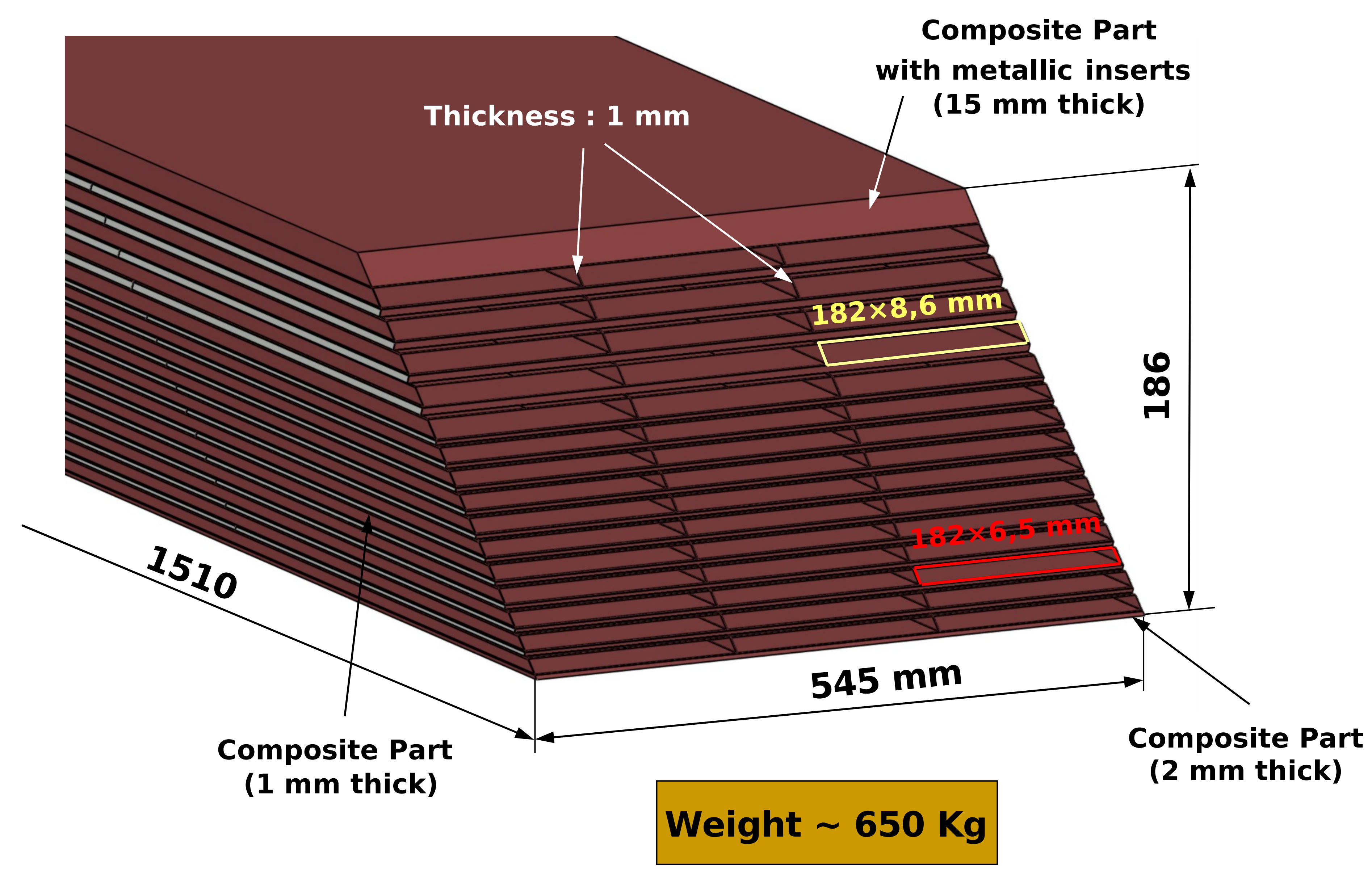
ECAL SLAB Interconnect



Options for Interconnection of ASU:
- glued joint step
- (glued) direct stitching
- FFC (Flat Flexible Cable)

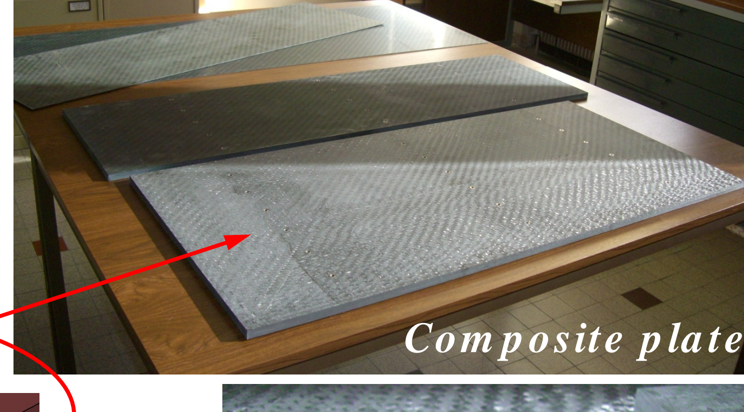
Read out Mode (Single line, multiple lines?)

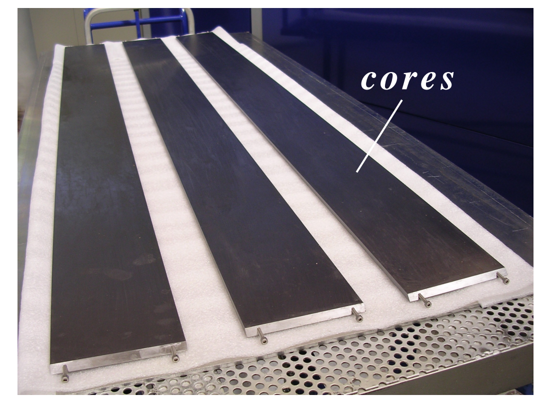
Alveolar Structure 1/2

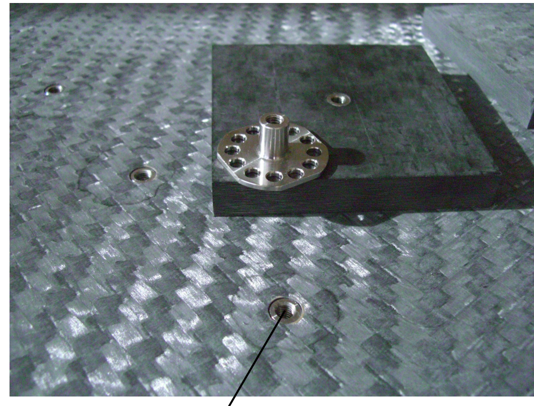


Alveolar Structure 1/2

Assembled structure : Each alveolar layer are done independently, cut to the right length (with 45°) and assembled alternatively with W plates in a second curing step
(2 width of cells : 126 mm and 182 mm)





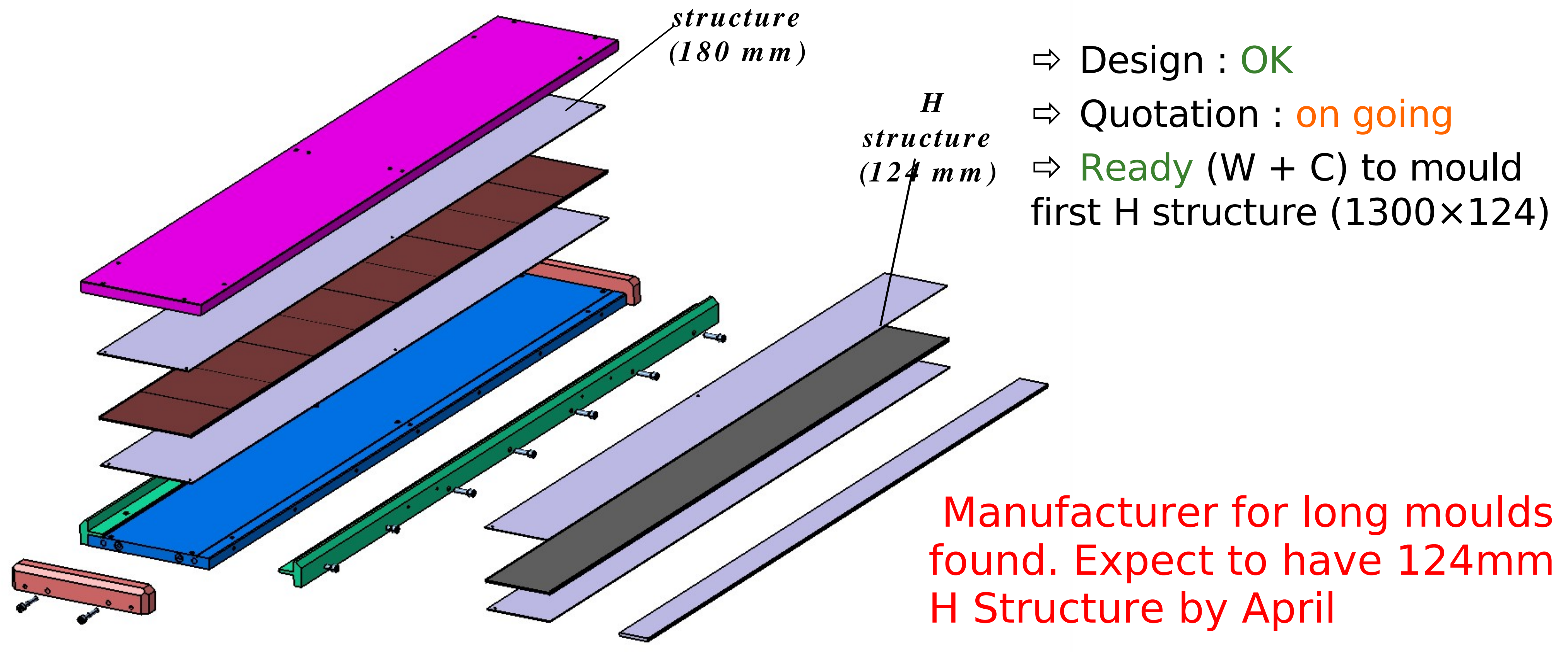


- ⇨ Global design : OK
- ⇨ "Alveolar layer" mould machining : on going
- ⇨ Design of assembly mould : on going
- ⇨ Ready : 4 composite plates (15mm and 2 mm)

Composite H Structure

Study and manufacturing of one mould for whole structures (feb 2008):

- Same principle than the mould used to do H physical prototype structures (autoclave)
- One long mould for both long and short H structures and 2 width (124 and 180 mm)



⇨ Design : OK

⇨ Quotation : on going

⇨ Ready (W + C) to mould first H structure (1300×124)

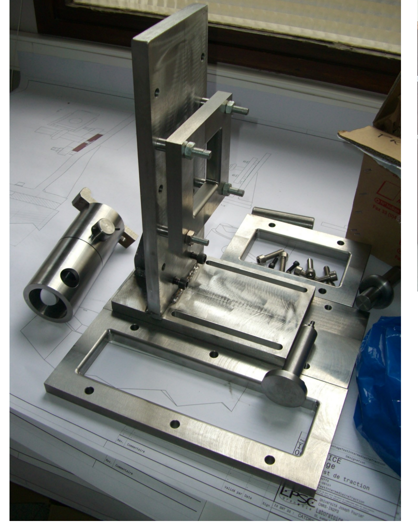
Manufacturer for long moulds found. Expect to have 124mm H Structure by April

Important Milestone:
Manufacturing of Demonstrator holding (faked) PCB and Wafer units allowing for mechanical tests and thermal measurements until summer vacations

Destructive Tests

Mechanical tests of interface (feb 2008):

- Destructive tests of fastening elements:
  until breaking of interface in order to evaluate constraints and elongations under different loading cases:
  - Tensile / Compression
  - Cutting / Bending
- Study and fabrication of testing tools: OK
- Check and validate simulation results by destructive tests for each issues
- Similar type of tests to be performed for characterization and calculation of inter- alveoli thin sheets of composite



tools for tensile and compression tests

Machine for destructive tests

Test pieces (interface)

Destructive Tests and Beyond – Latest News -

Modules: *studies*

- *Finite Element Model of modules to estimate the overall deflection, with new cells 180x8.6 (common to CALICE end-cap studies).*
- *Optimization of composite sheets : studies of main parameters for thick plates*
- *Fasteners design (rails, facilitated insertion of modules) and inserts drawings :* OK
- *Cooling system and technology: Thermal study - design and test of heat pipes*

Modules: *Tests*

- Metrology and Machining tests of tungsten plates. OK
- Moulding of the composite parts 15mmm & 2mm thick with metal inserts: OK
- Destructive tests on composite samples with inserts: OK
- Destructive tests on the mechanical interface ECAL/HCAL : OK
- Prototype of the cooling system's connection kit for slabs : *summer 2008…*

- Fastening system ECAL/HCA: rails: march 2008
- Destructive tests on the mechanical interface ECAL/HCAL : april 2008

Confirmations are to be given for thermal studies: FPGA consumption and position…

Other studies & tests on going on Composite Structures & Services for **CALICE (End-Caps)**

Thermal Analysis of Slab

Simulation of heat conduction just by the heat copper shield :

Influence of the FPGA dissipation (DIF) on current design of cooling system (Limit Condition of 20°C) :

LC of 20°C in the center of slab : ΔT = 7,95°C

Φ = **0,27 W/layer**
(25 µW per channel)
Φ_{FPGA} = **3 W/layer**

Copper layer : λ = 400 W/m/K
S = 180*0,4 mm2 ; L =

LC of 20°C in the center of slab : ΔT = 12.3°C

Network of contact areas / connector fixed on the 2 layers

Cooling pipe

1 layer copper

DIF

25x15x6.2mm

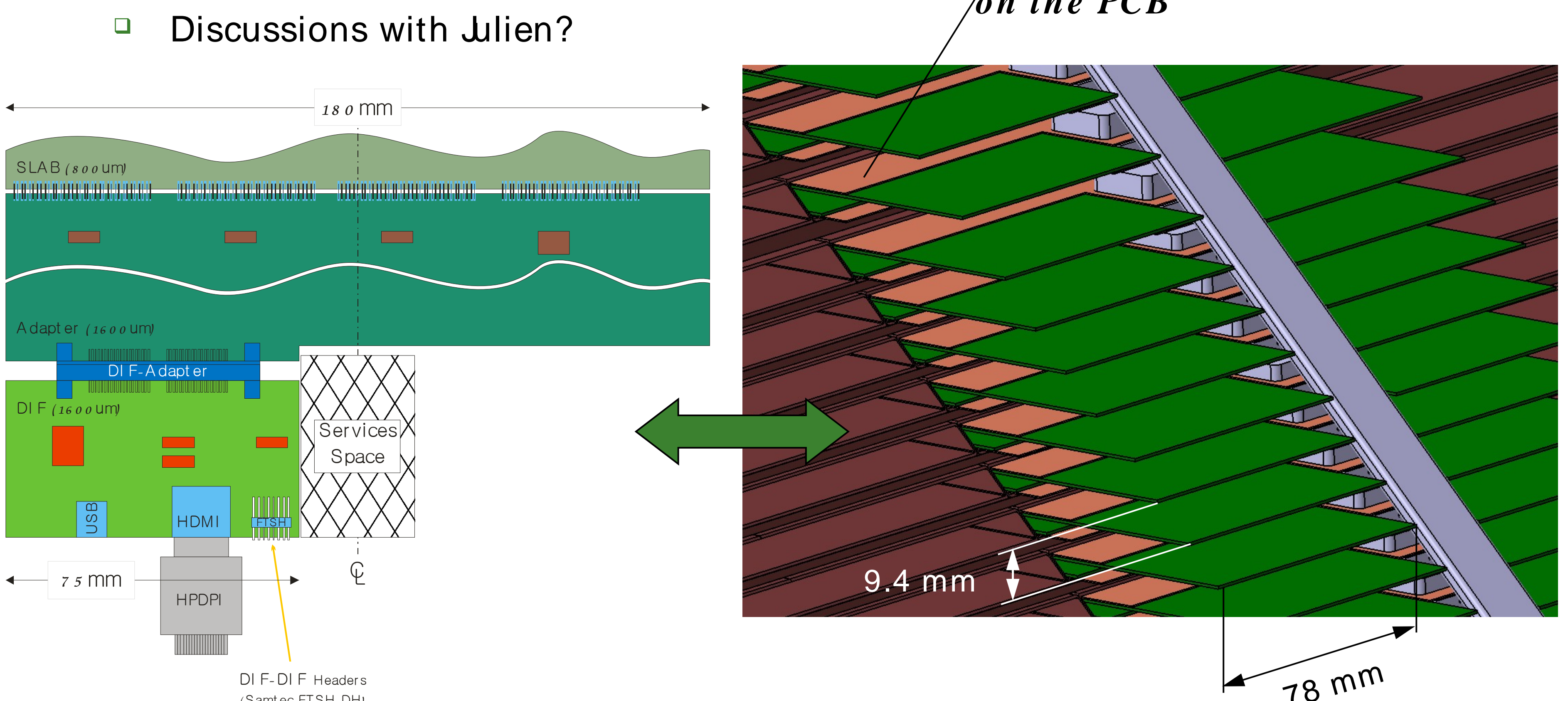
FPGA

ΔT and **size** of cooling pipe increase (ΦT = 8.1 W (SKIROC) to 98.1 W) (SKIROC + DIF)

Interface SLAB <-> DIF

Current Module design compatible with this proposal from Cambridge?

- Adapter board (size, thickness ...)
- Components size
- Connectors size
- Fastening devices / back-end system
- Discussions with Julien?



(from Maurice Goodrick, Bart Hommels)

One of the biggest unknowns in the game!!!

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

Assembling of A.S.U. (industrialization, gluing and tests) + backend system (DIF support) + services

Tests of wafers

Global Design + composite Structures

+

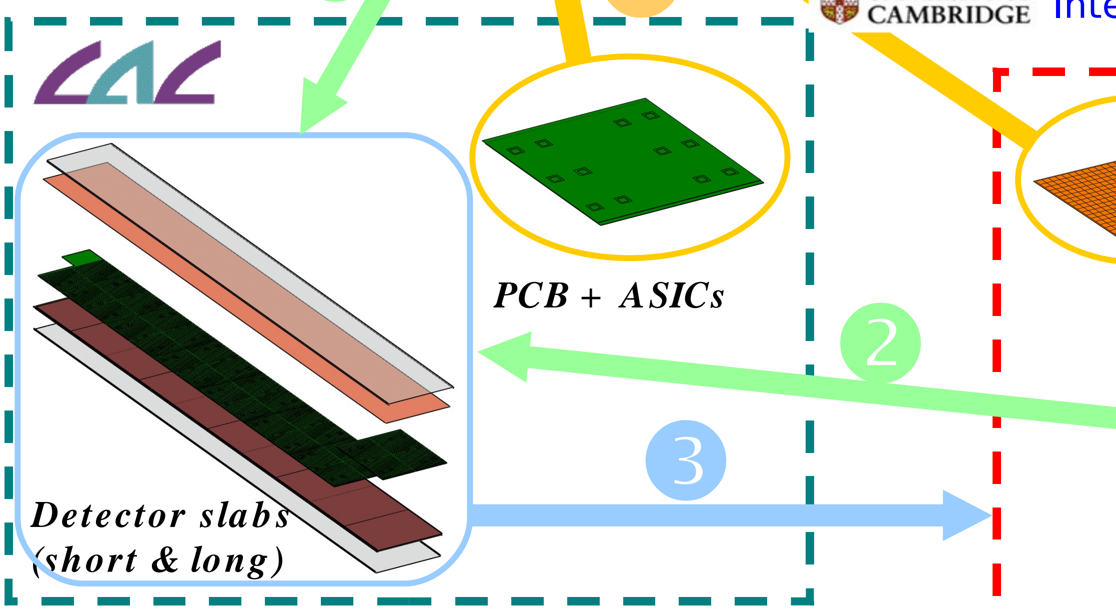
Thin PCB with embedded ASICs

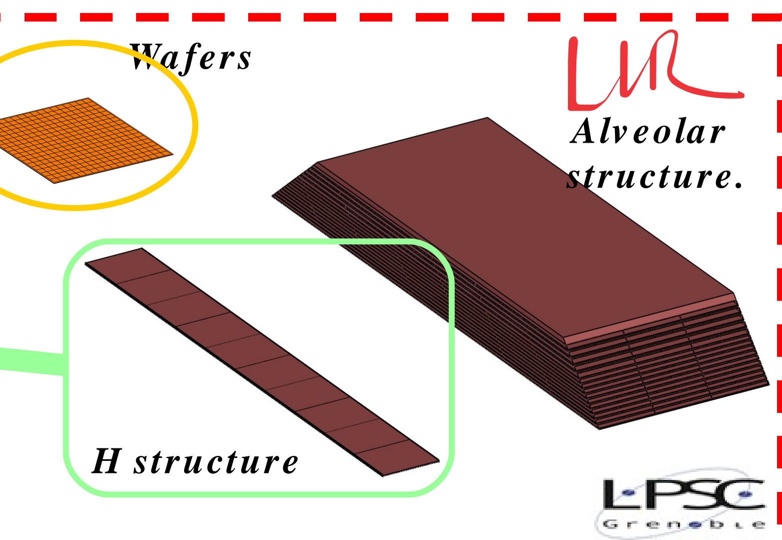
Detector slabs integration

External cooling system (+ Manchester)

Fastening system ECAL/HCAL+composite plates

Interconnection of ASU, DIF(?)





Status of Wafer Production

- 20 Wafers to be expected from Hamamatsu expected by Middle of April

  - 90x90mm2 wafers for 324 cells per wafer
  - 5x5 cell size
  => 324 Cells/wafer

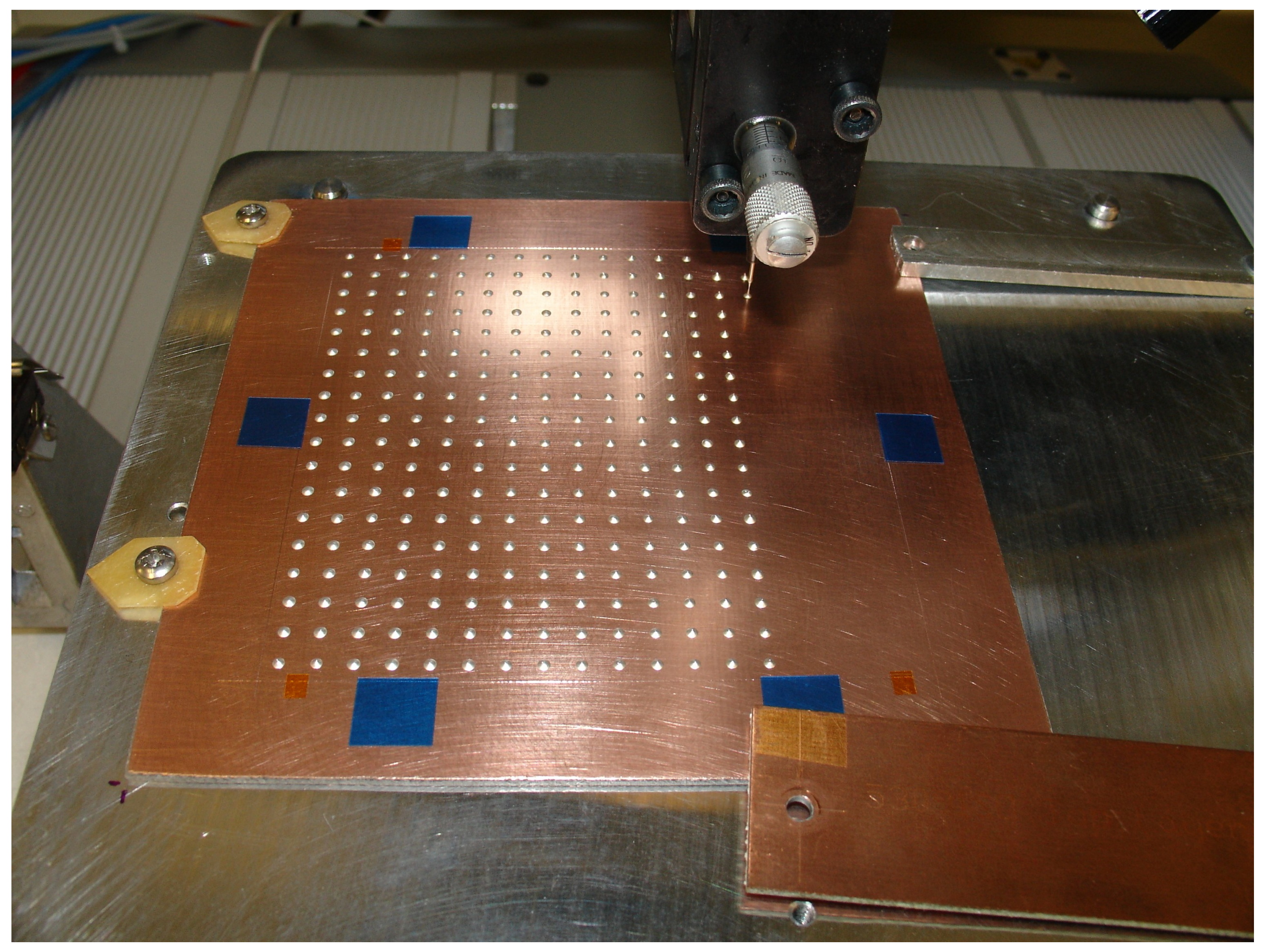
- Immediate start of Characterisation
  - Leakage Current (I-V curves)
  - Full depletion Voltage (C-V Curve)

- Can be used to test gluing with 'real' wafers
  (Depends on speed of Characterization Tests and quality of Wafers)

- On going: New designs of guard ring
  -> Talk by Francois

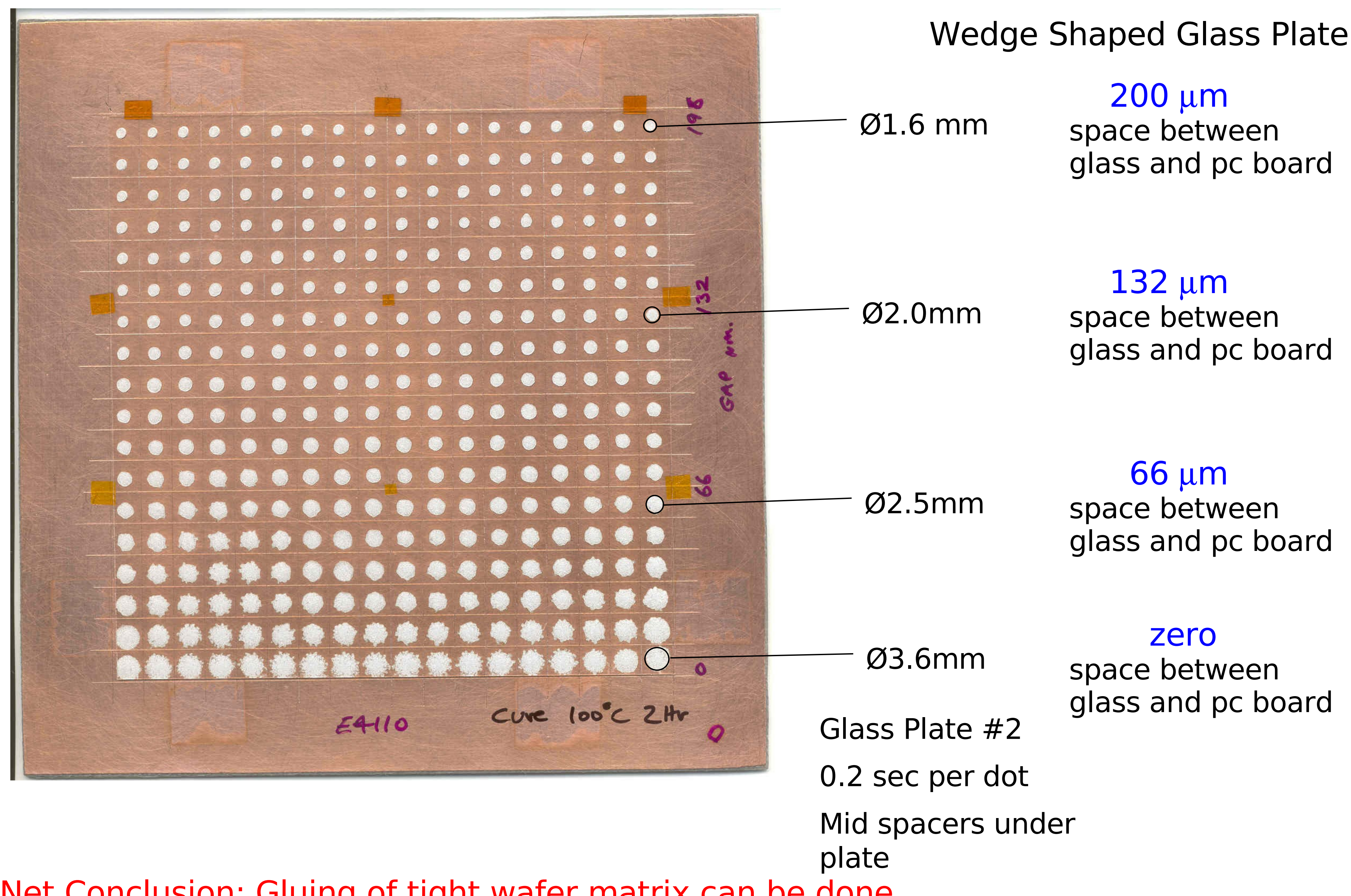
Mechanical/Electrical Connection between Wafer and PCB – Gluing Te

Using simple glass plates to mimic wafers



Placing glue dots

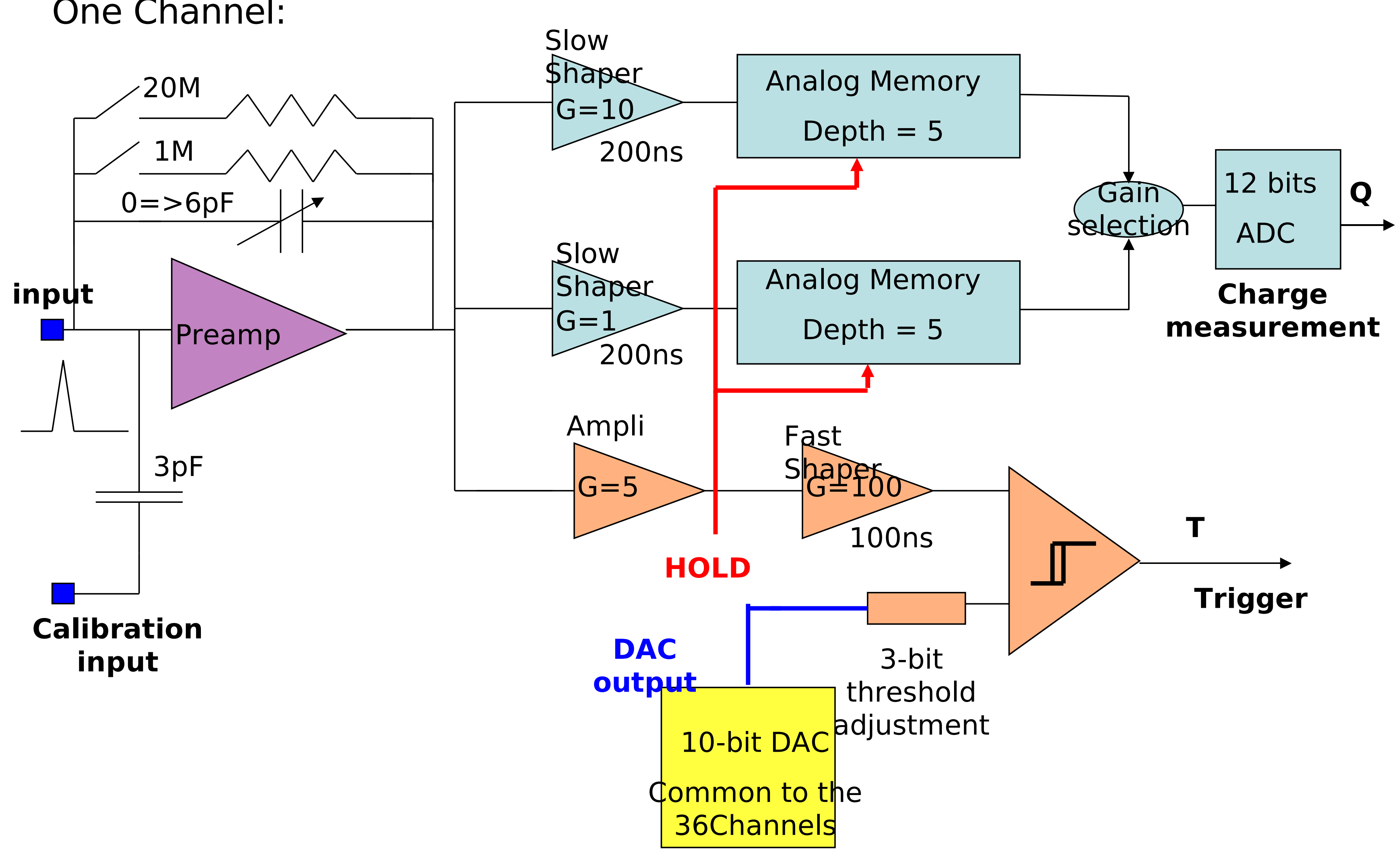
18 x 18 (324) dots on 5mm grid takes ~5min



Net Conclusion: Gluing of tight wafer matrix can be done

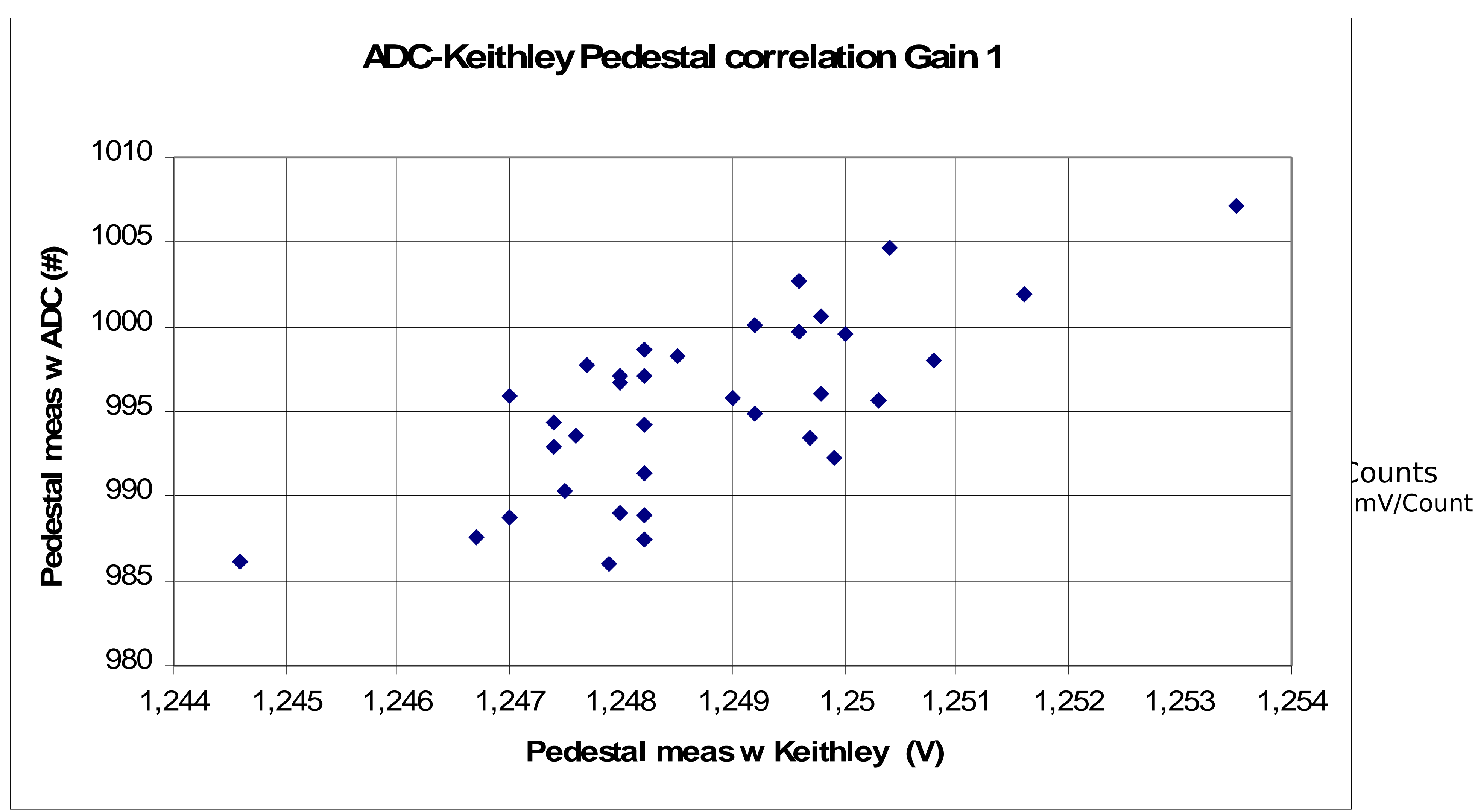
Dot thickness/width influences resistivity: Diameter control within 50μm seems feasible

SKIROC Chip



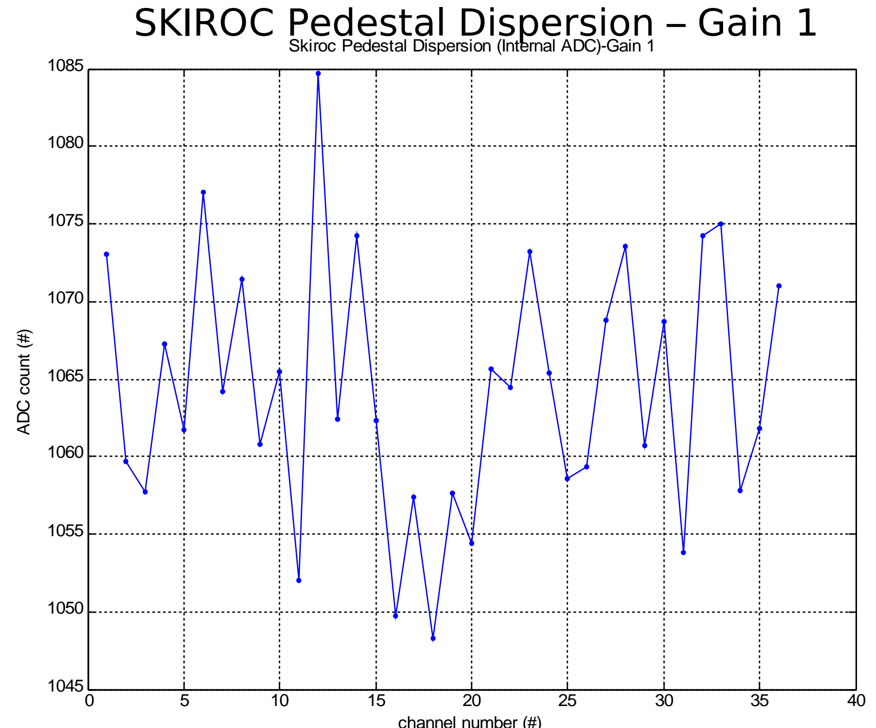
Test with 36 Channel Chip
SKIROC Chip still in design phase mainly due to high demands on compactness
Pixel Calorimeter is challenging technology

SKIROC Measurements



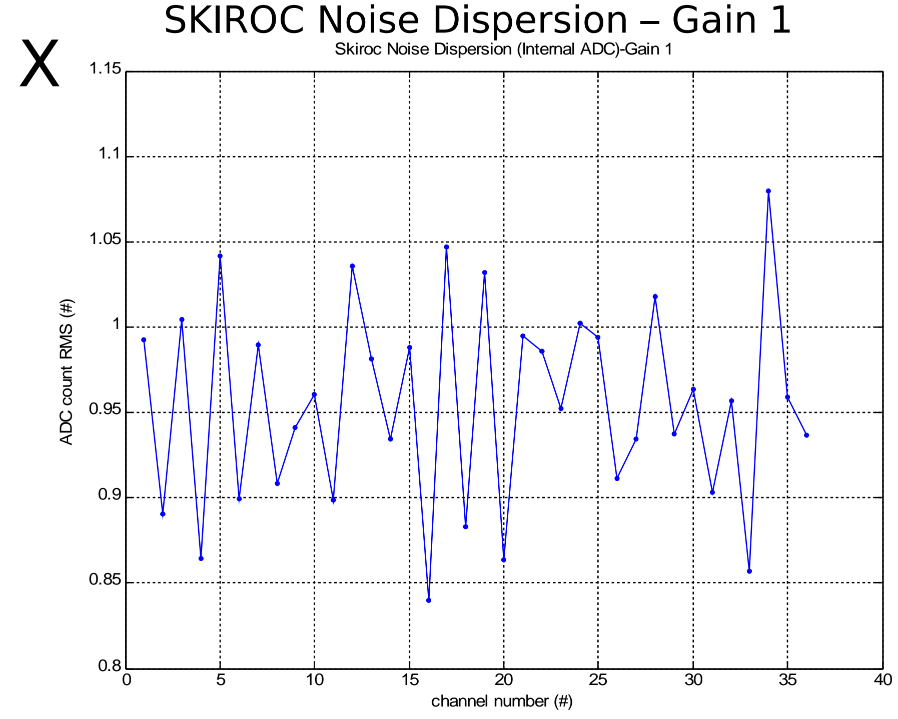
Independent measurements of pedestals compatible

SKIROC Pedestal Dispersion – Gain 1



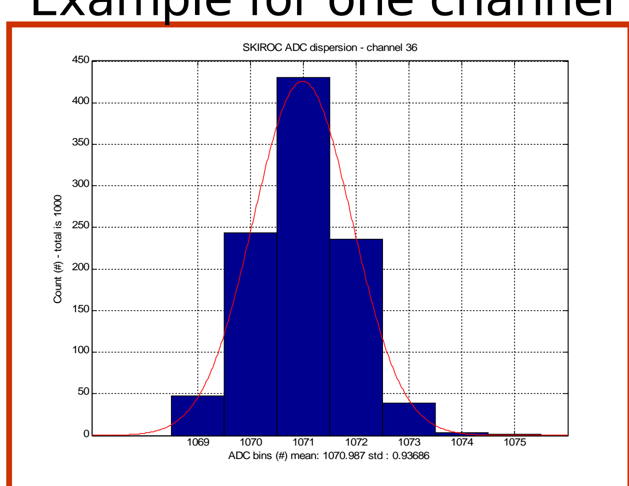
X

SKIROC Noise Dispersion – Gain 1



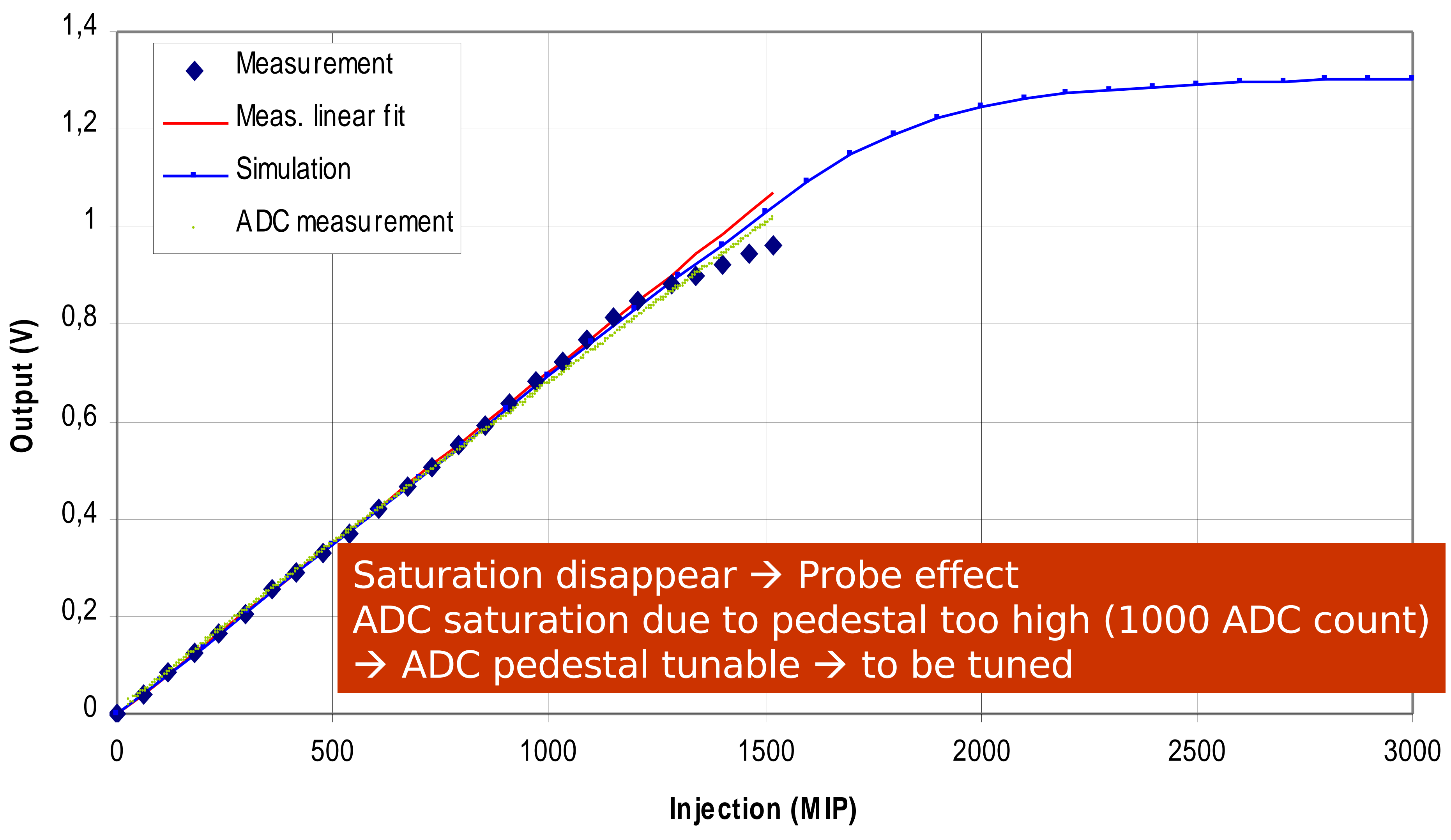
Random Distribution of Pedestals

Example for one channel



Gaussian Noise
~0.95 ADC Counts = 330 μV

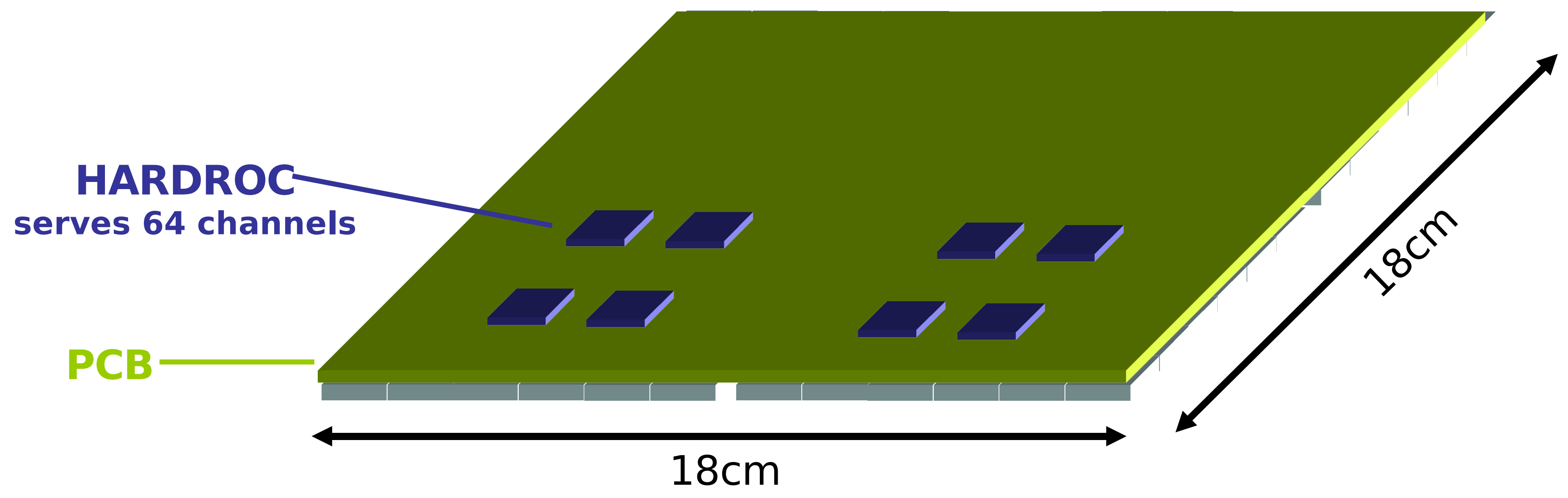
SKIROC - Linearity



- Saturation also observed in independent measurements
- Effect about to be understood

PCB Design: Towards FEV5 – First steps …

Use HARDROC Chip (for EU-DHCAL) to advance in PCB design



- PCB to be designed for 1296 Pads (=4 Wafer à 324 Pads)

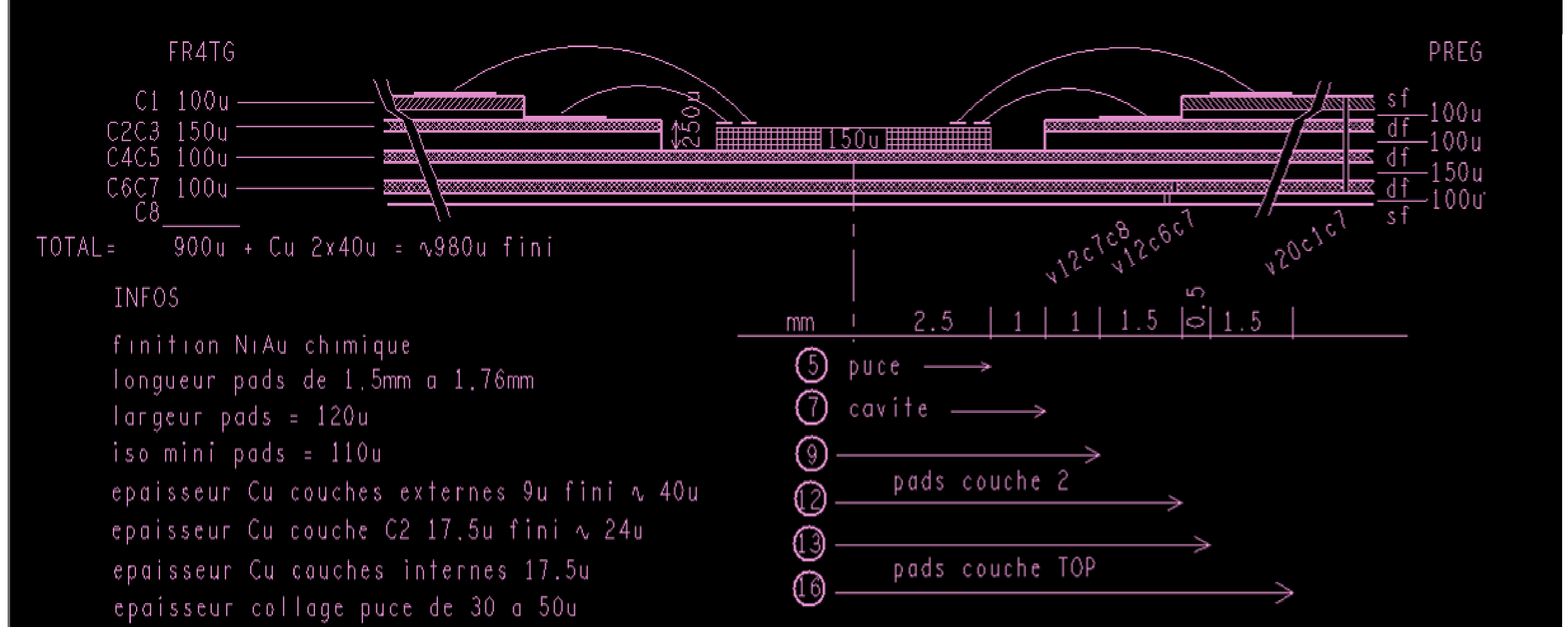
- High degree of compactness

Chip Integration in PCB

Pile-up

TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7



- Bonding wires from Chip to PCB challenging due to large number of channels
- Has to fit into overall mechanical tolerances (see above)

Schedule (Taken from Marc Anduze)

MANCHESTER 1824

Assembling of **A.S.U.** (industrialization, gluing and tests) :

first gluing studies (glass on PCB)	**March 08**
first resistive tests according to the size of the dot	**March 08**
Backend system (DIF support)	**Jan 09 ?**
Services (cooling system participation ?)	**Jan 09 ?**

Tests of **wafers** :

reception 30 first wafers	**April 08**
set-up ("mechanical box")	

Global Design

Composite **Structures** :

mould + first H structure (126 mm)	**March 08**
"alveolar layer" mould + first layer	**April 08**
assembly mould	**June 08**
demonstrator (2 or 3 layers – 126mm)	**Sept 08**

Thin PCB with embedded ASICs	**Jan 09 ?**
Detector slabs **integration**	**Jan 09 ?**

LPSC Grenoble

External **cooling system** (+ Manchester)	**June 08**
Fastening system ECAL/HCAL	**March 08**
composite plates	**Feb 08**

Lot's to be done