EUDET module – Electronics Integration

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for the DESY AHCAL developers

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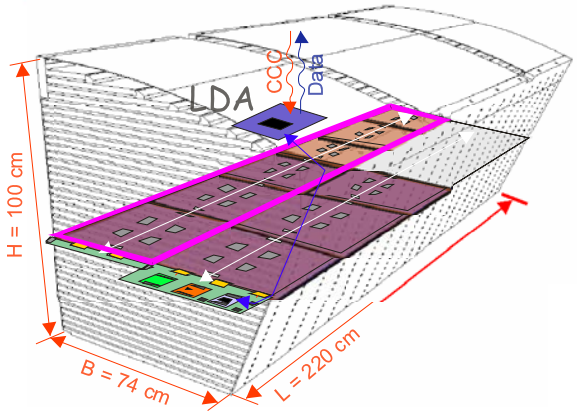
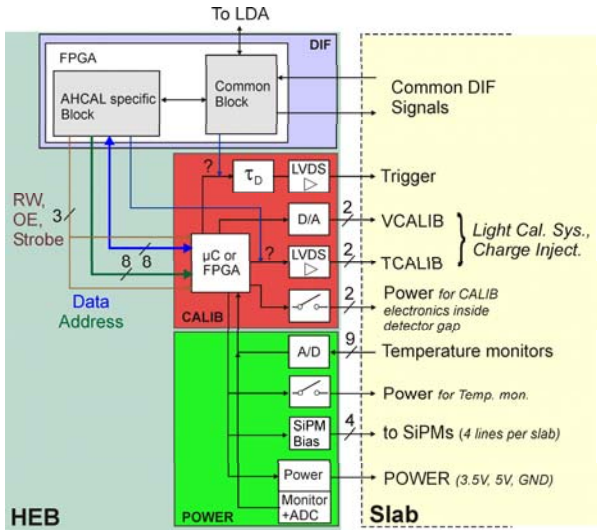
Next prototype: Architecture

FE

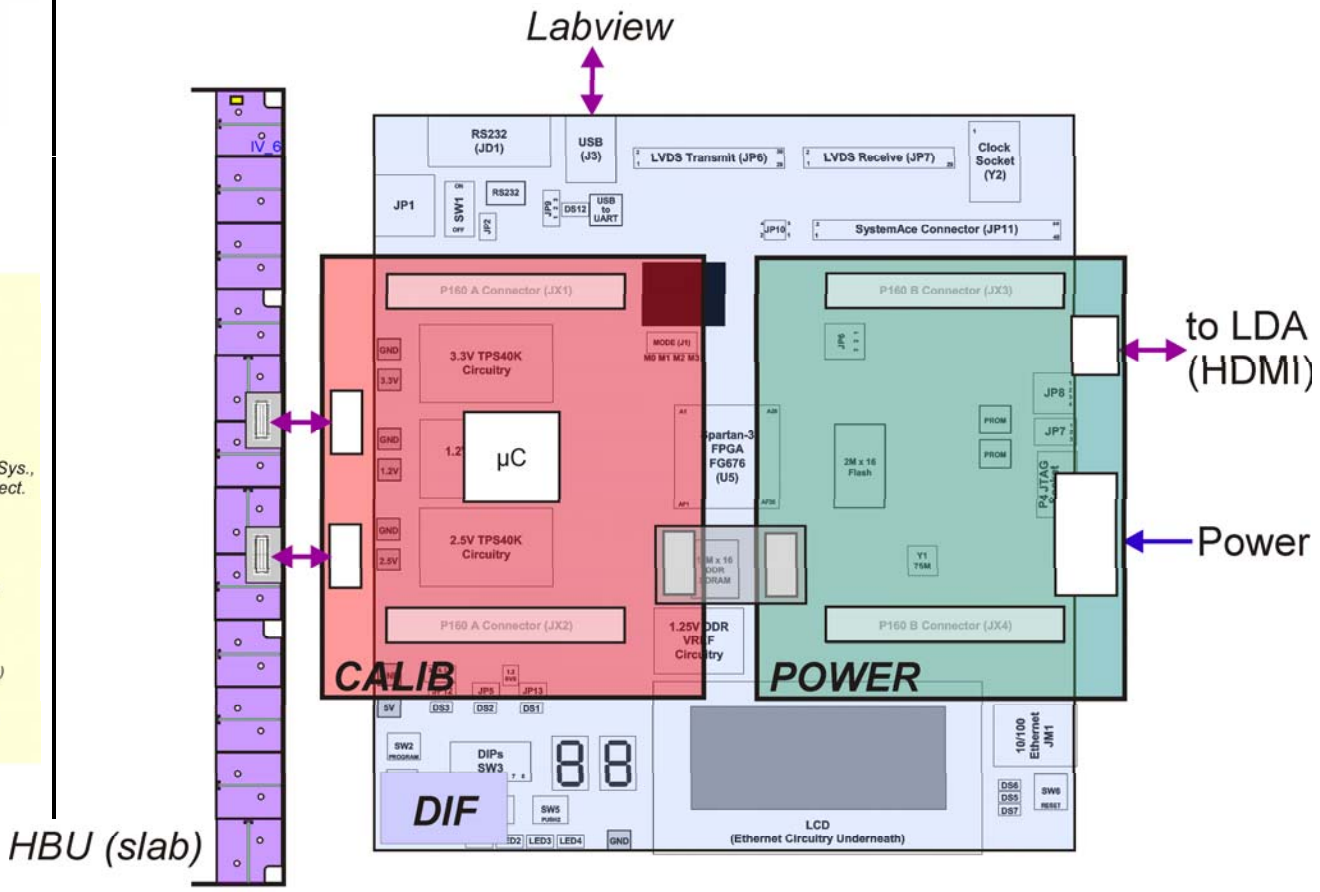


‚final' design proposal

DIF in 1st step: Commercial FPGA Board
CALIB and POWER: Mezzanine Modules
HBU in final extension: 144 Tiles



first setup idea



HCAL Base Unit (HBU)

FE

Integrates 144 scintillator tiles with SiPMs (MGPDs), 4 SPIROCs and a calibration system (gain monitoring)

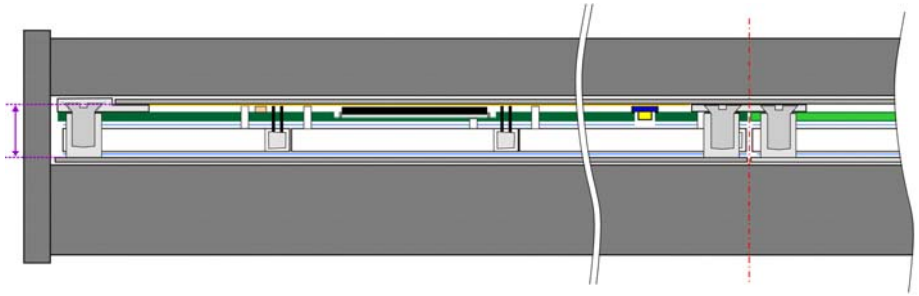
HBU prototype not in final height (current SPIROC: 4.3mm high, smaller package for next SPIROC in discussion)

All critical design features (e.g. cutouts for components in PCB) will be tested.

HBU design runs in parallel with SPIROC test and tile optimization
=> design time-schedule is not clear

Light-tight cassette for single HBUs (prototypes) in design.

Goal:



HBU Component Map Proposal

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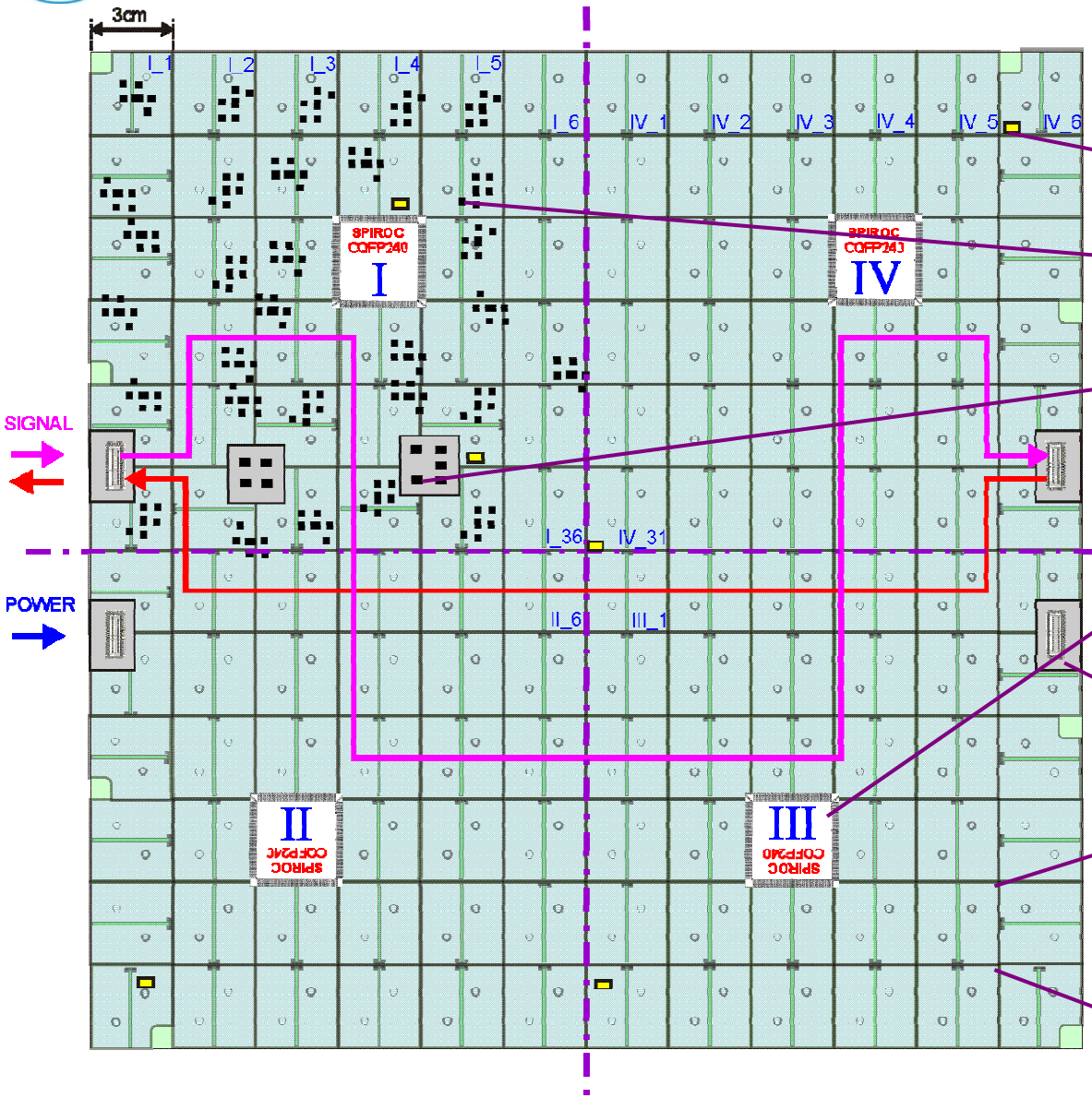


No tiles below SPIROCs

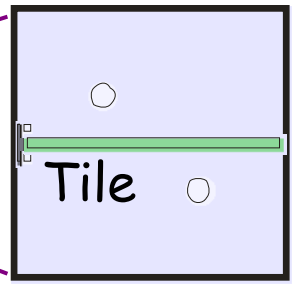
Temperature Sensor

LED per tile system

LED input electronics
(2 blocks per HBU)

SPIROC

80-pin Connector
(in PCB cutout)



HBU - Tile Integration

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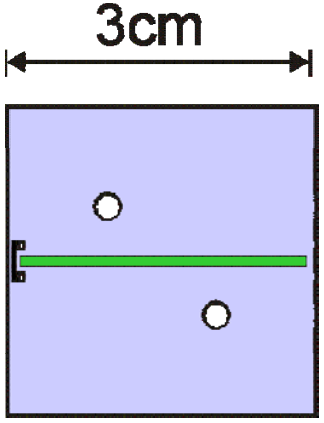
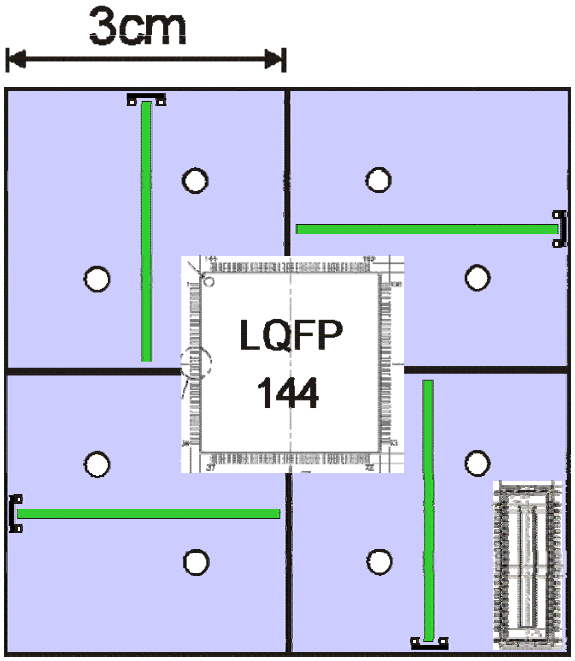
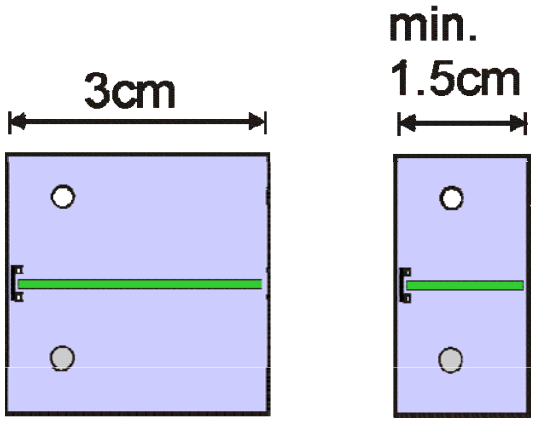


Standard tile with SiPM, WLS and alignment pins



Special tile grouping needed for component placement on HBU.



‚Alternative' positioning of alignment pins possible ? => more freedom for component placement and HBU inter-sizes (AHCAL stack: layer-to layer variations of width).

Final tile dimensions are precondition for HBU layout generation.

HBU Calibration Systems I

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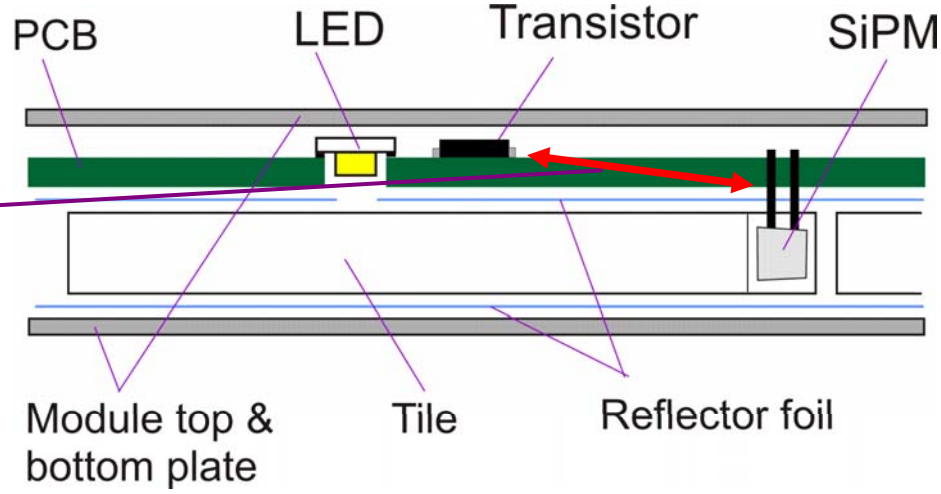
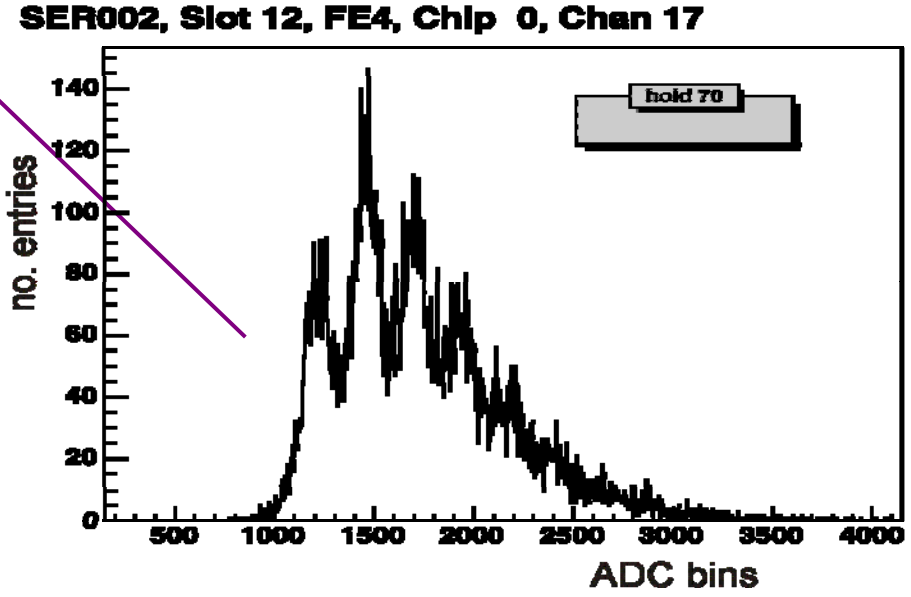
Concept under investigation at DESY: 1 LED per tile.
Concern: Fast LED trigger (transistor base) disturbs SiPM



First results (only few noise optimization): Single-photon-peak spectrum visible !!
⇒Our LED driver design and PCB+SiPM setup is suitable.



Detailed analysis follow:
LED component-to-component spread (optical power), dynamic range, crosstalk.
=> Wuppertal Univ.

HBU Calibration Systems II

FE

LED Light Calibration and Charge Injection for SPIROCs will be implemented.

Fast triggers (TCALIB) for both systems: differential to HBU (LVDS, 220cm slab length), level translation and fanout on HBU.

Maximum LED trigger rate: 200kHz

Power Dissipation of HBU calibration electronics:

326mW (LED system on HBU)

= 2.3mW per channel

= 23µW per channel @ 1% duty cycle (worst case!)

calibration electronics is switched off when not needed!

Detector Interface - DIF

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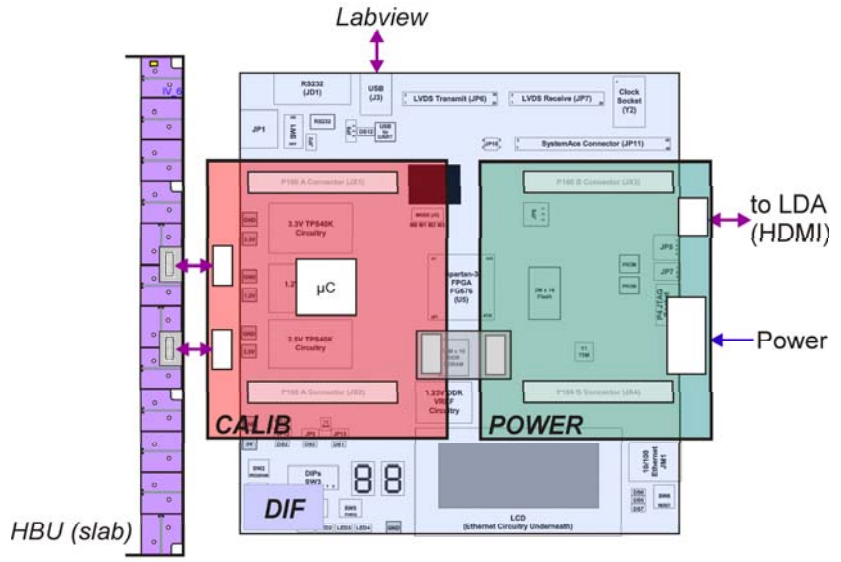
AHCAL prototype DIF is based
on commercial FPGA board.

DIF working group agreed on
signal list and DIF-slab communication.



AHCAL DIF requires VHDL programming:
-adaptation of common FPGA firmware (B. Hommels et al., Cambridge),
-definition of AHCAL specific FPGA code (operation of CALIB module)

New developer for AHCAL DIF prototype: Frantisek Krivan (DESY FEA).

Detector Interface - DIF

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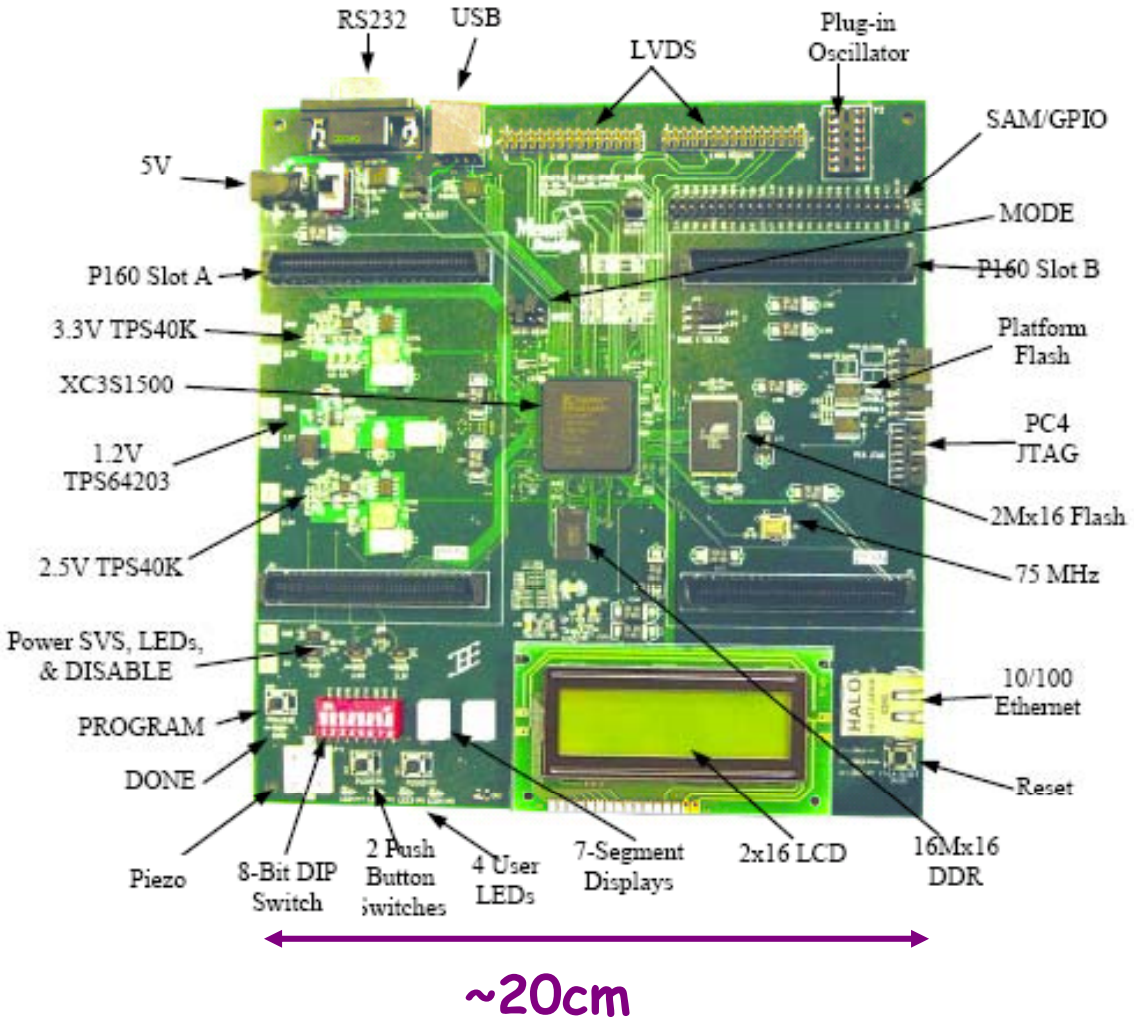
Commercial Spartan3
(Xilinx XC3S1500)
FPGA Board

Slots for mezzanines
(CALIB, POWER),
USB interface (Labview)

Board specs. have been
checked for suitability,

all pin lists are defined,

board has been ordered.



Calibration Module CALIB

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AHCAL prototype CALIB:
Operation of the AHCAL light (LED-) calibration and charge injection systems.

Contains Microcontroller (µC) for slow control, temperature readout, (layer-)power-supply switching.

CALIB module requires PCB board design and µC-programming.

New developer for AHCAL CALIB prototype: Mourad Zeribi (DESY FEB).

Calibration Module CALIB

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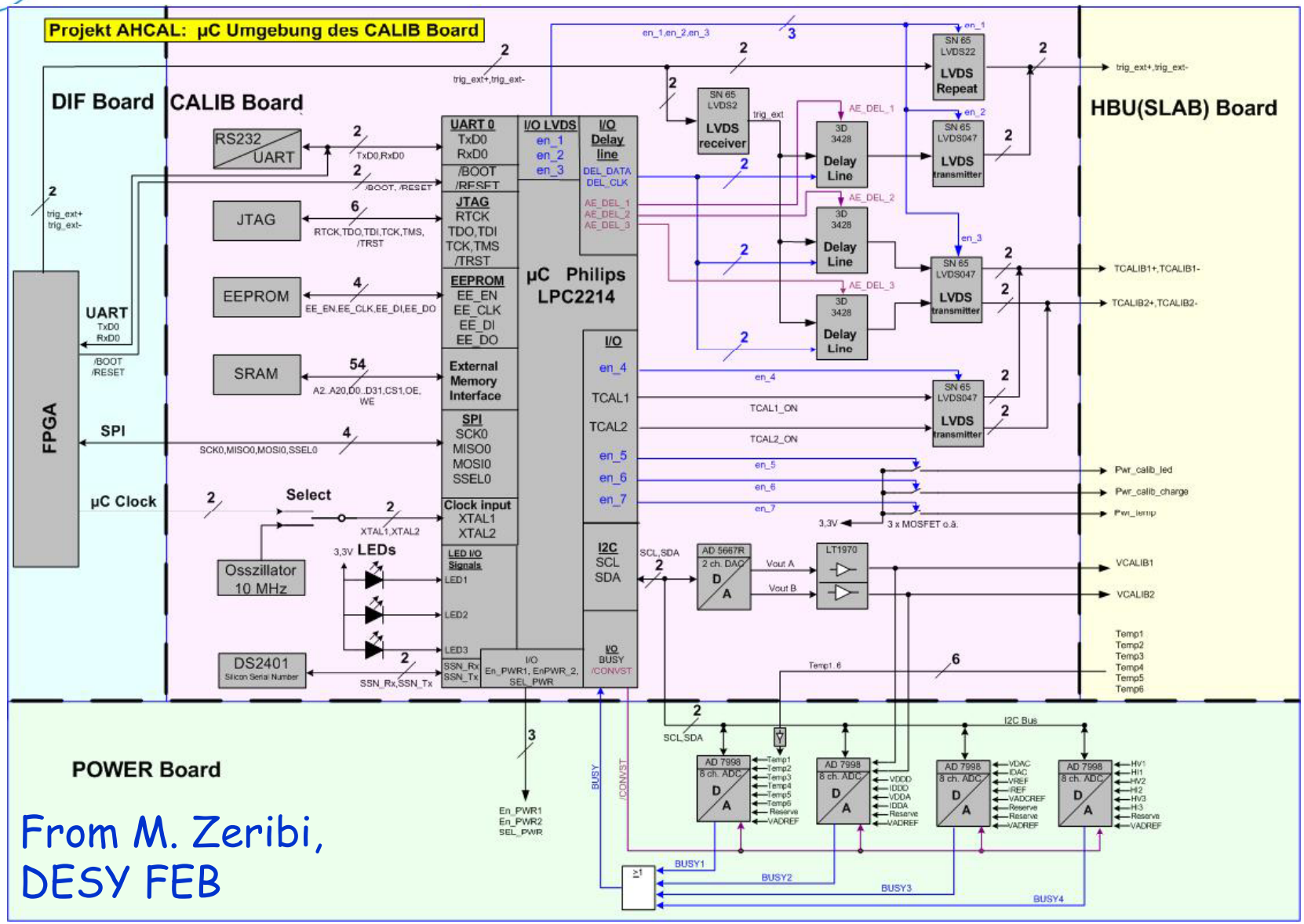

From M. Zeribi, DESY FEB

Power Supply Module POWER

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AHCAL prototype POWER:
Power supplies for detector slabs,
DIF and CALIB modules.

Regulators for ILC power cycling.

Filtering of the **input voltages:**
AHCAL: +12V, +6V, SiPM-bias (~+60V), GND

POWER module requires PCB board design.

New developer for AHCAL POWER prototype: Hans Wentzlaff (FEB).

Power cycling test setup

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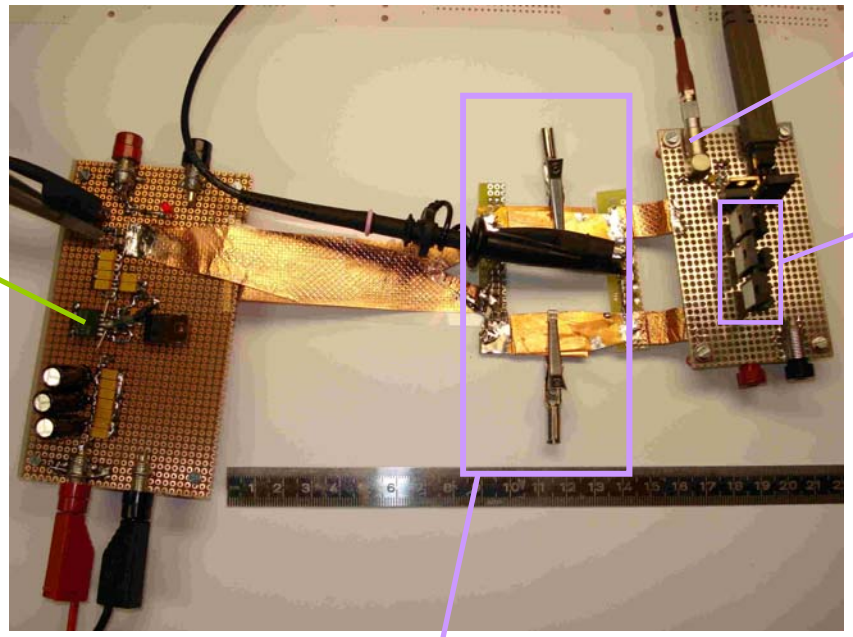
Test of the ILC power cycling: Detector electronics (load) is switched from „off" (no current) to „on" (up to 3A load).
=> Oscillations on 2.20m-long power-ground system?

Test Setup



Switch-Load input

Load (e.g. 1A) and block caps (e.g. 1µF) **„HBU" emulator**

Regulator (DUT) POWER module emulator

Test by H. Wentzlaff

Power and Ground Interfaces (detector plane of 2.20m will be connected in between here)

Power Cycling – Typical Result

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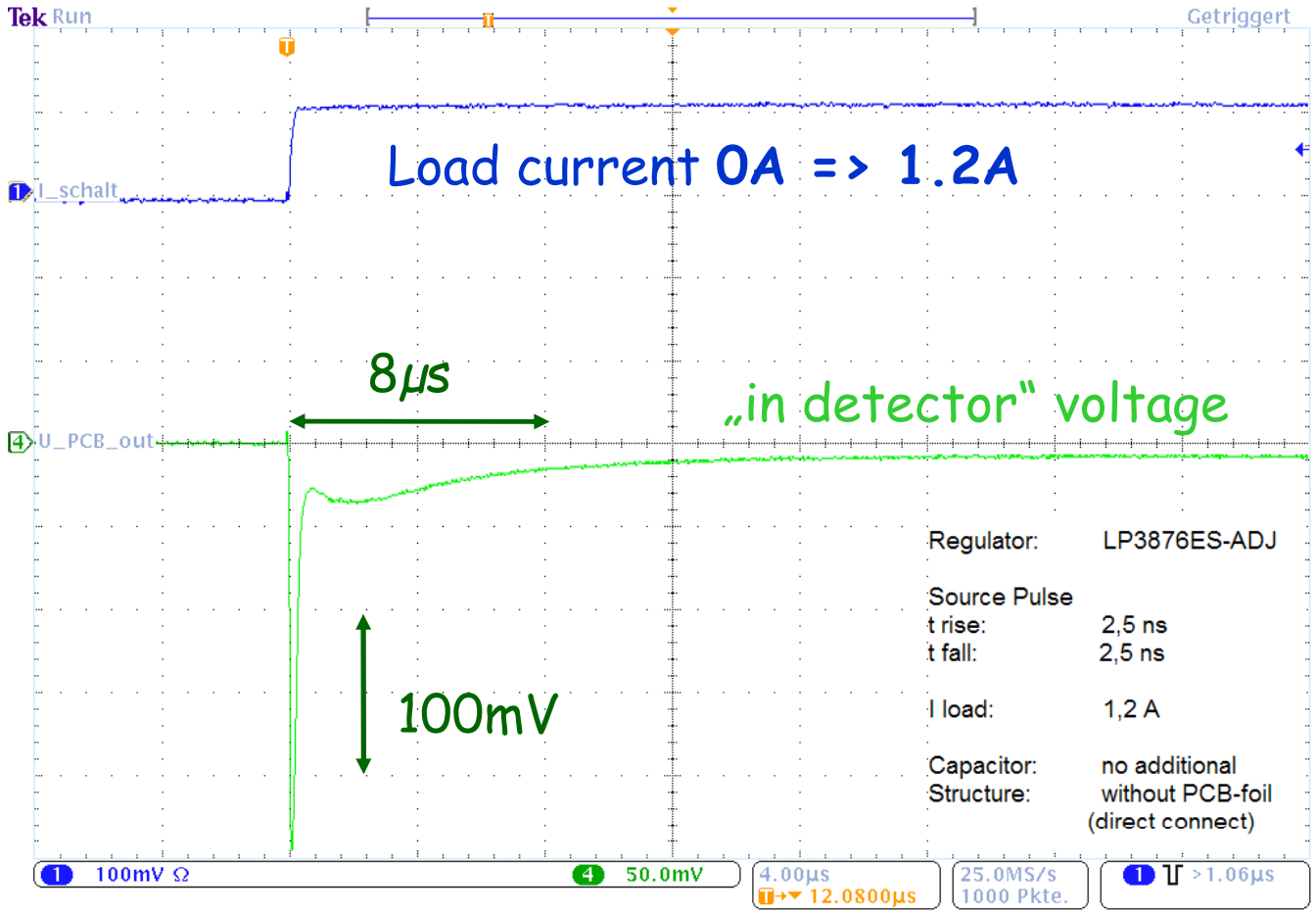

Voltage settling time of ~20µs fits well to ASICs power-up time.
But: With block caps of 1µF on the HBUs, a longer settling time (+50%) has to be expected.

Power Supply Module POWER

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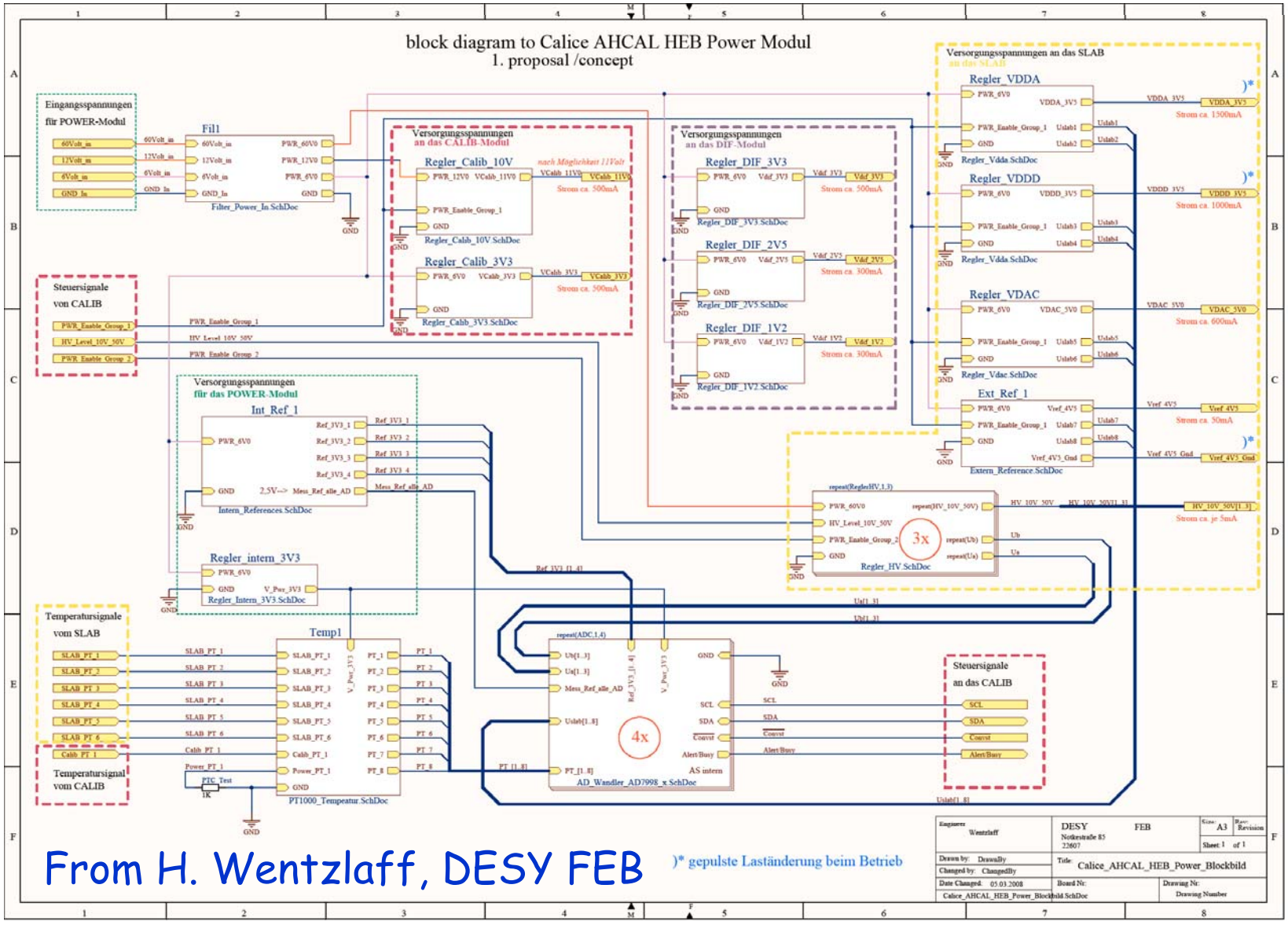

From H. Wentzlaff, DESY FEB

Timeline (condensed version)

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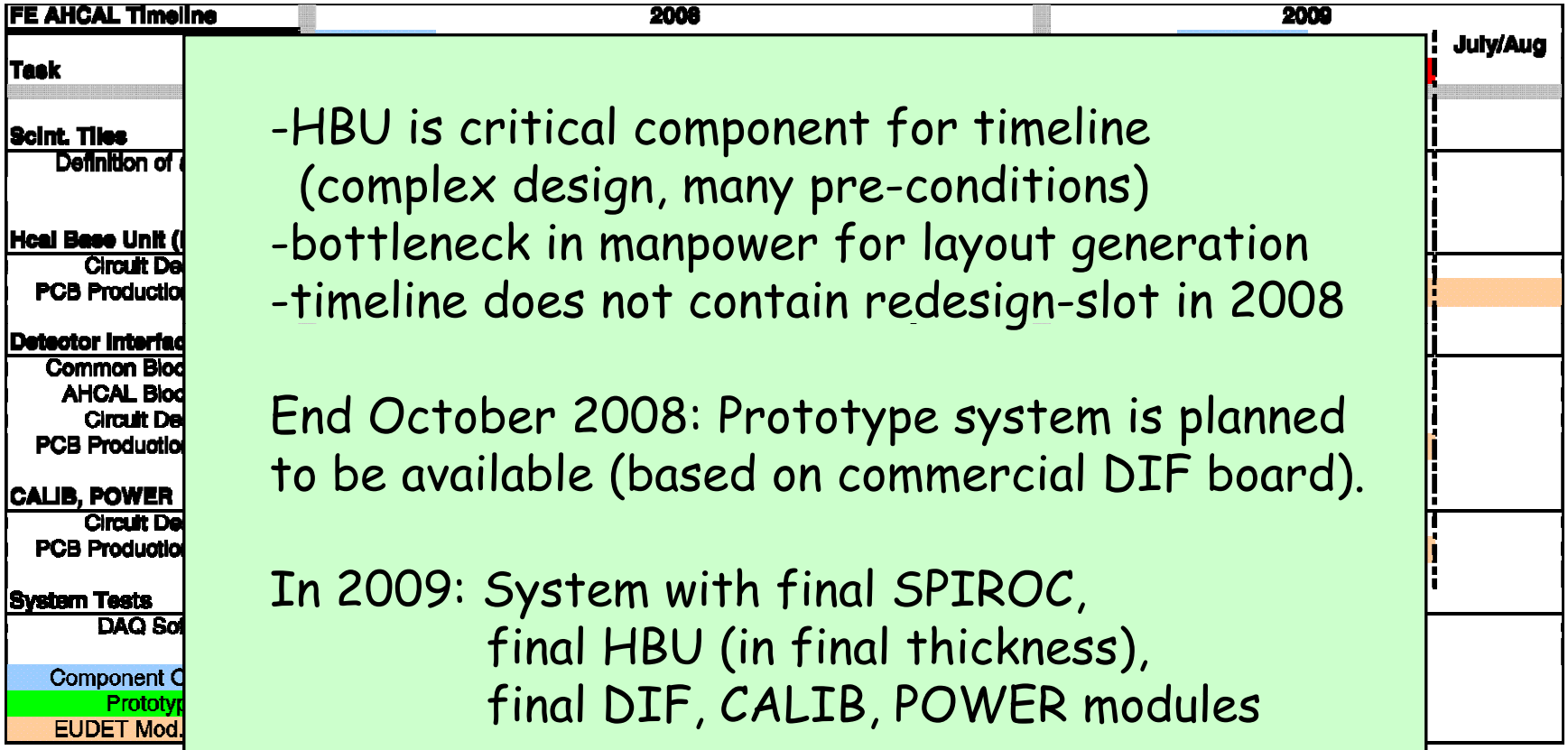

-HBU is critical component for timeline
(complex design, many pre-conditions)
-bottleneck in manpower for layout generation
-timeline does not contain redesign-slot in 2008

End October 2008: Prototype system is planned to be available (based on commercial DIF board).

In 2009: System with final SPIROC,
final HBU (in final thickness),
final DIF, CALIB, POWER modules

Conclusion

FE

New people reinforce the prototype design at DESY.

Design proposals have been set up for the prototype modules HBU, DIF, CALIB and POWER.
Schematic entry (PCB design tool) starts now.

Timeline is ambitious because it contains many preconditions.
A lot of things have to run in parallel => maybe bottlenecks.