IN2P3

LAL

Omega

CALICE Electronics issues

19 March, 2008

Orsay MicroElectronic Group Associated

Electronics for technological modules

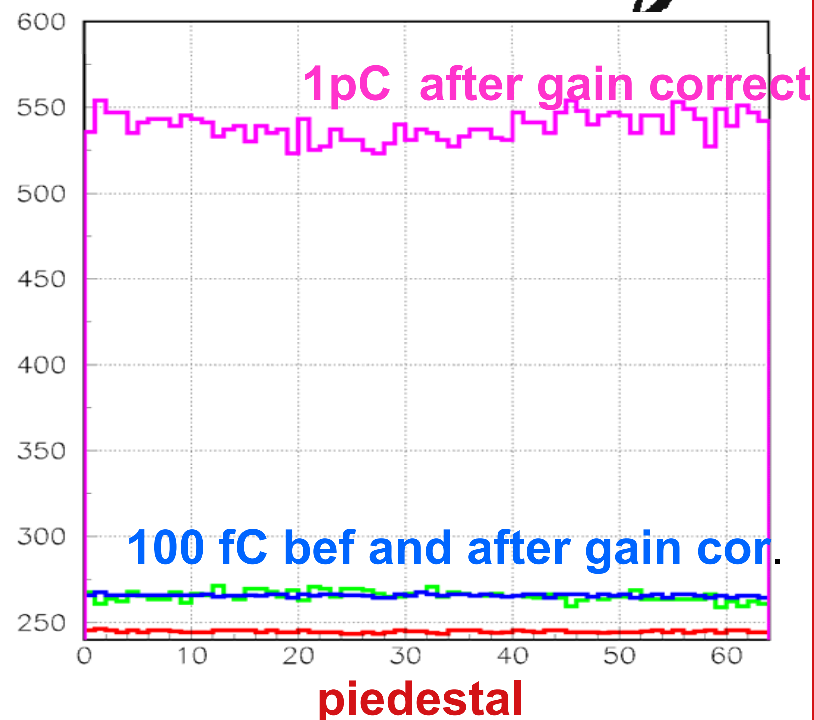
- Summary of Monday's meeting
- Some issues from London's meeting
- Difficult to summarize in 1h large ongoing activity and full day meetings !
- Mostly discussion on most pressing issues :
  - Hardroc, Spiroc and SKIROC results and plans [Omega,LPCC]
  - ASIC Production issues
  - ECAL ASUs and signals distribution [Cambridge, Manchester, LAL, LLR]
  - AHCAL HBUs [DESY]
  - DHCAL ASUs and DIF [Lyon, LAPP, LLR]
  - Power supplies considerations
  - 3rd generation R&D [Omega,LPCC,LPSC]

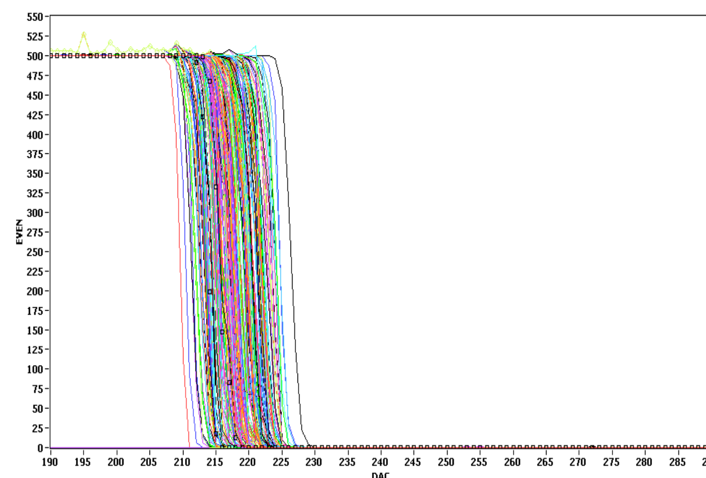
Summary of HARDROC measurements

- **Auto trigger with Qinj=10fC:**
  - **Qinj=10fC in Ch7**
  - **Vth0 and Vth1~5fC**
- **Auto trigger without signal:**
  - **Thresholds can be set down to a few fC without any autotrigger, despite the digital noise**
  - **Random counting< 1Hz/chip**
- POWER PULSING
  - TARGET: 10 µW/ channel with 0.5% duty cycle=> 640µW/3.5V=180 µA for the entire chip
  - Measurement: 125 µA for the entire chip
  - 1 bug (easy to fix): Bandgap V not power pulsed
  - PP of the analog part: (Injection of 100fC, Threshold= 30fC)

  => Awake time= 2 µs (All decoupling capacitors removed)
  - Power pulsing of the DAC:

  => 25 µs (slew rate limited)
- **Daisy chain of 4 Hardroc: PCB 4 Hardrocs** (see Imad's talk in the DHCAL session)

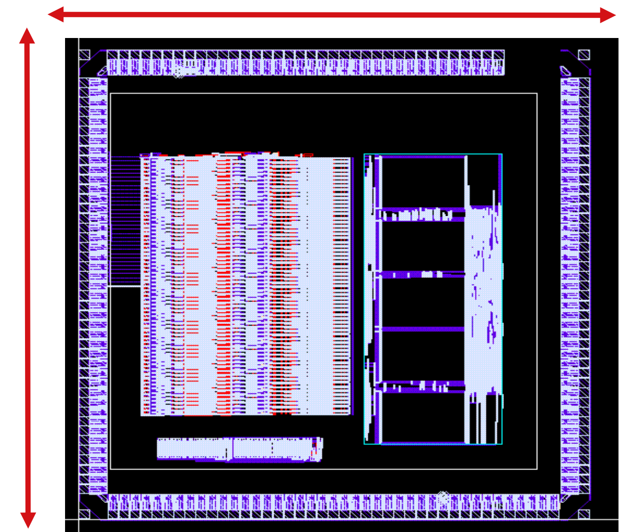




HARDROC2

- HARDROC1 could go to production directly
  - No major bug
  - Measurements going on since > 1 year : still some imperfections found
  - Main drawback is package size and double row bonding yield
- HaRDROC2 could be prototyped in june 08
  - Keep HARDROC1 basic architecture and backward compatibility
  - Have 3 very different thresholds
  - Move bonding pads to single row
  - + many small changes

  (gain accuracy, power pulsing…)
  - Area : 25 mm2
  - TQFP176 package : 24x24x1.4 mm



HARDROC2: FORSEEN MODIFICATIONS

HARDROC2:
FORSEEN MODIFICATIONS

Detector
in<i>

Ctest ch<i>
Slow Ctrl

in_ctest

2pF

Variable Gain Preamp

GAIN CORRECTION
8 bits instead of 6

cmd7 cmd6 cmd5 cmd4 cmd3 cmd2 cmd1 cmd0

From Slow Control
(Gain register)

HARDROC1

HARDROC2

Slow Shaper (ss)

in_ss

T/H

T/H buffer

2pF

Q_R

From Read register

OTA

EN_OTAQ
(pin 223)

out_SS
(pin 218)

Bipolar Fast Shaper (fsb)

Q_R

Valid_DC

DC_FSB (=out_fsb)
pin 212

out_FSB0

DISCRI 0

Q_R

EN_out_discri (Slow C)

Valid_out_trig
=EN_out_discri (Slow Ctrl)

direct_trigger0

RS_trigger0

Q_valid_trig
= valid_trig_chi
(SC)

LATCH

RazChn

ValEvt

Q_valid_trig

trigger0

10k

NOR64
(Internal trigger)

Vth0
(10 to100 fC)

Variable Gain:
G=1,1/2, 1/4,1/8

cmd3_FSB1 cmd2_FSB1 cmd1_FSB1 cmd0_FSB1

out_FSB1

DISCRI 1

EN_out_discri (Slow C)

direct_trigger1

RS_trigger1

LATCH

Q_valid_trig

RazChn

ValEvt

Q_valid_trig

trigger1

MASK BUG+BUFFER for out_RS trig

Vth1
(100fC to 1pC)

Variable Gain:
G=1/4,1/8,1/16, 1/32

cmd3_FSB2 cmd2_FSB2 cmd1_FSB2 cmd0_FSB2

out_FSB2

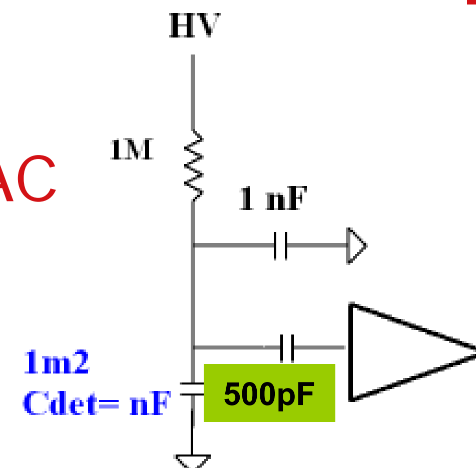
DISCRI 2

Vth2
(1pC to 10pC)

ENCODER of
trigger 0,1,2

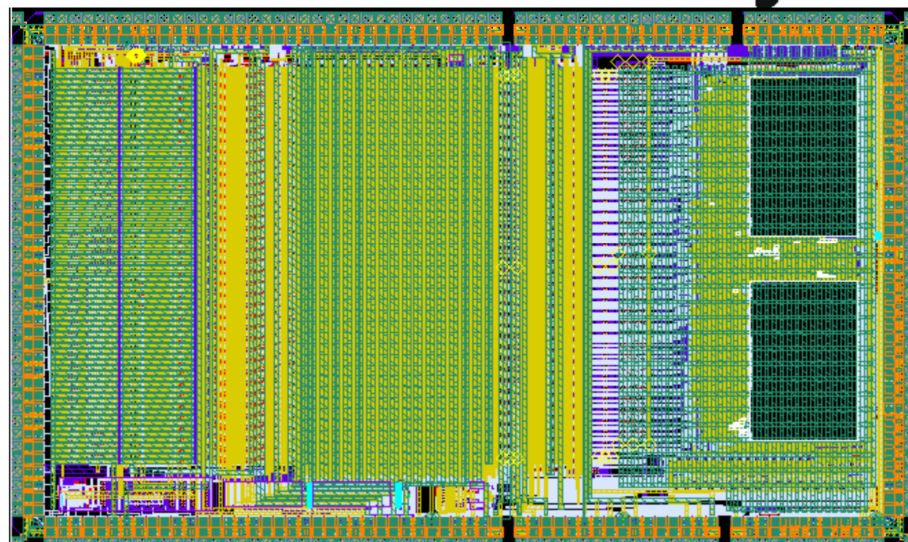
HV sparks (ESD)

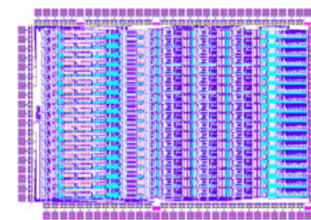
- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)
- From T2K large µmegas [E. Delagnes], AC coupling necessary for area > $10cm^2$:
  - **Maximum decoupling** capacitor that can be **integrated: ≈30pF** (50µm x 600 µm) and **loss of signal**
  - **EXTERNAL CAP=500 pF/ch** to ensure protection
  - Drawbacks of a decoupling cap: Xtalk, space
- HV sparks robustness for **large** GEM-like detectors requires dedicated design effort



SPIROC overview

- Silicon Photomultiplier Integrated Read Out Chip
  - A-HCAL read out
  - 36 channels
  - 30fC-300pC dynamic range
  - Charge measurement (15bits)
  - Time measurement (< 1ns)
  - Auto-trigger at 50fC (1/2 pe)
  - many SKIROC, HARDROC, and MAROC features re-used
  - First prototype received nov07





- Collaboration with DESY

Input DAC linearity

DAC linearity

Voltage (V): 5, 4,5, 4, 3,5, 3, 2,5, 2, 1,5, 1, 0,5, 0

DAC: 0, 50, 100, 150, 200, 250, 300

ch0, ch1, ch2, ch3, ch4, ch5, ch6, ch7, ch8, ch9, ch10, ch11, ch12, ch13, ch14, ch15, ch16, ch17, ch18, ch19, ch20, ch21, ch22

First measurement

High gain channel output

680fC (~4 pe @SiPM gain=10^{6}) in SPIROC

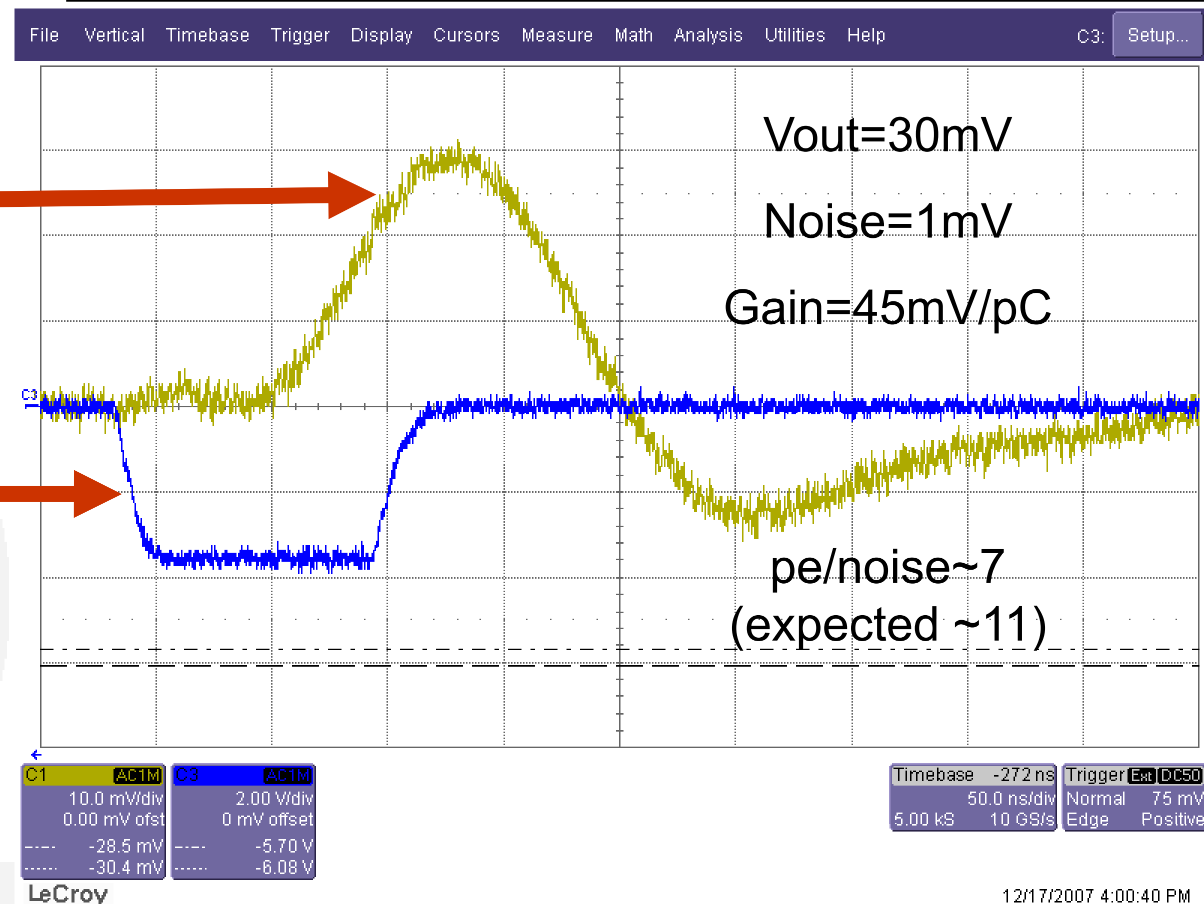
Charge measurement

Auto trigger

Set up:

Cf=400fF

Tau=50ns

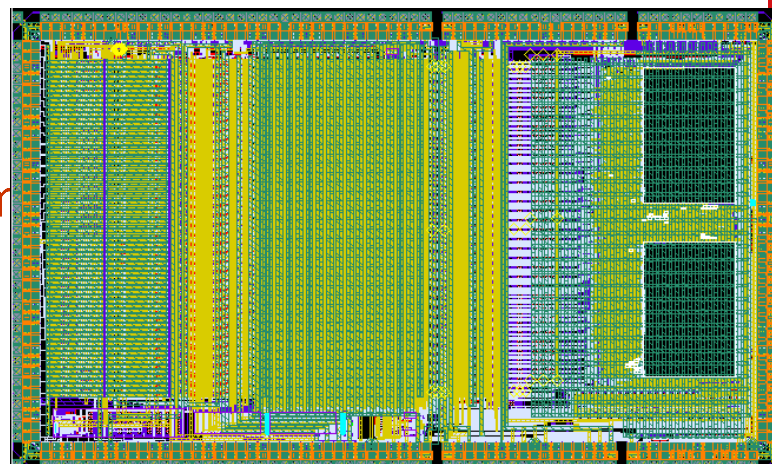


S-curves

SPIROC2

- SPIROC1 needs one more prototype before production
  - 2 major bugs : no probe, no ADC
  - Analog part so far OK, can be used to replace FLC_SiPM
  - Autotrigger at ~50-100 fC
  - Could be tested with existing detector and DAQ
  - Many more measurements to be done : complex chip

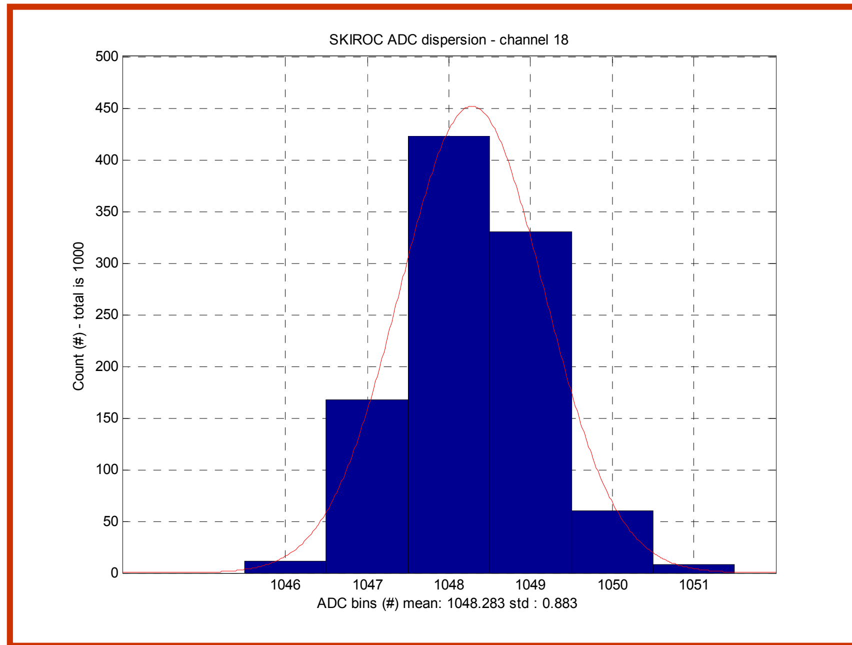
- SPIROC2 could be prototyped in june 08
  - If no major change
  - Possibly SKIROC compatible
  - TQFP208 package : 28x28x1.4 mm

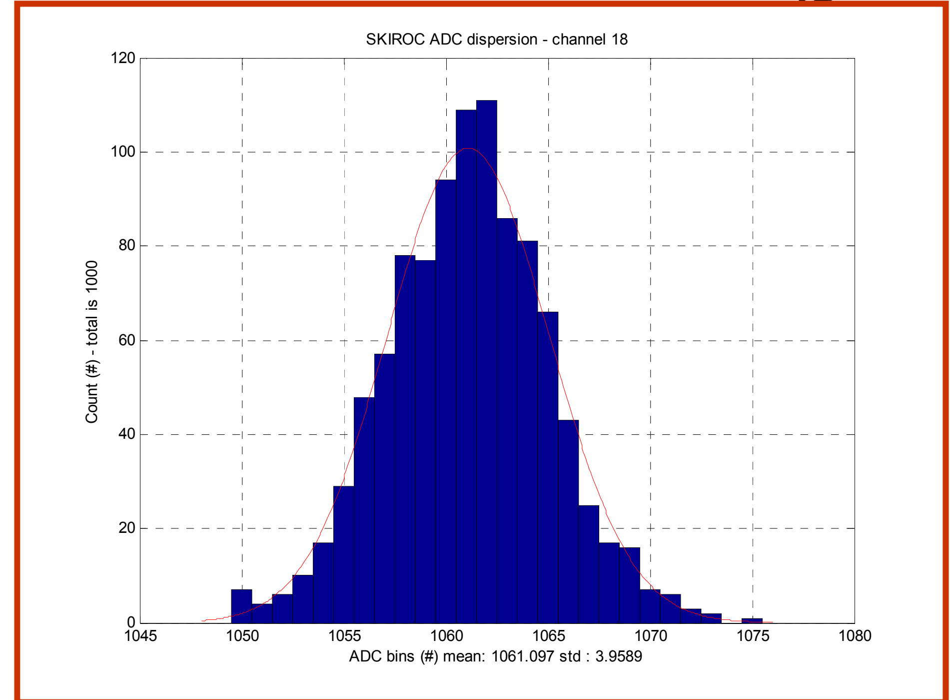


SKIROC status

- Chip in hand since 1 year
- Analog part OK
- Digital part outside (FPGA)
- New 12bit ADC measurements : good performance
  - ADC noise ~ 250 µV = 1 LSB
  - Good uniformity
- Many measurements to be done
  - ADC pedestal and gain stability
  - Autotrigger and S-curves
  - Power pulsing
  - ...

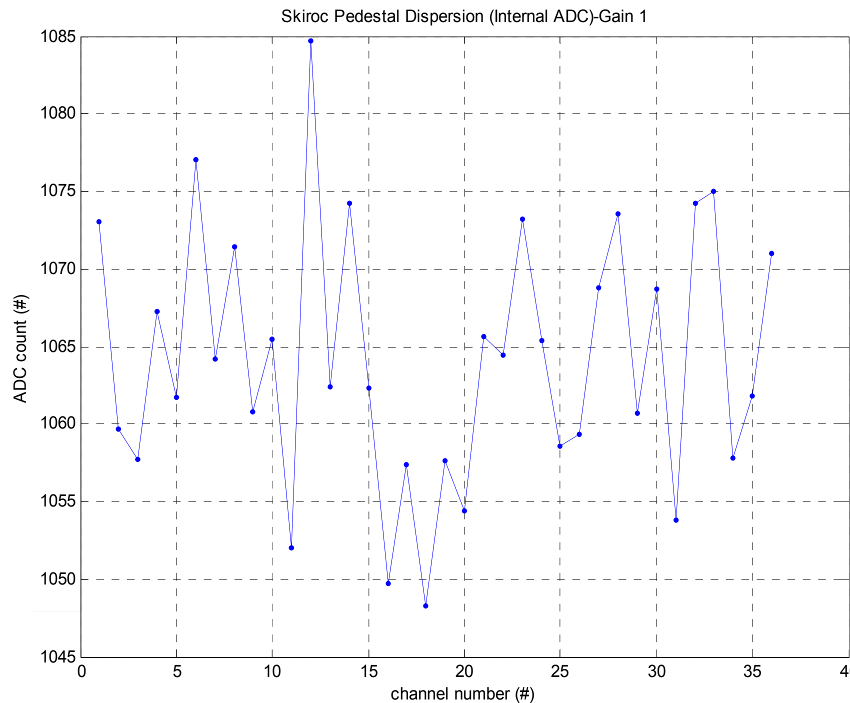
ADC noise – Gain 1 and 10

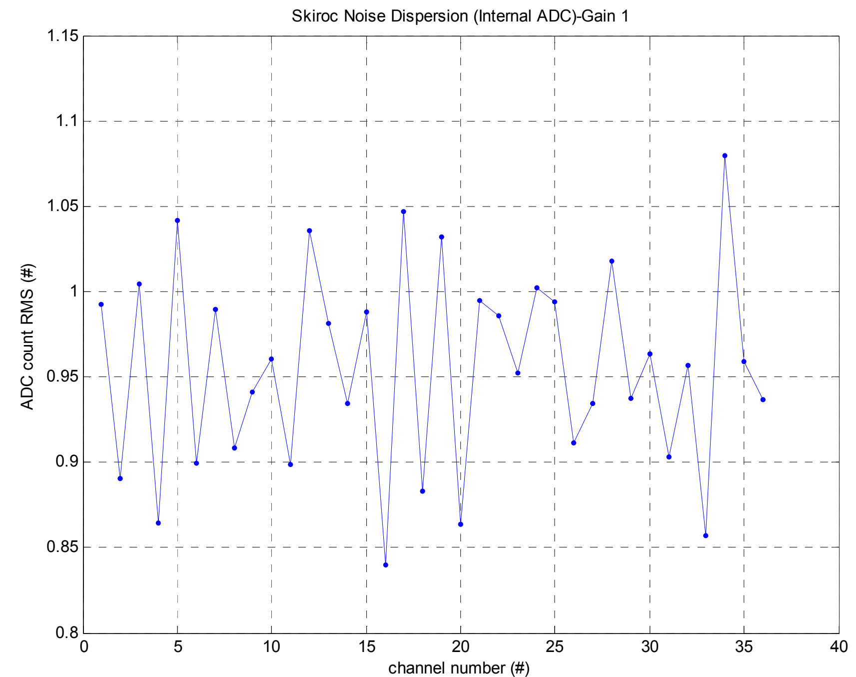




ADC bin = 350µV
Noise is gaussian

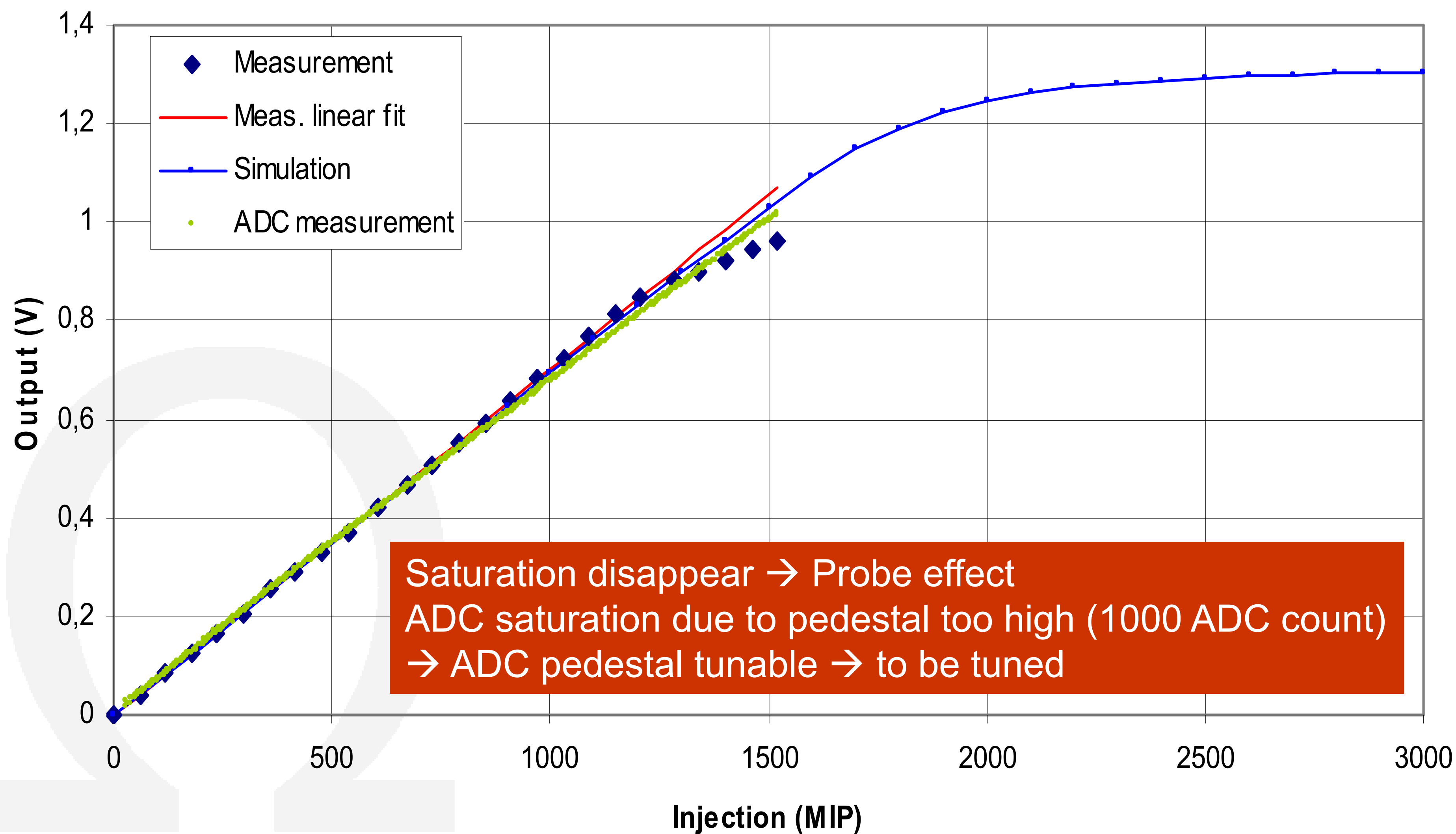
ADC Noise – Gain 1





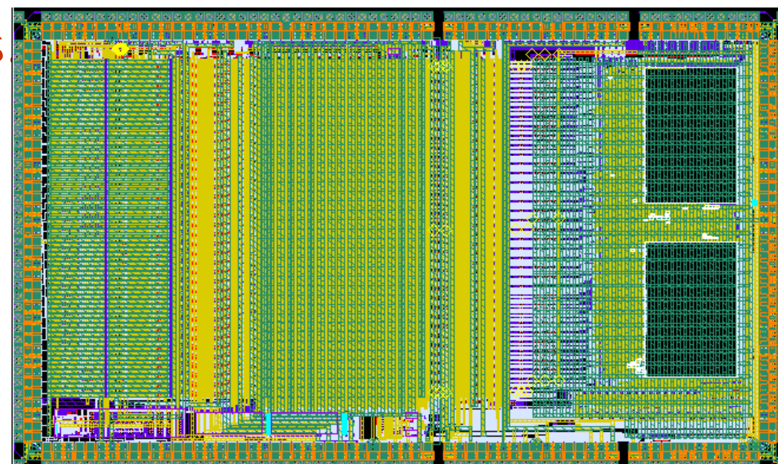
- Pedestal is nicely random – no pattern
- Noise is random → side effect comes from FE electronics, not ADC
- Mean noise is 0.95 ADC count RMS (330µV) - Good
- Results with analogue measurement is 250µV → a few ADC noise seen

Linearity with ADC



SKIROC2

- SKIROC1 cannot be used for detector
  - Digital part outside
  - needs one more prototype before production
  - Analog part so far OK, can be used to replace FLC_PHY3
  - Many more measurements to be done
- SKIROC2 could be SPIROC2
  - Bypass input capacitance
  - Possibly limited dynamic range
  - But ECAL PCB needs 64 channels.

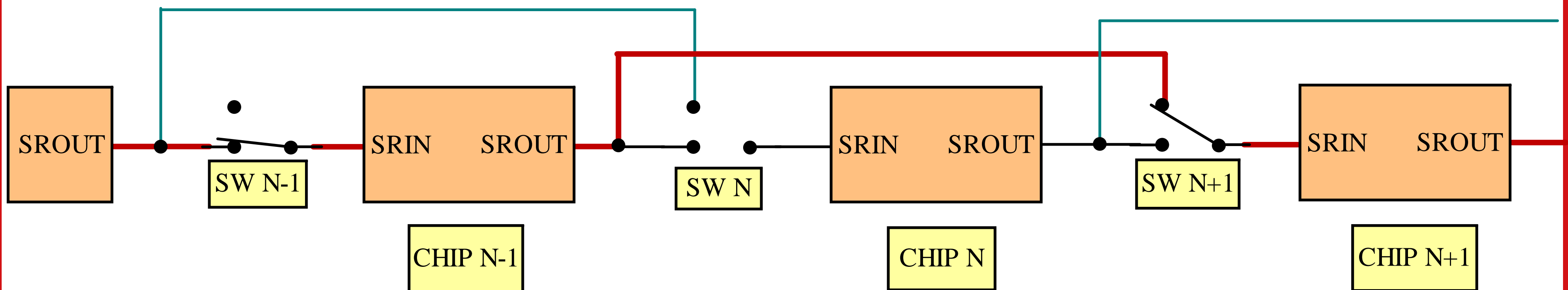


Digital part

- Digital part validated on hardroc
- VHDL code available
- Still many small changes coming up [see F. Dulucq]
  - Many improvements on Slow Control
  - Default mode
  - Last FF for daisy chain timing requirements
  - Reduce PAD number
  - Increase reliability:
  - Double some drivers
  - Possibility to disconnect bus drivers
  - Add bypass on critical signals
  - Remove "dummy frame" and improve digital operation
  - Management of PowerON for digital part
  - Start / Stop clocks
  - Start / Stop LVDS receivers...

Slow Control : DESY's proposal

- Add bypass jumpers on PCB



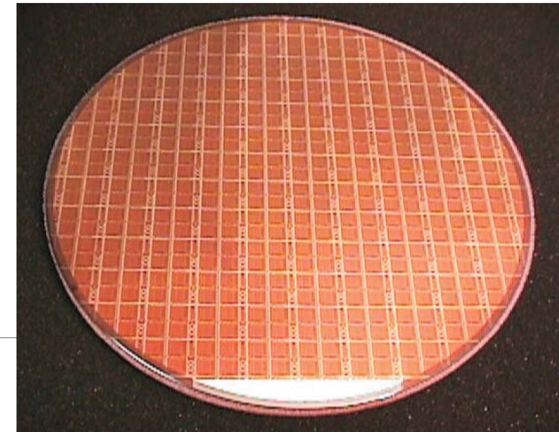
In red, SC flow if chip "N" fails

- Default position is chip "N" reads chip "N-1"
- If Chip N fails :
  - Switch N removed
  - Switch N+1 → in position to read chip "N-1"

Multi Project Run vs Dedicated Run

Omega

- HARDROC2: will be submitted in june 08 (MPW run)
- **MPW: 1k€/mm²** => Hardroc= **25 k€**
  - 25 dies delivered in September 08, to be packaged
  - About 300 dies available (no garanty): 100 euros/die + packaging
  - Price : **25 k€ + 100 € * nb_chips**



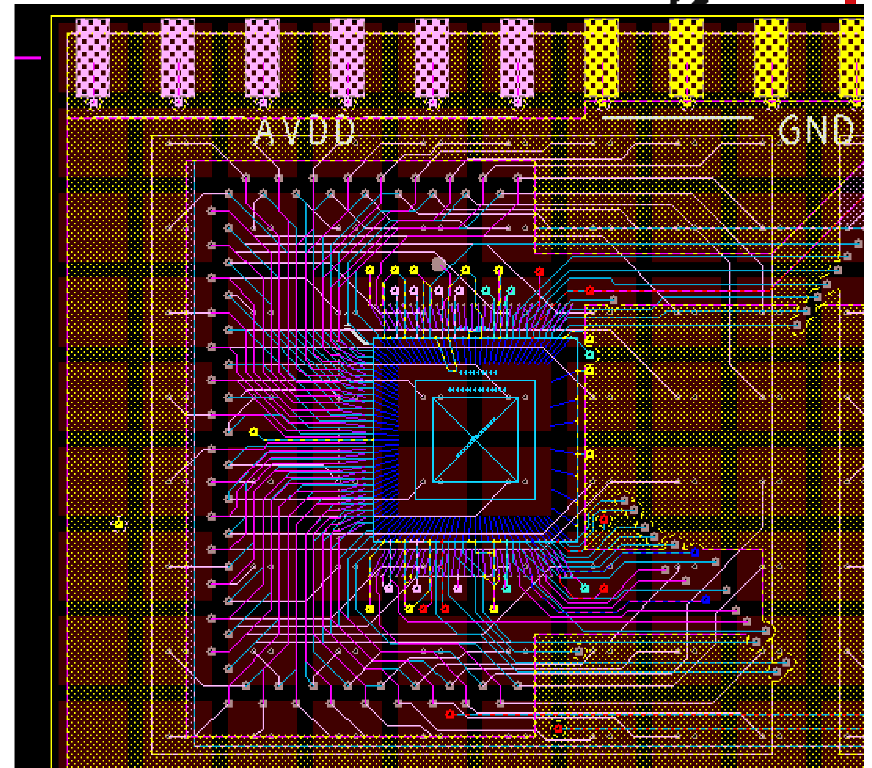
- **Engineering run:**
  - Wafer 8'' Available area=23 000 mm²
  - 1 reticle=20x20 mm²=400 mm²
  - => 65 reticles/wafer
  - 16 chips (25 mm²) / reticle => 1000 Hardroc/wafer
  - Cost : **150 k€ (masks) + 5k€/wafer**
  - Price : **150 k€ + 5 € * nb_chips**
  - **valuable for more than 1250 chips**

Tentative schedule

- June 08 : submission of HaRDROC2 and SPIROC2
- Sept 08 : chips in hand and for standalone tests
- March 09 : production run with HaRDROC2, SPIROC2 and (challenging) SKIROC2 (64ch)
- June 09 chips available for ASUs

PCB developments

- ECAL : ASU prototype
  - FEV5 expected soon
  - Uses 4 HArdroc chips
  - Can test stitching
  - Connects to proto DIF

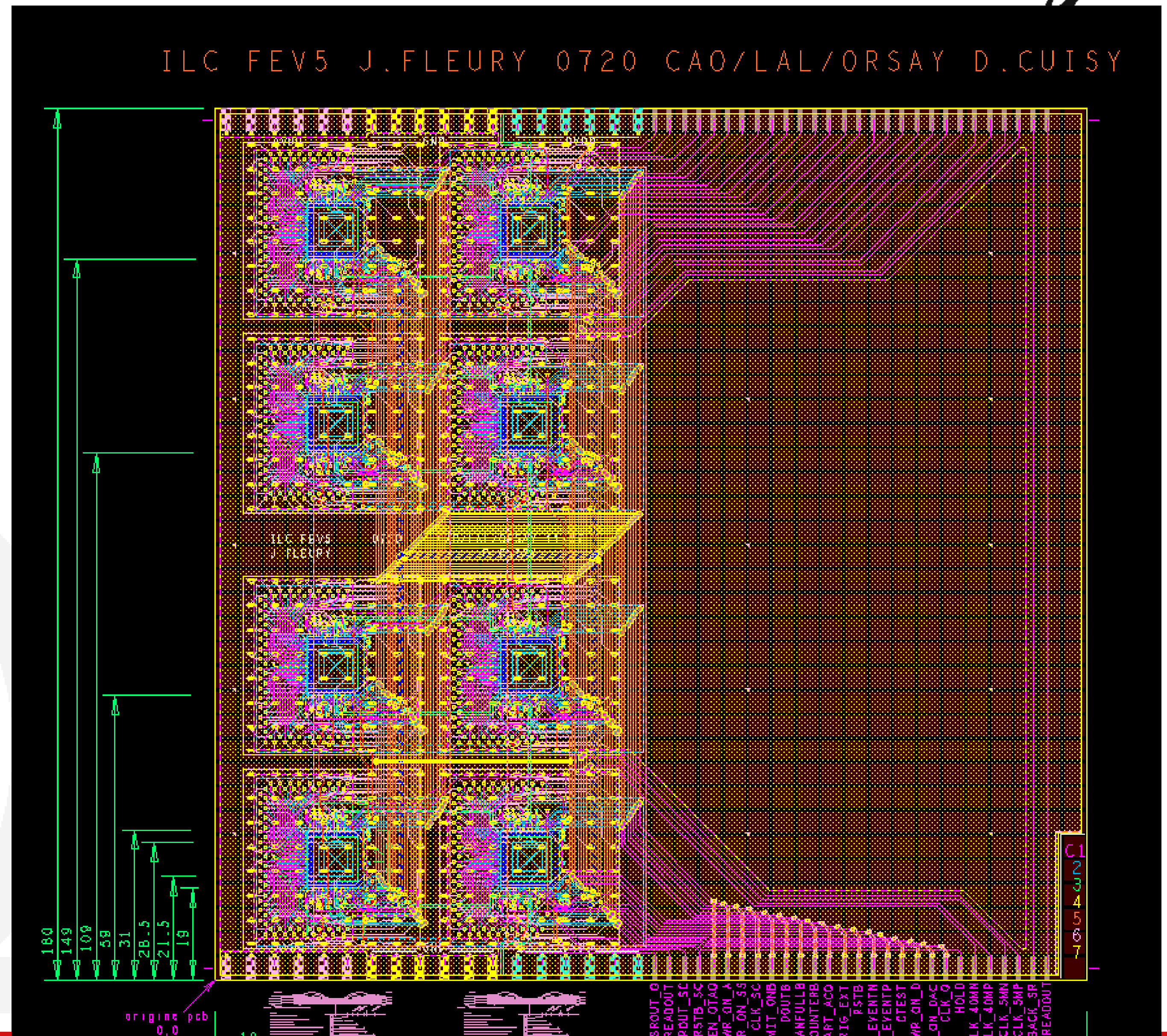


- AHCAL : HBU
  - First prototype with Spiroc

- DHCAL : m2 prototype boards
  - For RPCs and µMEGAS : different sizes and connections

Layout : general

- Very dense
- Chips inside
- Daisy chain connection
- 1 mm thick



Chip Embedding + PCB Pile-up

Pile-up	
TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7

FR4TG
PREG
C1 100u
C2C3 150u
C4C5 100u
C6C7 100u
C8
250u
150u
sf
df
df
df
sf
100u
100u
150u
100u
TOTAL= 900u + Cu 2x40u = ∿980u fini
v12c7c8
v12c6c7
v20c1c7
mm 2.5 | 1 | 1 | 1.5 | 0.5 | 1.5 |

INFOS
finition NiAu chimique
longueur pads de 1.5mm a 1.76mm
largeur pads = 120u
iso mini pads = 110u
epaisseur Cu couches externes 9u fini ∿ 40u
epaisseur Cu couche C2 17.5u fini ∿ 24u
epaisseur Cu couches internes 17.5u
epaisseur collage puce de 30 a 50u

5 puce →
7 cavite →
9 →
pads couche 2
12 →
13 →
pads couche TOP
16 →

ECAL SLAB Interconnect

DAQ Architecture – Overall view

~150 VFE ASICs on each side of SLAB

ODR

LDA

LDA

LDA

LDA

DIF

DIF

DIF

DIF

DIF

DIF

SLAB

SLAB

SLAB

SLAB

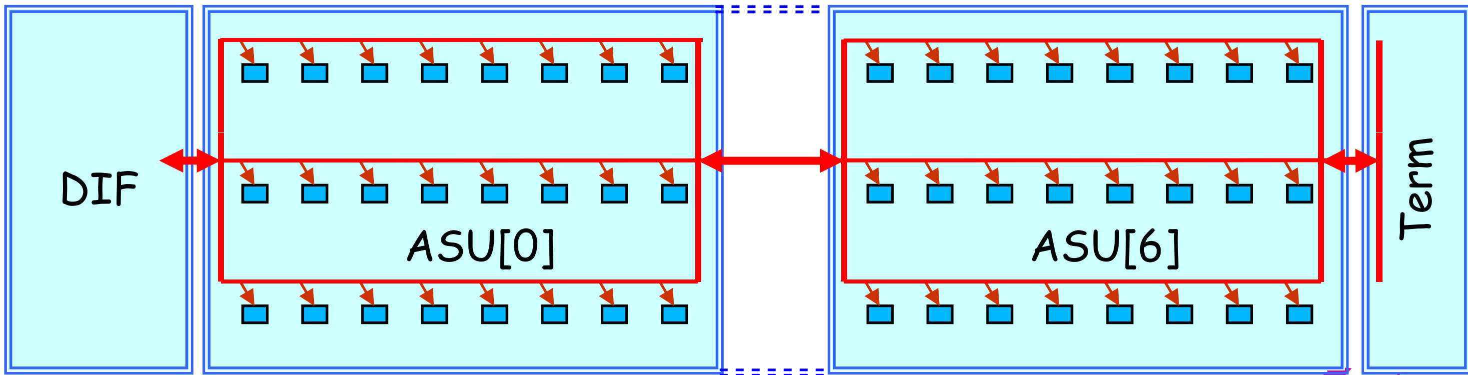
SLAB

SLAB

ECAL SLAB Interconnect

DIF – ASU – ASU -,,,- Terminator

6 or 7 ASUs on each side of a SLAB



7 or 8 interconnections – each of many ways

Termination of LVDS lines & loop back R/O Token

?? Integrate on all ASUs as option

ECAL SLAB Interconnect – Why Multi-Rows?

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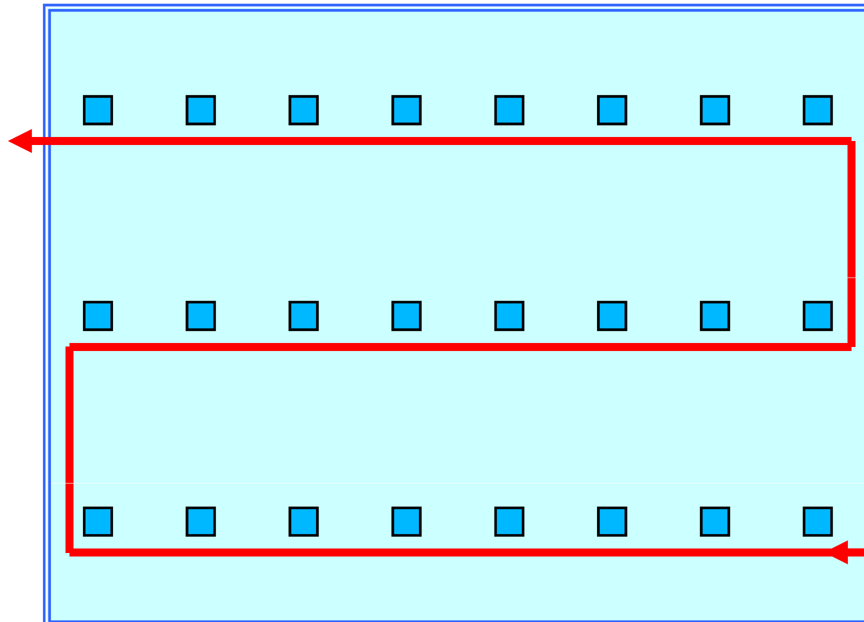
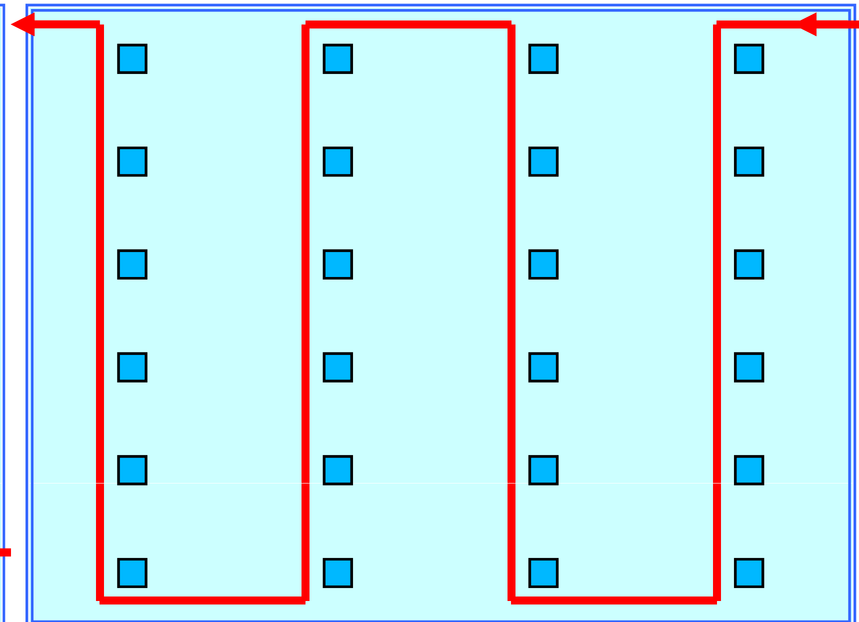
How to read them out – **single trace**

3 rows of VFEs



6 rows of VFEs



Per ASU: L ~ 850mm, C ~ 85pF	Per ASU: L ~ 900mm, C ~ 90pF
Per Slab of 7 ASUs: L ~ 6m, C ~ 600pF	Per Slab of 7 ASUs: L ~ 6.3m, C ~ 630pF

Do these look **BIG ??** - we'll look at that later

ECAL SLAB Interconnect – Why Multi-Rows?

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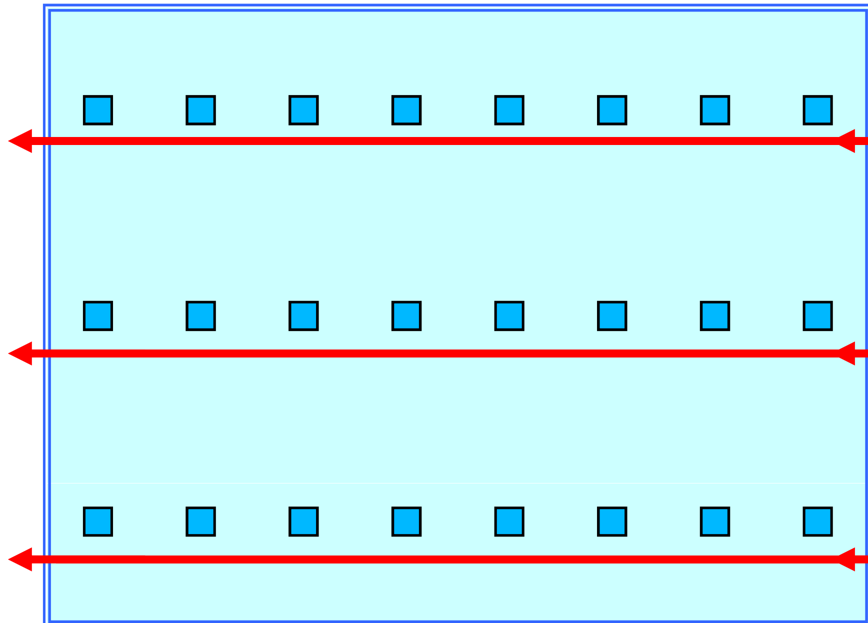
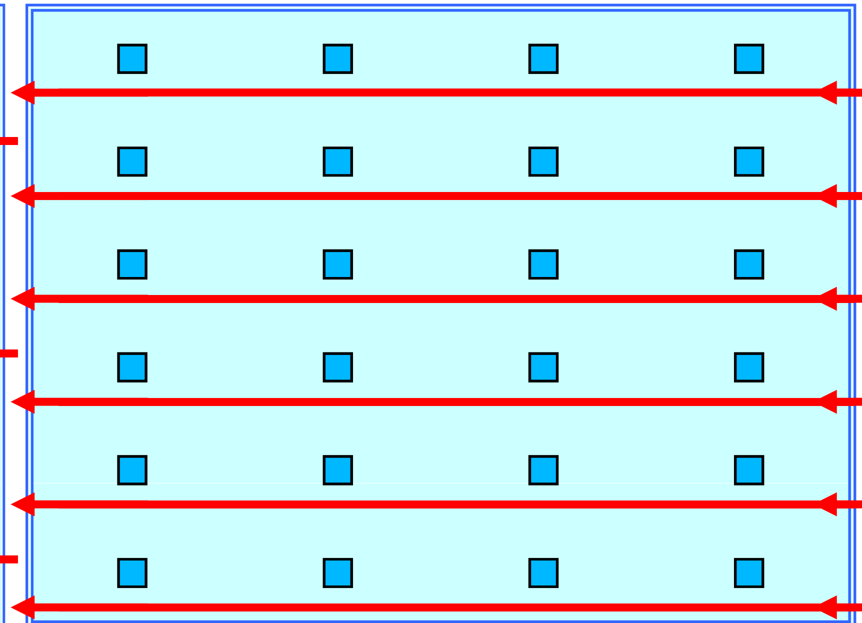
How to read them out – **multiple trace**

3 rows of VFEs, 3 traces



6 rows of VFEs, 6 traces



Per ASU: L = 240mm, C ~ 24pF

Per Slab of 7 ASUs:
Per trace: L ~ 1.7m, C ~ 170pF

Per ASU: L = 240mm, C ~ 24pF

Per Slab of 7 ASUs:
Per trace: L ~ 1.7m, C ~ 170pF

How much difference will this make?

ECAL SLAB Interconnect - using FFCs

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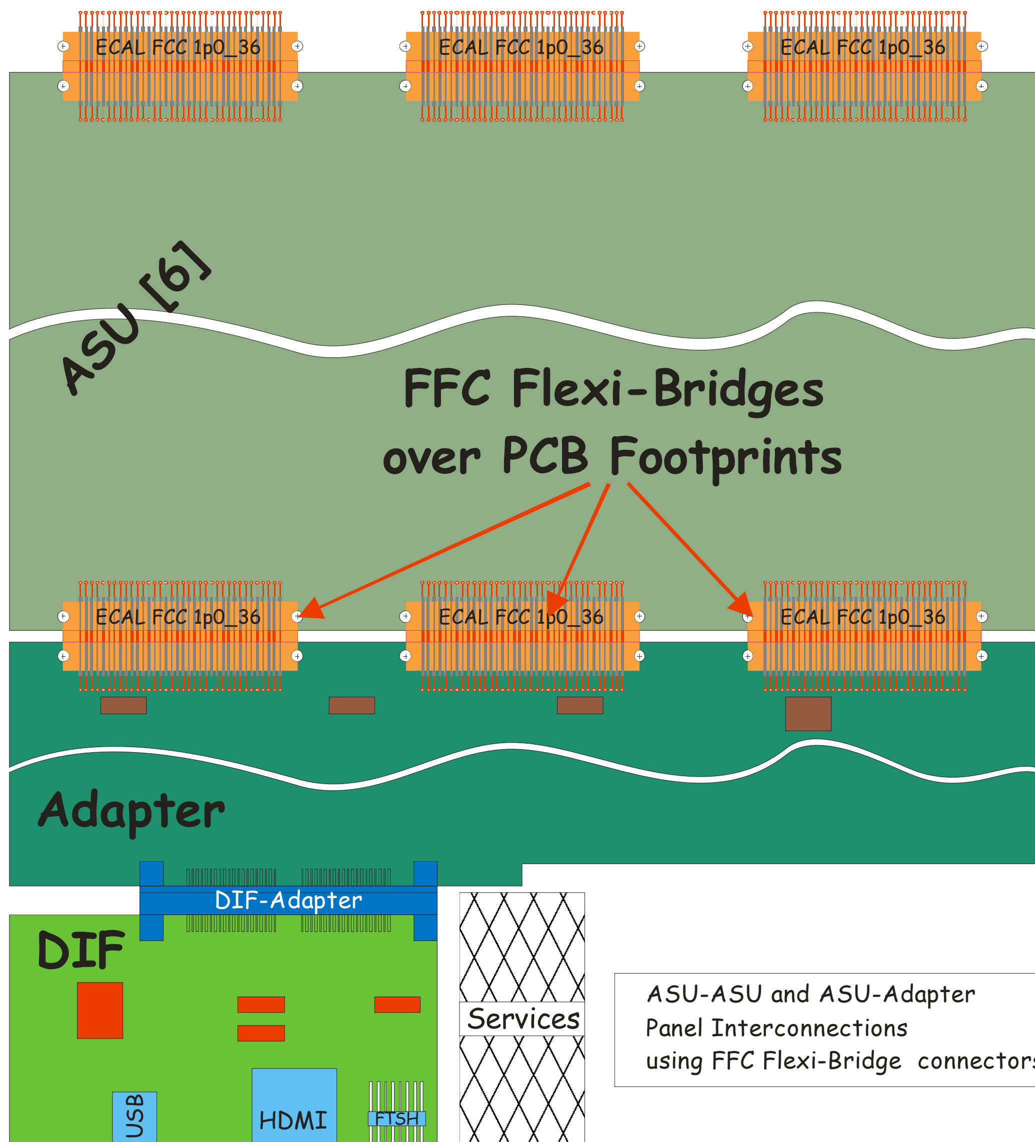
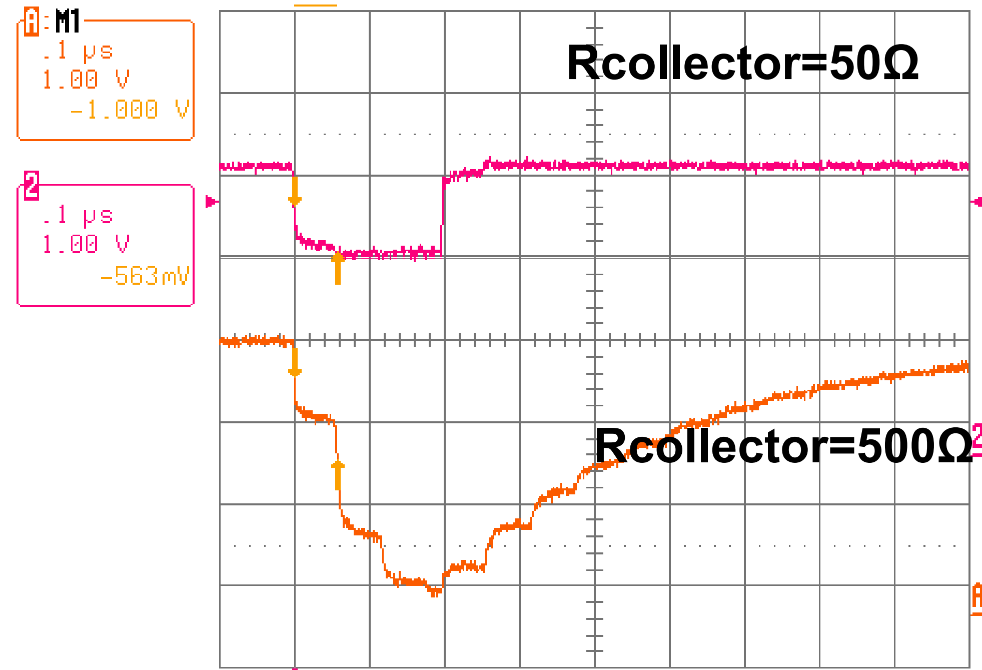
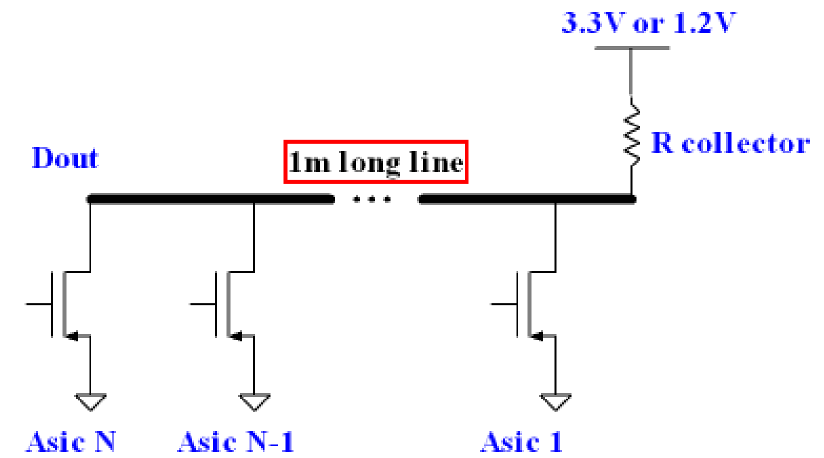


ASU-ASU and ASU-Adapter
Panel Interconnections
using FFC Flexi-Bridge connectors

Open collector signals after 1m long line

- 5 m data line / slab -> 500 pF
- Multiple reflections when unterminated : 1 MHz max
- 50 ohm termination => clean, 10 MHz R/O possible, power dissipation 10 mW/slab in DIF
- Need to change driver transistor size in ASICs



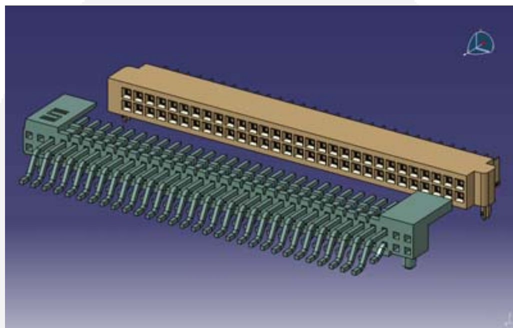


DIF issues

- Common connector specification
- 90 pins
- Thanks to DIF task force

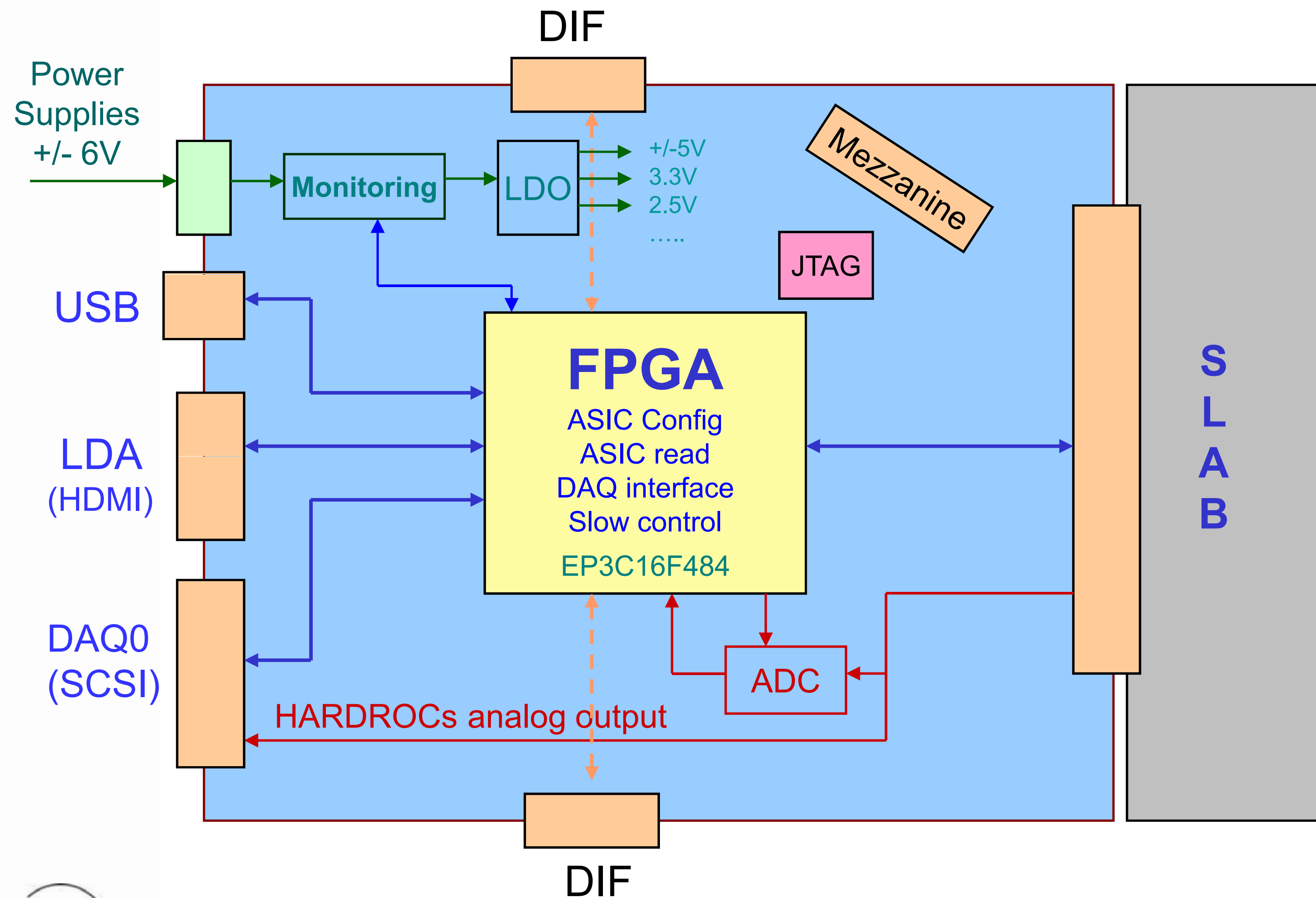
	N pins
Analog	3
User Single Ended	22
Controls Single Ended	5
Digital Readout	12
Power pulsing controls	5
LVDS signals	16
Slow controls signals	8
POWER pins	6
GND	13
TOTAL	**90**

Signal	Pin	Pin	Signal
GND	1	2	GND
MUX3_CSn	3	4	Analog_0
MUX2_CSn	5	6	GND
MUX1_CSn	7	8	Analog_1
spare1	9	10	GND
MUX_ENN	11	12	C_test
MUX_WRN	13	14	GND
spare2	15	16	MUX_A4
en_otaq	17	18	MUX_A3
GND	19	20	MUX_A2
SR_reset	21	22	MUX_A1
hold	23	24	MUX_A0
spare3	25	26	Ramfullext
SR_IN	27	28	Reset_BCID
spare4	29	30	GND
SR_OUT	31	32	Resetn
spare5	33	34	Start_Conv_daqb
SR_clk	35	36	End_Readout
GND	37	38	Start_acq
TransmitOn_3	39	40	RamFull
Pwr_analog	41	42	Dout_3
TransmitOn_2	43	44	GND
Pwr_dac	45	46	Dout_2
Pwr_ss/Pwr_sca	47	48	Start_Readout
GND	49	50	Trig_ext
TransmitOn_1	51	52	Start_Readout_Bypass
Pwr_digital	53	54	Dout_1
TransmitOn_0	55	56	GND
Pwr_adc	57	58	Dout_0
SC_SROUT	59	60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61	62	SC_SRIN
SC_select	63	64	SC_reset
SC_clk	65	66	SC_load
User_LVDS_P	67	68	User_LVDS_N
Trig_Ext_P	69	70	Trig_Ext_N
DVDD	71	72	AVDD
Clk_5MHz_0_P	73	74	Clk_5MHz_0_N
Clk_5MHz_1_P	75	76	Clk_5MHz_1_N
GND	77	78	GND
Clk_40MHz_0_P	79	80	Clk_40MHz_0_N
Clk_40MHz_1_P	81	82	Clk_40MHz_1_N
DVDD	83	84	AVDD
Raz_Chn_P	85	86	Raz_Chn_N
Val_Evt_P	87	88	Val_Evt_N
AVDD	89	90	AVDD

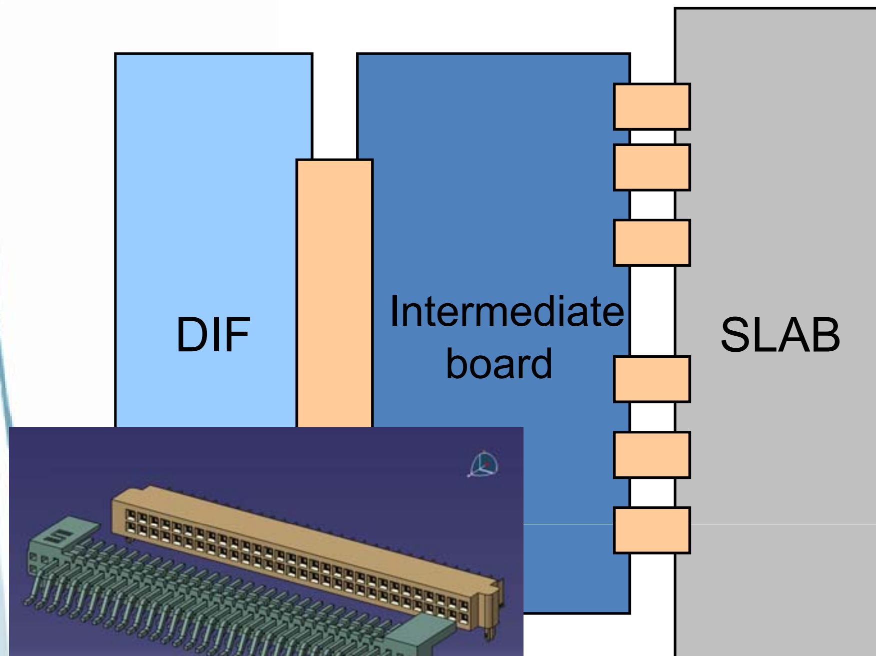


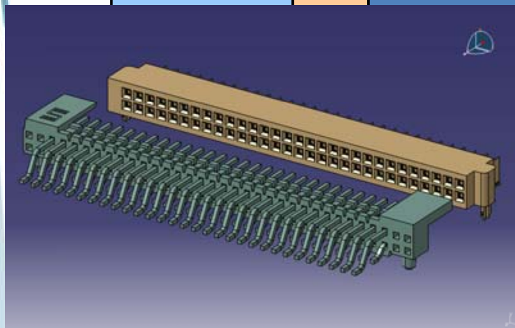
Samtec FSH/ SFMH ?

Architecture of the DIF board



Interface with the SLAB





Samtec FSH/ SFMH ?

Connection with the slab is the same as the one between 2 ASUs.

0 Ω resistor, …

- Use of a small intermediate board, which is specific to the FE ASIC and ASU.
- The DIF can be used :
  - Whatever the FE ASIC.
  - Whatever the slab (RPC, uM)
  - Whatever the slab to slab connection.
- 1rst ASU is the same as the others.

AHCAL Half Sector - Reminder

FEB

AHCAL Slab

6 HBUs in a row

HBU

HCAL Base Unit

typ. 12 x 12 tiles

LDA

CCC

Data

SPIROC

typ. 4 on a HBU

H = 100 cm

B = 74 cm

L = 220 cm

HEB

HCAL Endcap Board

Hosts mezzanine modules:

DIF, CALIB and POWER

HLD

HCAL Layer Distributor

DIF: AHCAL specific part

FEB

Very first idea about a possible setup.

To LDA

DIF

FPGA

AHCAL specific Block

Common Block

Common DIF Signals

?

τ_D

LVDS

Trigger

RW, OE, Strobe

3

D/A

2

VCALIB

Light Cal. Sys., Charge Inject.

8 8

µC or FPGA

?

LVDS

2

TCALIB

2

Power *for CALIB electronics inside detector gap*

CALIB

A/D

9

Temperature monitors

Power *for Temp. mon.*

SiPM Bias

4

to SiPMs *(4 lines per slab)*

Data

Address

µC or FPGA

8 8

Power

POWER *(3.5V, 5V, GND)*

Monitor +ADC

HEB

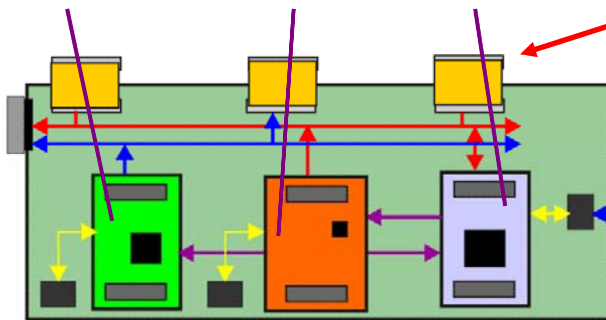
POWER

Slab

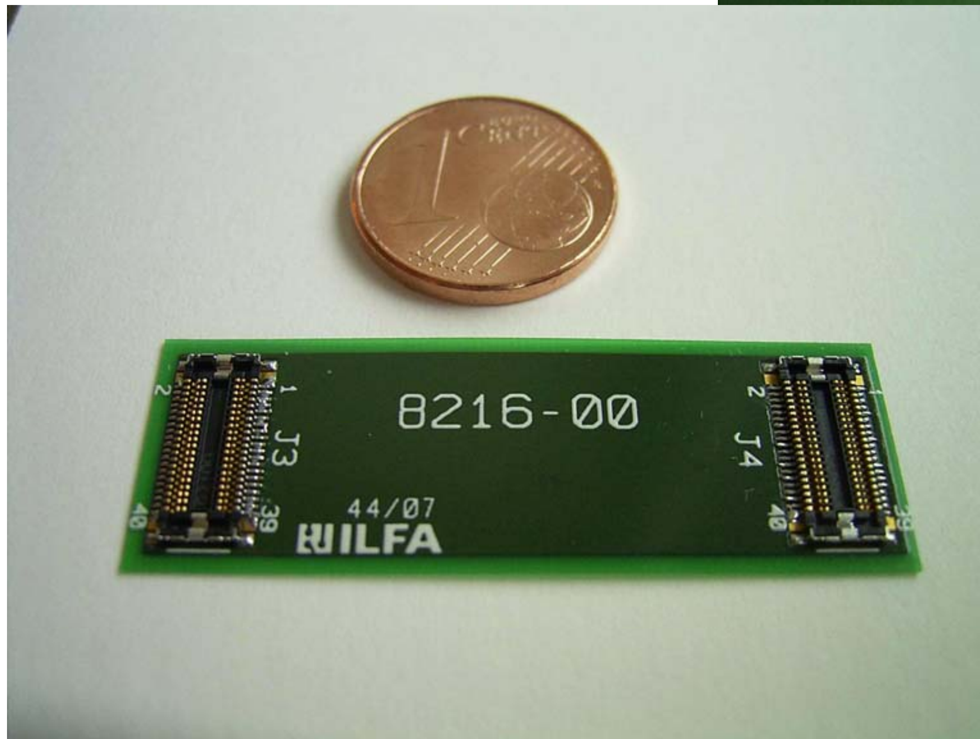
Interconnection

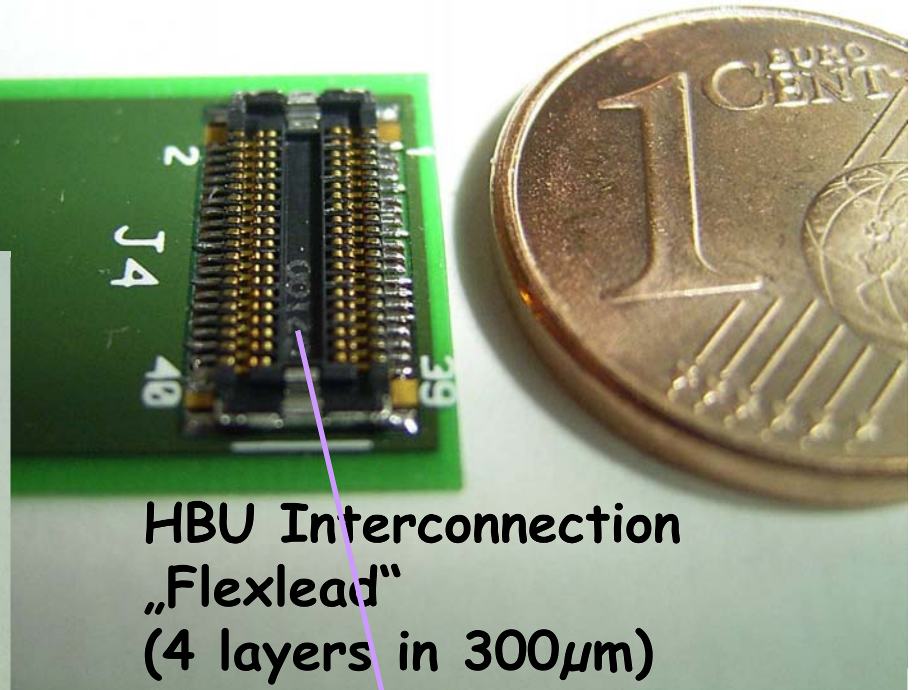
FEB

POWER CALIB DIF



Probably need something more roust here (outside the gap)





HBU Interconnection „Flexlead" (4 layers in 300µm)

Connector stacking height (both parts): 800µm

DAQ architecture

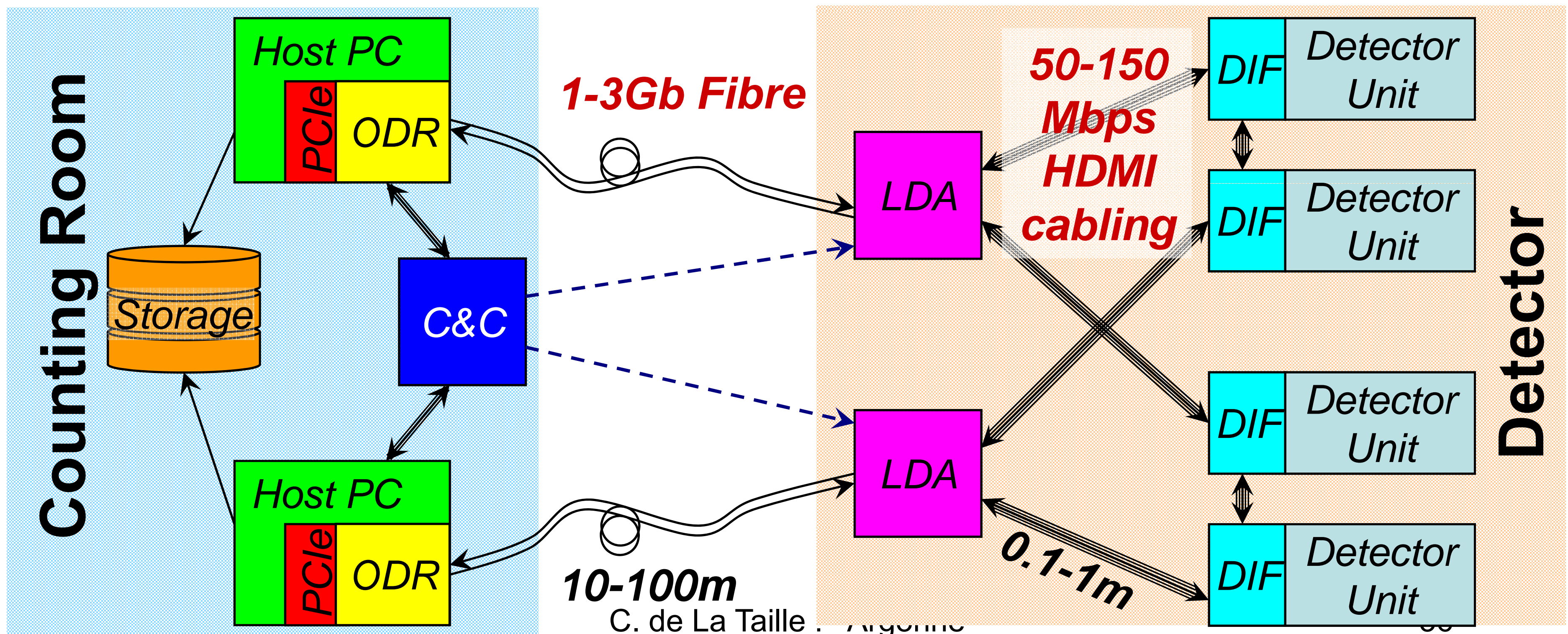
Detector Unit: Sensors & ASICs

DIF: Detector InterFace - connects generic DAQ and services

LDA: Link/Data Aggregator – fanout/in DIFs & drive link to ODR

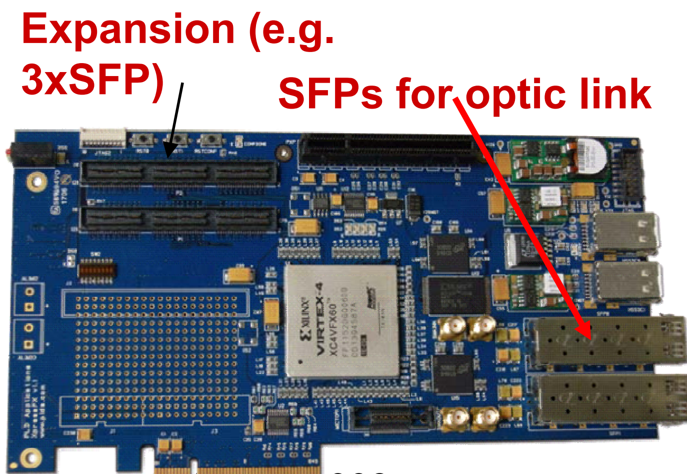
ODR: Off Detector Receiver – PC interface for system.

C&C: Clock & Control: Fanout to ODRs (or LDAs)



Off Detector Receiver (ODR)

- Receives module data from LDA
  - PCI-Express card, hosted in PC.
  - 1-4 links/card (or more), 1-2 cards/PC
  - Buffers and transfers to store as fast as possible
- Sends controls and config to LDA for distribution to DIFs
- Performance studies & optimisation on-going



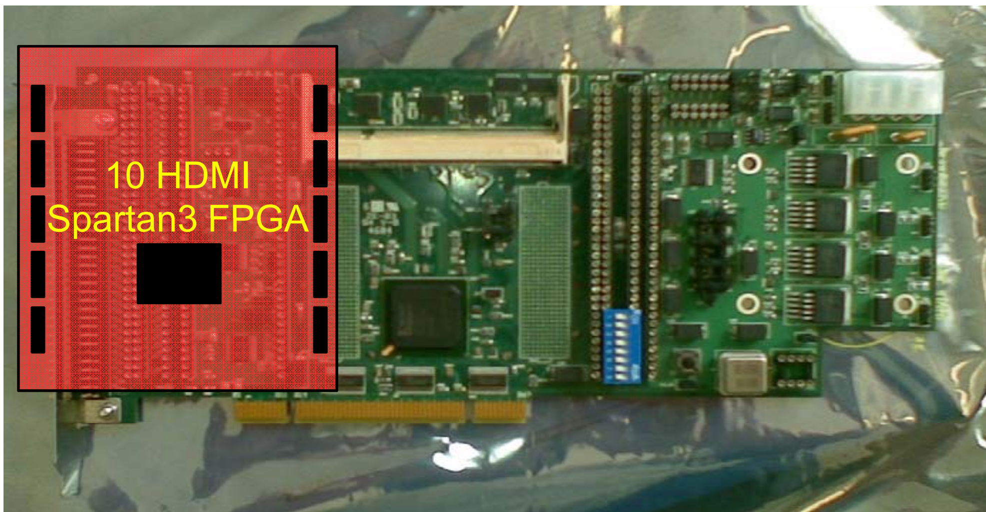
Hardware:

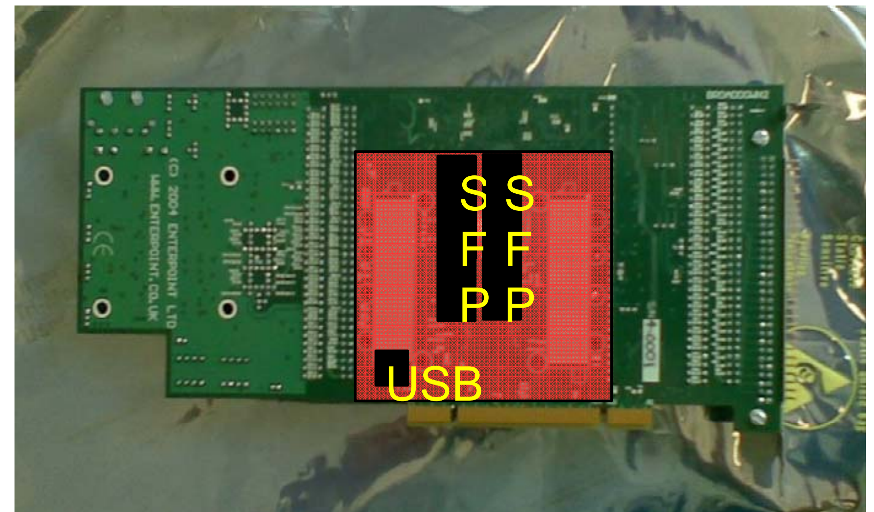
- Using commercial FPGA dev-board:
  - PLDA XPressFX100
  - Xilinx Virtex 4, 8xPCIe, 2x SFP (3 more with expansion board)

Link Data Aggregator (LDA)

Hardware:

- PCBs designed and get customized in 1week time by Enterpoint
- Carrier BD2 board likely to be constrained to at least a Spartan3 2000 model
- Gigabit links as shown below, 1 Ethernet and a TI TLK chipset
- USB used as a testbench interface when debugging





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Link Data Aggregator (LDA)

Firmware:

- Ethernet interface based on Xilinx IP cores
- DIF interface based on custom SERDES with state machines for link control. Self contained, with a design for the DIF partner SERDES as well
- Possible to reuse parts from previous Virtex4 network tests
- No work done on TLK interface as of yet

1 LDA can serve 10 DIFS

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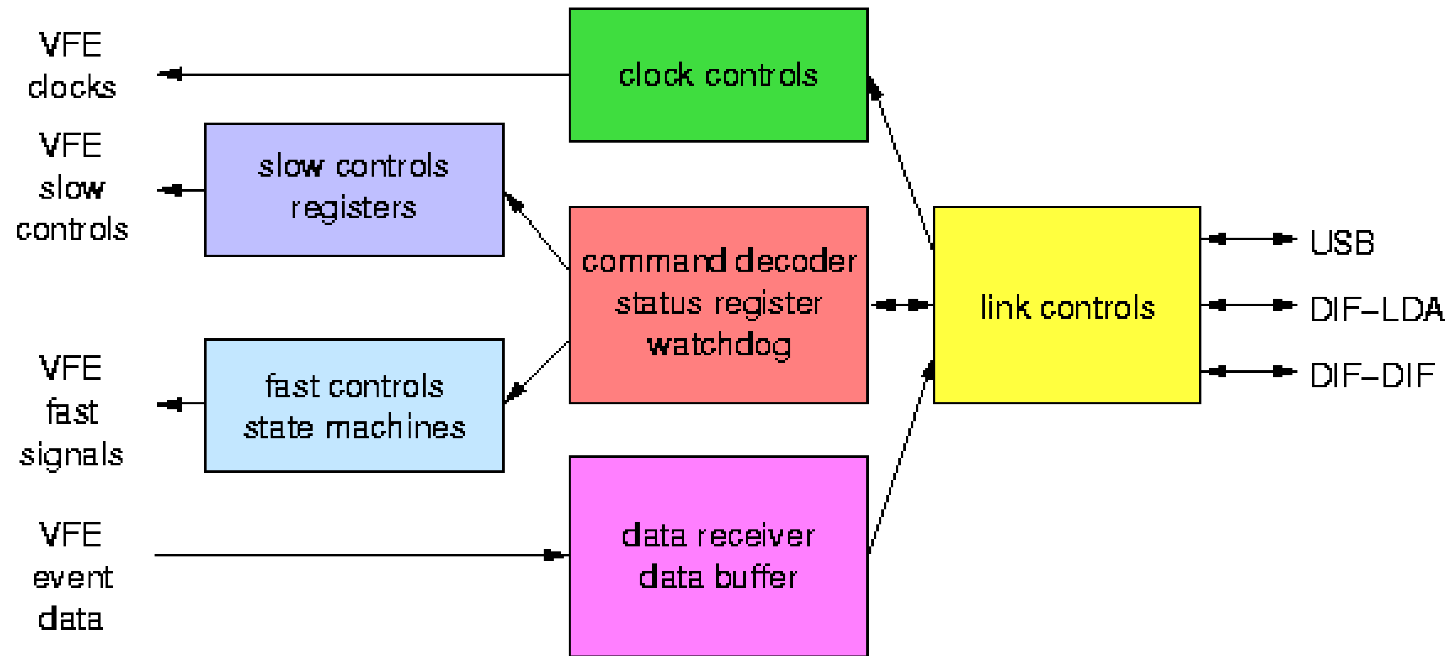
Detector Interface (DIF) status



- keep DIF simple hence predictable (no local 'memory management', for example)
- DIF proto: large Xilinx FPGA, to be slimmed down for final DIF
- design 'frozen' (but not too cold), board layout well under way

Power supplies

- A very critical issue !!!
- Power supplies won't be dimensionned for continuous operation, but for 1/100 of the load.
- Need local storage (capacitors, even a battery!) on power board and regulators to accomodate large voltage swing
- Simple calculation (ECAL)
  - Slab = 24 000 channels
  - 1 mA/channel unpulsed => 24 A/slab
  - With a 24 000µF capacitor dV/dt = 1V/ms => acceptable

Done and to do list

- DONE
  - Second generation ASICs prototypes
  - Auto-trigger
  - Daisy-chain readout

- TO BE DONE :
  - PCB stitching (in progress)
  - Tests of bonding chip on board for ECAL (in progress)
  - DIF prototypes (in progress)
  - Tests of power budget with existing chips and boards
  - Tests of power pulsing with Imad's boards
  - Integration issues (in progress)
  - Design of Power distribution (no one' s looking)
  - HV distribution and robustness
  - Testbeam with 2nd generation detectors
  - MEASUREMENTS, MEASUREMENTS, MEASUREMENTS