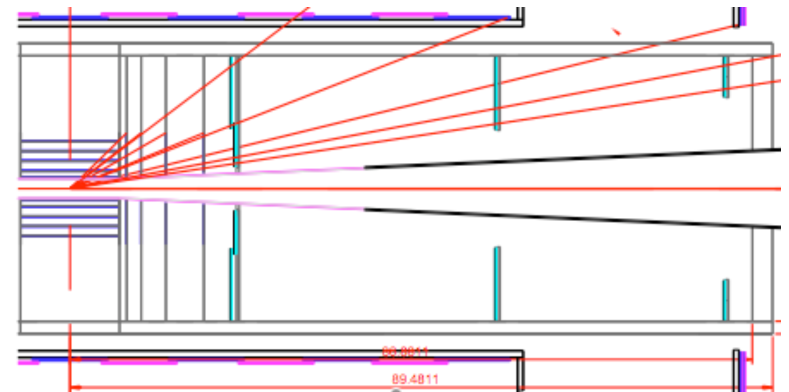
Vertex Detector

- SiD Vertex Concept
  - High magnetic field allows for small inner radius for the inner layer
  - Barrel and disk system
    - Provides good forward tracking
    - Always at least one barrel hit/track
    - Unique to SiD
  - Integrated mechanical design with tracker



- But we don't
  - Understand optimization of the disks
  - Have functional pattern recognition or physics simulation
  - Understand power and interconnection issues
- We do want to preserve technology options for the sensors, which limits detail in a final design

Vertex Subsystem

VTX Groups
- SLAC
- FNAL
- UK (Bristol, Oxford, RAL)
- MPI
- Prague
- Oregon

Coverage of some areas is spotty because
- – Sensor R&D groups tend to focus on detector technology rather than the detector concept
- – Tools are not available
- – Manpower is not available
- – Funding is not available

- Add or direct effort into more experiment-specific or generic (non-sexy) problems
- While keeping the R&D work active and well-supported

Vertex System Design Issues

- Mechanical Design
  - Series of meetings had been running organized by Bill and Joel.
  - Barrel geometry is specified
  - Disk design is still at an early stage
    - Mass constraints
    - Power constraints
  - Conceptual design for CF support cylinder
    - Hope to build a prototype at FNAL
  - Many mechanical issues depend on sensor technology, electronics design - these have to wait.
- There is a solid base overall mechanical design which can accommodate various sensor and readout options.
- Joel will discuss this in more detail

Summary of Hardware Efforts

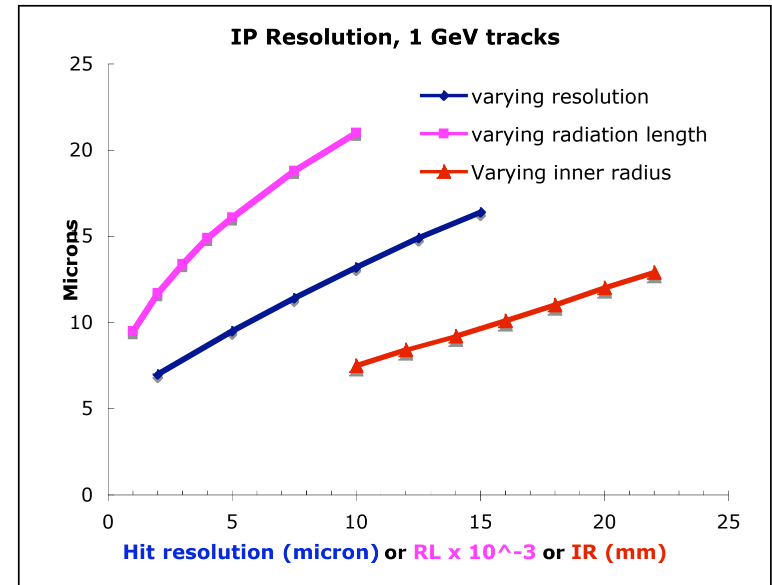
- Sensor R&D
  - UK - LCFI
    - CPCCD , ISIS CCD
  - FNAL
    - 3D Electronics, SOI
  - MPI, Prague
    - DEPFET detectors
  - Oregon
    - CMOS MAPS

- Other R&D
  - UK
    - Support structures
    - Mechanical
  - FNAL
    - Mechanical Design
    - Serial Power
    - Thinning
  - MPI
    - Thinning and support
  - SLAC
    - Electronic system integration

Not covered - other powering schemes, pulsed power studies, interconnections
Understanding of power => understanding of mass distribution

Basic Parameters

- IP resolution will be determined by mass, inner radius, and pixel size. More complex questions include:
  - How resolution is degraded with angle in the forward direction
  - What are the pattern recognition constraints?
- Optimizations
  - Mix in decreased time resolution technologies in outer layers
  - Vertex pixel size optimization (power/pixel size tradeoffs)

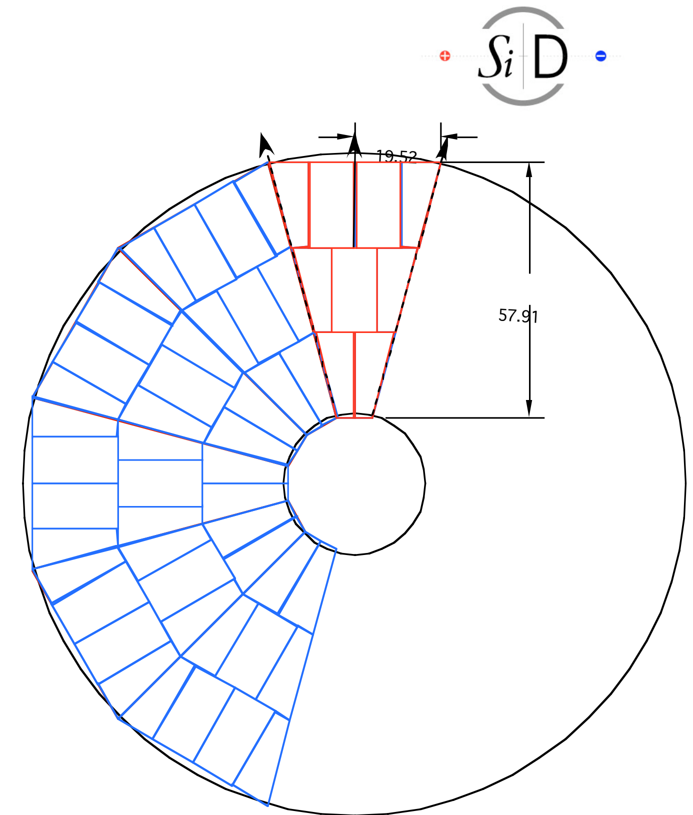


Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resoluton
- 1.4 cm inner radius

Varying each parameter

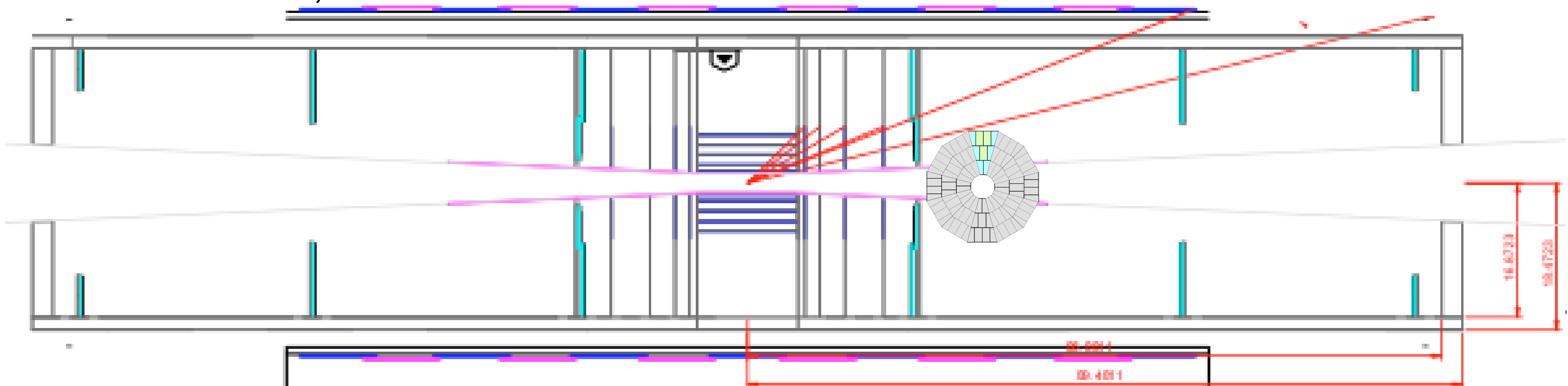
Disks

- Assuming pixels for the forward region
  - What are we asking of the forward disks
    - IP resolution - dominated by barrels
    - Pattern recognition
  - Integration with forward silicon design
    - Determines momentum res., angle measurement
  - Pixel size
    - Maximum size -> minimum power
    - Support and geometry



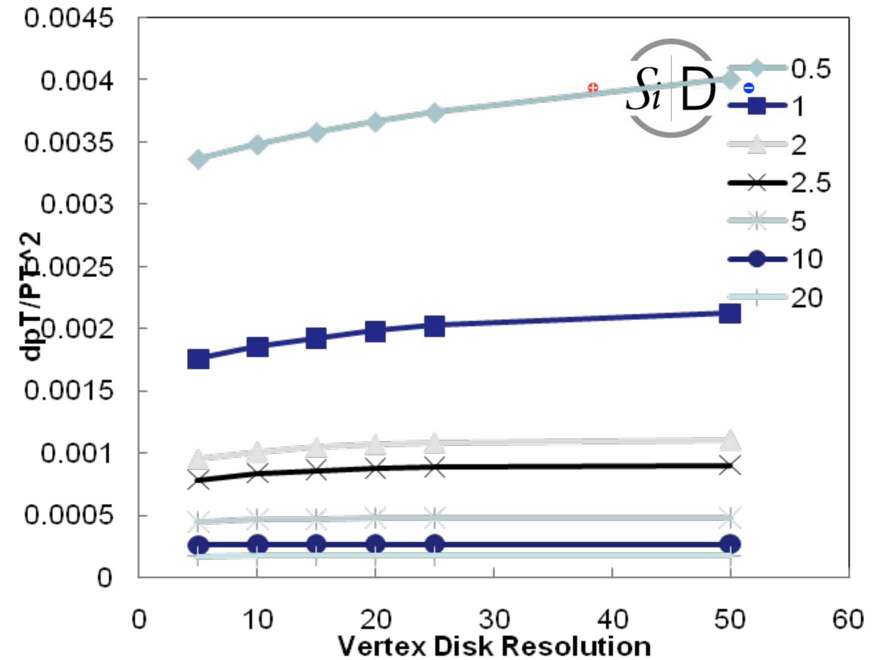
3D DBI-based concept
Chips tiled on 1/2 disk sensor

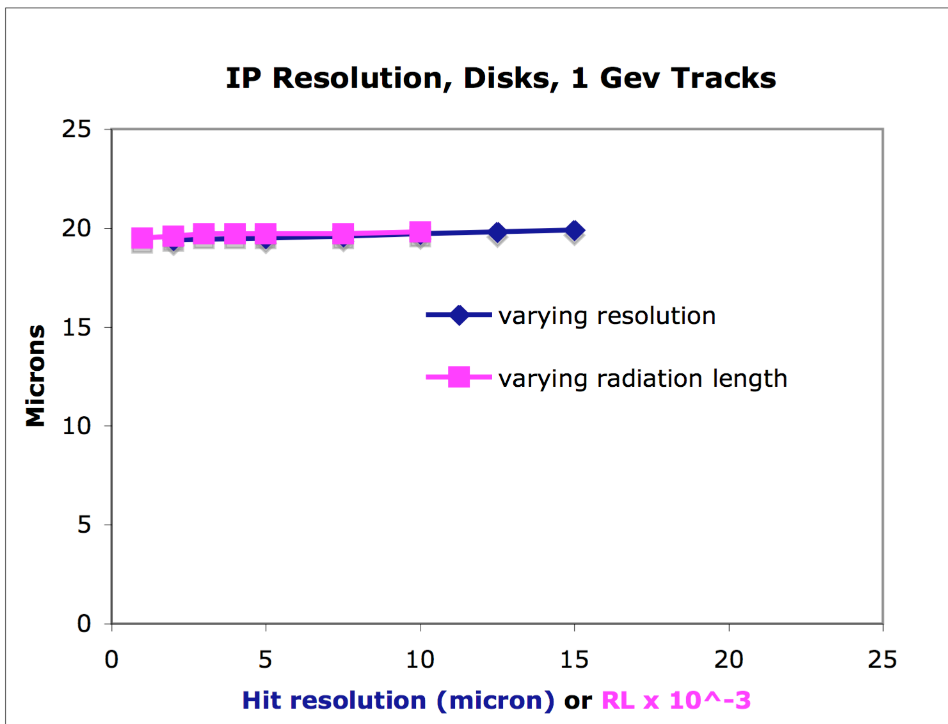
Vertex barrel ~ 150,000 mm^2
Vertex Disks ~ 120,000 mm^2

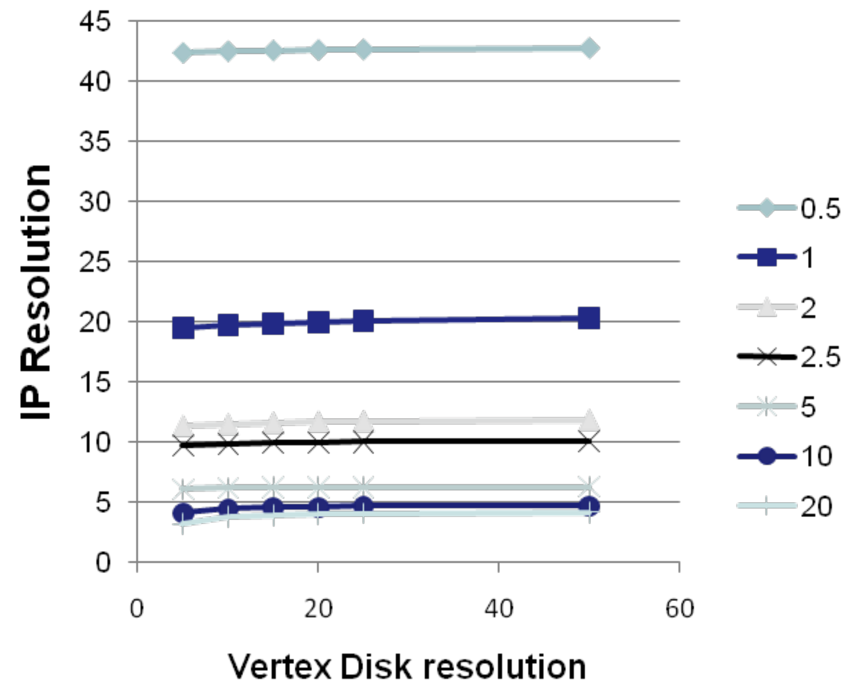


Disk Parametric Study

• Parametric study of momentum and
• Impact parameter resolution as a function of disk spatial resolution
• Based on this there is no way to specify pixel size in disks
• Different if barrel hit is missed or degraded







Cabling and Interconnect

- Power delivery design
  - Serial power / DC-DC conversion / Capacitive switching
  - Controls
  - Regulation locations, number of cables to outside
  - Division of modules?
- Cable routing. Along beam pipe or along support cylinder
- Optical or electrical interconnect
  - power required, location
- Sensor/cable interface design.
- Lorentz forces.
- Pulsed power R&D –This an important aspect of any ILC –based electronics system and needs to be studied.

Data Load

SiD

bits/hit		30		Rolling Shutter			
				0.001	sec/train		

layer	Hits/crossing	hits/train	hits/sec	bits/sec	ladders	bits/sec/Ladder
1	2000	5.64E+06	5.64E+09	1.69E+11	12	1.41E+10
2	1200	3.38E+06	3.38E+09	1.02E+11	12	8.46E+09
3	800	2.26E+06	2.26E+09	6.77E+10	18	3.76E+09
4	500	1.41E+06	1.41E+09	4.23E+10	24	1.76E+09
5	500	1.41E+06	1.41E+09	4.23E+10	30	1.41E+09
Rolling Shutter		1.41E+07	1.41E+10	4.23E+11	96	
Between Trains			7.09E+07	2.13E+09		

Optical or Electrical?

- Optical interconnect generally favored for long lengths, high bit rate.
- Bit rates for the most aggressive scenarios (>10 Gb/sec/ladder) are probably only practical optically
- Difference is not hugh, power is ~5-15 mW/connection x 96 ladders ~ 0.5 - 1.5 W. Significant but sustainable

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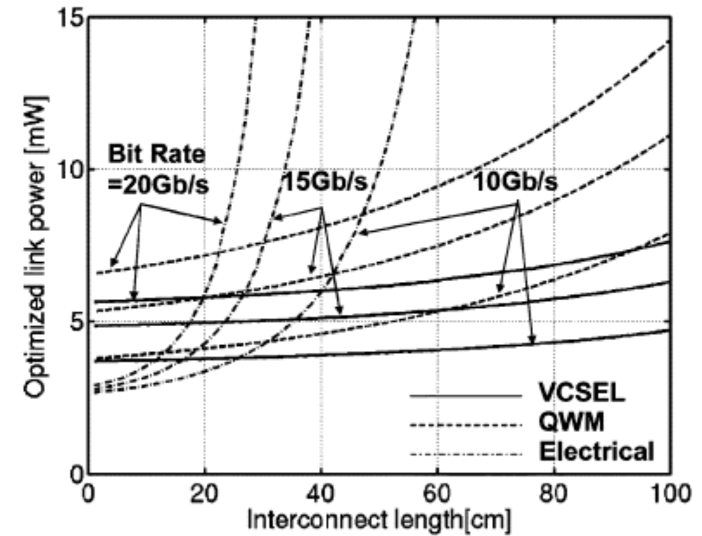


Fig. 5. Power comparison between the electrical and the optical interconnect showing the critical lengths at a detector capacitance of 25 fF.

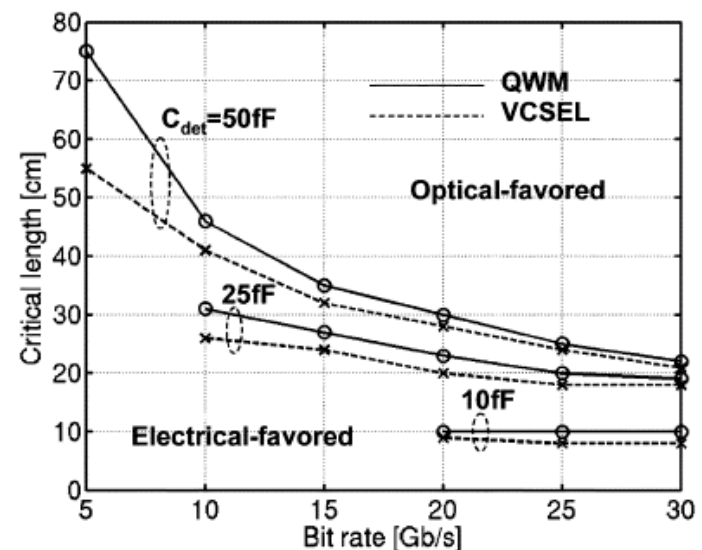


Fig. 6. Critical length in terms of system bit rate for the QWM and the VCSEL transmitter technologies.

Simulation

- What is needed to understand pattern recognition performance?
  - Overall tracking in 3D over full angular range
  - Ability to change geometries and sensor characteristics
  - Ability to add beam background
  - Use Nick Sinev's package for charge deposition where important
- What is needed to understand physics performance?
- Are the standard benchmarks what we want? Would like a mode or modes that allows us to:
  - Cleanly study capabilities
  - Emphasize forward tracking (SiD strength)
  - Incrementally build understanding –adding more complex studies as appropriate
  - Interact efficiently with benchmarking studies groups
- A_{FB} in $e^+e^- \rightarrow bb$, cc, while not on the compulsory list, is an appealing reaction to start with.

Vertex Simulation Goals

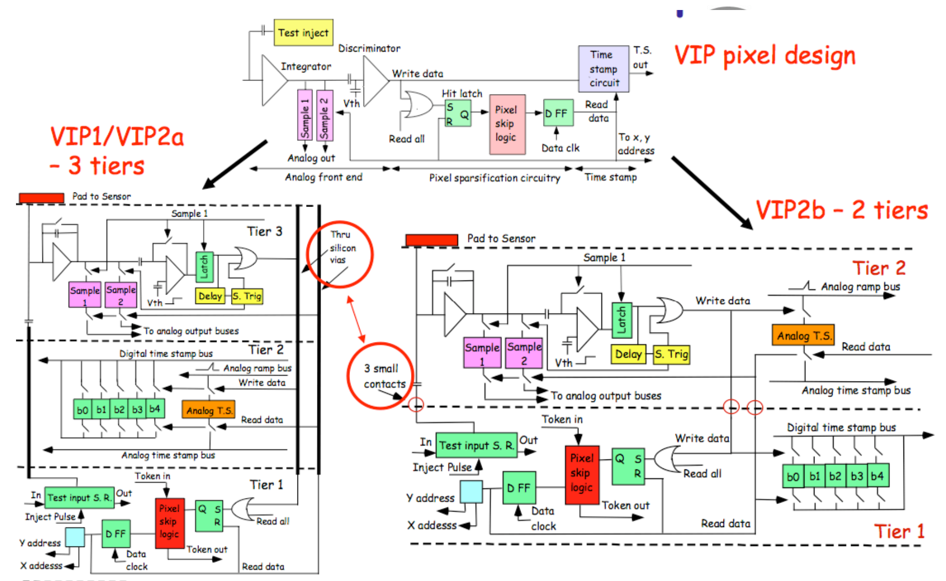
- Understand effects of forward pixel size
- Understand effects of material associated with barrel services
- Understand the requirements for time resolution as a function of barrel layer
- Understand the effects of inclined tracks in the forward direction
- Begin to study the effects of various technological options

- Understand the physics capabilities of the detector.

Conclusions (but not the end)

- Maintain coherence between developing the concept design and R&D efforts
  - Develop physics simulation with pattern recognition
    - Initial aim would be for internal studies
    - Use it to motivate decisions
    - Depends on full simulation package with beam backgrounds, pattern recognition, and charge deposition
  - Increase participation in tracking/vertex meetings
  - Integrate R&D groups in simulation and system design
  - Find groups to study
    - Interconnection
    - Power engineering (serial, DC/DC, pulsed)
- I suggest a 1-2 day vertex design and simulation workshop at a future SiD meeting.

Summary of Fermilab Activities

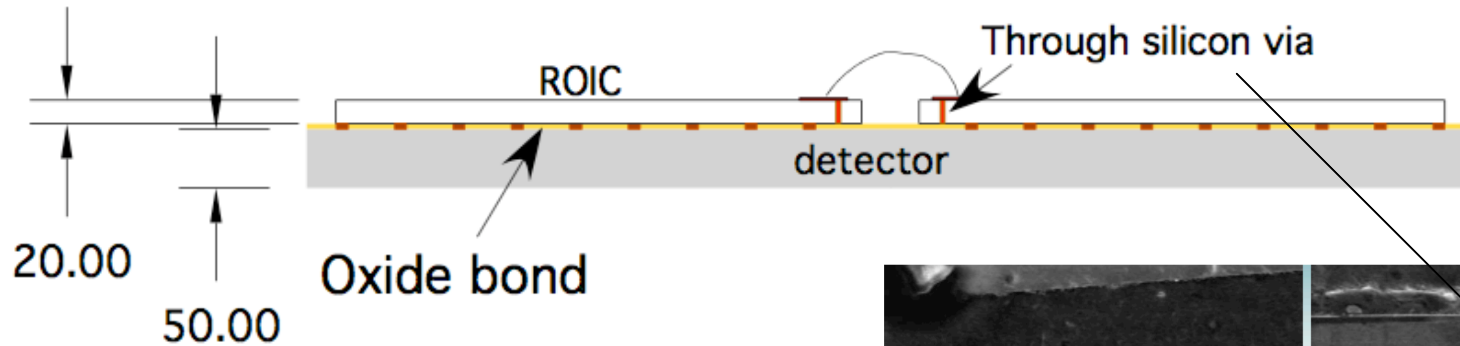


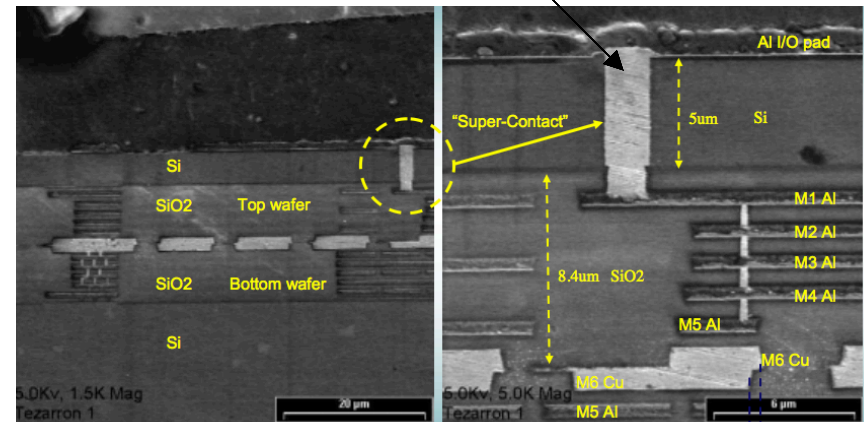
- Completing testing of VIP three tier 3D ILC chip from MIT-LL
  - Received in Dec
    - poor yield, processing isues
  - Overall design looks good (used in INFN CMOS MAPS SDR0 chip)

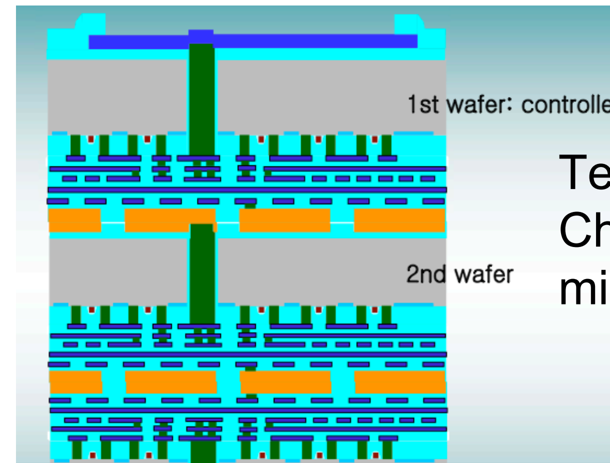
  Details in R. Yarema Ringberg talk:
  http://indico.mppmu.mpg.de/indico/getFile.py/access?contribId=12&sessionId=6&resId=0&materialId=slides&confId=184
- Test MIT-LL sensors thinned to 50 microns using 3M thinning process and laser annealed.
- Test oxide-bonded (Ziptronix DBI) BTeV chips and MIT-LL sensors thinned to 50 microns after bonding.
- Submit VIP-2a to upcoming MIT-LL 3D run
- Modify VIP chip to two tiers in 0.13 micron Chartered process
  - Fermilab will sponsor a Chartered/Tezzaron two tier 3D multiproject run in ~December
- Continue laser annealing and thinning development work

The Chartered/Tezzaron path, which uses exclusively commercial vendors and a high volume CMOS fab seems most promising to us at the moment.

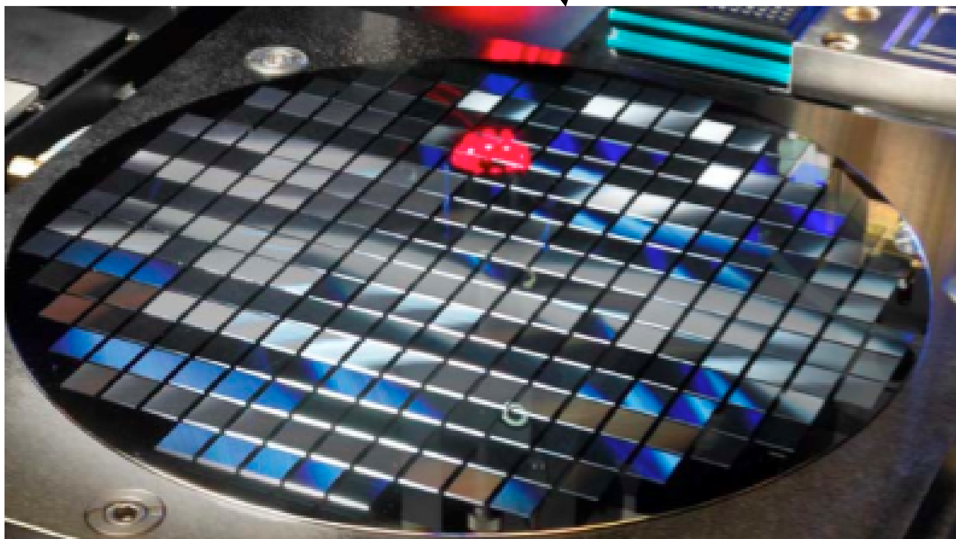
3D Vertex Sensor Concept







Tezzaron/ Chartered 0.13 micron process



Ziptronix DBI process