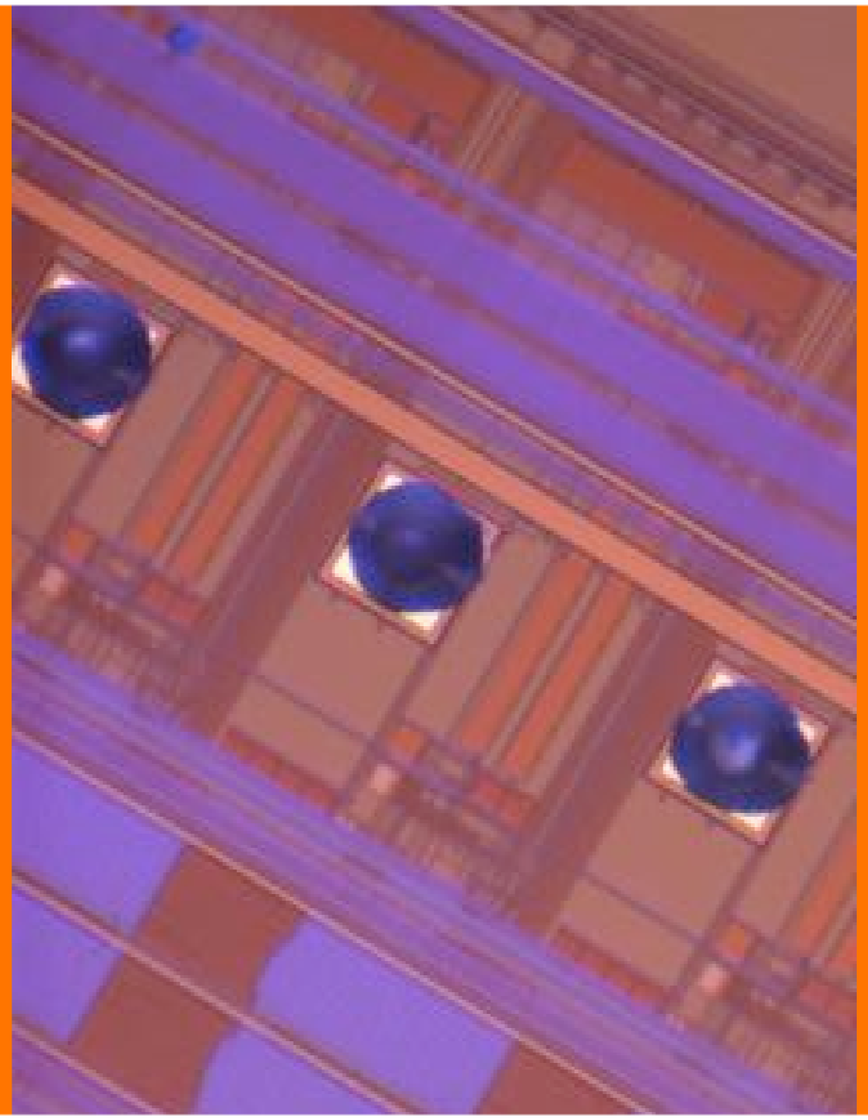
# Status of the KPiX Readout ASIC



*Tim Nelson* - SLAC
David Strom - **U. OREGON**

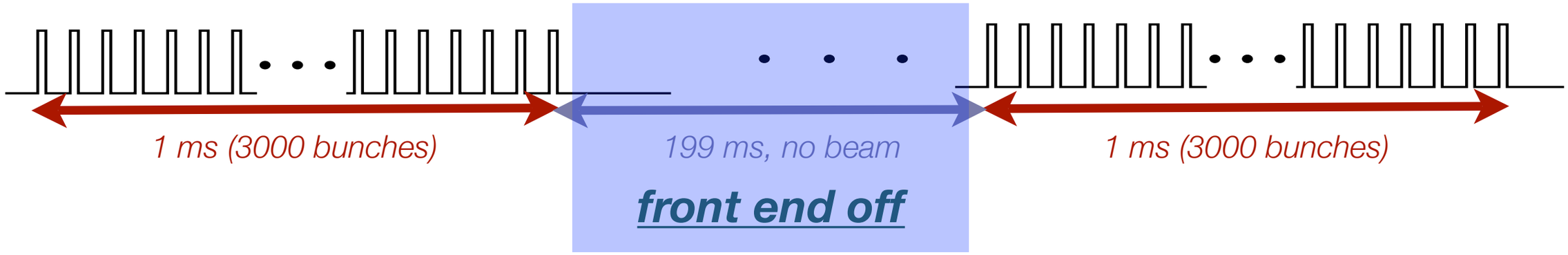
*Si*D Workshop

RAL - April, 14 2008

# My, How You've Grown!

- *Annecy* - ECal Mechanics
- *UT Arlington* - GEM detectors (HCal)
- *BNL* - Electronics
- *UC Davis* - Bump bonding, Cabling
- *Oregon* - Testing, ECal Detectors, Mechanics, Simulation
- *SLAC* - Electronics, Testing, Tracking Detectors, Mechanics, Simulation
- *UW Madison* - RPC detectors (Muon)

# The Hows and Whys of ILC Readout Electronics




- Pulsed operation of front end results in ~100X reduction in dissipated power
  - Minimizes services: *cooling*, cable plant
  - *Many* ILC detector ideas don't work without pulsed power
    - dense Si-W calorimetry
    - low-mass tracking
  - This is a common element of readout efforts for the ILC and critical to feasibility of finely segmented Si-W calorimetry and low-mass silicon tracking

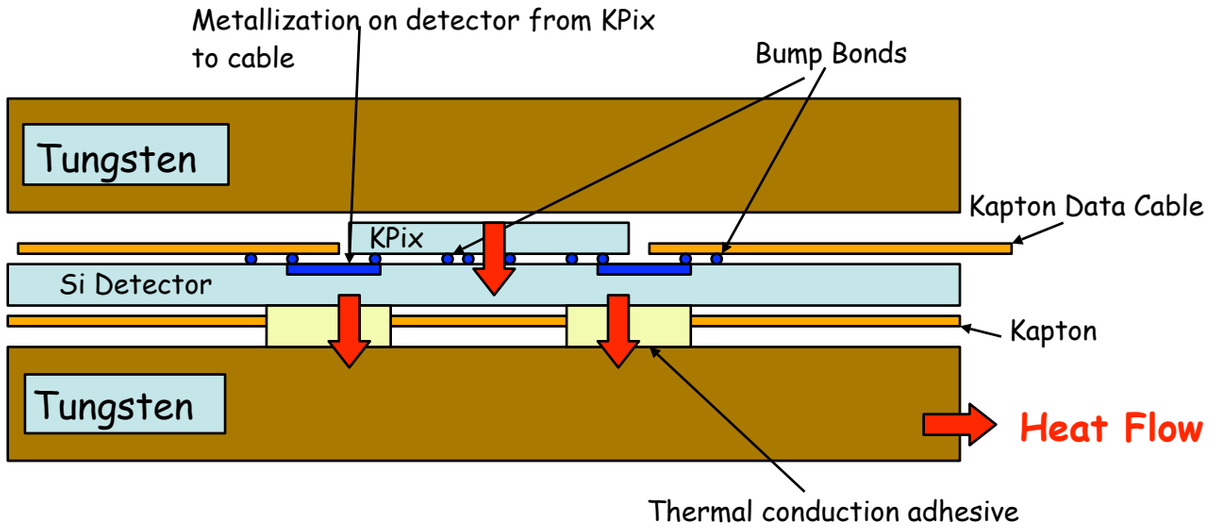
# What is Special About *KPiX*?


***digital section inactive***

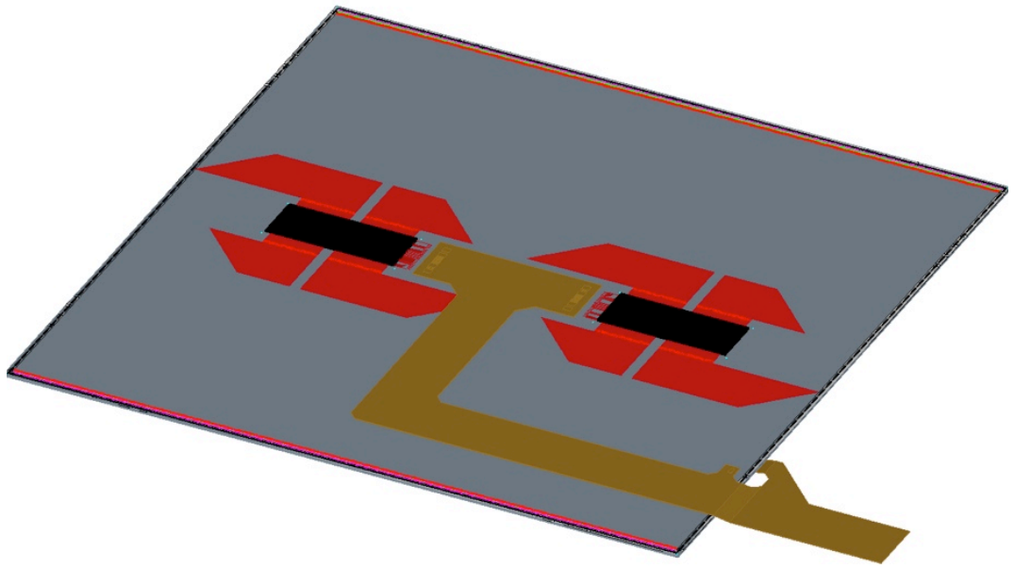
- *KPiX* stores readout in 4 analog buffers
  - hit time-stamped to a single bunch crossing, reducing background susceptibility
  - digitization and readout occurs between bunch trains, minimizing potential for pickup of digital activity on analog front end
  - Allows chip to be more closely coupled to detector electrodes
  - ➡ *Together with an enormous repertoire of built-in capabilities and flexibility of configuration, KPiX may be bump-bonded directly to sensors*

# K*PiX* Impact

- *SiD* ECal
  minimizes gap, and therefore the effective Moliere radius critical for particle flow in jets




- *SiD* Tracker
  minimizes hybrid and cable material critical for minimizing showering inside of ECal, momentum resolution



# KPiX Basics

- 0.25$\mu$m TSMC
- 32×32 array = 1024 channels
- working with 2×32 prototypes, KPiX64

## First versions targeted only at ECal

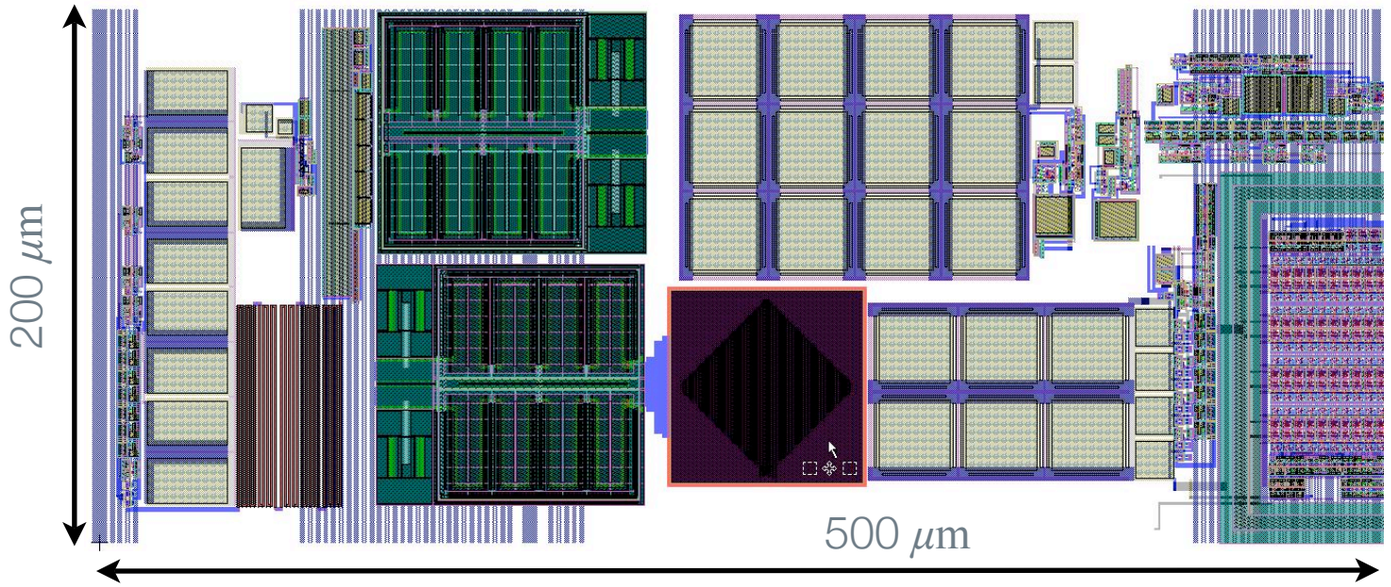
- automatic range switching for large charge depositions in ECal
- bias current servo for DC coupled sensors
- built-in calibration

## Other applications demand additions

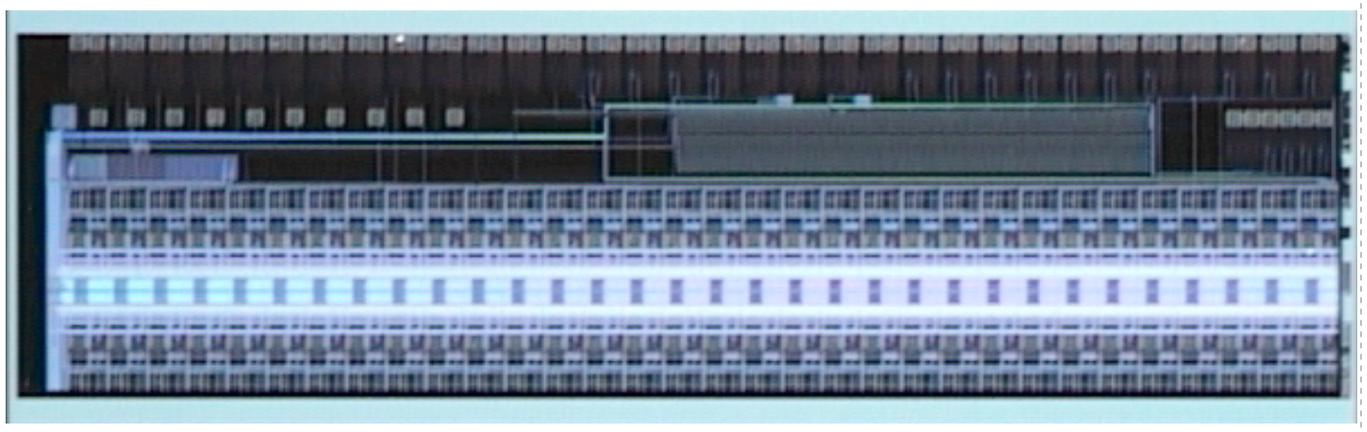
- Nearest neighbor logic, high-gain feedback capacitor for tracker
- External trigger for test beam
- Polarity selection (GEM readout)

*All these features tested and working*

a single cell of KPiX

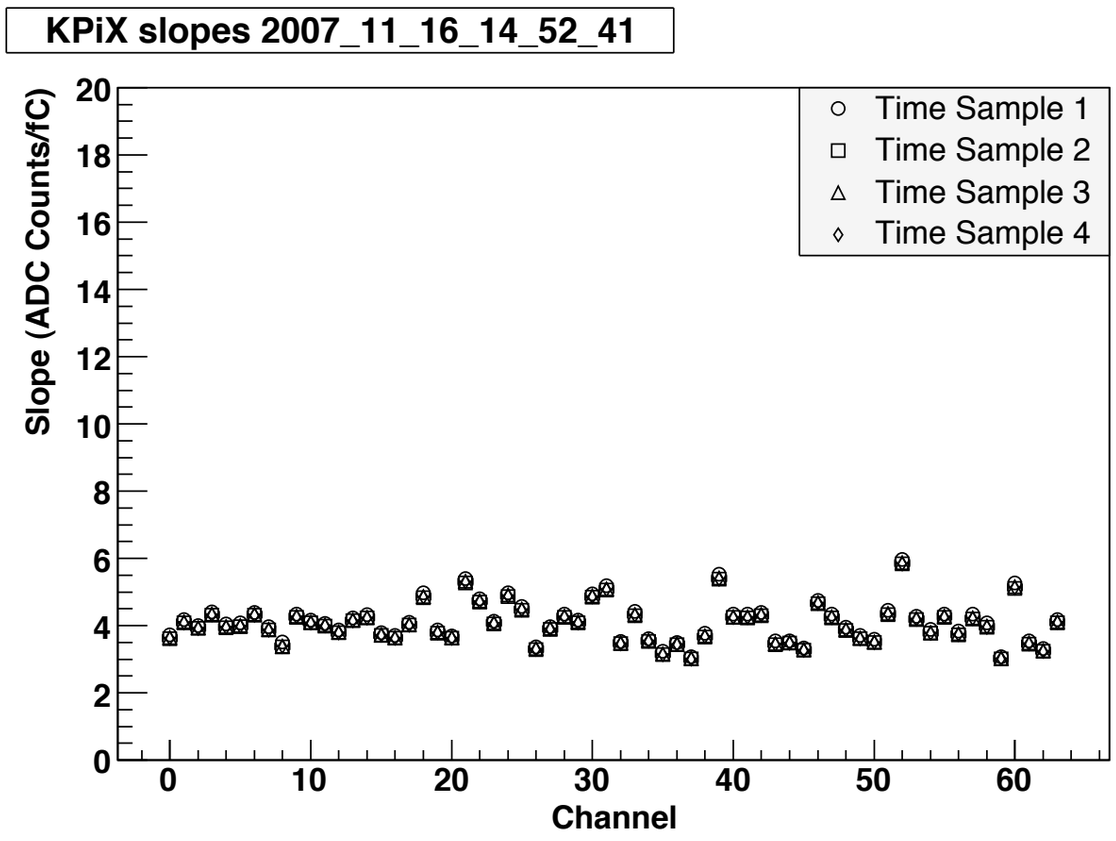


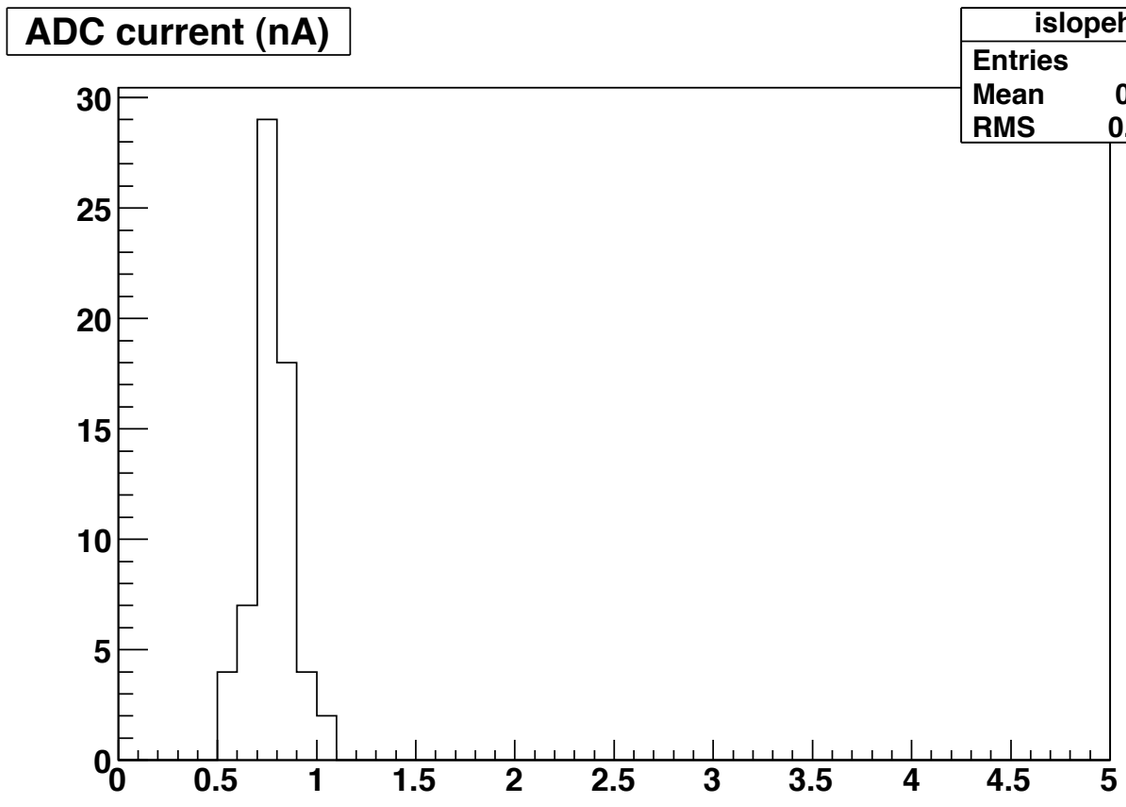

KPiX64



# Improvements in KPiX5, KPiX6

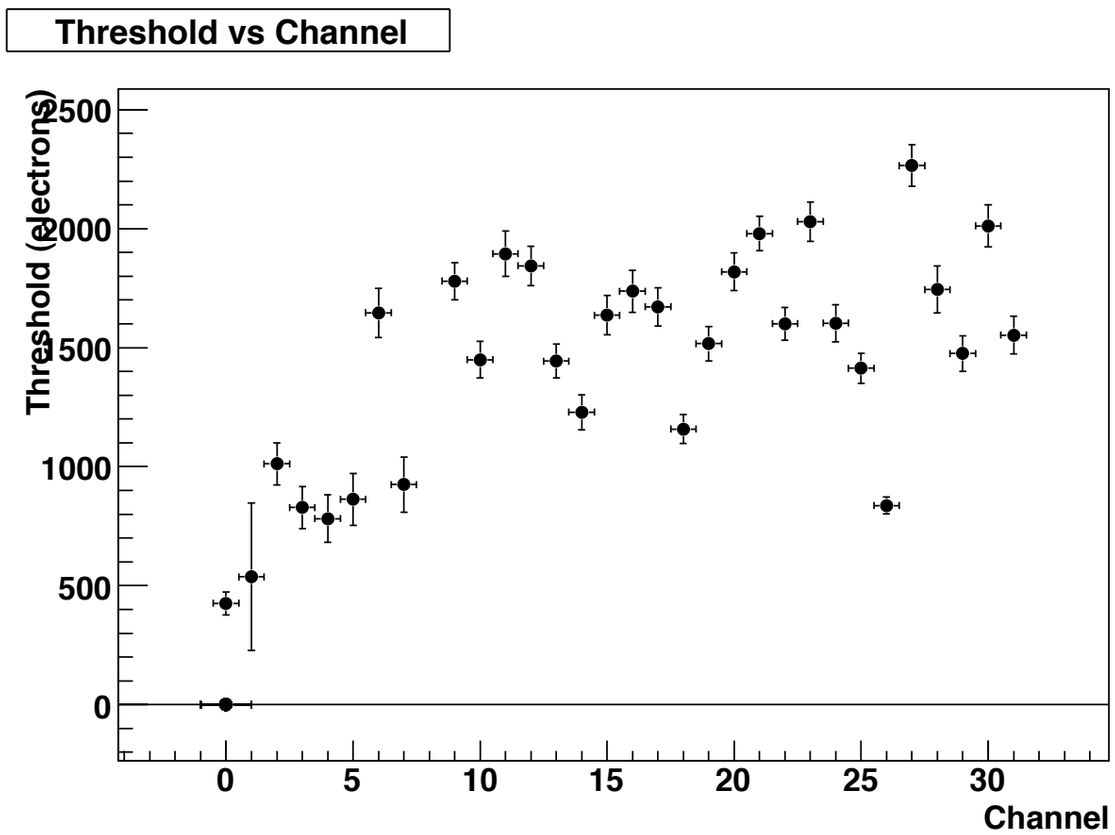
## ADC Gain Consistency

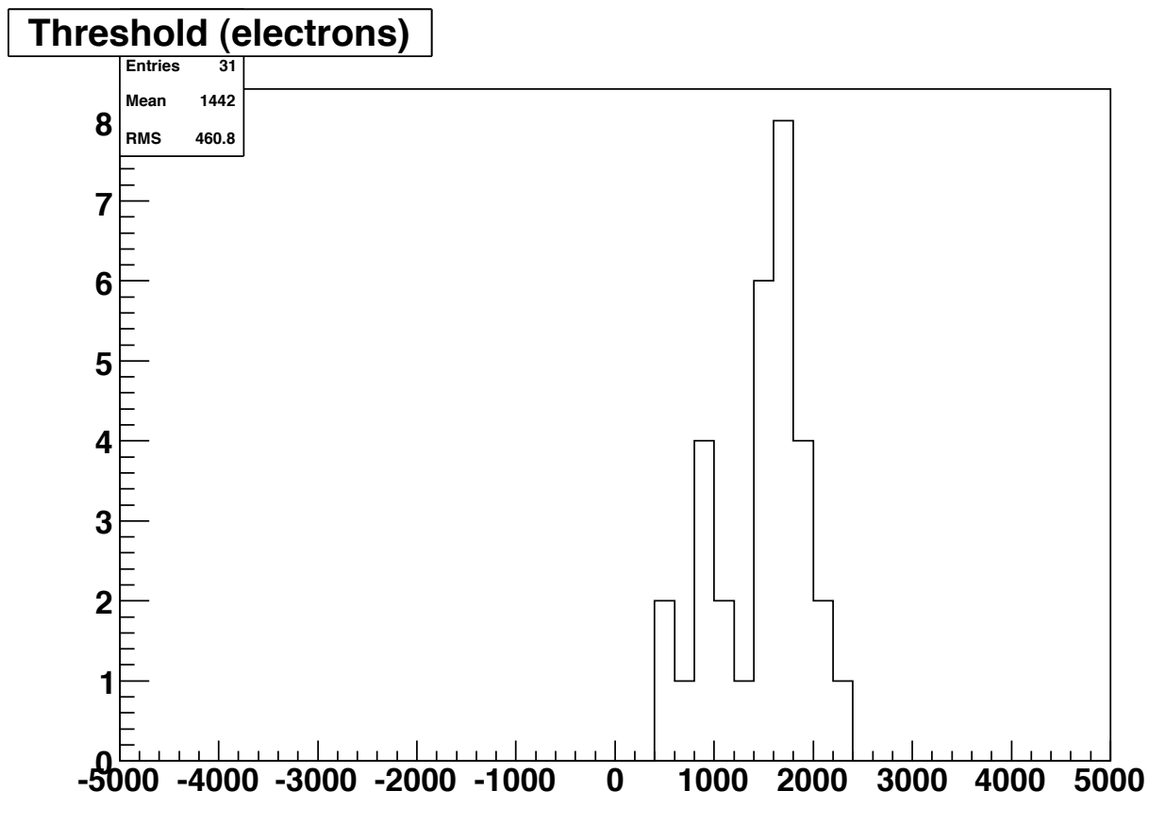


# Improvements in *KPiX5*, *KPiX6*

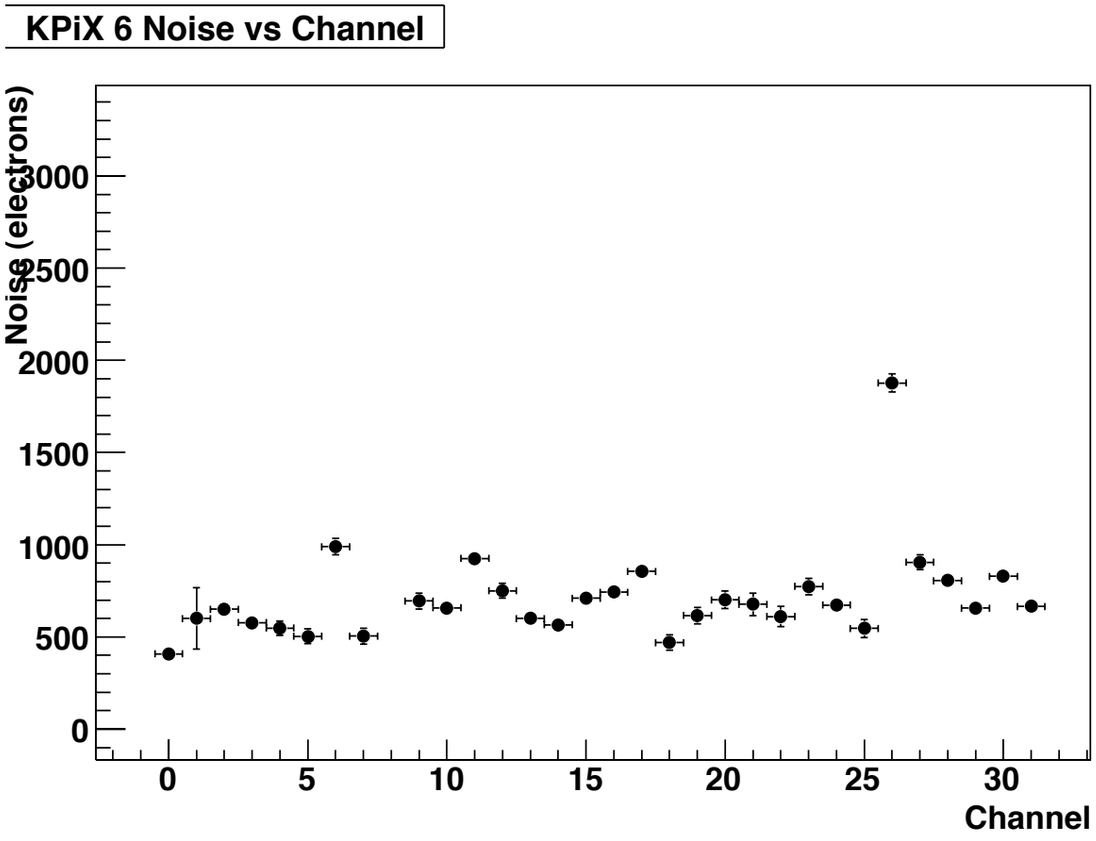
## Trigger Threshold Consistency



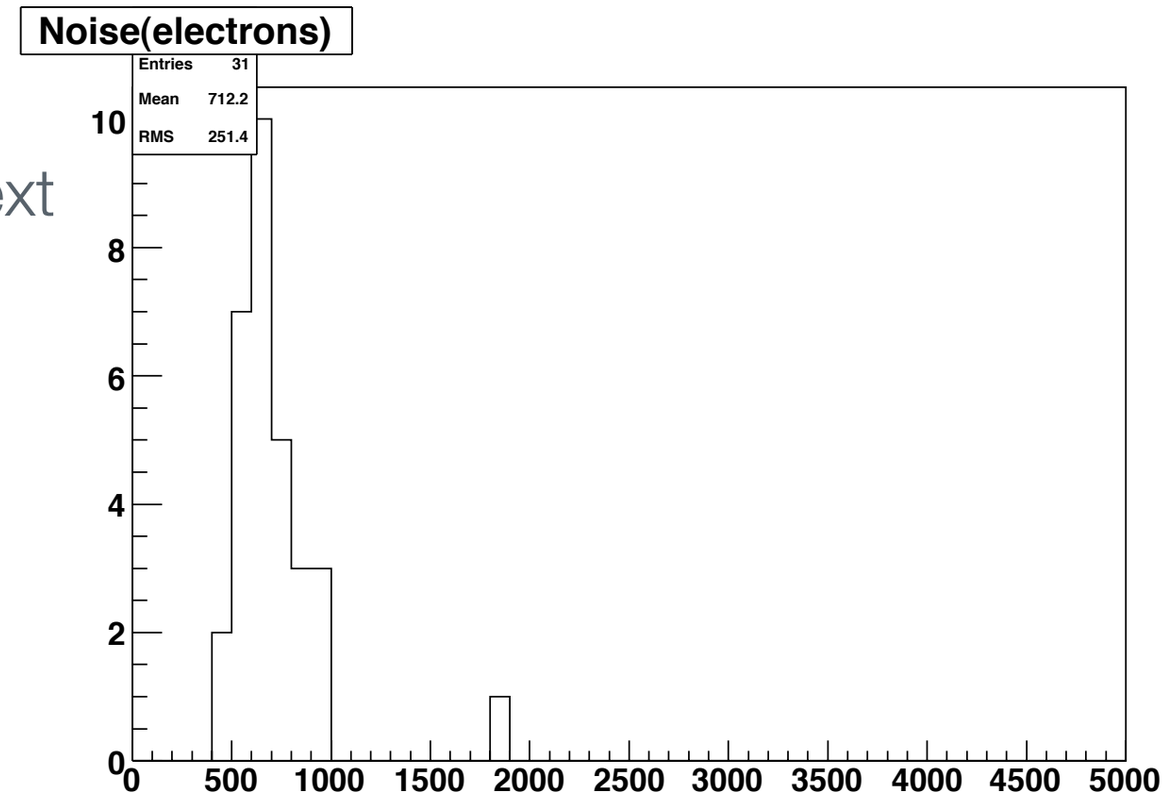



# Improvements in *KPiX5*, *KPiX6*

## Noise in Trigger Branch

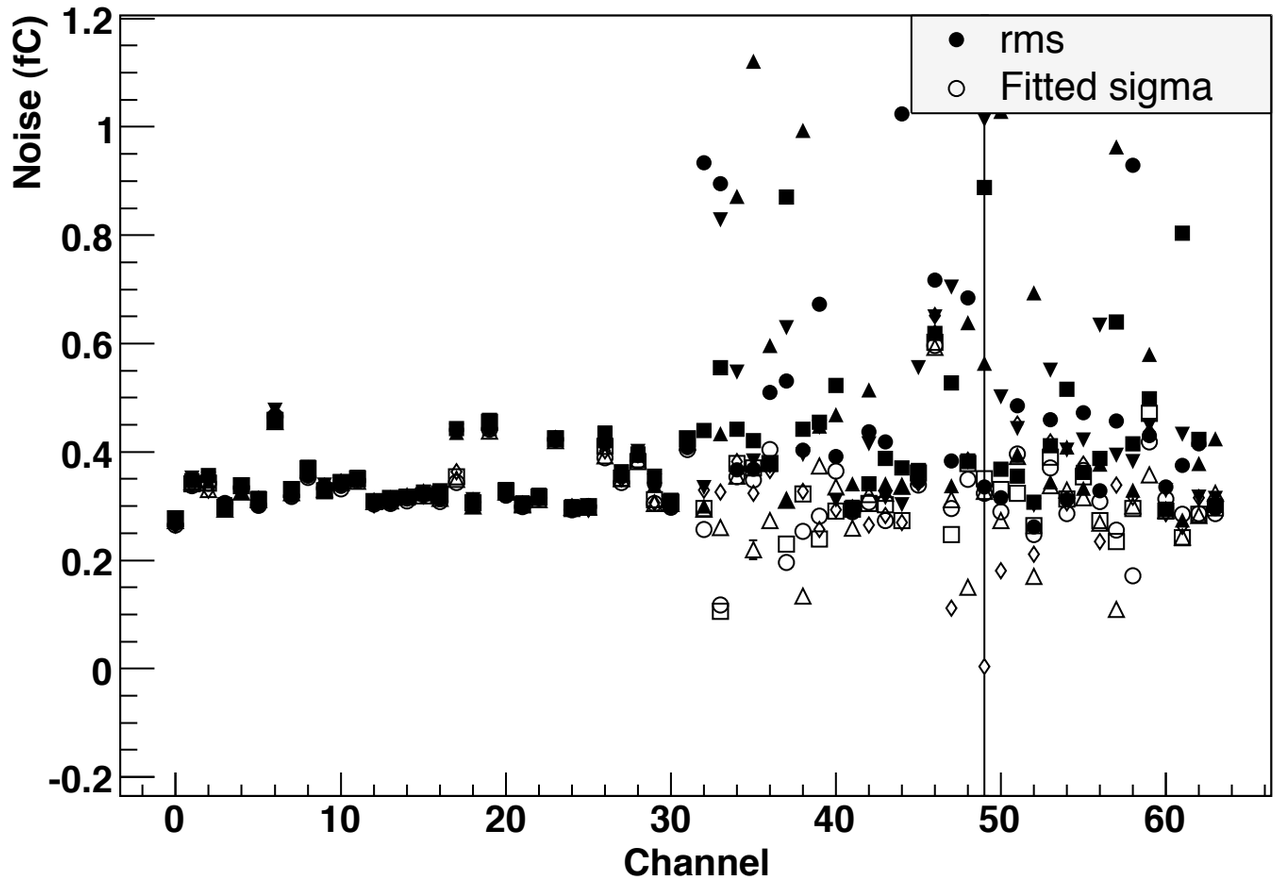



Text



# Remaining Issue

- Noise from ADC is still too high
  - Performance in trigger branch exonerates charge amplifier
  - Tests with different front-end gains exonerate ADC
  - Not many possibilities remain: suspect it may be an effect of the periodic reset
  - Bit errors seen in upper 32 channels are understood



# KPiX 7

- Most significant change is addition of continuous reset, selectable under register control
- Never ask the chip designer what the interesting changes are: “All of them, of course!”

| Document # | Date Effective February 11, 2008 |
|---|---|
| Prepared by Dietrich Freytag | |
| Subsystem/Office Electronics Subsystem | |

**Changes KPiX_7**

1. **Shield between Memory Busses.**

A shield trace, connected to DVDD, was inserted for the full length between the pairs of digital read-out busses in the digital memory. In the standard read-out method used, the memory bus is floating after pre-charge and is vulnerable to be pulled into the high state by the neighboring data bus, a problem we encountered in KPiX_5 and _6.

2. **Further Reinforcement of Power Busses**

Low impedance power busses seem to be essential to achieve uniform thresholds over all cells. In KPiX_5, some vertical power busses were reinforced by as much as a factor ten, and the horizontal connections by factors of five, apparently with good results. There are some indications about differences between the two adjacent columns, pointing to possibly insufficient conductivity in the horizontal direction. If such a problem does indeed exist for two columns, it will become much more serious when expanding to 32 columns.

The new approach is to also install wide horizontal connections in each row, while up to now the horizontal connections were made only at the top and the bottom of the array. In effect, I am trying to approximate power planes, rather than power busses, as much as possible. The fact that five metal layers are available in the TSMC technology helps in this. Obviously, there need to be holes in the planes to allow for wiring of components. Some circuit blocks in the digital section had to be relocated to make room for the new horizontal connections.

3. **Changes in Calibrator.**

The wiring in the block deriving the two-phase clock for the calibration shift register from the calibration strobe has been compressed by moving components and improving the wiring. This makes room for wider power busses in the digital section. It also prepares for the use of this block to generate a two phase clock for the timing shift register from the early bunch clock (see section on bunch clocks).

Three MOS capacitors have been replaced with their FET equivalent.

4. **Changes to Shaper.**

The shaper in KPiX_6 has a shut-off switch, activated by the trigger, to avoid overdriving it with large signals. This seems to work fine. There is also an option to disconnect the shaper under digital control. It appears that, due to pick-up from the trigger signal, there are triggers in spite of the shut off. This turns out to be beneficial for KPiX_6, because it extends the forced trigger up to the hold time. The next version has the forced trigger signal extended by a latching circuit (see below). Thus, there is no need for this incidental trigger extension.



The above conclusions about the spurious triggers are supported by simulation. It was found that a very small coupling (5 fF) from the trigger line to the shaper input produced a shaper signal equivalent to a 6 fC input signal. There are two possible causes for the presumed coupling. The forced trigger signal is routed close to the large area input capacitor to the shaper, possibly causing enough capacitive coupling. In addition, a logic gate processing the trigger signal was located next to the input capacitor, possibly injecting a signal into the substrate, which could then be picked up by the large area input capacitor.

In the new lay-out, the logic gate and the wiring for the trigger signal were relocated far away from the input capacitor. In addition, to further shield the capacitor from pick up, an nwell was inserted underneath it and a metal guard ring, connected to AVDD, was placed around it. Two FETs, which had been disabled in KPiX_6, were removed entirely.

5. **Latch for External and Forced Triggers.**

The external and forced trigger signals will start the data acquisition cycle if they are long enough to be caught by the next bunch clock signal. In order to cause storage of the correct amplitude, the trigger signal must cover the time interval to the hold time, holding off the periodic reset. That required adjustment of the external trigger duration is awkward in operation. To assure the operational requirement of the correct trigger duration, a latch was added to the circuitry. The logic is identical to the one used for the internal trigger signal, which is latched when the signal rises above threshold, and reset at hold time.

In addition, the method of generating the OR between internal and external triggers has been changed from wired OR to a regular CMOS-OR, so that the additional current drawn by the wired OR at trigger time is eliminated.

6. **Improved Wiring Timing Generator.**

The block “t-logic” was compressed and relocated within the digital area to make room for the new analog power busses providing conductivity in the horizontal direction.

7. **Extended Time Window for Range Switch.**

Up to KPiX_6, the time window for switching to the low gain range ends with the late bunch clock, 100 ns after the signal, assuming that the signal occurs at the end of the early bunch clock. That does not leave enough time to accurately determine the trip point for range switching, especially when the rise times of the signals vary because of non-uniform capacitive loads at the inputs of different cells. The new end-point for the timing window is derived from the timing generator in each cell. It is now 350 ns after signal time. The acceptance window is the complement of memory-enable, as before, ensuring that no range switch occurs during writing into the analog-memory.



8. **Modified Write into Analog Memory.**

The current (up to KPiX_6) approach to writing into analog memory is to have the selected storage capacitor always connected to the charge amplifier, interrupted only during each late bunch clock to avoid memory writes during range switching. That periodic connect/disconnect is quite awkward and may possibly cause noise problems. In addition, bucket_0 and the group of buckets 1-3 were treated differently. Bucket_0 was set to the charge amplifier quiescent value during power-up reset, while buckets 1-3 relied on the periodic connects to the charge amplifier for updating the reference level. Since the hold operation takes place after only a few time constants, some of the previous history on the storage capacitor may not be completely wiped out. Experimentally, we observed a gain 2.7% higher in bucket_0 than in buckets 1-3, while the variations in buckets 1-3 were only 0.5%.

The new approach is to connect each storage capacitor to the charge amplifier only when needed, that is all of them during the power-up reset, and then each of them individually during the period 350 ns after the signal up to the hold time. In this way all capacitors are treated the same. The only difference is that later buckets are kept floating for a longer period after power-up reset until signal time. We have determined that drifts in that state are very small.

9. **Disable Periodic Reset.**

An option to disable the periodic reset to the charge amplifier (and to the inverter for the negative input option) is provided, controlled by bit_0 in the control register: “disable_periodic_reset”. If this bit is set low, the old configuration of periodic resets with the bunch clock frequency is established. When the periodic reset is disabled, no signals related to the bunch clock are transmitted into the analog section. The bunch clock is simply a timing signal controlling the data acquisition, confined to the digital section.

10. **Enable DC Reset.**

An option to enable a DC reset to the charge amplifier is provided, controlled by bit_1 in the control register: “enable_DC_reset”. If this bit is set low, the old configuration with no DC reset is established. The DC reset is of comparatively low impedance, ~10 Megohm, yielding a differentiation time constant of ~4 us. In order to avoid losing signal due to the DC reset in the few-microsecond interval to hold time, the reset is turned off upon receipt of a trigger. Note that the DC reset is not yet provided for the inverting amplifier for the negative input option.

11. **Buffers for Charge Amplifier and Shaper Probe Signals.**

Buffers were installed for the probed charge amplifier and shaper signals in channel 8. These are simple DC coupled NMOS followers with a 10 kOhm source-load, The response is quite fast, at the few nsec level, but there is a DC offset and a finite output impedance. Because of different DC levels out of the charge amplifier and the shaper, the properties of the two buffers are slightly



different. The buffer for the charge amplifier runs at 120 uA, has an output impedance of 2 kOhm and produces an offset of -.68 V. The buffer for the shaper runs at 40 uA, has an output impedance of 3.3 kOhm and produces an offset of -.45 V (all according to simulation). During power down the buffers draw no current.

12. **Filter Capacitor for BVDD.**

When the (“dirty”) net BVDD was split off from AVDD, the 10 pF filter capacitor remained on AVDD and BVDD was left without filtering. Since pulsed currents are drawn from BVDD, local filtering should be advantageous for noise suppression. A 7 pF filter capacitor was added to BVDD in each cell, for a total of 7 nF for the full sized chip.

13. **Bus Routing for BVDD.**

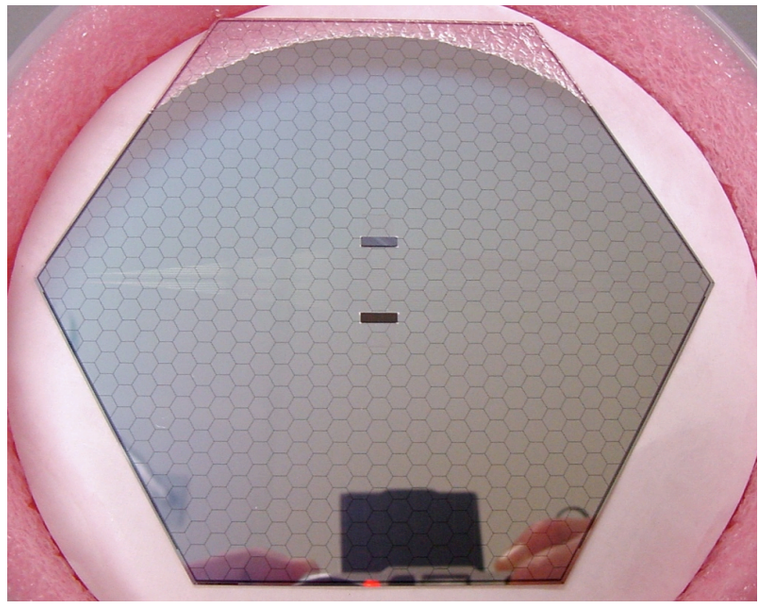
The busses for BVDD and BGND on the metal-5 layer were running across the charge injection capacitors of the calibration section. This provided a fairly large overlap of metal-5 and top capacitor metals coupling directly into the charge amplifier input. Since the BVDD net carries pulsed currents, this could possibly have injected noise into the charge amplifier. The BVDD nets were rerouted into a different part of the analog section. The busses running across the charge injection capacitors have been left in place and connected to AVDD, the AC ground, thus providing a shield for the charge amplifier input.

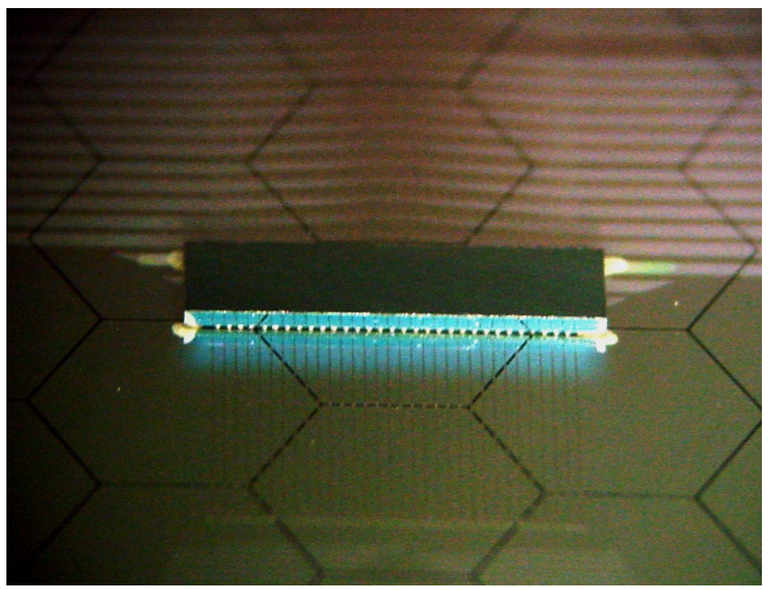
# Bump Bonding

*Bump-bonding is a critical process for our designs*

- At these pitches, gold-stud bumping becomes feasible, especially attractive for small-run R&D
- First attempts by Palomar Technologies on KPiX-5 and ECal prototype sensors somewhat successful
- Only 96% yield on first two test chips
- Corrosion problem between epoxy used for making final bond and Al pads: at worst we will have to add Ti-W as one would for indium bumping

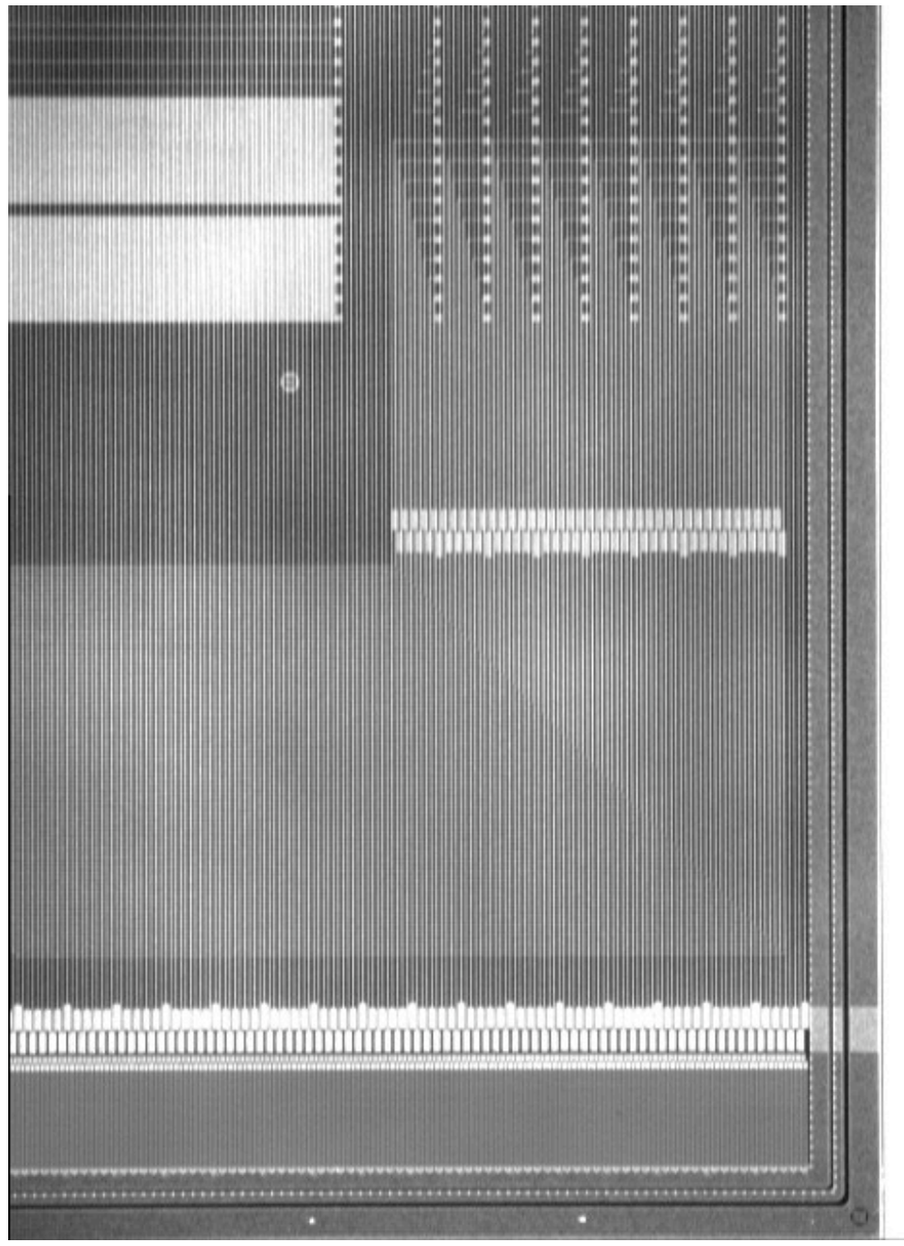
*Encouraging progress for an unfamiliar technique: anticipate using this process for prototype modules*





# Prototype Tracking Sensors

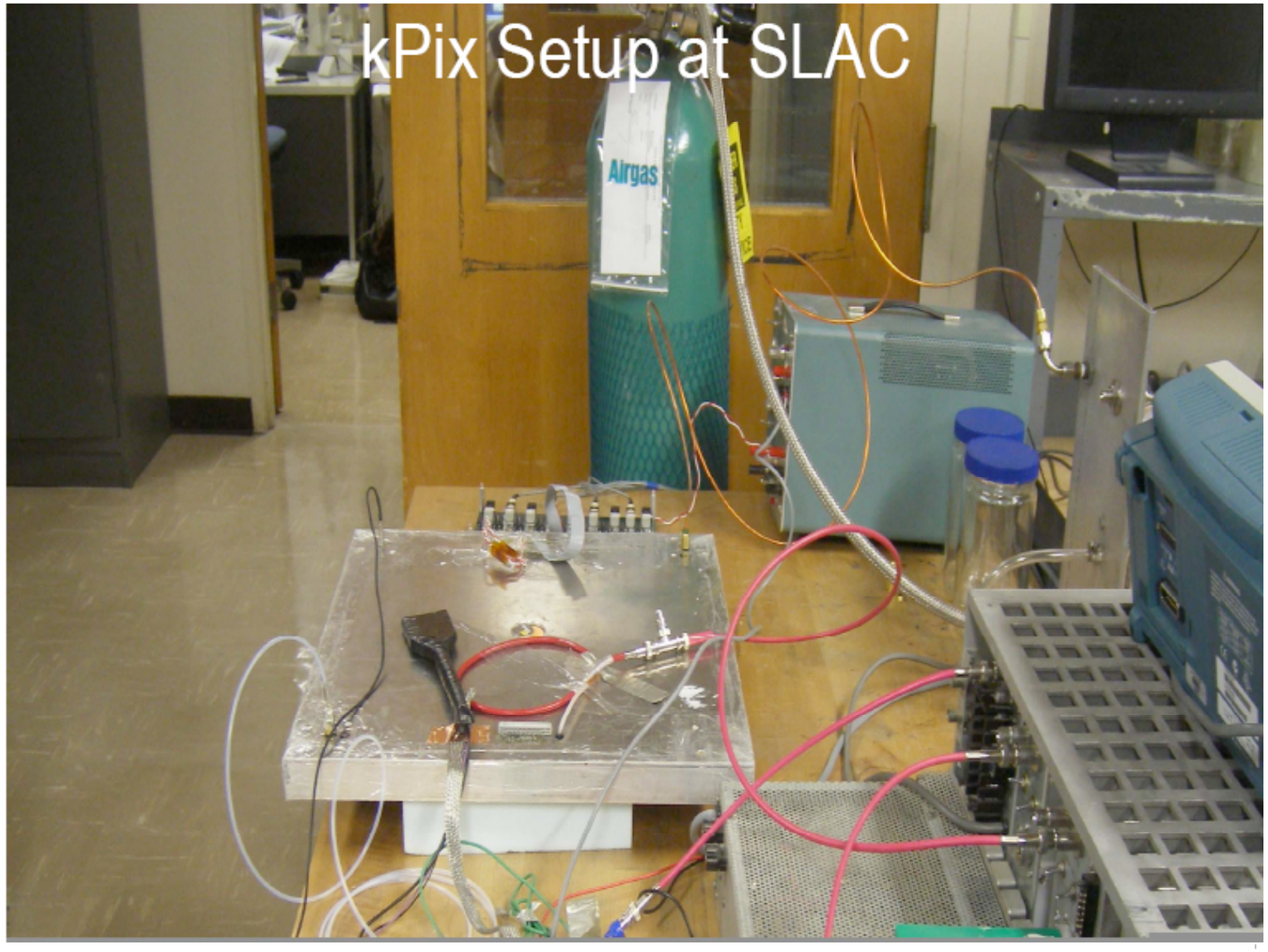
- Received prototype sensors from HPK on March 30.
  - 20 full-sized tracking sensors for module prototypes
  - 40 smaller sensors designed for testing RF pickup issues from bump-bonded *KPiX*
- Quality is excellent:
  bad channel rate <1/10000 (!!)
- Will be testing at UNM/UCSC/SLAC/FNAL in the coming weeks.



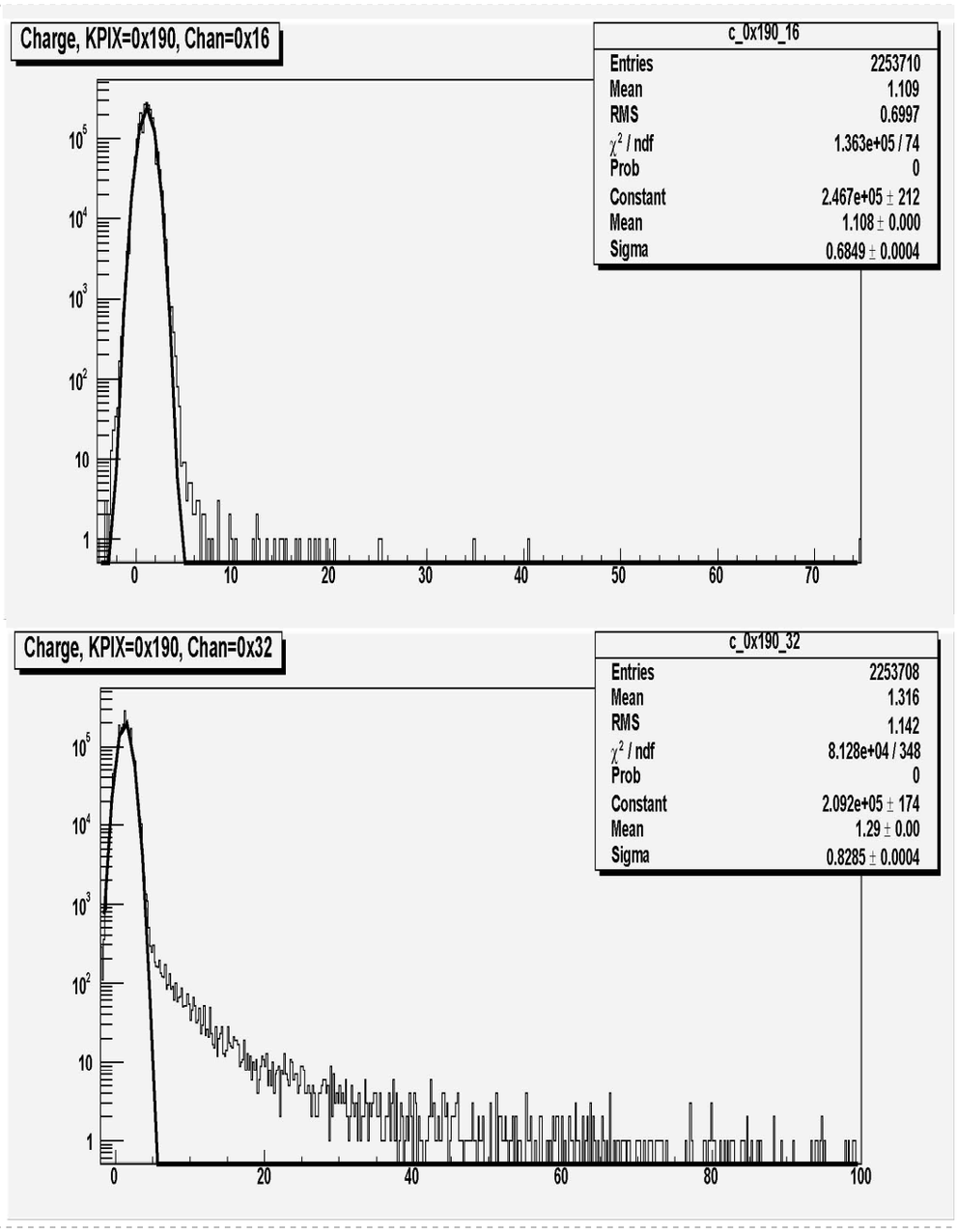
# GEM Readout

## *UT Arlington (Andy White, Jae Yu)*

- KPiX bonded to large PC board with readout pads
- Board routes signals from readout pads to KPiX chip
- Successful bench testing using simple setup at SLAC



# GEM Signals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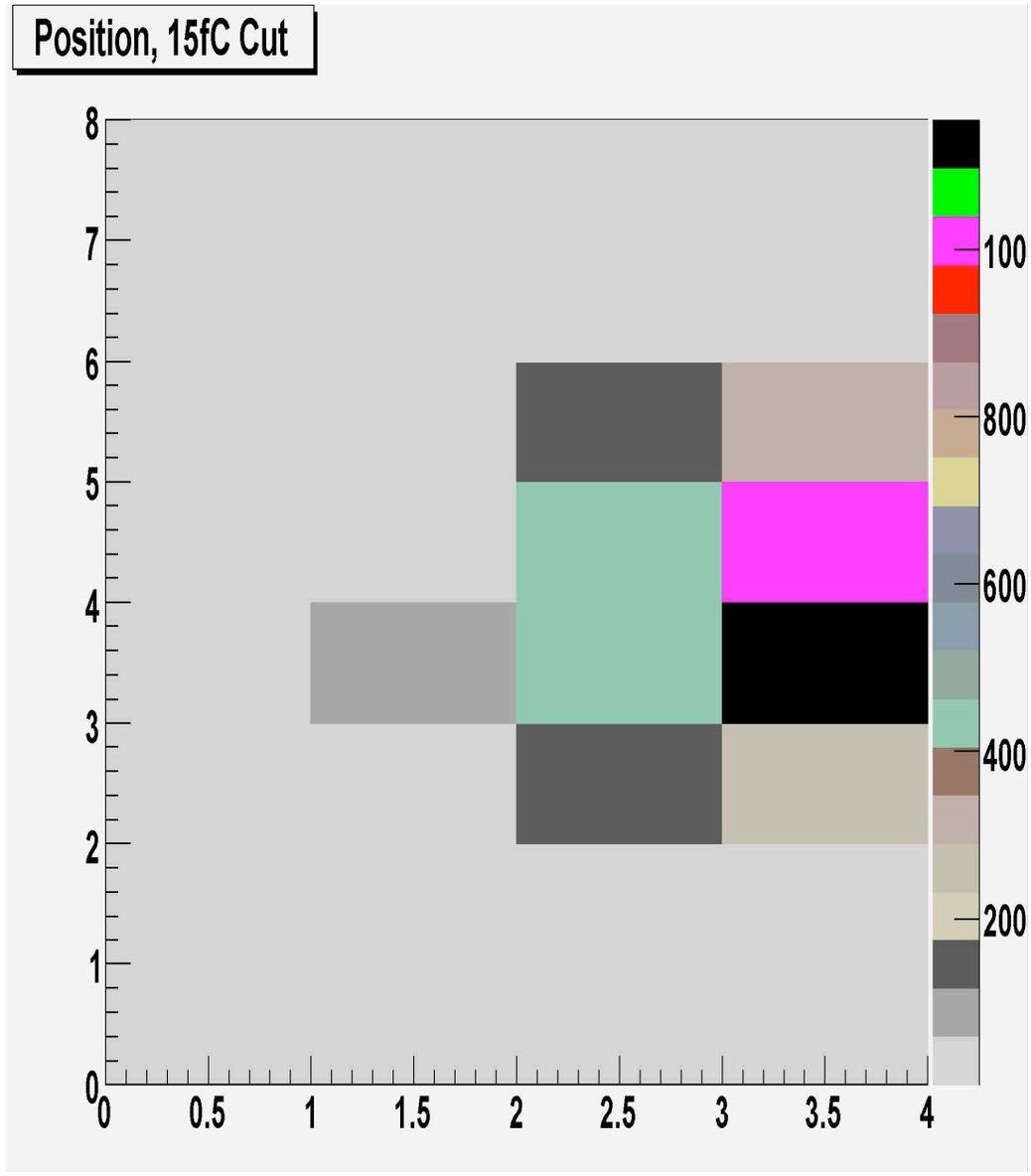
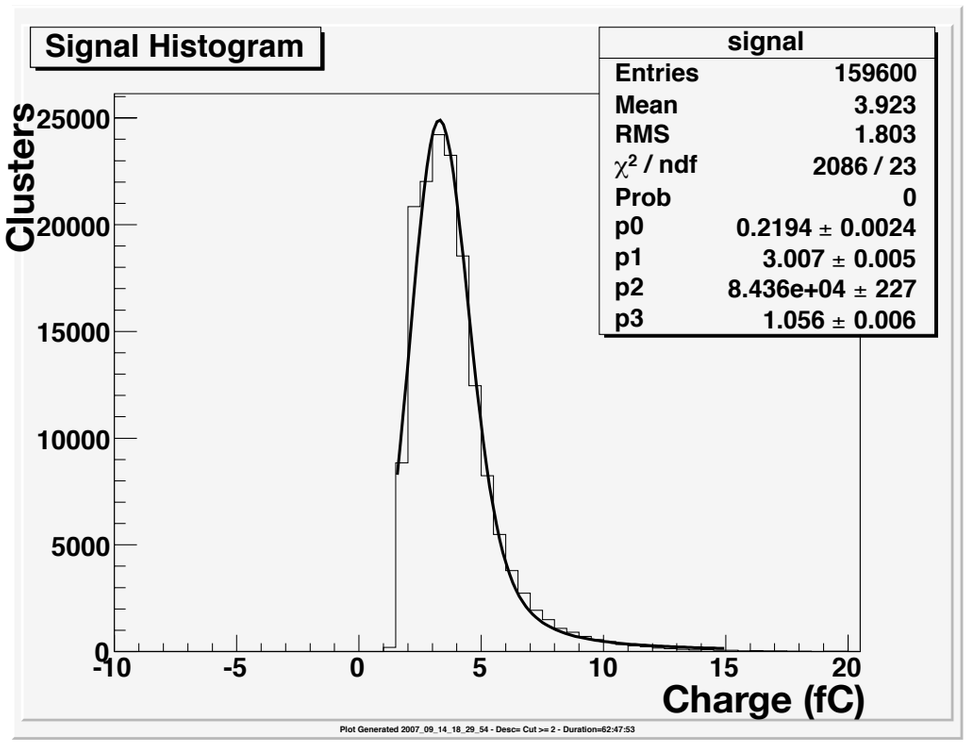
c_0x190_16
Entries 2253710
Mean 1.109
RMS 0.6997
χ² / ndf 1.363e+05 / 74
Prob 0
Constant 2.467e+05 ± 212
Mean 1.108 ± 0.000
Sigma 0.6849 ± 0.0004
Charge, KPIX=0x190, Chan=0x32
c_0x190_32
Entries 2253708
Mean 1.316
RMS 1.142
χ² / ndf 8.128e+04 / 348
Prob 0
Constant 2.092e+05 ± 174
Mean 1.29 ± 0.00
Sigma 0.8285 ± 0.0004


Position, 15fC Cut
100
800
600
400
200

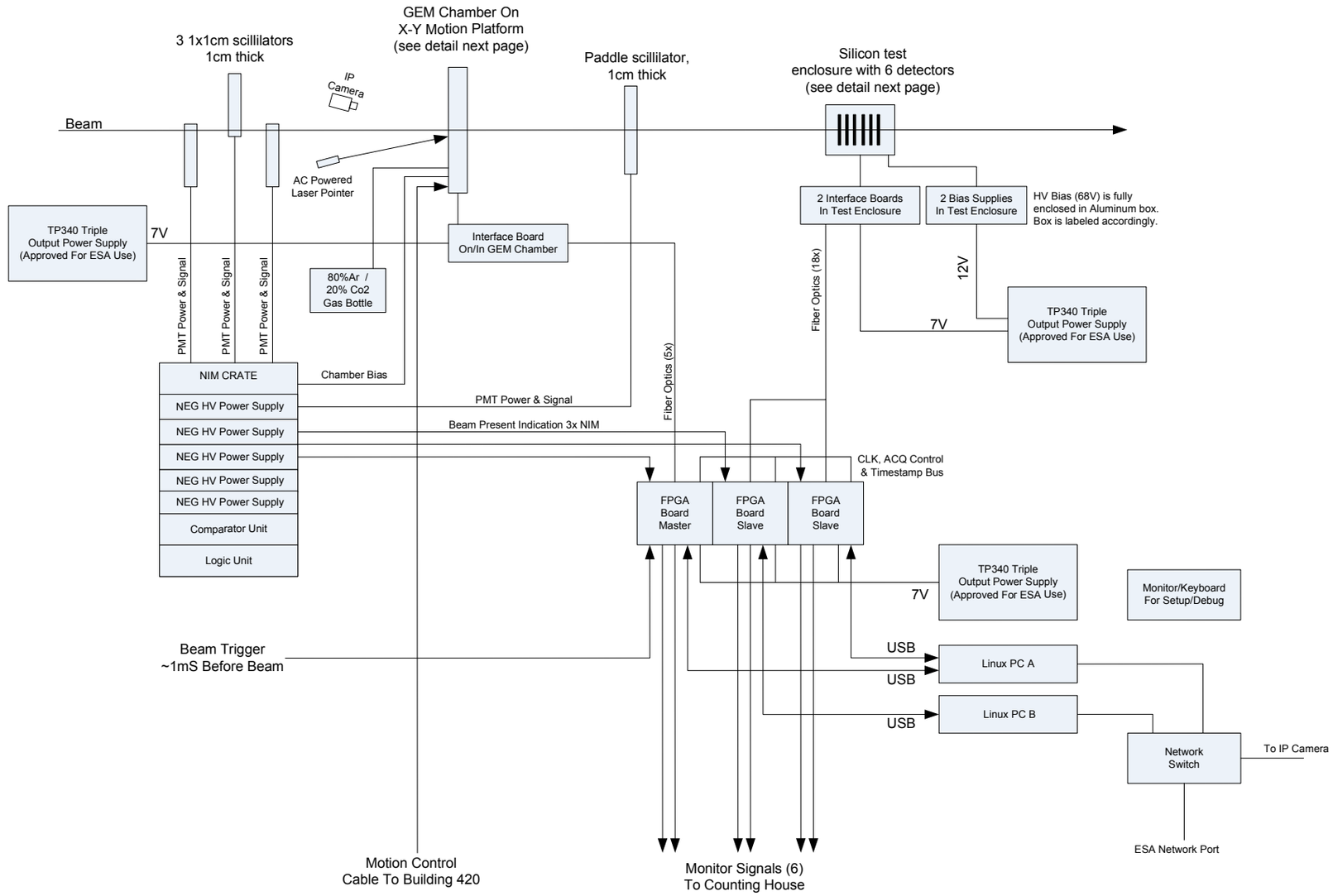
# Test-beam in End Station A

- Performed first test-beam with CDF Layer00 sensors in ESA last fall
- No significant operational issues beyond know problems with *KPiX4*




# Test-beam in End Station A

- Planning a more comprehensive run in late July
  - 6 tracker planes
  - ECal prototypes
  - Bump-bonded *KPiX*
  - At least one type of GEM module
- Some uncertainty: caught in the wheels of ESA shutting down..



# Conclusions and Plans

- Nearly all of the outstanding issues with *KPiX* have been resolved
- In addition to improved performance, each successive generation has offered new capabilities enabling its use in more detector subsystems
- We are considering modifications required for warm-machine operation
- An interface board is underway to allow *KPiX* to integrate RPC signals
- *KPiX7* should be the last “small format” version of the chip
- Although far from producing any physics, July test-beam in ESA will allow us to operate a significant “vertical slice” of the *Si*D detector
- The horizons for *KPiX* are so broad now that we could always use more help!