DHCAL status, progress & future

Based on RPC efforts in CALICE

mostly by US groups

H.Weerts
for DHCAL group

Argonne National Lab

Background

H.Weerts

To use PFA algorithm for SiD need fine hadronic calorimeter with very fine longitudinal and transverse segmentation.

Up to now such a hadronic calorimeter has not been realized in a experiment.

Several solutions have been proposed; CALICE collab. pursues several

Solution investigated here is a gas based digital calorimeter

- Based on work with RPCs, use RPCs in avalanche mode.
- 1x1 cm sampling transverse
- Design digital/ one bit readout system
- Build vertical slice of whole system to test

Several years

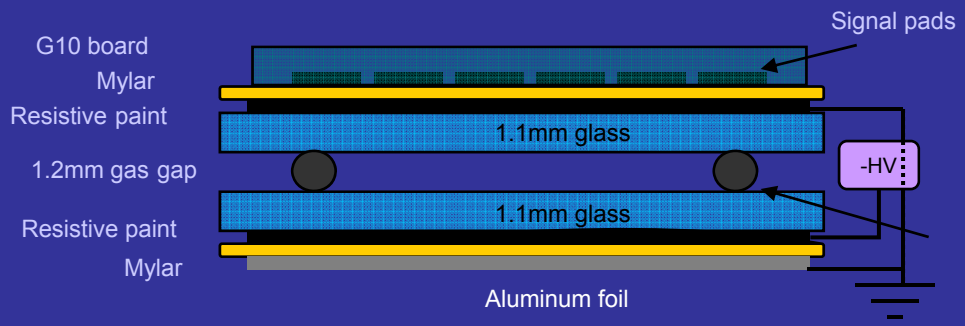
Last year

Groups: Argonne, Boston, Fermilab & Iowa (built & run slice test)

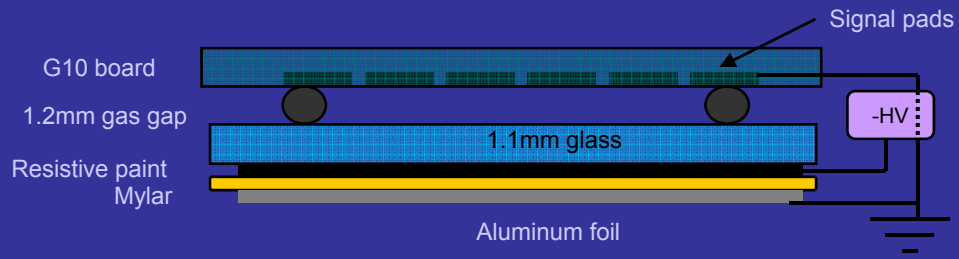
RPC Designs

H.Weerts

Two-glass design



One-glass ('exotic') design



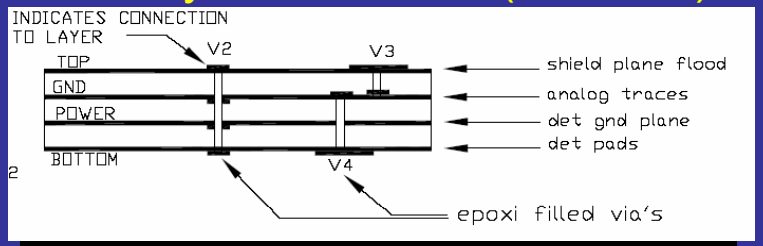
History

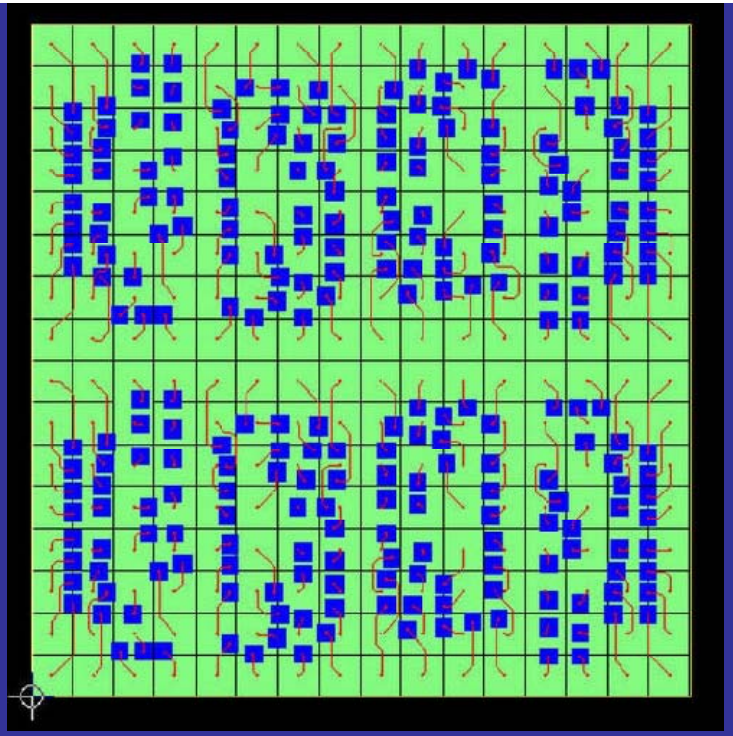
- RPCs developed over last few years & tested
- Digital readout system designed
- DCAL chip designed & prototype built with Fermilab
- ……
- …..stuck, little funding
- …..
- 2006 decide to build slice test
- DCAL chip new prototype
- 2007 construct & operate
- Two months in cosmic & debug mode
- Testbeam at Fermilab in summer
- Results now

Current Pad Board & Front End Board **Design**

H.Weerts

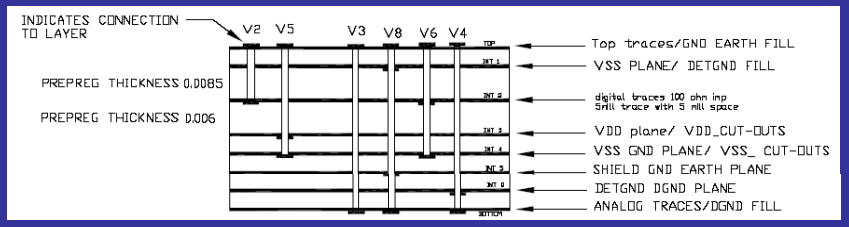
4-layer Pad-board (3 shown)

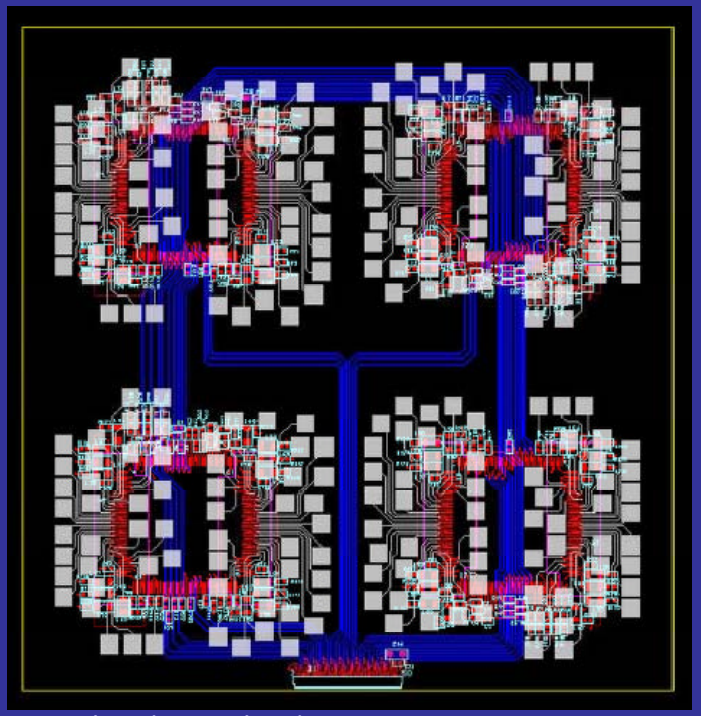




Blind vias to route sensitive signals to glue pads – needed to minimize contact with digital lines in FEB

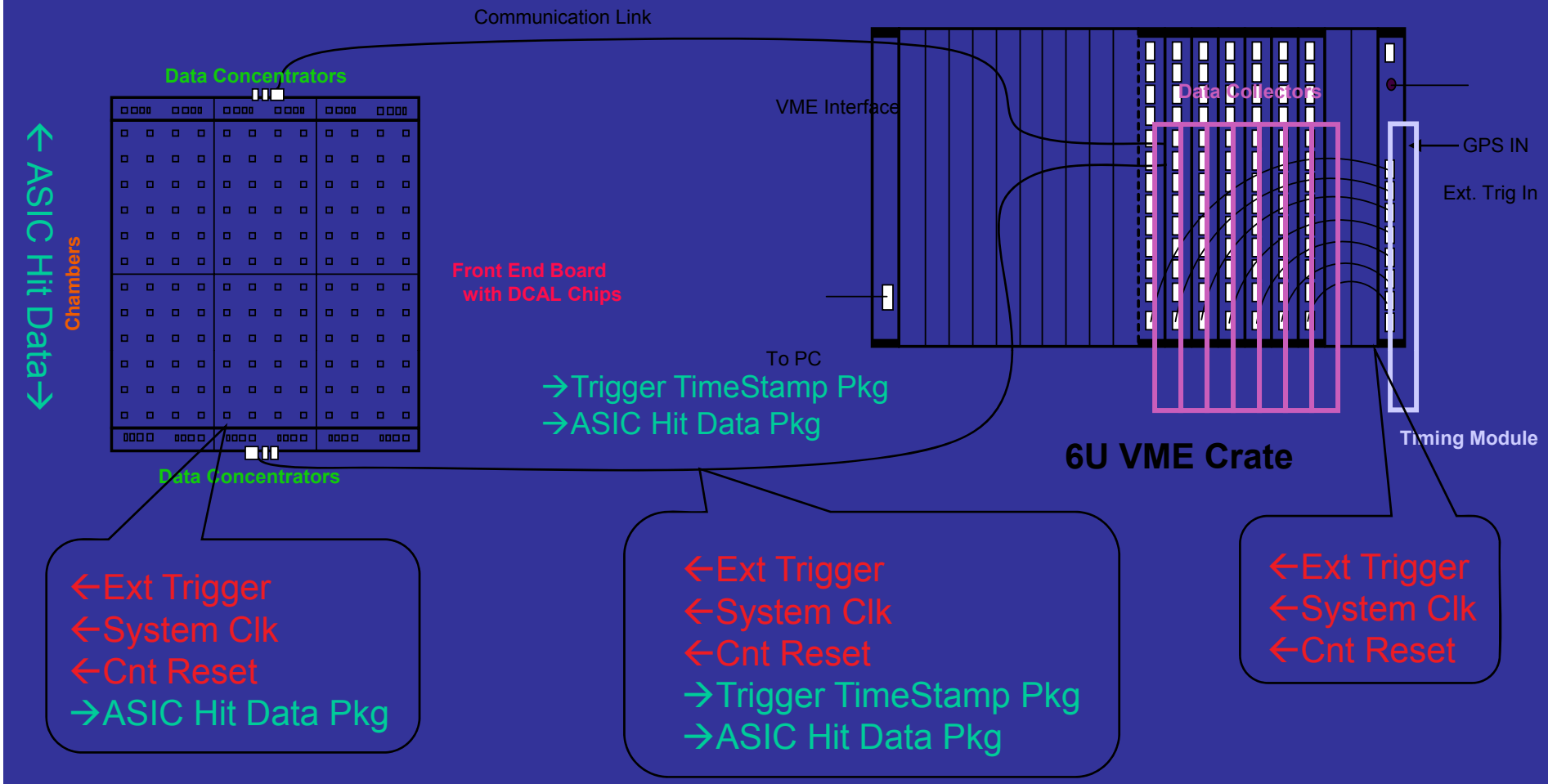
8-layer FE-board (3 layers shown)





Also has blind vias
→ Very complex board design to minimize crosstalk & digital noise pickup

System Physical Implementation



Basic data block: 16-bite package (trigger timestamp OR hit data)

Test Beam Setup and Data Collection

Beam

The gas distribution rack

The stack containing nine layers within the blue hanging file structure

Same set up also used in cosmic ray test stand; just rotated(Blue frame)

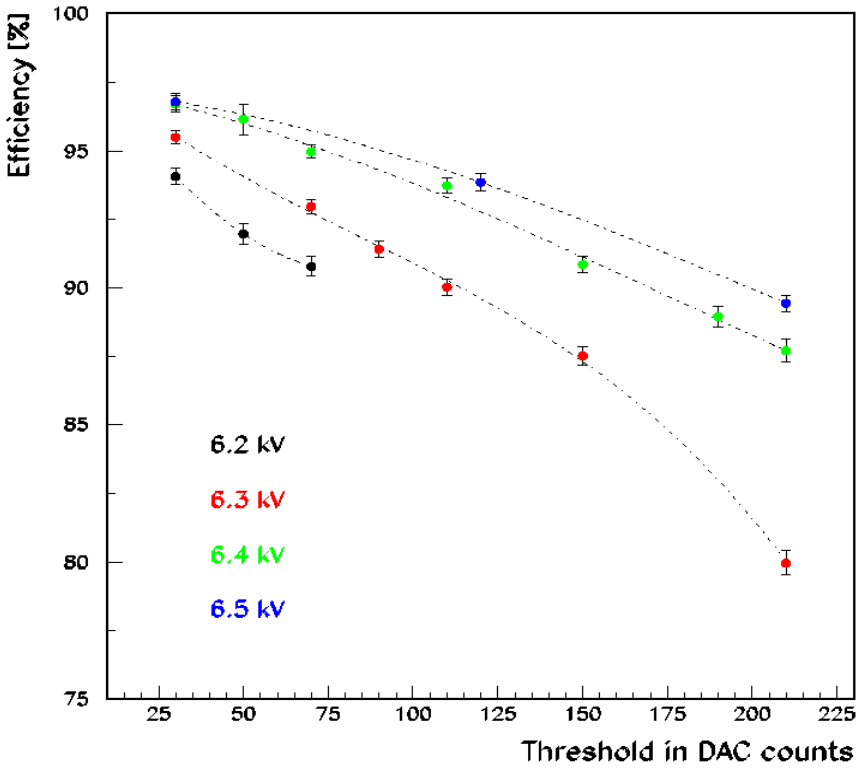
Measurement of RPC efficiency, multiplicity

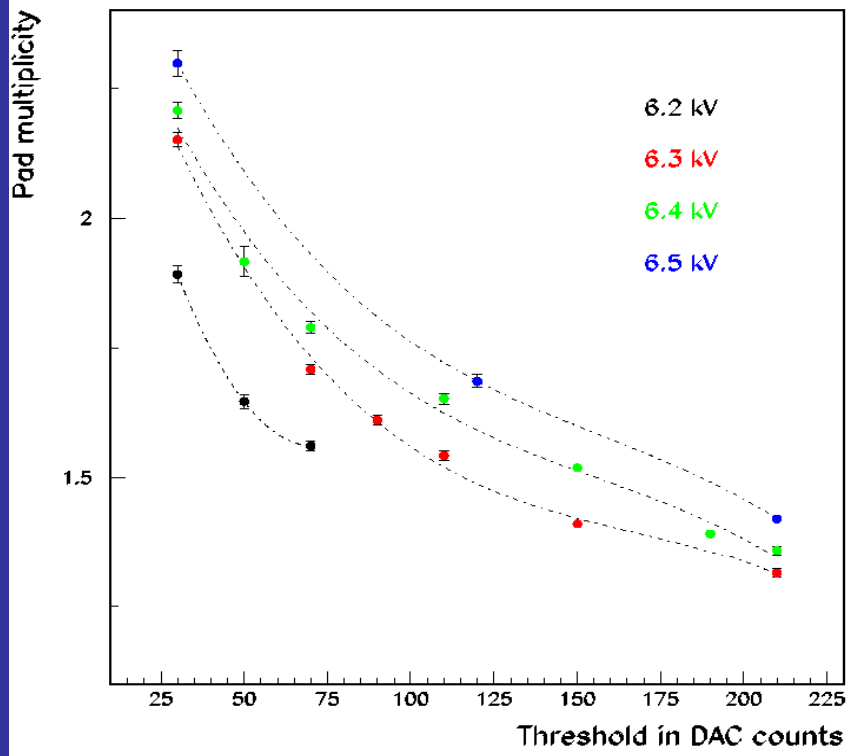
Determine operating point in: high voltage & signal threshold corresponding to the required efficiency & multiplicity.

Paper accepted by Journal of Instrumentation

Dependence on High Voltage

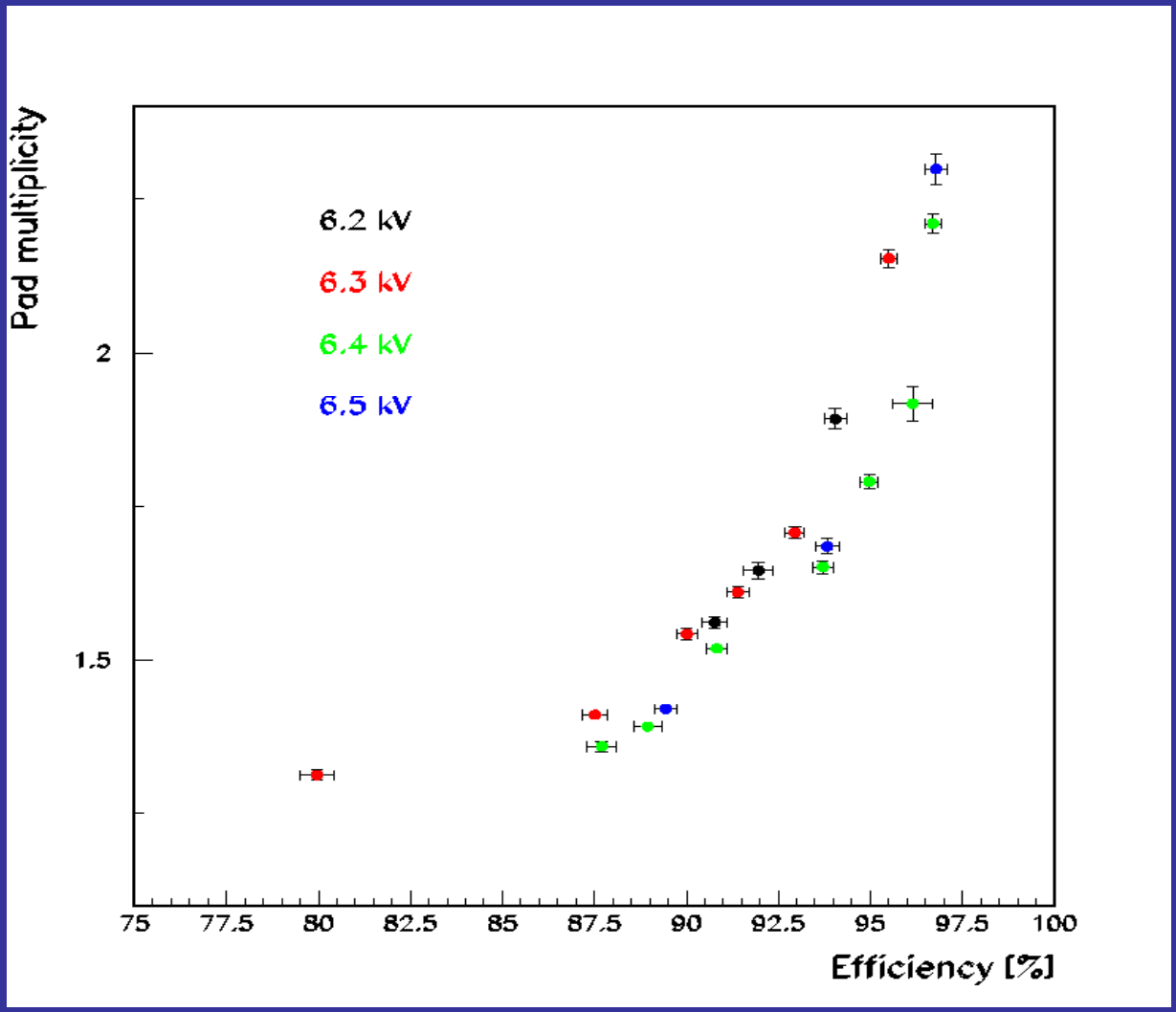
H.Weerts





Dependence on High Voltage

H.Weerts

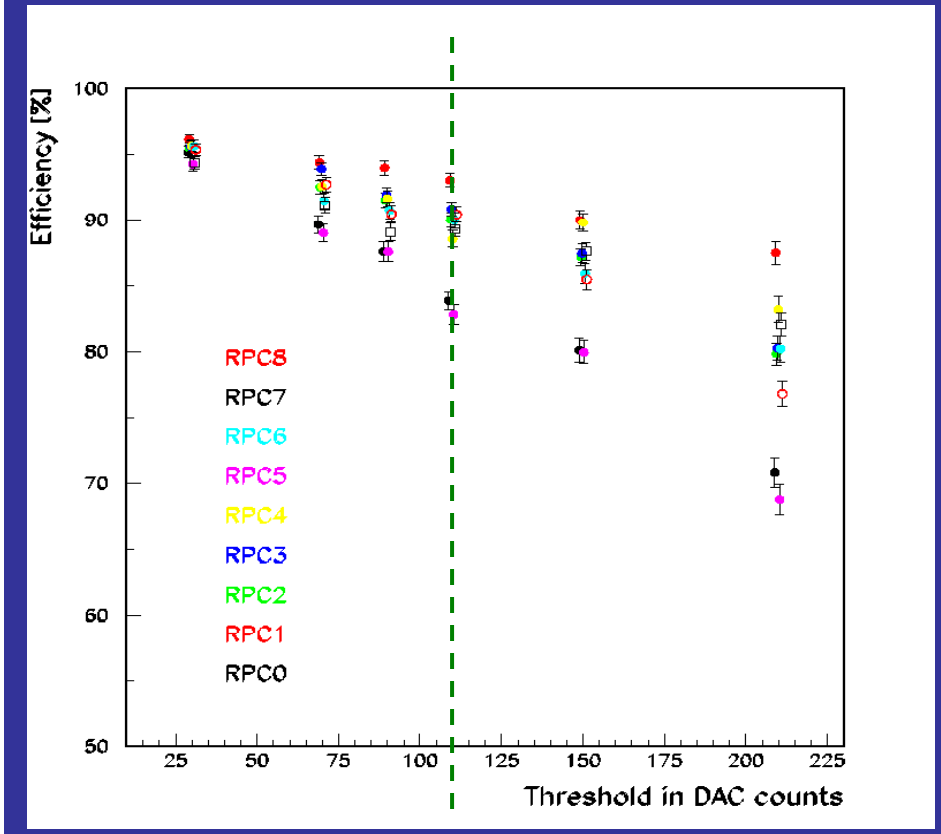


With higher HV lower pad multiplicity for a given efficiency

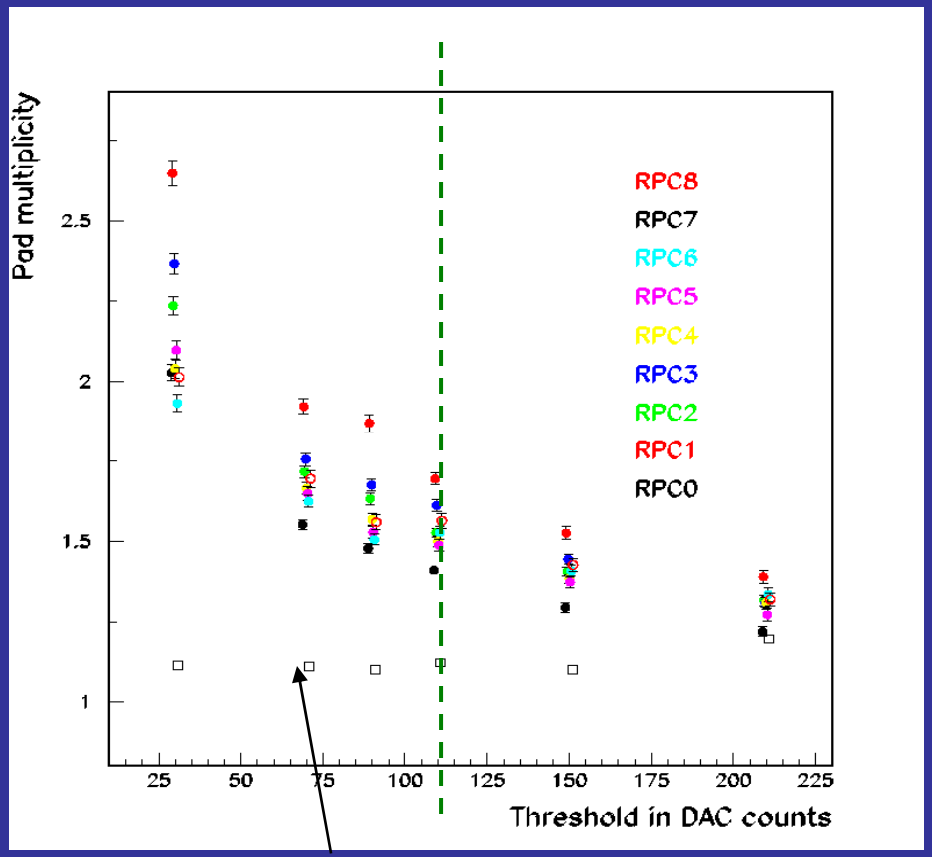
Dependence on Threshold

H.Weerts

Operating point: eff ~ 90%



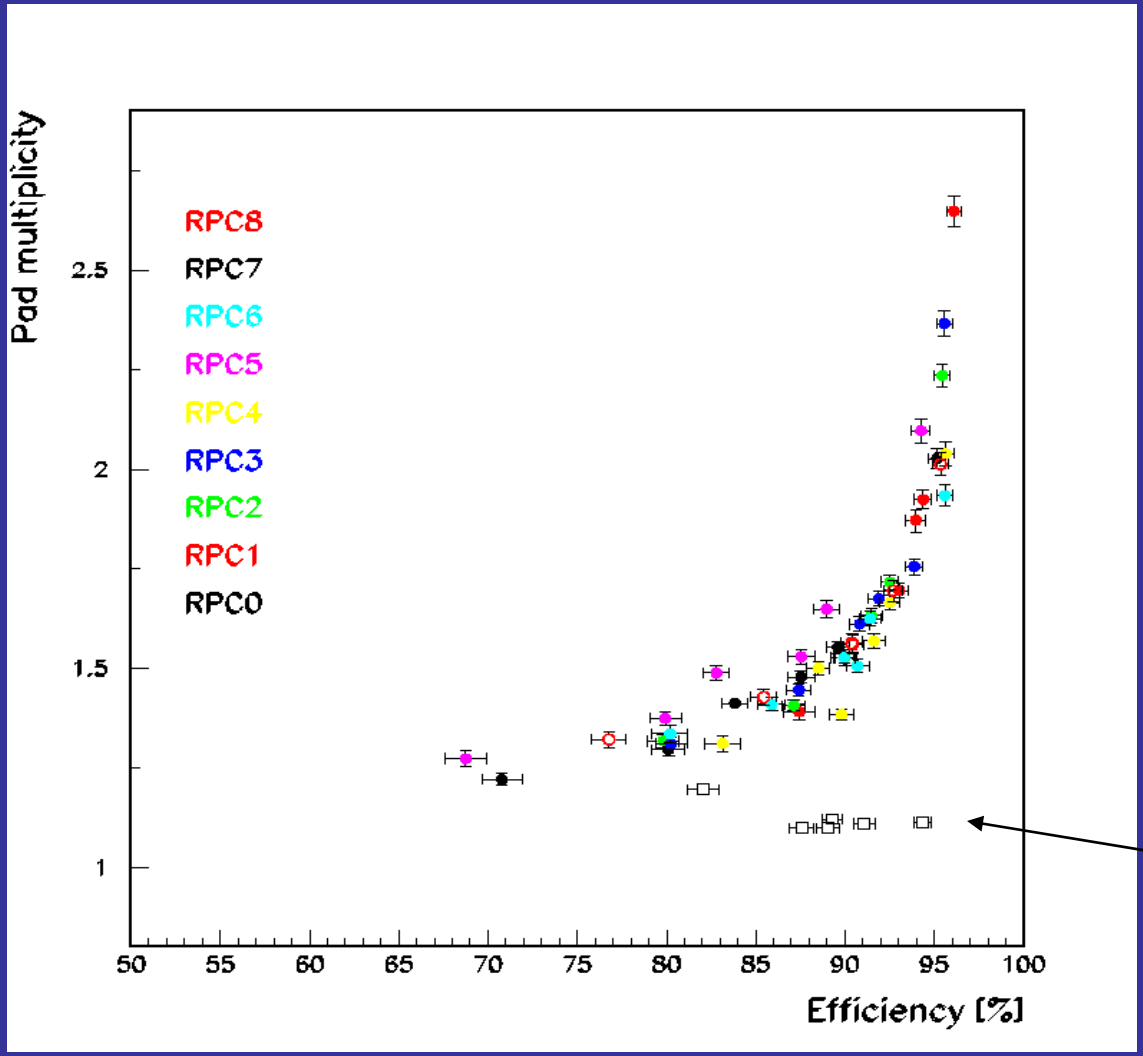
Operating point: M ~ 1.4 – 1.7



The chambers were operated with a high voltage of 6.3/6.0 kV

Dependence on Threshold

H.Weerts

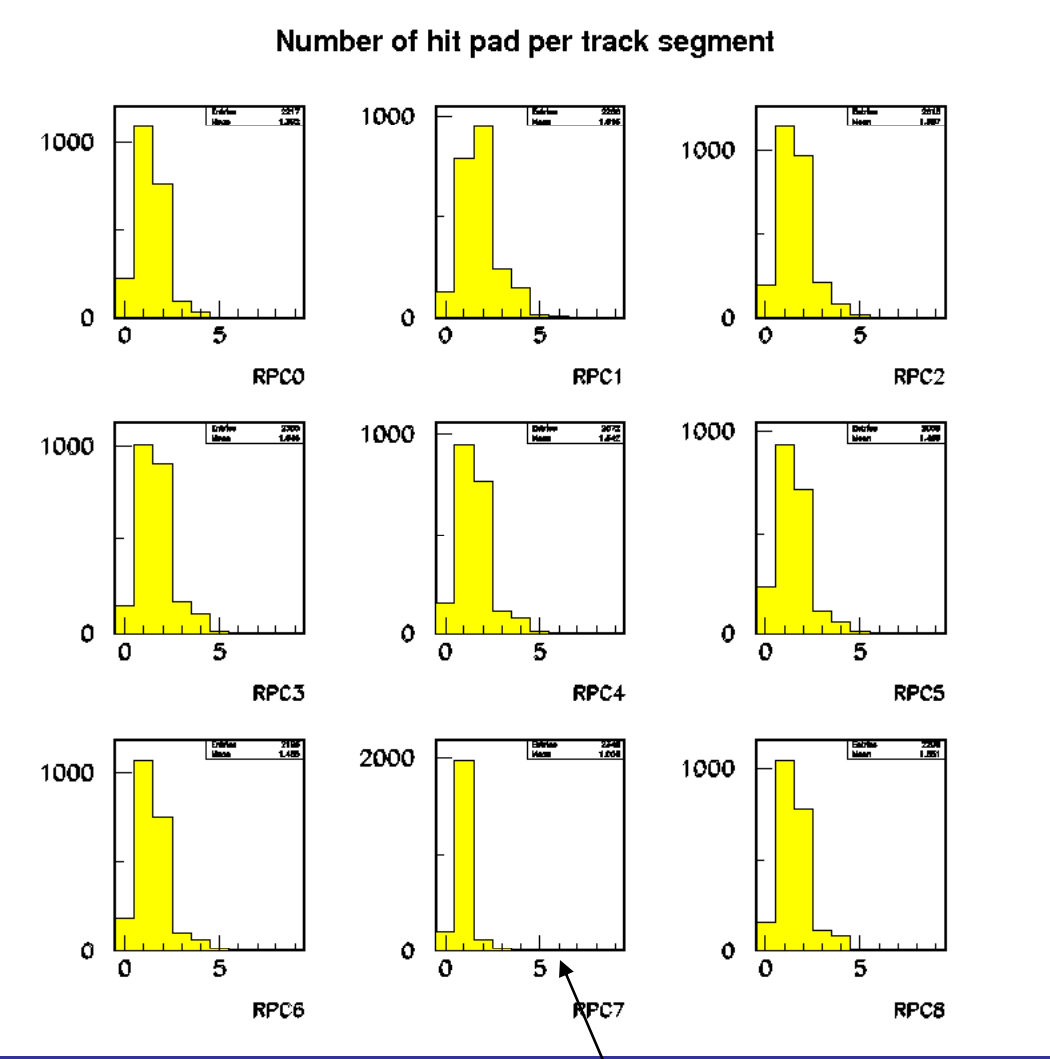


Exotic chamber

The chambers were operated with a high voltage of 6.3/6.0 kV

Number of Hits

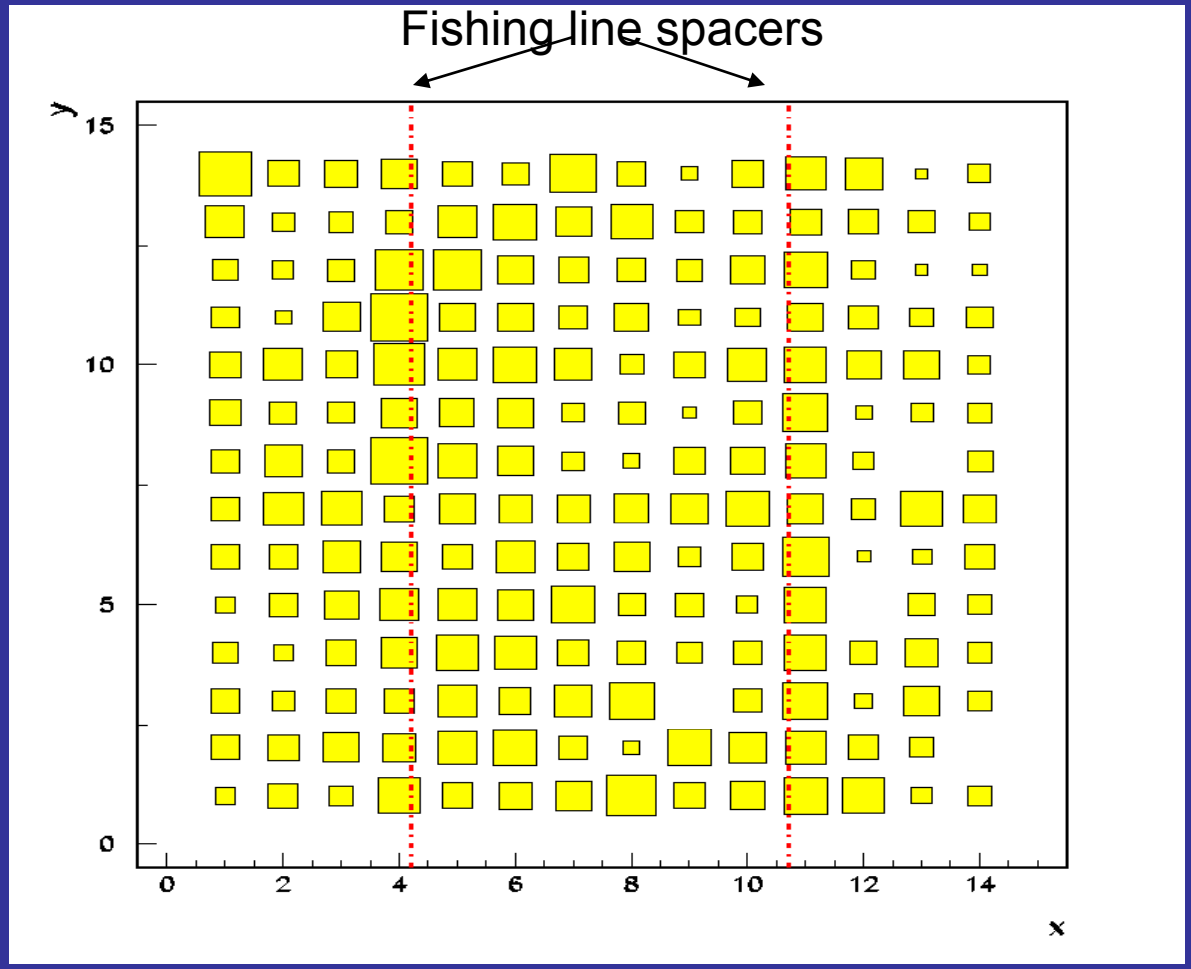
H.Weerts



The chambers were operated with a high voltage of 6.3/6.0 kV. The threshold was set at 110 counts.

x-y Map of Inefficiency

H.Weerts



Largest boxes correspond to an inefficiency of ~15%

The data were collected with a high voltage of 6.3 kV and a threshold of 110 counts.

RPC noise measurement

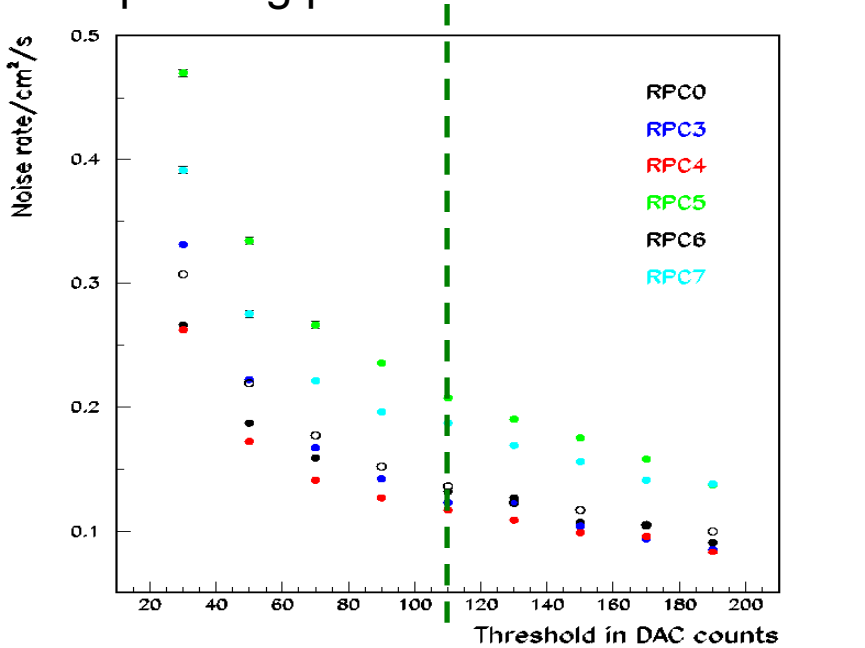
Included in same paper

H.Weerts

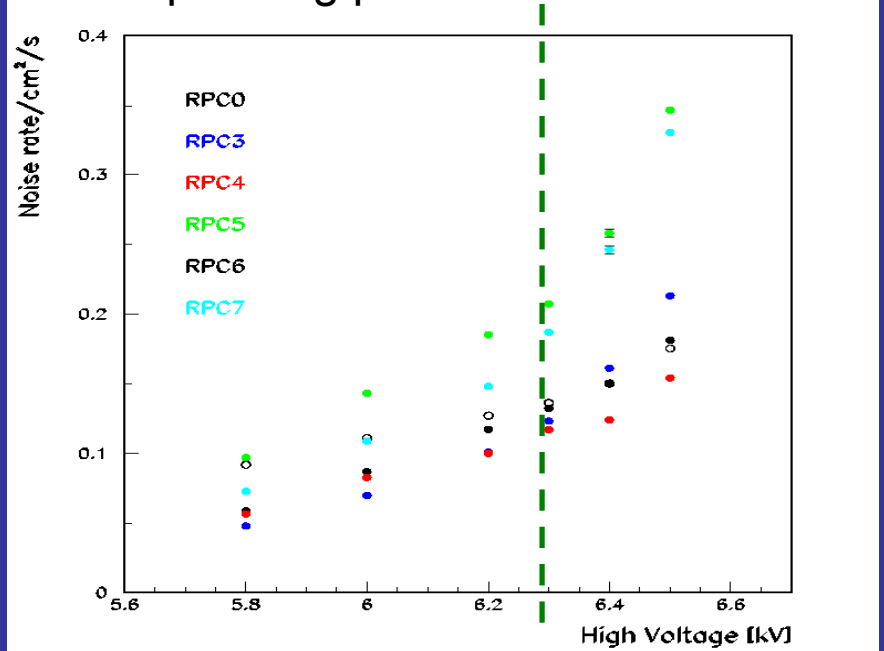
Measurement of the Noise Rate

The noise rate was measured using the self-trigger data acquisition mode of the DCAL chip.

Operating point: 0.1 – 0.2 Hz/cm^2



Operating point: 0.1 – 0.2 Hz/cm^2

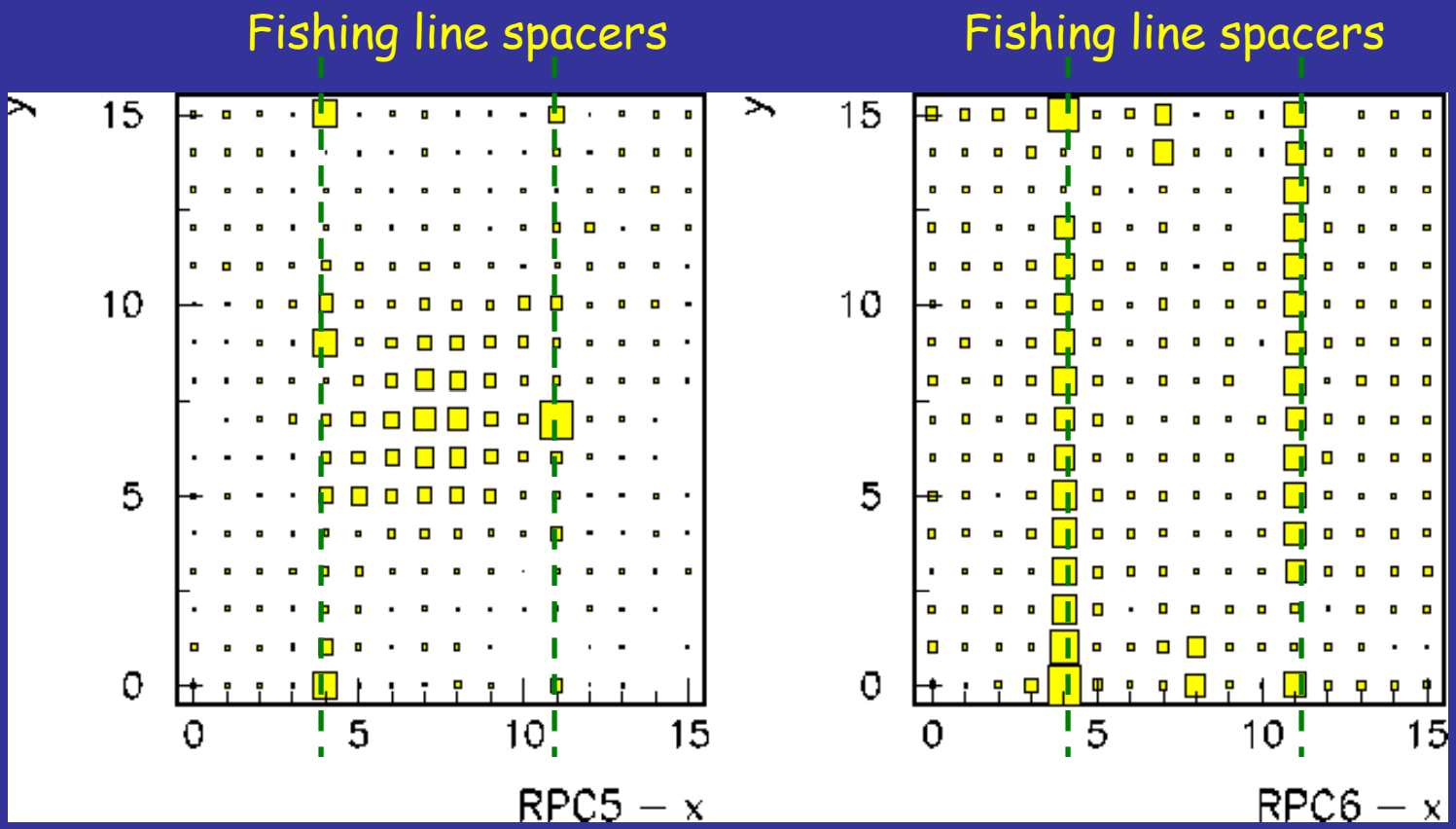


The measurements were performed with a high voltage setting of 6.3 (6.0) kV, for the default (exotic - RPC6) chambers.The rate at our default threshold setting of 110 DAC counts corresponds to about 0.15 Hz/cm^2. Extrapolated to a calorimeter with ~50·10^6 channels, this rate in turn corresponds to 0.2 hits/event. With the high voltage to the chambers turned off the noise rate was found to be less than 4·10^{-5} Hz/cm^2.

The measurements were performed with a threshold at 110 counts. The high voltage values for the exotic chamber (open circles) were set at 300 V less than indicated in the plot.

Measurement of the Noise Rate

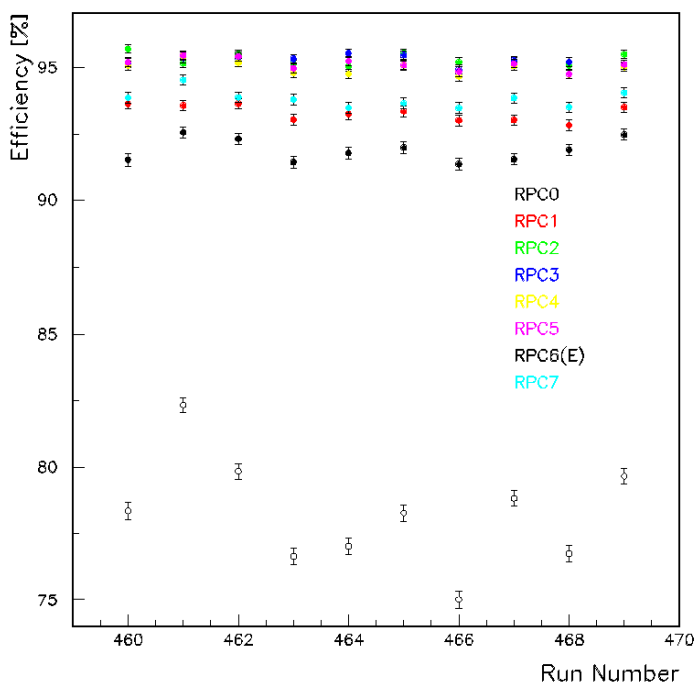
H.Weerts

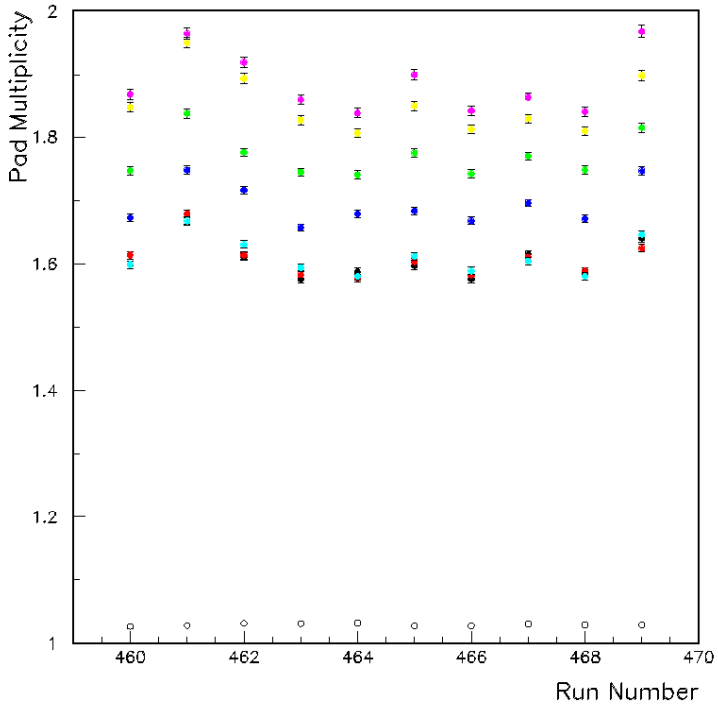


x – y map of the noise hits for a typical default (RPC5) and the 'exotic' (RPC6) chamber. A clear clustering along the fishing lines located approximately at x = 4.2 and 10.7 is visible.

Measurements with Cosmic Rays

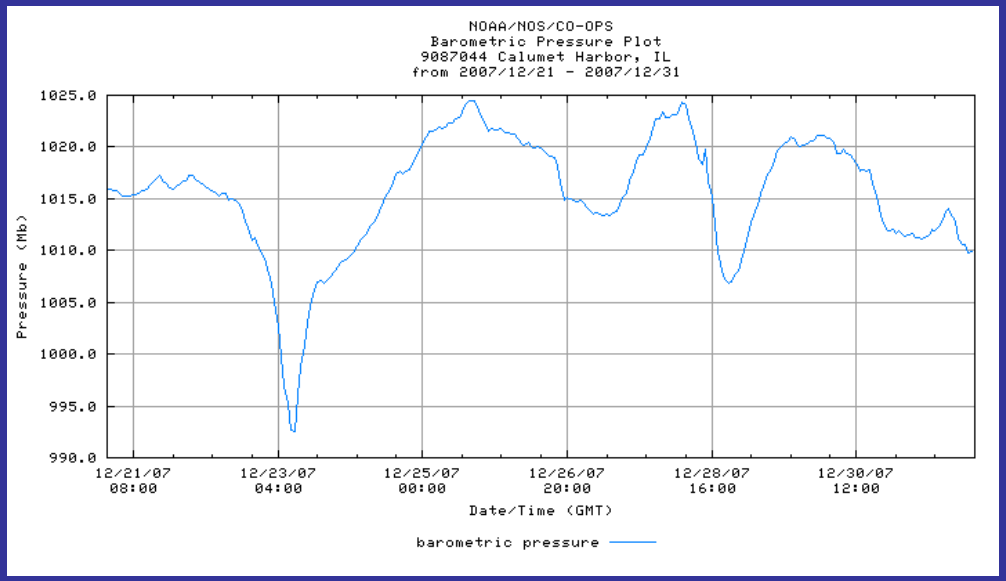
H.Weerts



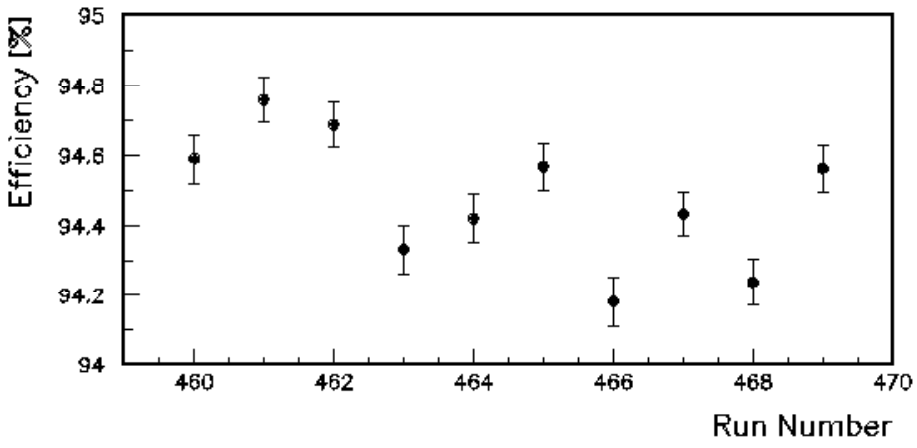


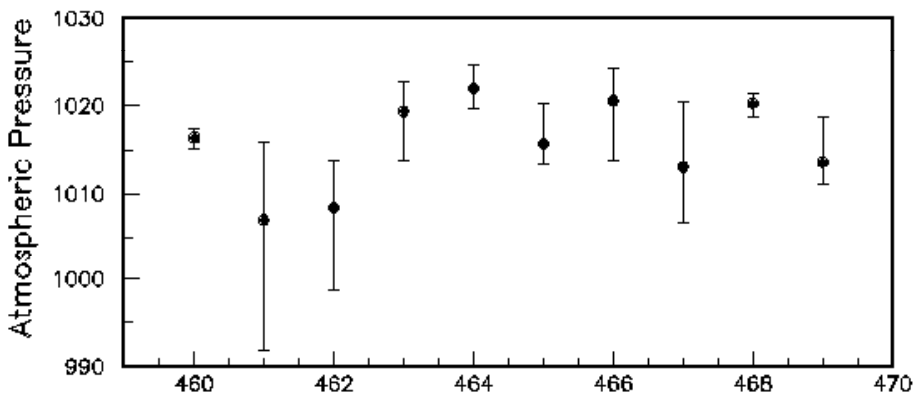
Noticed correlation in efficiencies and pad multiplicities

10 days



Barometric pressure at Calumet Harbor, IL

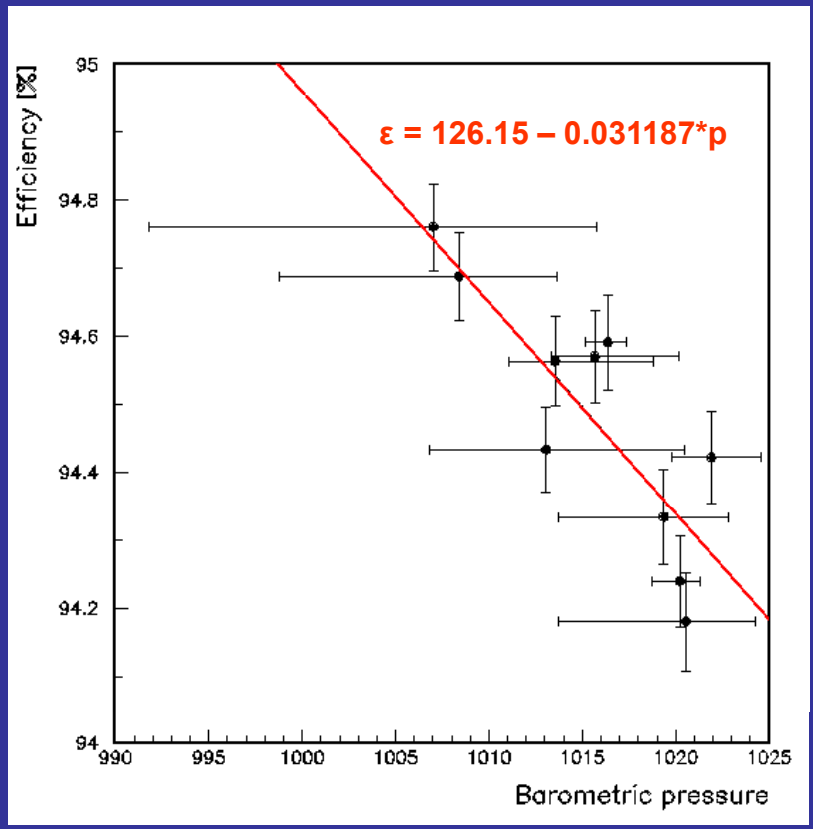




Error bars on pressure show range

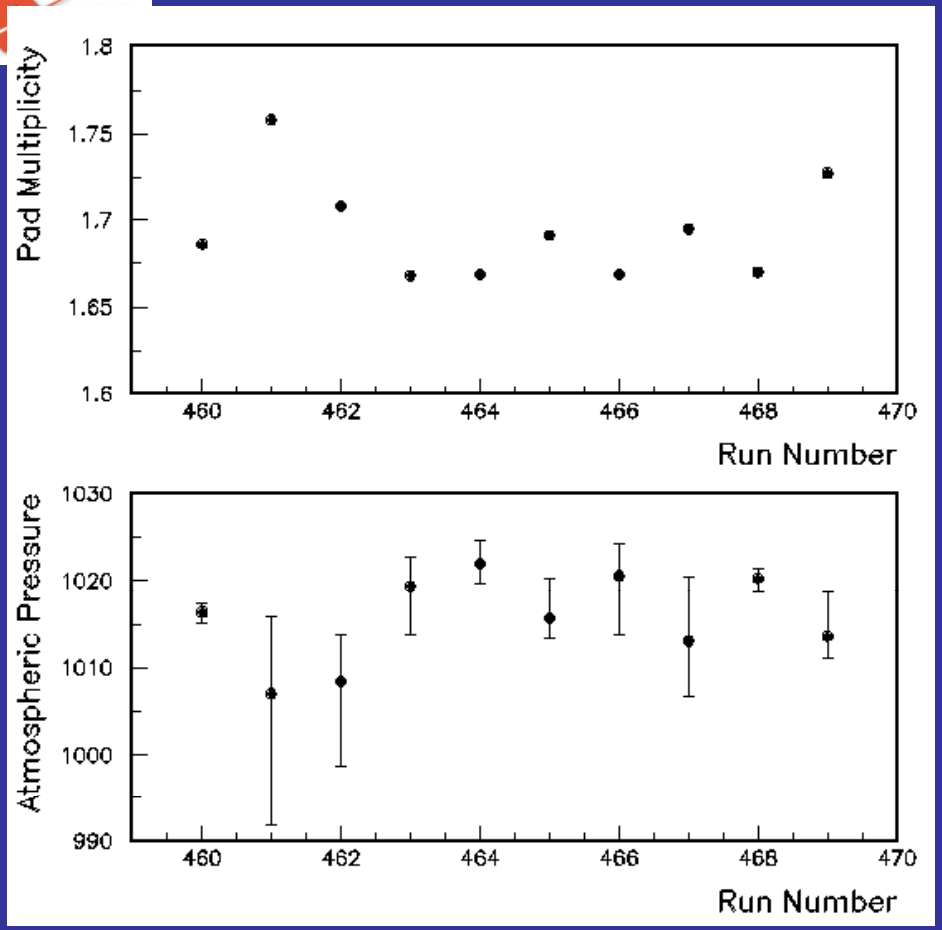
Average over all non-exotic chambers

Higher pressure → lower efficiency



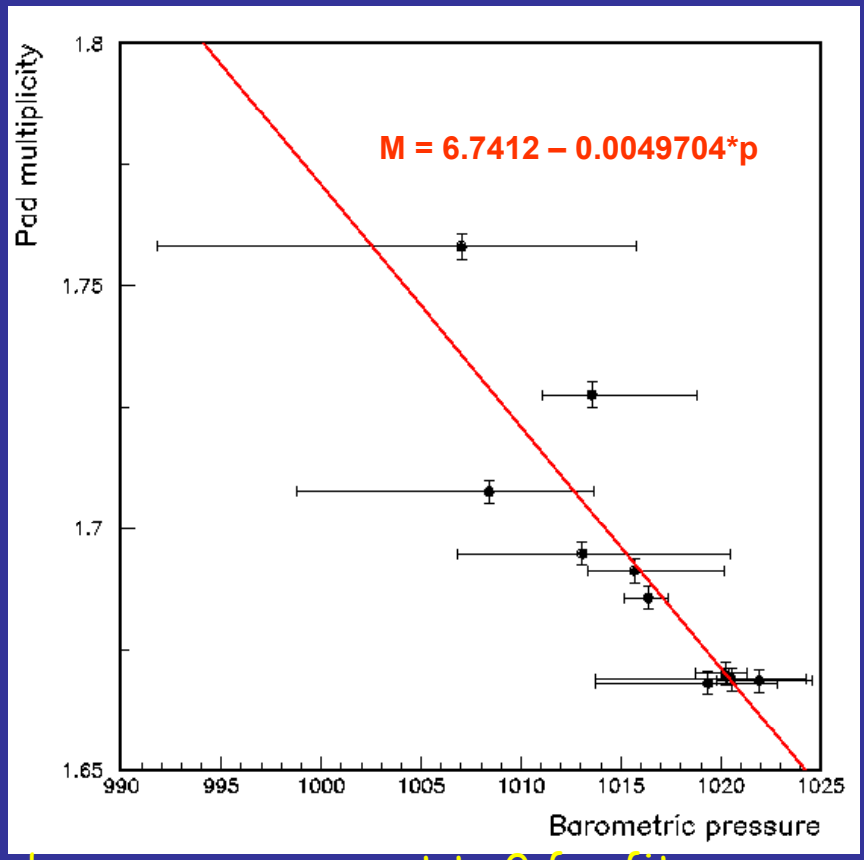
$\Delta\varepsilon/\varepsilon = -0.34\ \Delta p/p$

Error bars on pressure set to 0 for fit



Average over all non-exotic chambers

Higher pressure → lower multiplicity



Error bars on pressure show range

$\Delta M/M = -3.0\ \Delta p/p$

Error bars on pressure set to 0 for fit

DHCAL as a calorimeter

measurement of positron shower
and pion shower

Will be short on this; presented several times already

Analysis of Positron Data

H.Weerts

Two independent analyses

a) Study of energy response
b) Study of longitudinal development

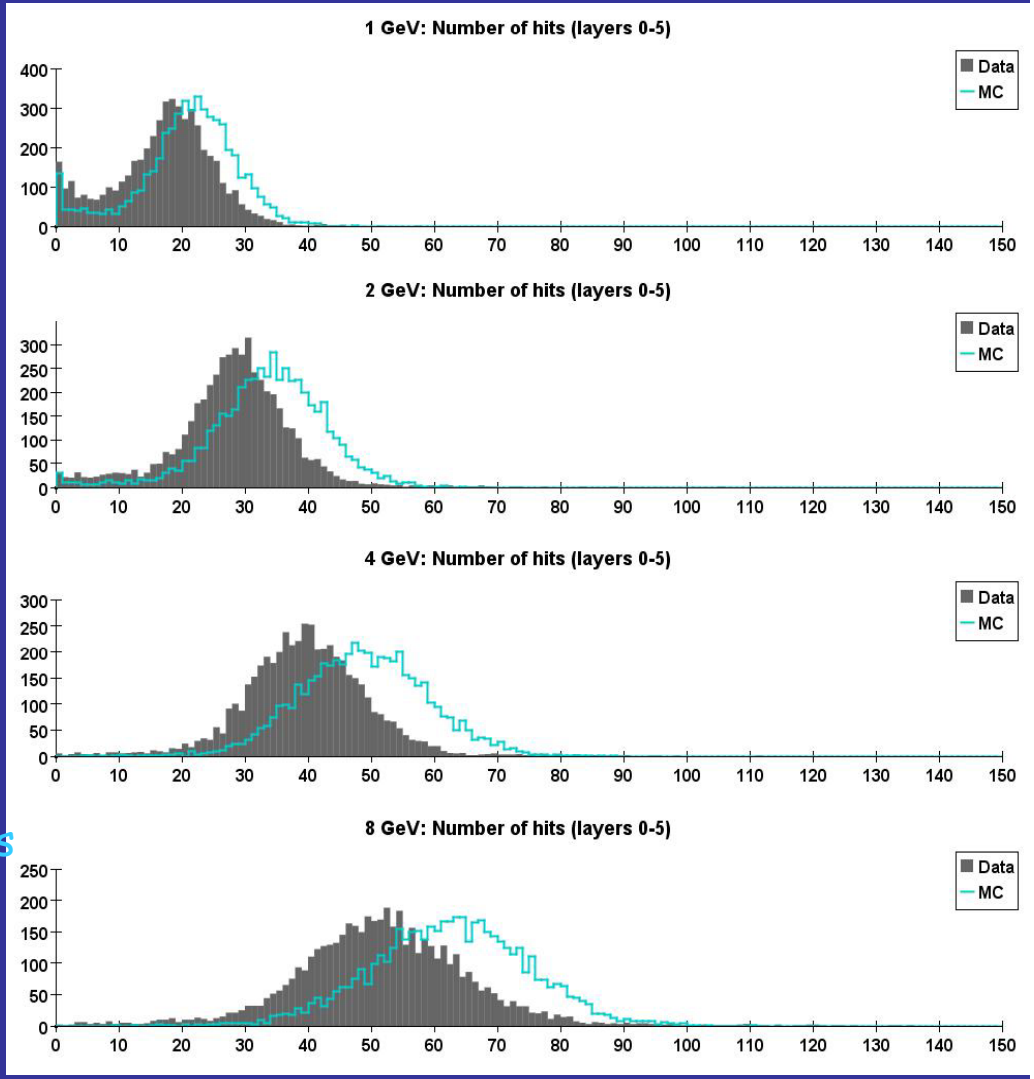
→ Results still very preliminary

Data sample

- Data at 1, 2, 4, 8, and 16 GeV

Monte Carlo simulation

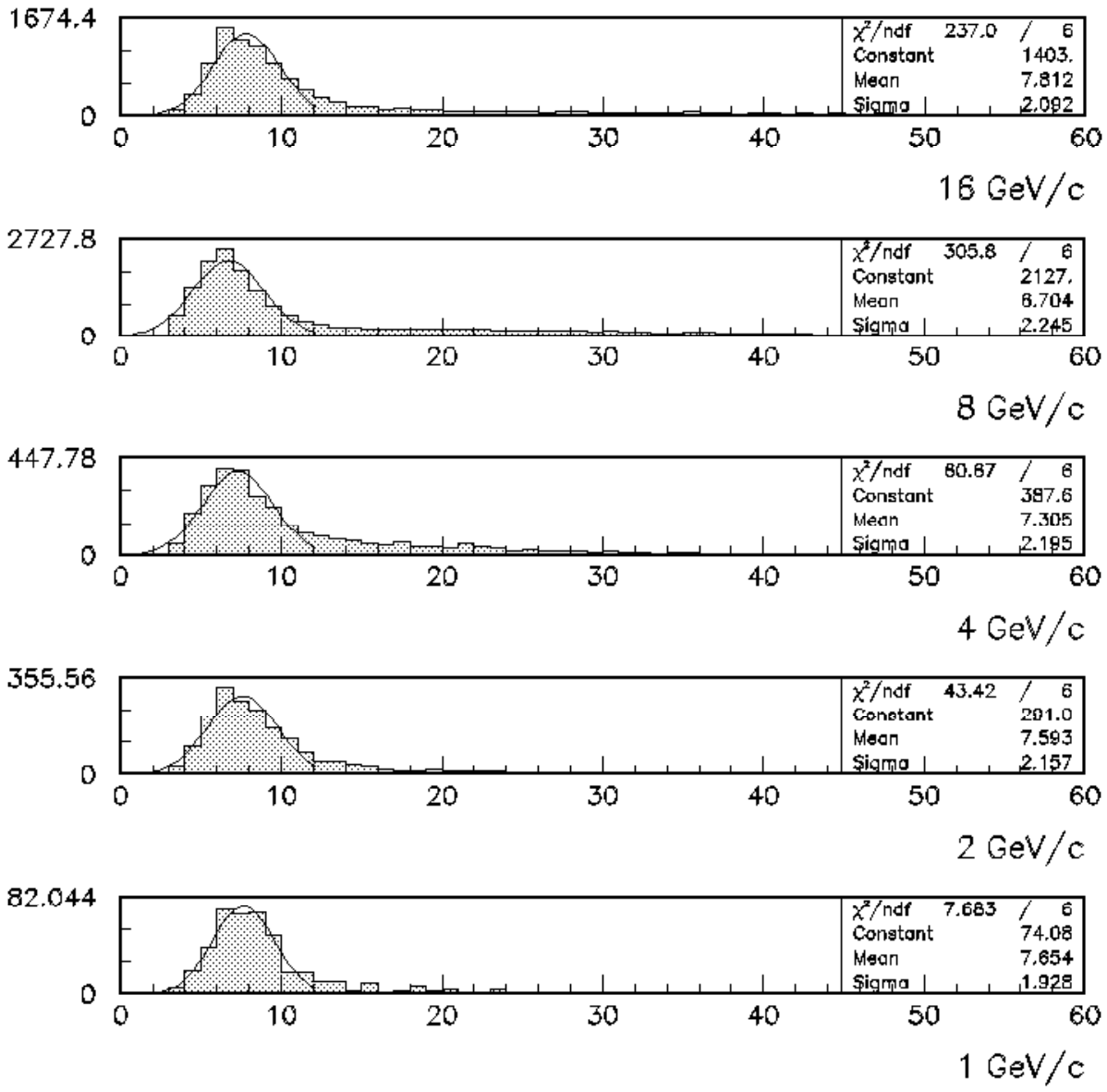
- Needs calibration constants from μ-runs
- Needs careful implementation of pad multiplicities
- Current comparison based on assumptions and ignoring details



Pion Analysis

H.Weerts

Hit distribution: MIP-like events (muons and non-interacting pions)



Data selection:

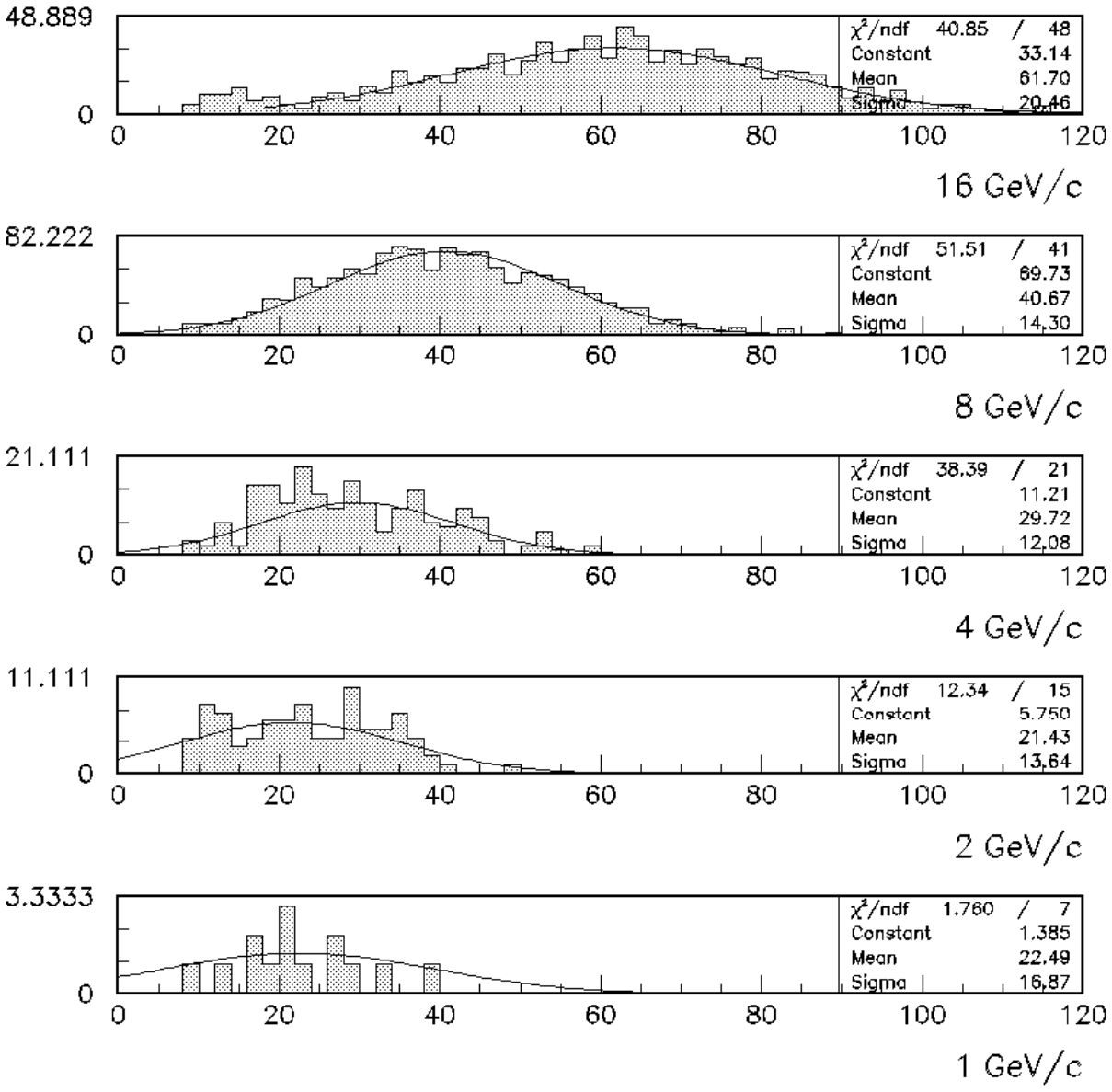
Exactly one cluster in first layer
Distance R< 5
Number of hits in first layer <5
Number of hits in second layer <5

Nice MIP peaks

Some contamination from 'late' showers

Hit distribution: showering events (shower starts at ~ 1 – 2 layers)

H.Weerts



Data selection:

Exactly one cluster in first layer
Distance R< 5
Number of hits in first layer <5
Number of hits in second layer >4

Some MIP contamination at 16 GeV/c

Not much data at 1 and 2 GeV/c

System stability
Electronic noise
Readout errors

System stability

- RPC stack has been running since July, 2007
  - Running 24/7 up to now (~9 mons), with very few interruptions
  - Most tests with 8 RPCs (max: 9, min:6), ~ 2k channels
  - Readout system is very stable
  - RPCs are also very stable
    - Produced 12 RPCs (including 1 exotic) for Slice Test
    - 1 physically broken during a display
    - 1 paint layer damaged by humidity at MTBF (other chambers used different paint, immune of the problem)
    - 2 RPCs accidentally 'damaged' by impure gas
      - "damage" = regional higher noise rate, but otherwise OK to use
    - All other (8) RPCs are problem free (including the exotic!)
      - Noise levels (aging indicator) are very low and very stable!
- Electronic system has amazing noise performance
  - Electron noise floor at Thr = 10 – 15 DAC cnts (low gain, HV off)
  - Normally running at Thr ~ 110 DAC cnts

Data Error: current status

H.Weerts

- Most errors have been successfully eliminated through system improvement
  - Improved grounding
  - Improved detector noise
  - New firmware
- Only one data error left – under study
  - Originally thought it was not harmful
  - Recent tests shows that system drop data packages (trigger timestamp AND hit data) at ~0.5% level
  - Extensive tests started recently (identified the problem on a single piece of the readout system)
  - Expect to solve the problem in the near future – then we will have a PERFECT (fully debugged) readout system

Long term running & availability of VST has been critical

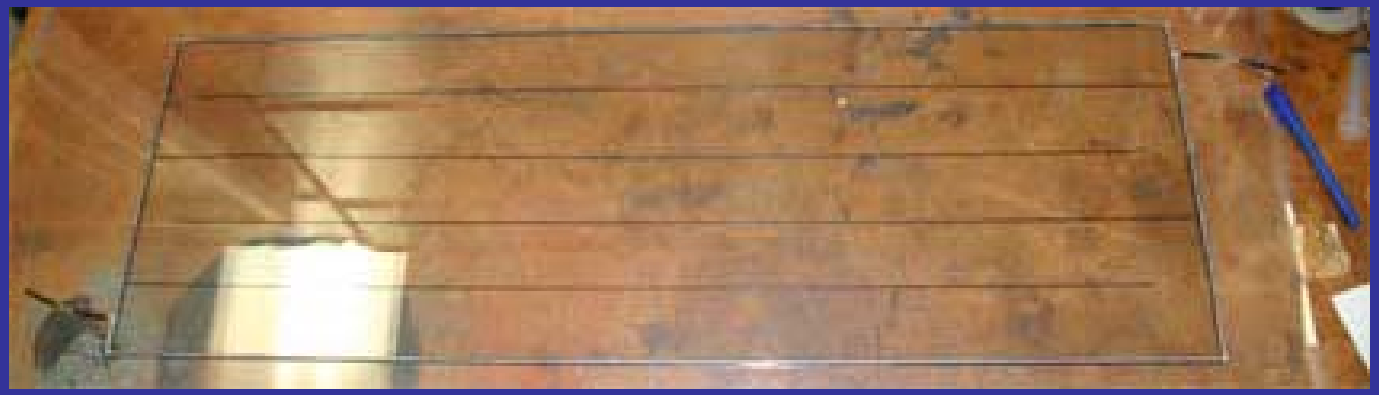
With a fully debugged VST readout, we are confident in building $1m^3$

Full size RPC prototype chamber dead area

Large RPC production: 1st RPC (almost) done

H.Weerts

- 1st full size RPC constructed for 1m^3
  - Used 1.2mm glass, 96cm x 32cm (VST: 1.1mm glass, 20cm x 20cm)
- Slightly modified assembly procedure works for large chamber
  - Chamber is gas tight (~ 5 meters long glue trace!)
  - Chamber is relatively stiff, deformation doesn't affect gas tightness
  - Good for large scale production
- Chamber dead area: 4.7%
  - Frame: 3.3% (irreducible, unless go for larger chamber)
  - Fishing line: 1.4% (can be reduced, if use other spacer)
  - Not including HV connector and gas tubing (supposedly sit in gap between modules in a real detector

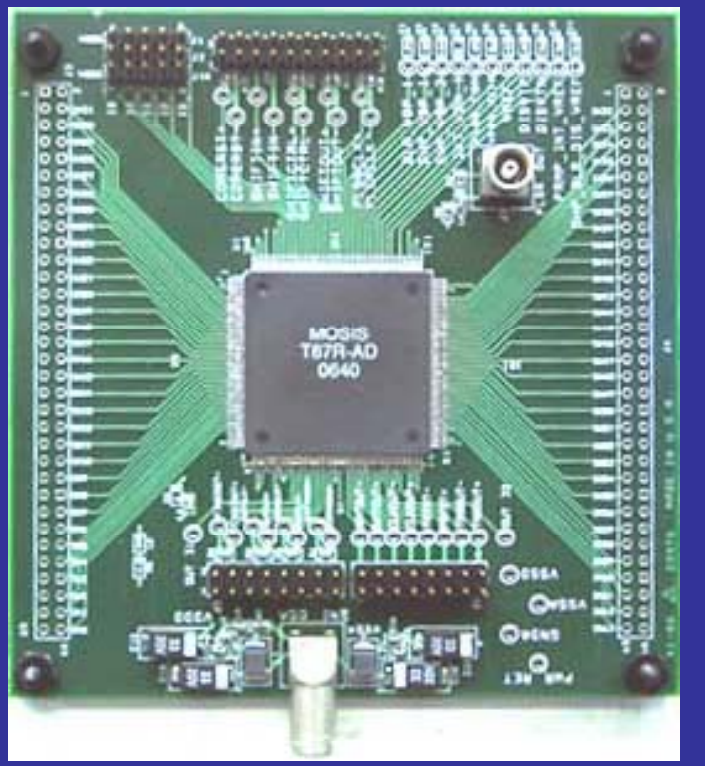


Further R&D

Last DCAL modifications before production

H.Weerts

- 50% data lost when output buffer is empty
  - Not a problem in triggered running
  - Simple bug in ASIC logic: identified, corrected and simulated
- Noise introduced by internal test lines
  - OK for RPC, fixed for ASICs on GEM board
  - Simple fix in chip packaging
- Problem with mask register and CI-mask register
  - Original design use asynchronous clear -- more sensitive to noise
  - Improved detector to reduce noise
  - Modify ASIC: needs some design time (~1 week)
- Problem with slow control readout
  - A bug in the ASIC prevents daisy chaining slow control readout – addressed in FE board design
  - Trivial change already implemented

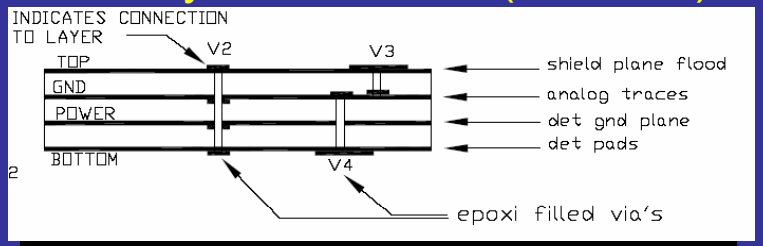


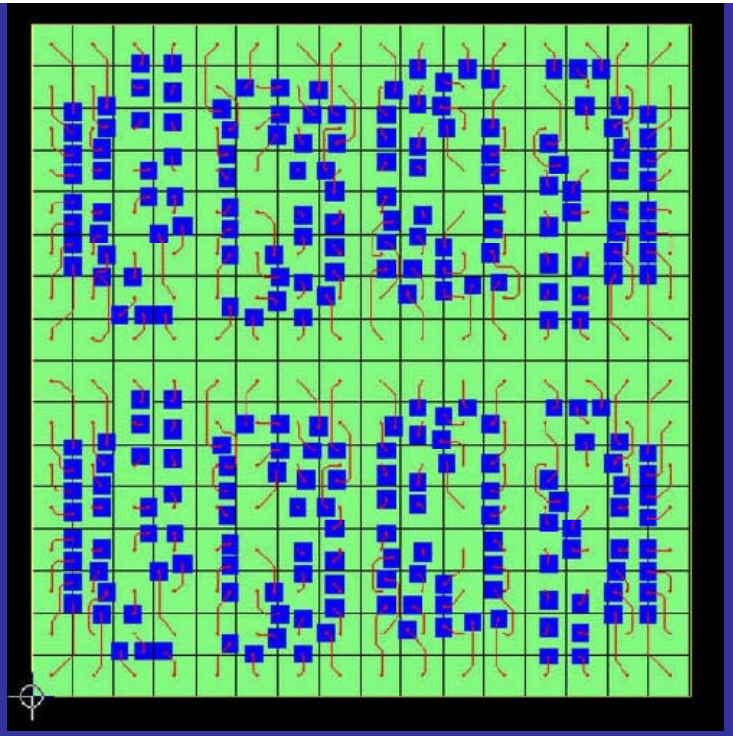
No more prototype run needed before chip production

Current Pad Board & Front End Board **Design**

H.Weerts

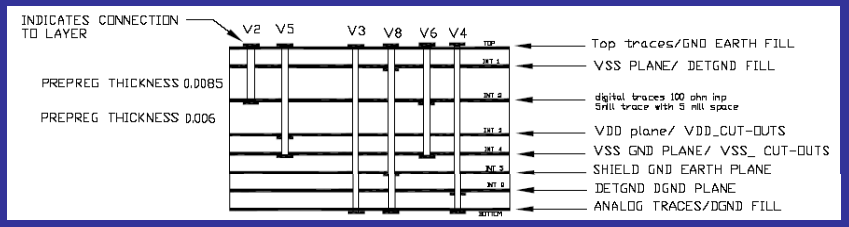
4-layer Pad-board (3 shown)

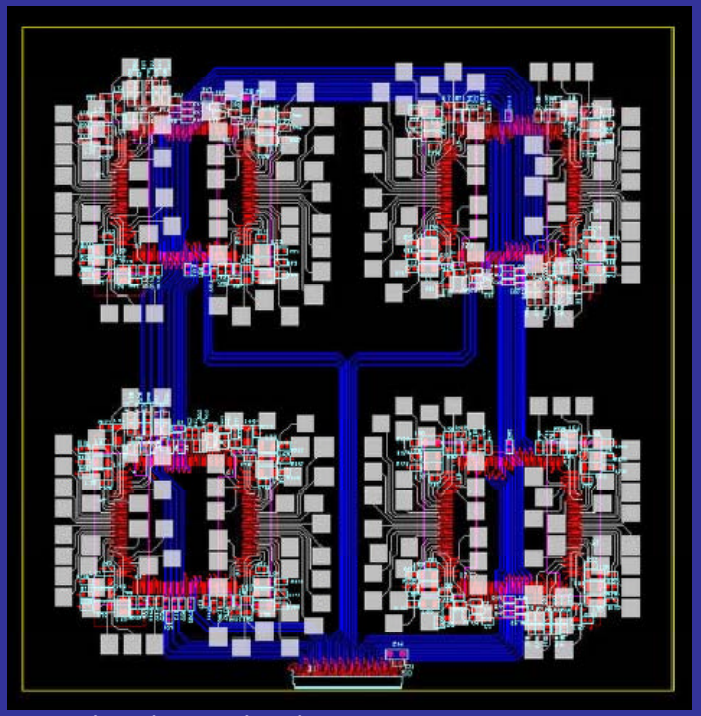




Blind vias to route sensitive signals to glue pads – needed to minimize contact with digital lines in FEB

8-layer FE-board (3 layers shown)





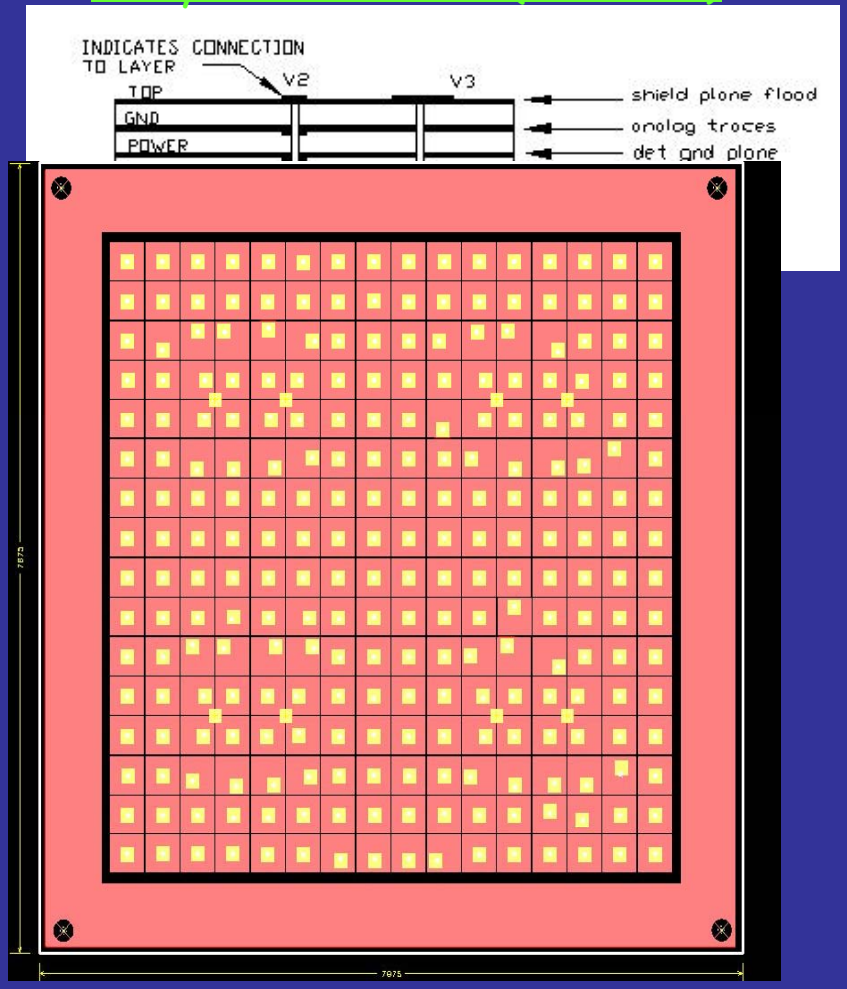
Also has blind vias
→ Very complex board design to minimize crosstalk & digital noise pickup

- Current design has extremely good noise performance
  - Noise floor: only 10 – 15 ADC count (low gain)
  - System comfortably runs @ 30 ADC count or even lower (normal runs @110 ADC count)
  - Left a lot of head room for cost reduction
- Have designed new 16 cm x 16 cm FEB with ***NO*** blind vias
  - Still 8 layer
  - Still has ground shielding layers to protect charge signals
  - Primary change: now ALL vias come down to glue pad layer (bottom)
- Have designed ***Two*** new 16 cm x 16 cm Pad Boards also with ***NO*** blind vias
  - One is 2 layer, with no internal ground plane
  - One is 4 layer with 2 internal ground layers

New Pad Board & Front End Board Design

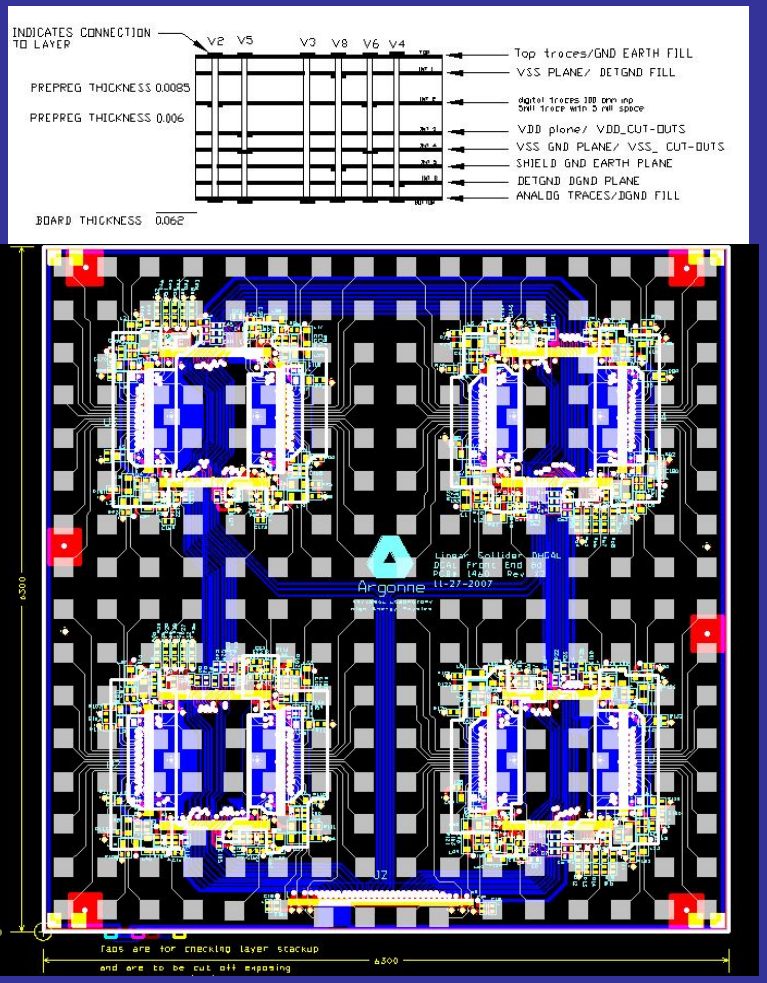
H.Weerts

4-layer Pad-board (3 shown)



No blind vias

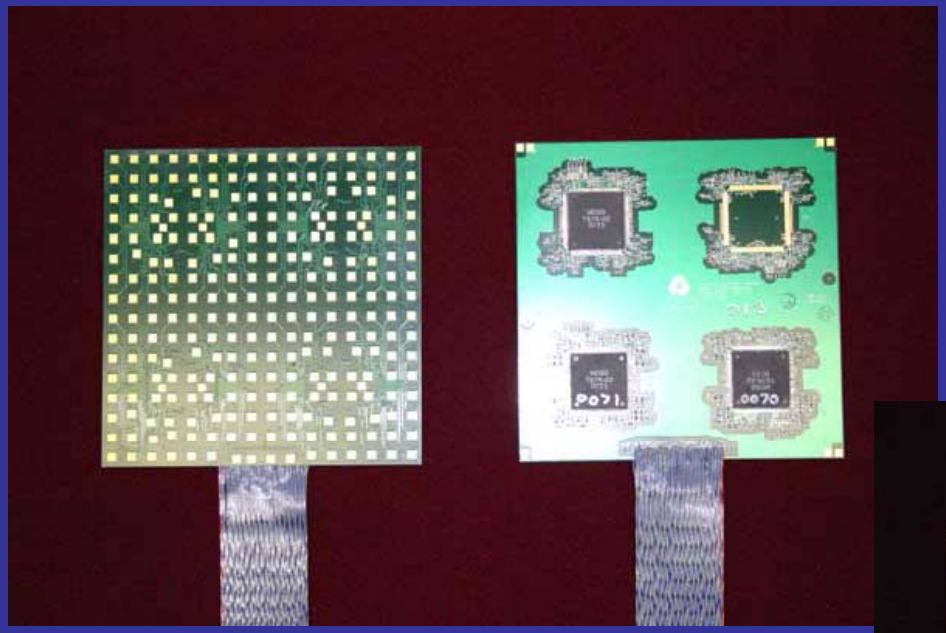
8-layer FE-board (3 layers shown)

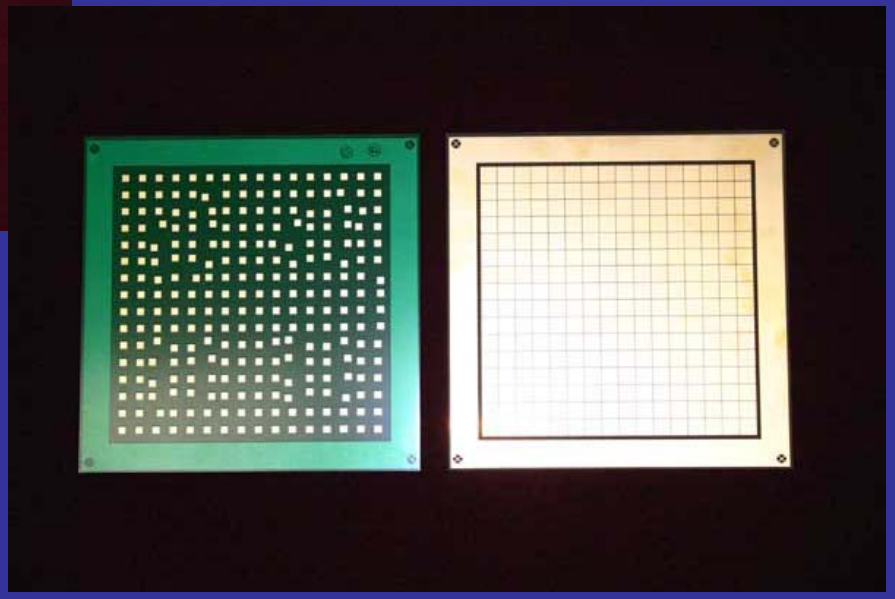


No blind vias

New Pad Board & Front End Board

H.Weerts

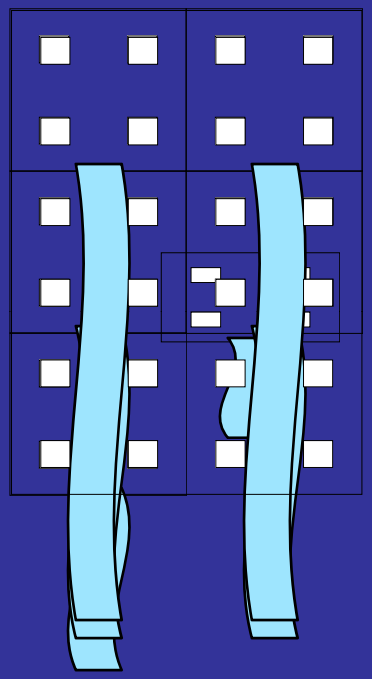




Boards are manufactured, being stuffed and tested

FEB – Current Thinking

- If the new design is successful, we can make larger boards:



⇨*Could not make larger boards before with blind vias – Too Difficult*

⇨ *Larger boards are cheaper, eliminates cables & connectors, reduces impedance mismatches, improves reliability, etc.*

Cost

Assuming new design of Pad/Front-end boards is viable
Includes labor and M&S

In US$	10 layers			40 layers		
Item	Cost	Contingency	Total	Cost	Contingency	Total
RPCs	16,000	4,000	20,000	34,000	8,000	42,000
EDIA	70,000	0	70,000	70,000	0	70,000
DCAL	202,000	24,000	226,000	311,000	54,000	365,000
FEB	36,000	18,000	54,000	*134,000*	67,000	201,000
DCON	11,000	5,000	16,000	26,000	13,000	39,000
PadB	11,000	6,000	17,000	*43,000*	21,0000	64,000
DCOL	18,000	9,000	27,000	80,000	40,000	120,000
Misc	14,000	7,000	21,000	54,000	27,000	81,000
Total	378,000	73,000	451,000	752,000	230,000	982,000

With Pad/Front-end boards from the VST → add ~$290,000 + contingency (40 layers)

Reduction from: 424K → 134K (factor of 3)

Substantial reduction from original estimate because of VST work

Plans

Under all circumstances

Will complete ongoing studies
Will publish results from Vertical Slice Test

Instrumentation paper puiblished in IEEE
Muon calibration paper (almost) accepted by JINST
Positron response paper – analysis complete, simulation needed, draft in preparation
Pion response paper – analysis complete, simulation needed
RPC rate measurement – not initiated yet

Assuming availability of funds

Will complete changes to DCAL chip and will produce chips
Will start assembly of large chambers
Will complete design of integrated Front-end boards and Data Concentrators
Will produce entire readout system

→ ready for test beams in early 2009

Have received funding for FY08(last week): $290K to start

Goal: be part of CALICE HCAL @ FNAL in 2009

Summary

VST was very successful (system now virtually error – free)

→ First evidence of viability of the Digital Hadron Calorimeter approach
→ Validation of technical implementation (chambers and electronic readout)
→ Results being analyzed and published
→ System very stable over period of 9 months

1 m^3 prototype section necessary to (extrapolation by x200)

→ Provide detailed measurements of hadronic showers with RPCs
→ Validate hadron shower models
→ Gain further operational experience

Readiness for construction

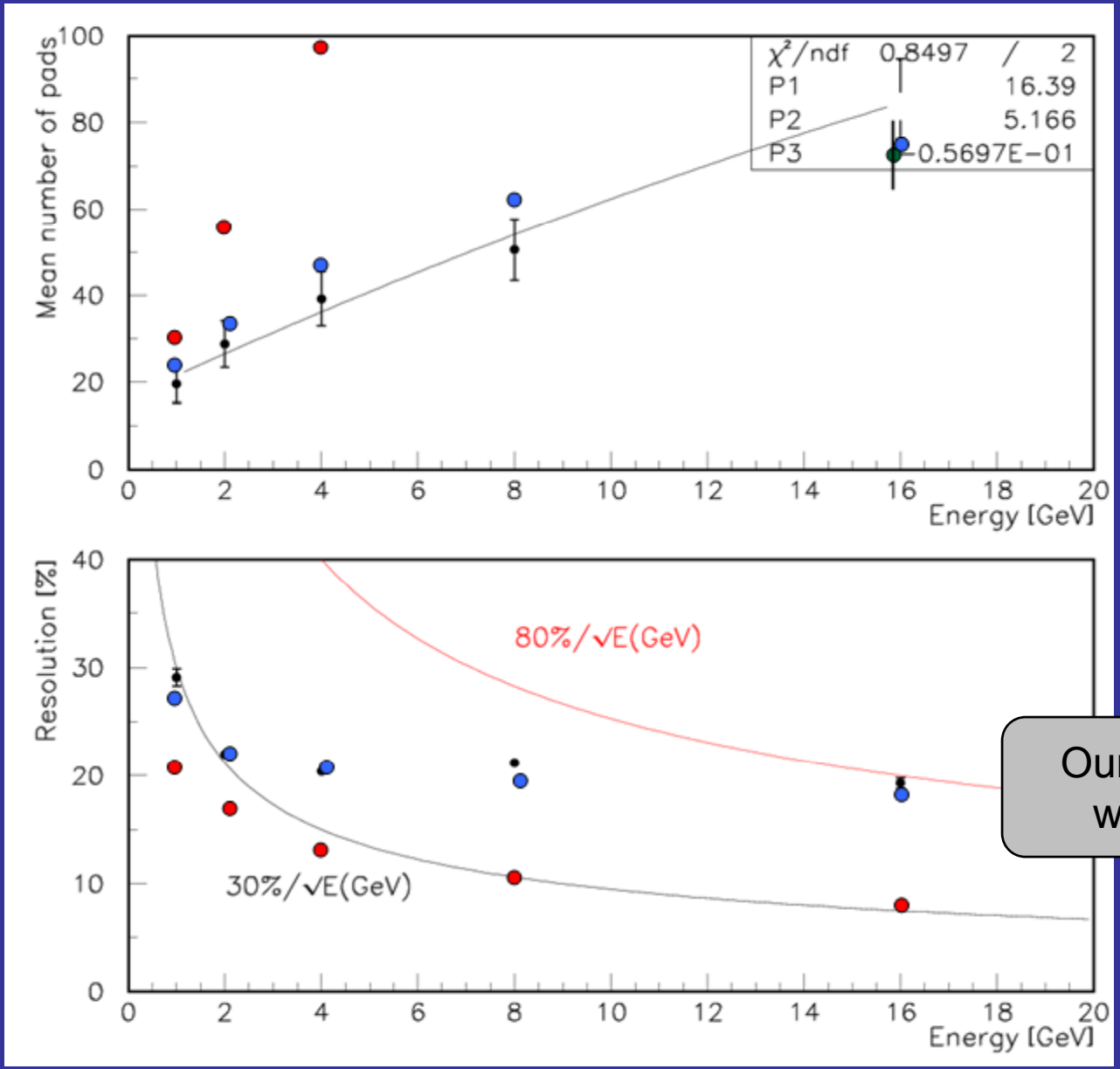
→ Larger RPCs (having been designed and constructed) now under test
→ Small modifications to DCAL chip still necessary (no prototyping required)
→ Second (and cheaper) iteration of Pad- and FE-boards being tested
→ Concept of merging of FE-board and Data concentrator being developed

Currently

→ Received partial funding; decide on path to take

THE END

Energy response and resolution for positron



Data with 6 layers

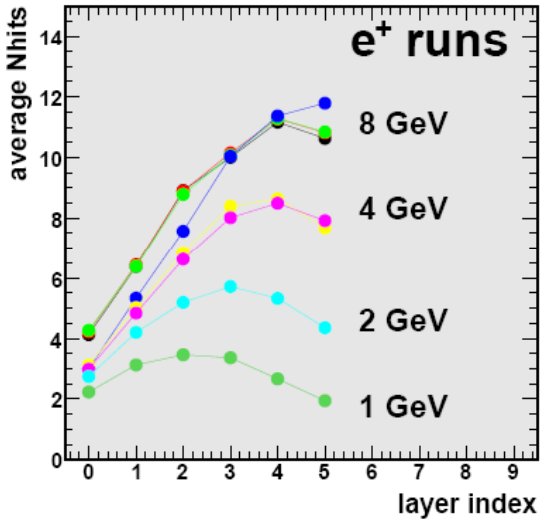
Monte Carlo simulation with 6 layers

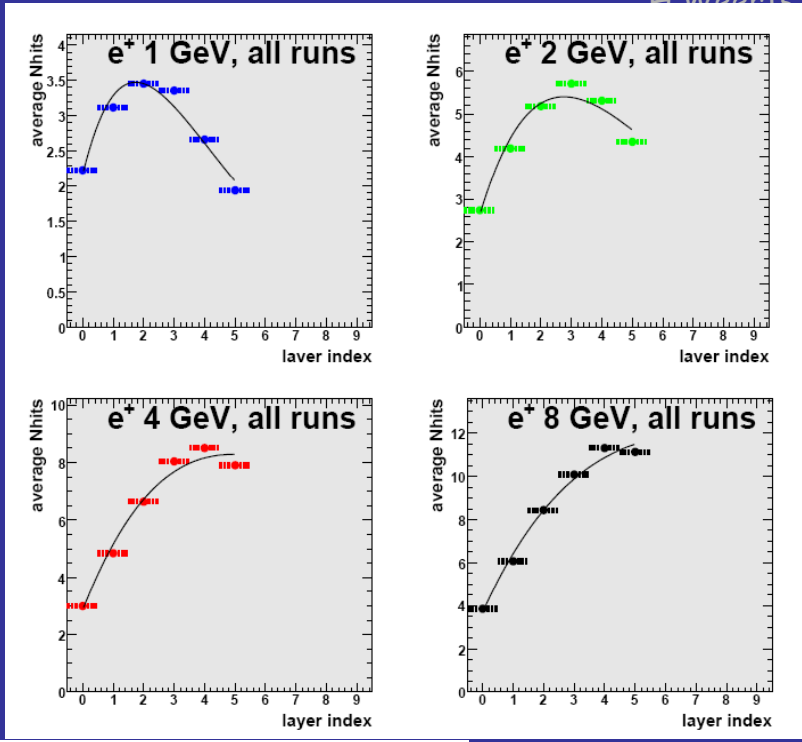
Monte Carlo simulation with infinite depth

Our little calorimeter stack works as a calorimeter

Shower longitudinal profiles

Shower maximum contained in 6 layers
Significant energy leakage (at higher energies)

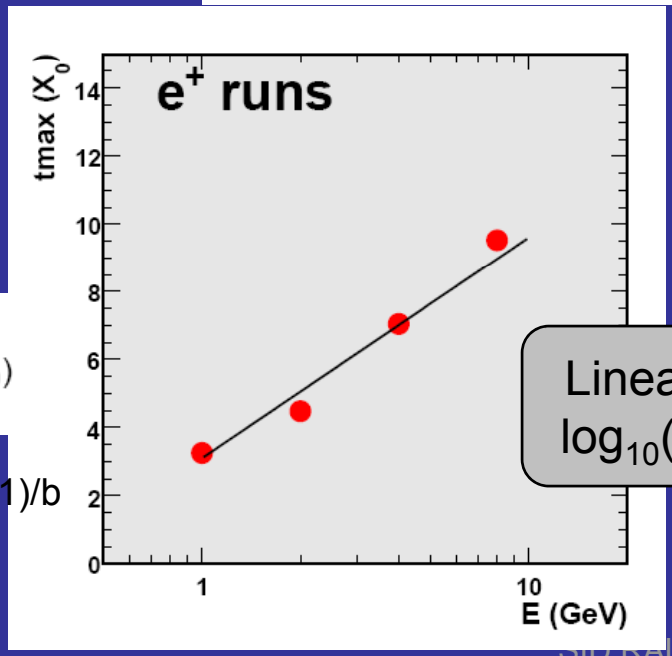




Fit to empirical formula

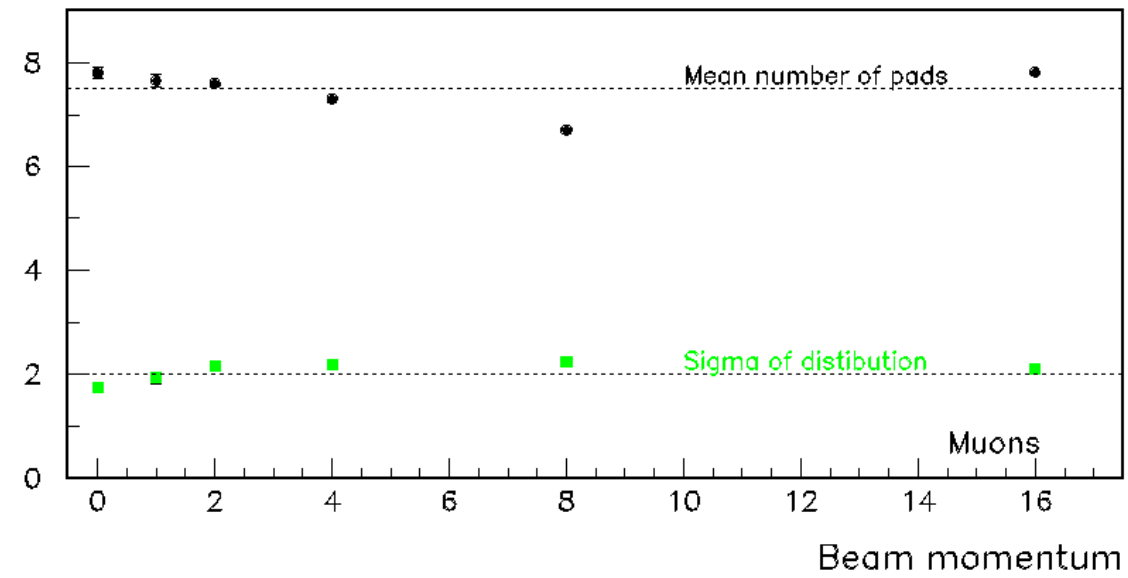
$$\frac{dE}{dt} = E_0 \cdot b \cdot \frac{(bt)^{a-1} e^{-bt}}{\Gamma(a)} \quad \text{(with } t = x/X_0\text{)}$$

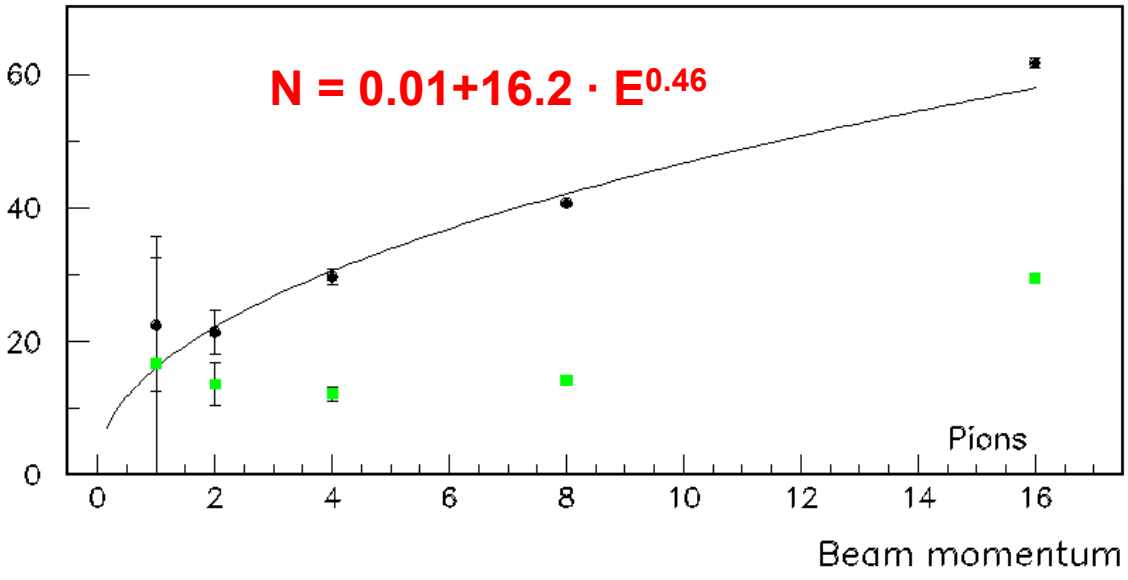
with the shower maximuma at t_{max} = (a-1)/b



Linear increase with $\log_{10}$(E) as expected

Linearity – Resolution





MIP-like events

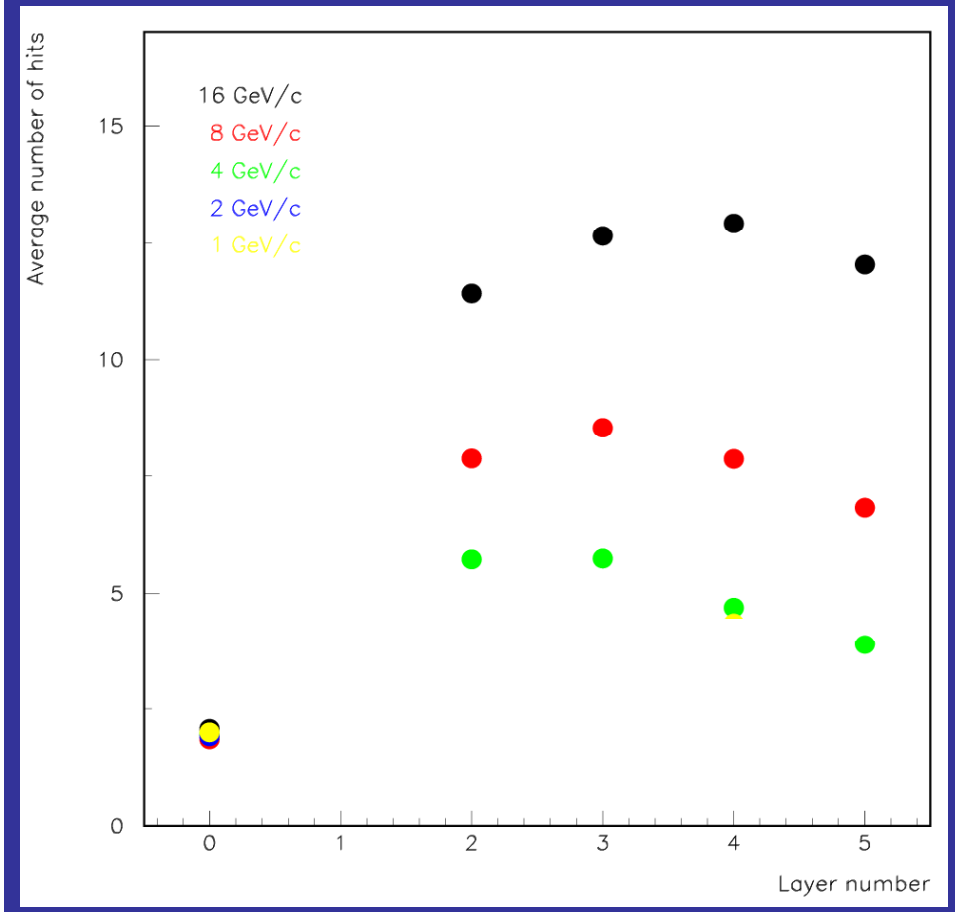
Reasonably stable

Brick run data shown at p = 0 (essentially all muons)

Showering events

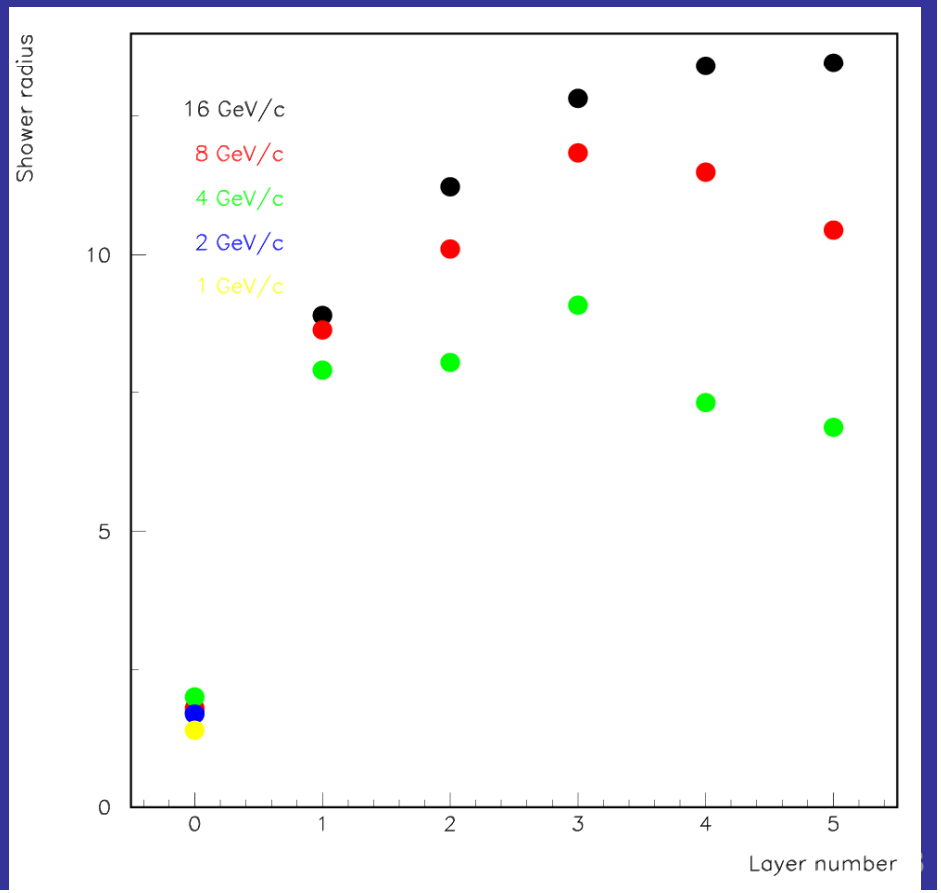
$N = 0.01+20.24 \cdot E^{0.44}$
(for positrons)

Pion runs – Average shower shape – Pion selection
(showering events)



Effect of cut on nhit>4 clearly visible for p ≤ 8

Statistics too poor for p ≤ 4



→ needs to be simulated

Data Error summary

H.Weerts

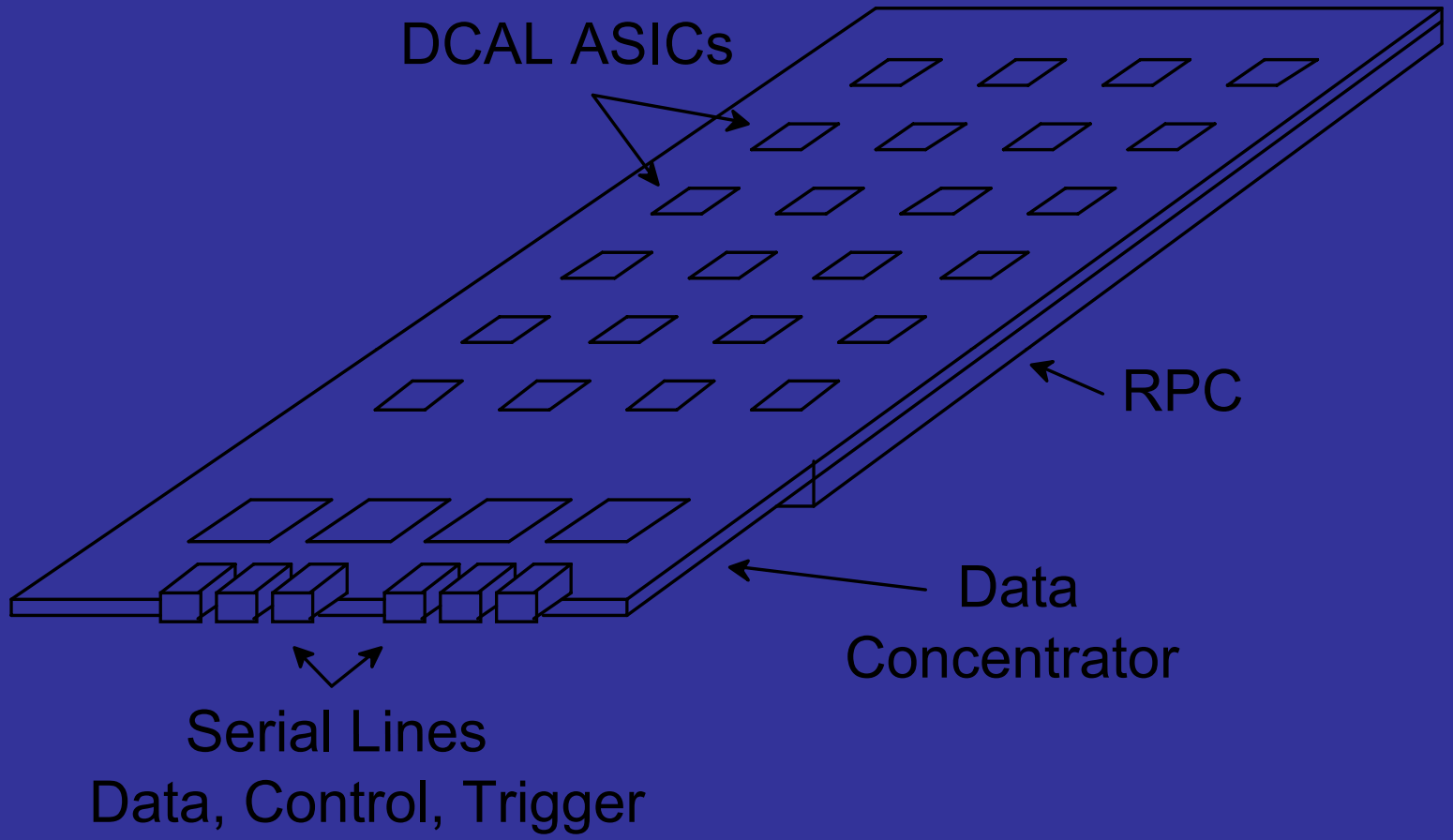
- All data/system errors were thoroughly studied
- An event reconstruction program was developed to build events correctly out of data with errors
  - Used to re-run all test beam data
  - Identify events with know data errors
- Known data errors: (~15 different errors)

Fatal Errors (bit definition): original data can not be recovered
bit 0: x beginning of run (BOR) events (or junk data at the beginning of a run)
bit 1: x end of run event (due to DAQ program, last event of a run may have lost data packages)
bit 2: x additional junk byte(s) (DCON error bits 1, 2, out of bound time stamp, non-matching time stamp)
bit 3: x fake trigger (only a few DCON shows up, with or without hit pattern)
bit 4: x "0" data + leading bit error
bit 5: x check sum error + reserved bit set
bit 6: x "0" time stamp (but other bytes are non-zero)
bit 7: x wrong time stamp (in DCON or in individual chips, wrong T > correct T)
bit 8: x trigger bit error (trigger bit bit[14][7] = 1, but hit patter != all 1's) (always have check sum error as well)

Non-fatal Errors (bit definition): original data can be recovered
bit 0: - wrong time stamp (in DCON or in individual chips, wrong T must be < correct T)
bit 1: x missing (a few) DCON in trigger timestamps
bit 2: x duplicate 16-byte data package
bit 3: x late trigger package (after some data package appeared, or even appears in the next event)
bit 4: x late data package (appeared in the next event)

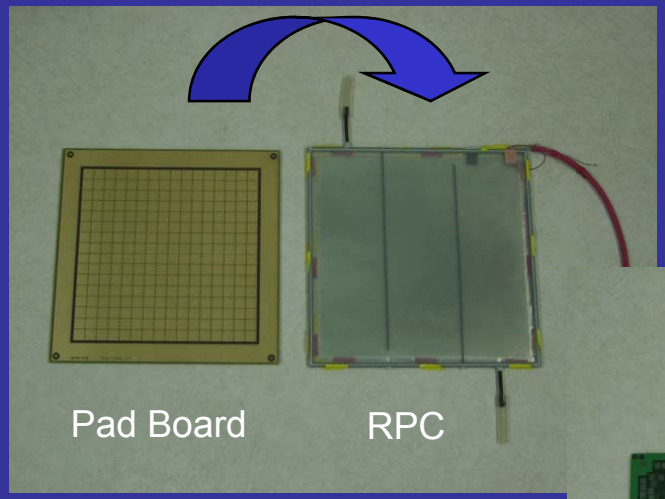
Other: (mostly in charge injection runs) fake counter reset

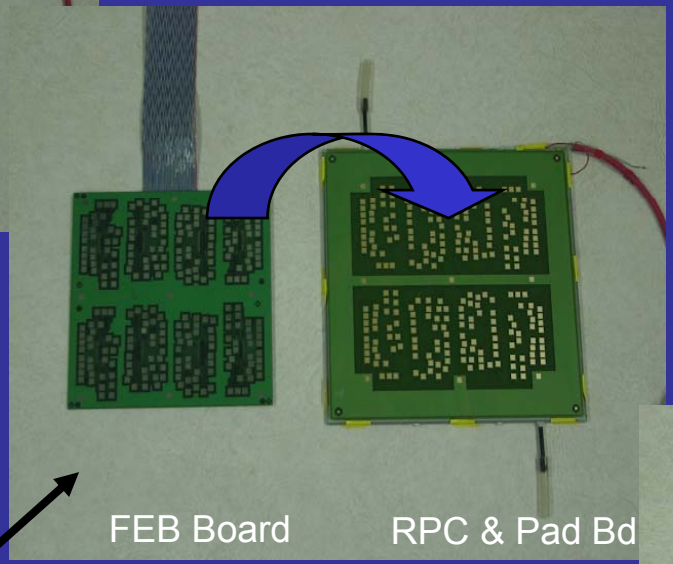
- Going a step further: Make FEB & Data Concentrator Monolithic…

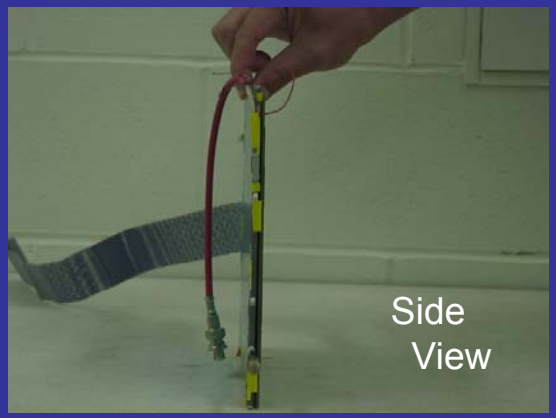


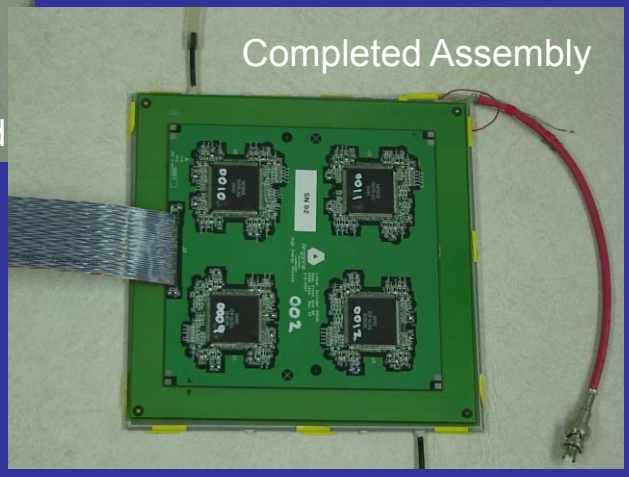
Vertical Slice Electronics Construction

H.Weerts









Assembled & Tested Beforehand
Use conductive epoxy to glue together

Large RPC production: frame extrusion

H.Weerts

- VST chamber frames are all machined
  - Very time consuming and labor intensive (costly)
  - Critical dimension can be controlled to ~ 10% accuracy
- $1m^3$ chamber frames will be extruded
  - Once setup, production is very cheap
  - Very good uniformity over long distance
  - Only need small amount of machining to cut into length/shape
- 1^{st} prototype run: ~3 weeks ago
  - Critical dimension controlled to ~5% accuracy over several meters
  - One non-critical dimension was off by over 10%
  - Sample used to produce the 1^{st} full size RPC for $1m^3$
- 2^{nd} prototype run: last week
  - All dimensions agree with spec
  - Will go for production (miles of them)

FEB & Data Concentrator – Work in Progress

H.Weerts

- New Data Concentrators – One services 24 chips
  - Idea: Column Architecture