SiD Vertex Detector

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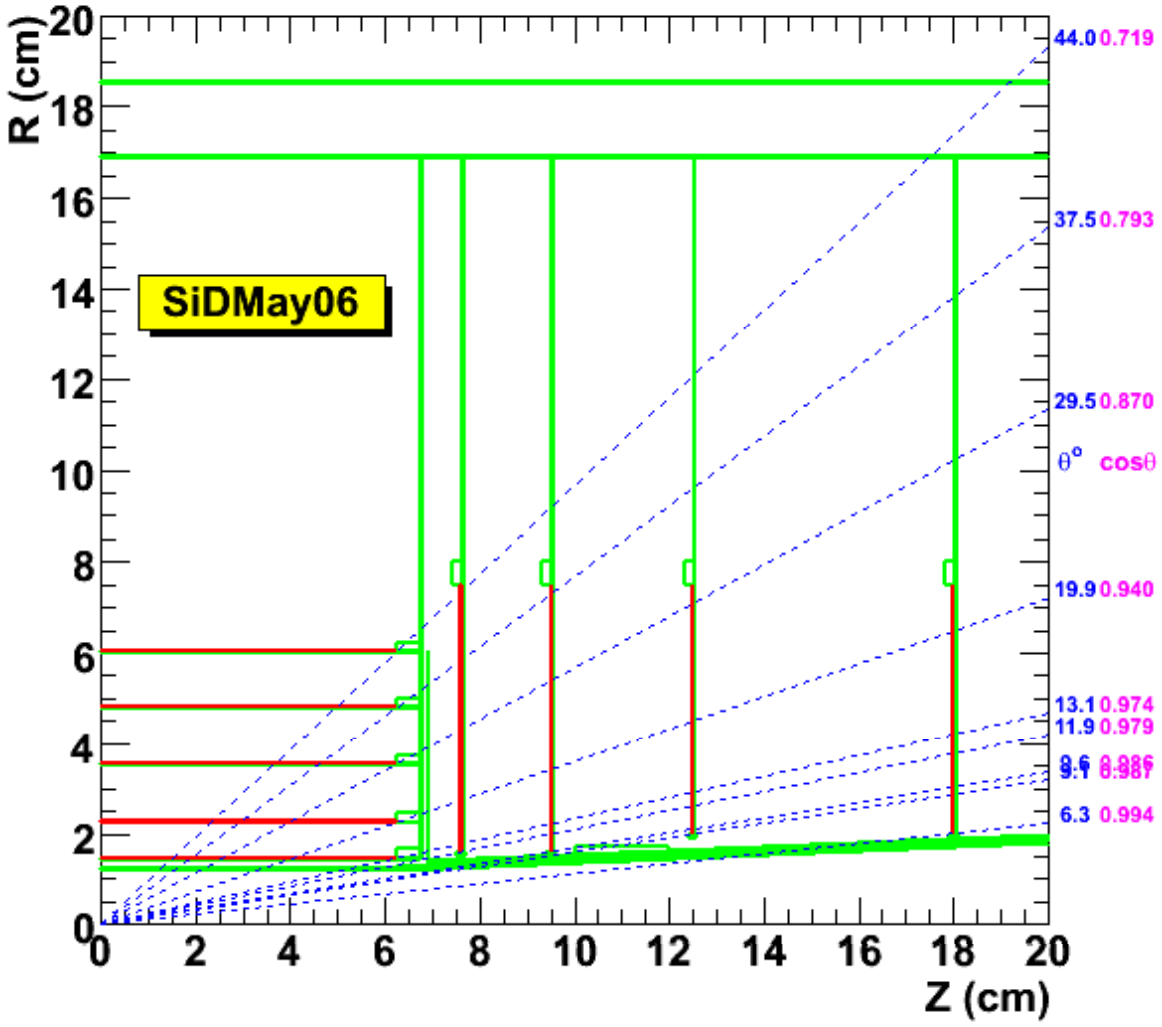
Outline

- Geometry
- General considerations
- Simulations

  – Most of slides taken from Ron Lipton’s talk at the SiD workshop in Abingdon, UK 14-16 April and Su Dong’s talk at ALCPG2007 at Fermilab, October 2007

SiD VXD Geometry



At ILC the forward region as important as central

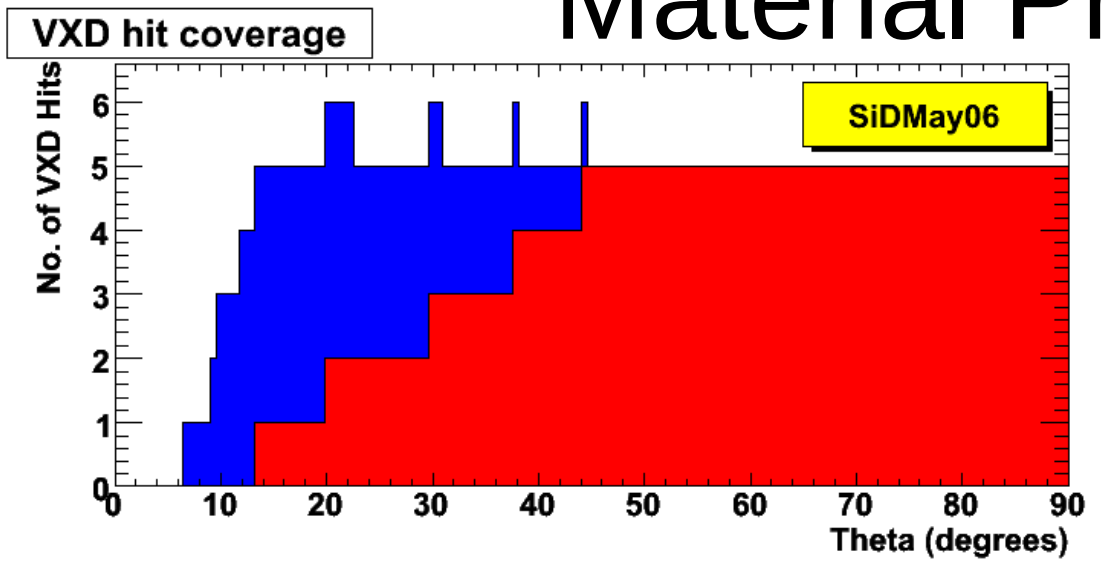
Barrel+endcap geometry to provide largest possible acceptance avoid shallow angle track entrance

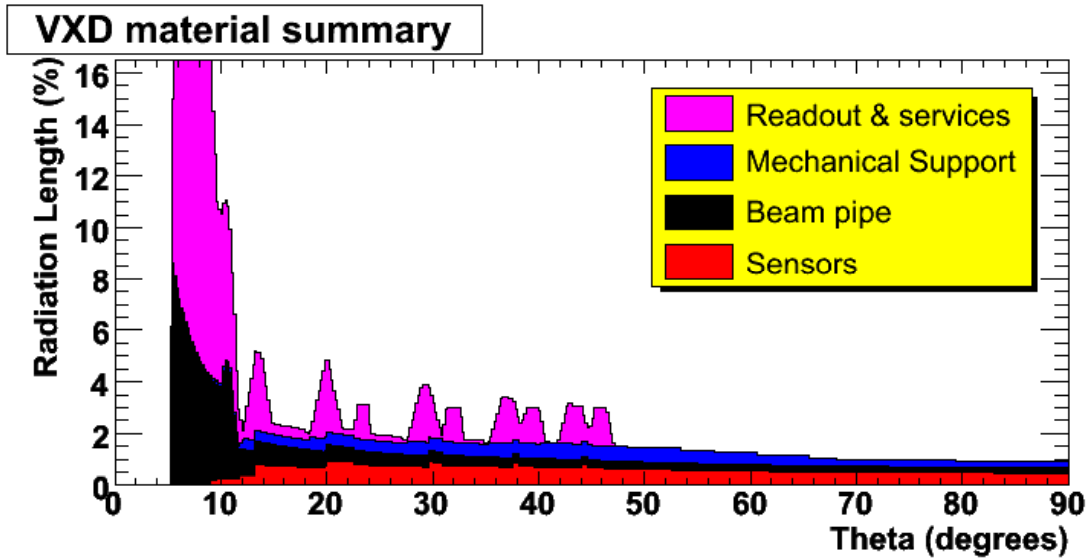
Trade-off for more demanding light weight support and service designs.

SiD Geometry Considerations

- No track at very shallow entrance angle. Full coverage of 5 VXD hits up to $|\cos\theta|\sim0.98$.
- Sensors has slightly thicker (e.g. 30μm) active region would not cause too much resolution degradation.
- Less fear in barrel wafer shape issues when pushing for thin ladders with a shorter barrel.
- Endcap sensors don’t care much about Lorentz effect

Material Profile



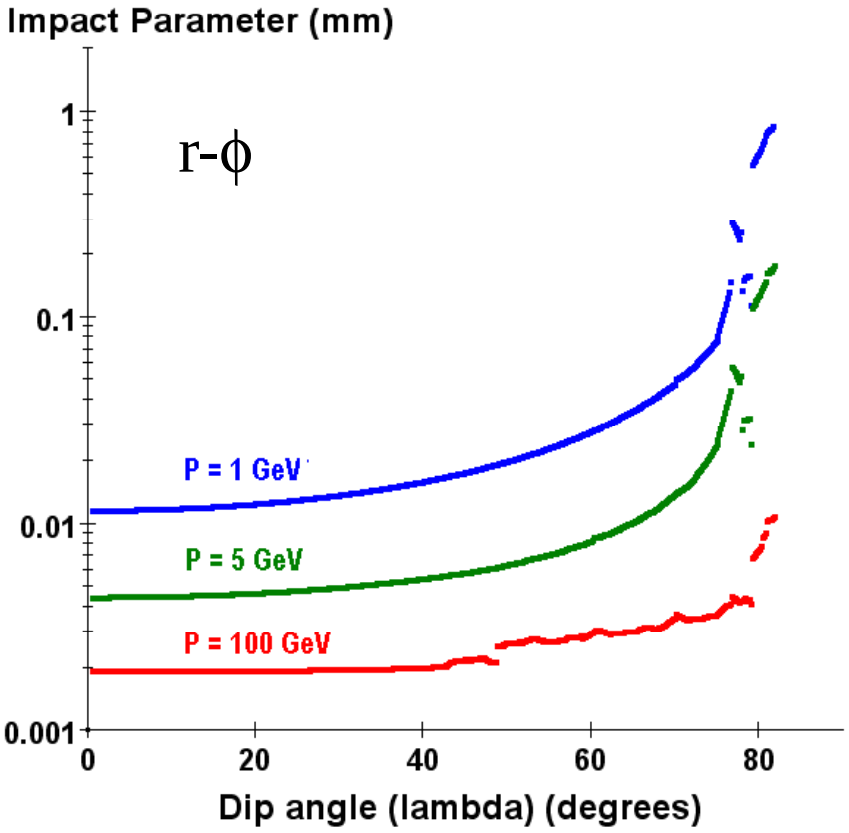


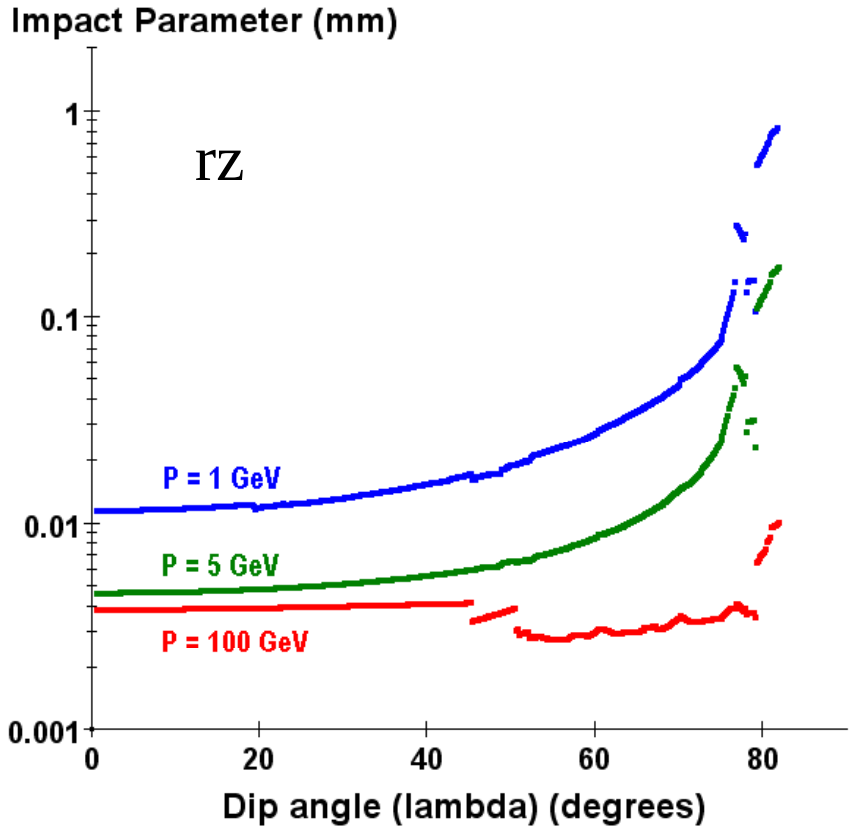
Real mechanical design but services are toy model

Not all material has same influence on impact parameter resolution.

Simulated Resolution Performance (I)

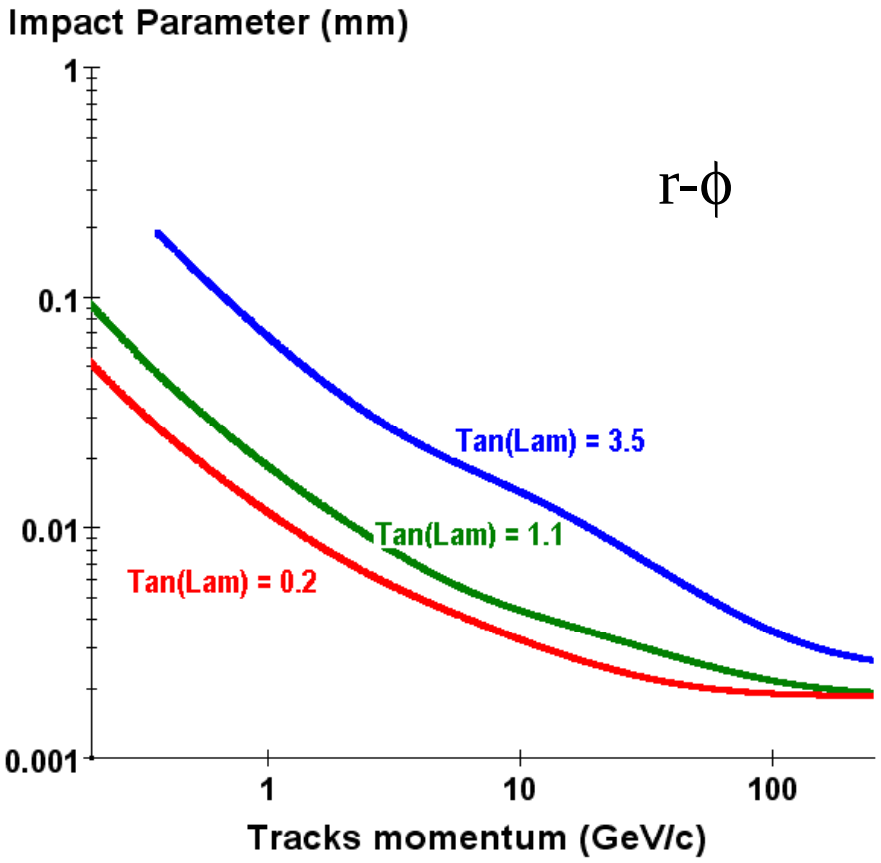
Nick Sinev

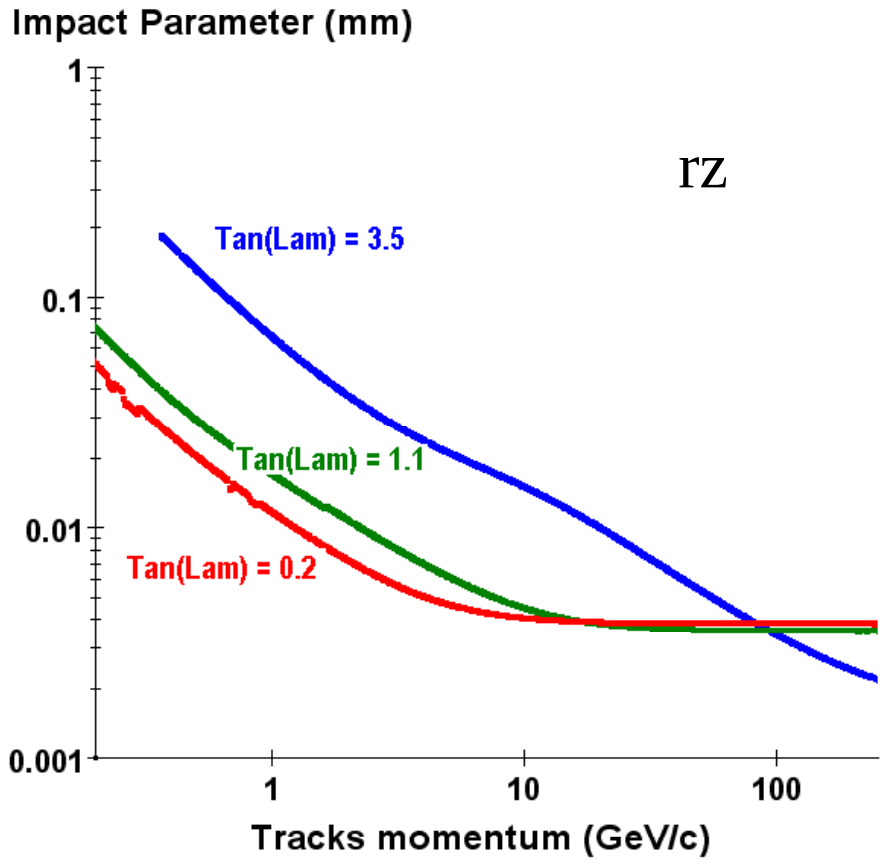




Simulated Resolution Performance (II)

Nick Sinev





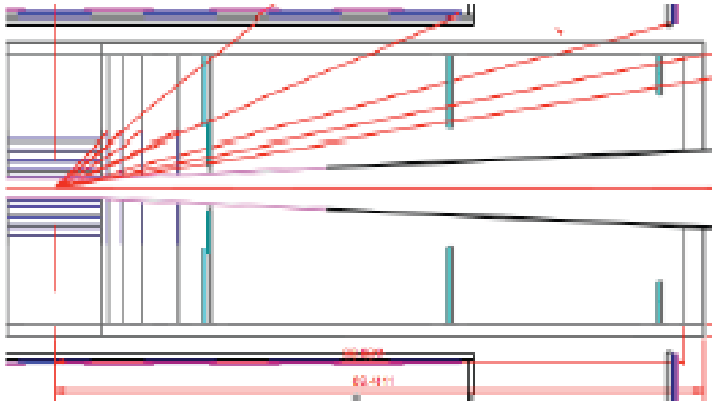
Mixed Sensor Technology in VD

- Discussed possibility to use different technologies for
  - Inner layer(s)
    - Most important but in most hostile environment
    - Small, thin pixels with low noise
    - Time stamping
    - May afford more power at the ends - falling out of fiducial and Layer 1 is only 9% of the total barrel area
  - Outer layers
    - Many more sensors – low power technology
    - No time stamping ?
  - Disks
    - Thicker sensors ok
    - Easier services

- Extra freedom to choose adequate technology might be useful to optimize the design

Vertex Detector

- SiD Vertex Concept
  - High magnetic field allows for small inner radius for the inner layer
  - Barrel and disk system
    - Provides good forward tracking
    - Always at least one barrel hit/track
    - Unique to SiD
  - Integrated mechanical design with tracker



- But we don't
  - Understand optimization of the disks
  - Have functional pattern recognition or physics simulation
  - Understand power and interconnection issues
- We do want to preserve technology options for the sensors, which limits detail in a final design

Vertex Subsystem

Coverage of some areas is spotty because

- Sensor R&D groups tend to focus on detector technology rather than the detector concept
- Tools are not available
- Manpower is not available
- Funding is not available

VTX Groups

- SLAC
- FNAL
- UK (Bristol, Oxford, RAL)
- MPI
- Prague
- Oregon

- Add or direct effort into more experiment-specific or generic (non-sexy) problems
- While keeping the R&D work active and well-supported

Vertex System Design Issues

- Mechanical Design
  - Series of meetings had been running organized by Bill and Joel.
  - Barrel geometry is specified
  - Disk design is still at an early stage
    - Mass constraints
    - Power constraints
  - Conceptual design for CF support cylinder
    - Hope to build a prototype at FNAL
  - Many mechanical issues depend on sensor technology, electronics design - these have to wait.
- There is a solid base overall mechanical design which can accommodate various sensor and readout options.
- Joel will discuss this in more detail

Summary of Hardware Efforts

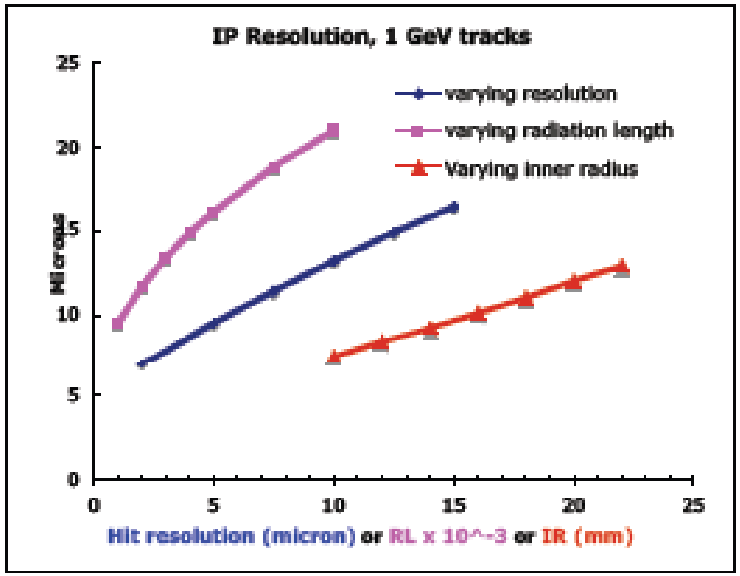
- Sensor R&D
  - UK - LCFI
    - CPCCD , ISIS CCD
  - FNAL
    - 3D Electronics, SOI
  - MPI, Prague
    - DEPFET detectors
  - Oregon
    - CMOS MAPS

- Other R&D
  - UK
    - Support structures
    - Mechanical
  - FNAL
    - Mechanical Design
    - Serial Power
    - Thinning
  - MPI
    - Thinning and support
  - SLAC
    - Electronic system integration

Not covered - other powering schemes, pulsed power studies, interconnections
Understanding of power => understanding of mass distribution

Basic Parameters

- IP resolution will be determined by mass, inner radius, and pixel size. More complex questions include:
  - How resolution is degraded with angle in the forward direction
  - What are the pattern recognition constraints?
- Optimizations
  - Mix in decreased time resolution technologies in outer layers
  - Vertex pixel size optimization (power/pixel size tradeoffs)

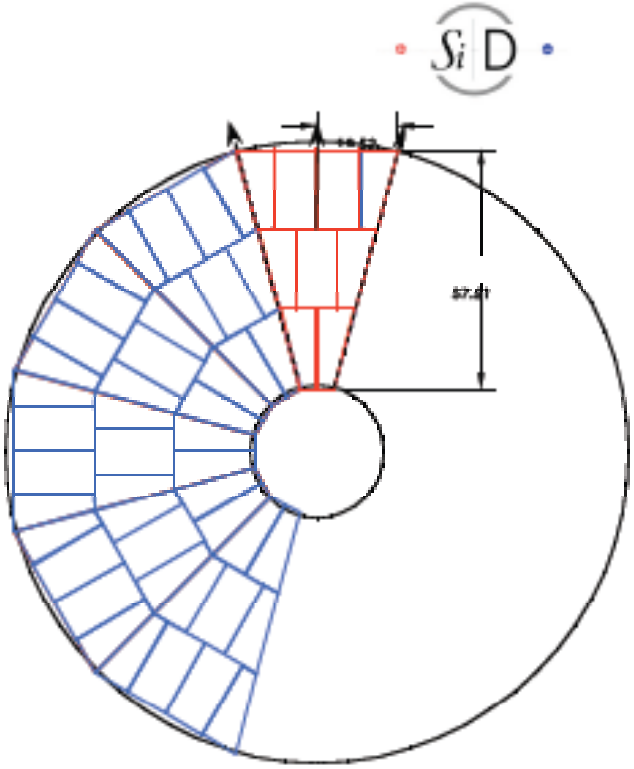


Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resoluton
- 1.4 cm inner radius

Varying each parameter

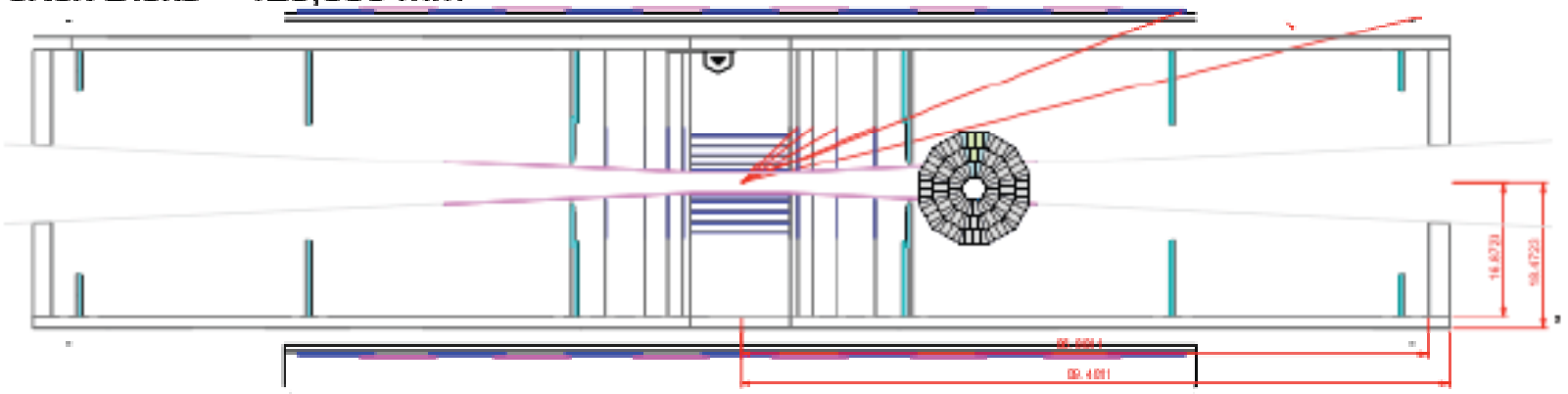
Disks

- Assuming pixels for the forward region
  - What are we asking of the forward disks
    - IP resolution - dominated by barrels
    - Pattern recognition
  - Integration with forward silicon design
    - Determines momentum res., angle measurement
  - Pixel size
    - Maximum size -> minimum power
    - Support and geometry



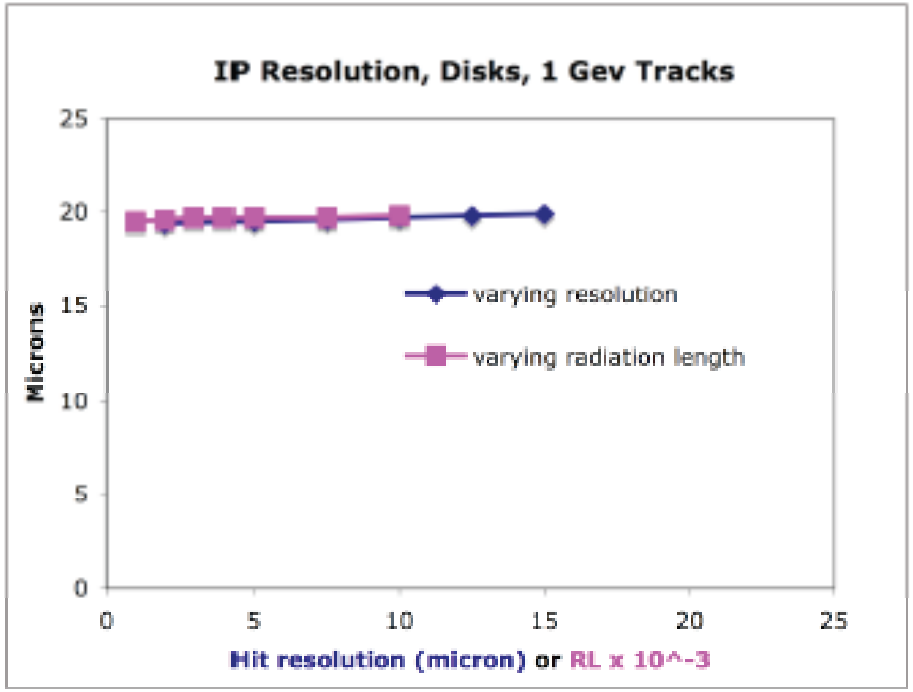
3D DBI-based concept
Chips tiled on 1/2 disk sensor

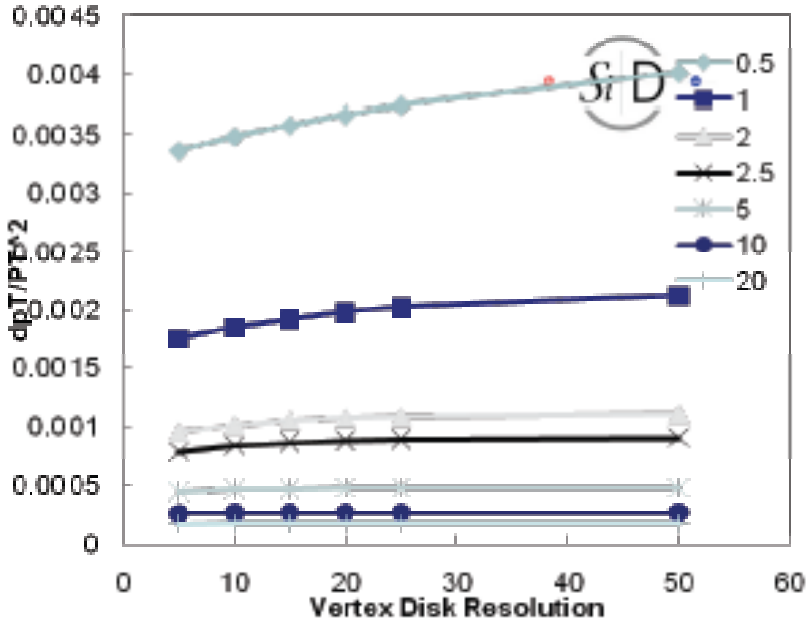
Vertex barrel ~ 150,000 mm²
Vertex Disks ~ 120,000 mm²

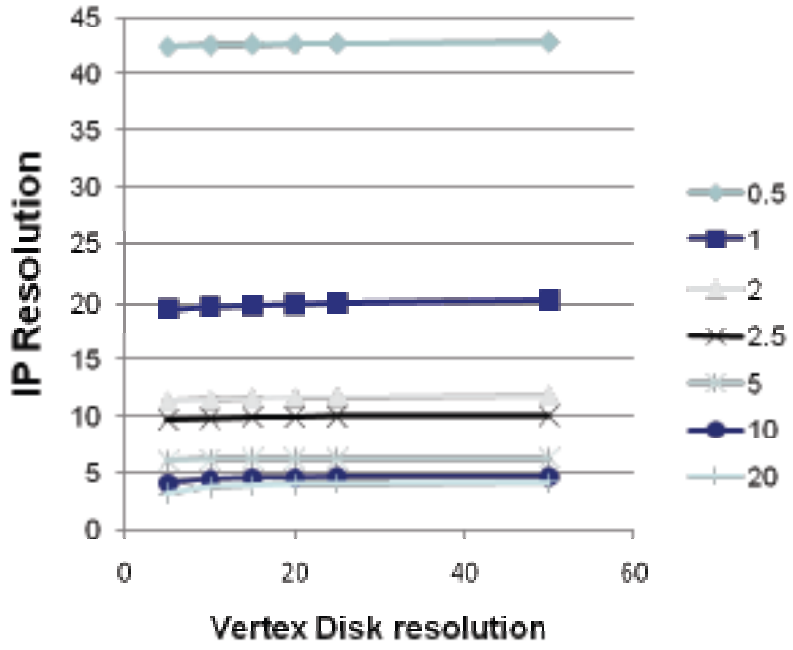


Disk Parametric Study

- Parametric study of momentum and
- Impact parameter resolution as a function of disk spatial resolution
- Based on this there is no way to specify pixel size in disks
- Different if barrel hit is missed or degraded







Cabling and Interconnect

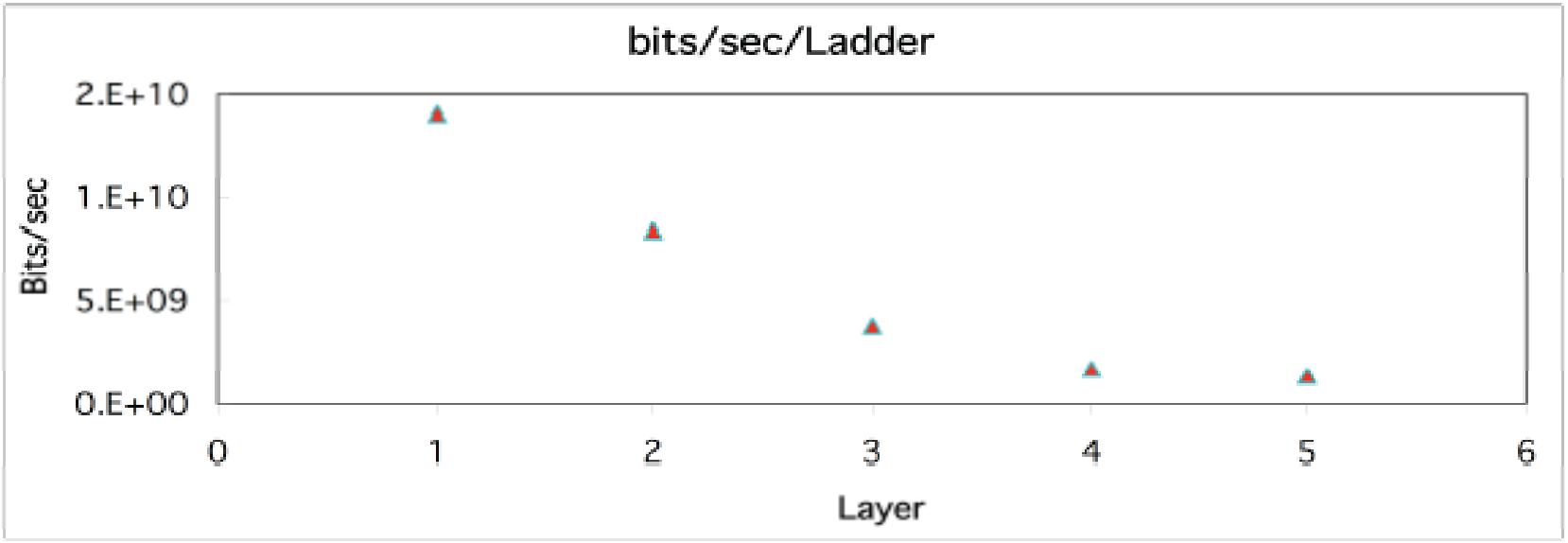
- Power delivery design
  - Serial power / DC-DC conversion / Capacitive switching
  - Controls
  - Regulation locations, number of cables to outside
  - Division of modules?
- Cable routing. Along beam pipe or along support cylinder
- Optical or electrical interconnect
  - power required, location
- Sensor/cable interface design.
- Lorentz forces.
- Pulsed power R&D –This an important aspect of any ILC –based electronics system and needs to be studied.

Data Load

bits/hit 30

Rolling Shutter 0.001 sec/train

layer	Hits/crossing	hits/train	hits/sec	bits/sec	ladders	bits/sec/Ladder
1	2000	5.64E+06	5.64E+09	1.69E+11	12	1.41E+10
2	1200	3.38E+06	3.38E+09	1.02E+11	12	8.46E+09
3	800	2.26E+06	2.26E+09	6.77E+10	18	3.76E+09
4	500	1.41E+06	1.41E+09	4.23E+10	24	1.76E+09
5	500	1.41E+06	1.41E+09	4.23E+10	30	1.41E+09
Rolling Shutter		1.41E+07	1.41E+10	4.23E+11	96	
Between Trains			7.09E+07	2.13E+09		



Optical or Electrical?

- Optical interconnect generally favored for long lengths, high bit rate.
- Bit rates for the most aggressive scenarios (>10 Gb/sec/ladder) are probably only practical optically
- Difference is not hugh, power is ~5-15 mW/connection x 96 ladders ~ 0.5 - 1.5 W. Significant but sustainable

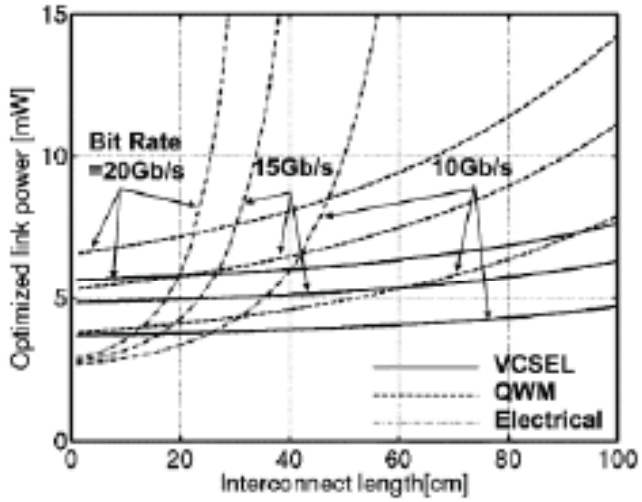


Fig. 5. Power comparison between the electrical and the optical interconnect showing the critical lengths at a detector capacitance of 25 fF.

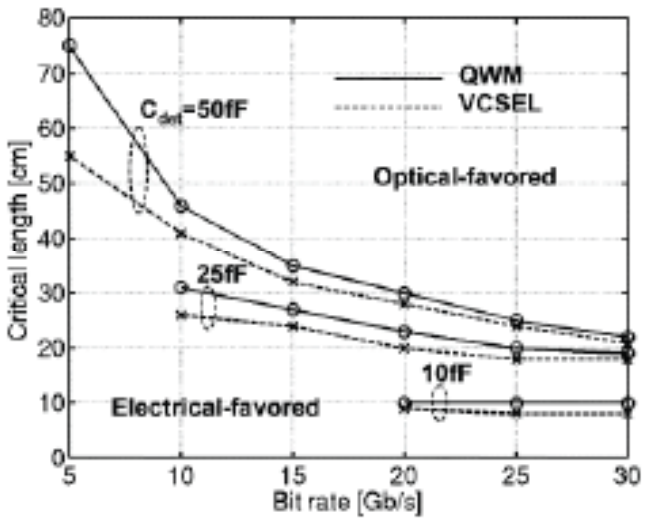


Fig. 6. Critical length in terms of system bit rate for the QWM and the VCSEL transmitter technologies.

Simulation

- What is needed to understand pattern recognition performance?
  - Overall tracking in 3D over full angular range
  - Ability to change geometries and sensor characteristics
  - Ability to add beam background
  - Use Nick Sinev's package for charge deposition where important
- What is needed to understand physics performance?
- Are the standard benchmarks what we want? Would like a mode or modes that allows us to:
  - Cleanly study capabilities
  - Emphasize forward tracking (SiD strength)
  - Incrementally build understanding –adding more complex studies as appropriate
  - Interact efficiently with benchmarking studies groups
- A_{FB} in $e^+e^- \rightarrow bb$, cc, while not on the compulsory list, is an appealing reaction to start with.

Vertex Simulation Goals

- Understand effects of forward pixel size
- Understand effects of material associated with barrel services
- Understand the requirements for time resolution as a function of barrel layer
- Understand the effects of inclined tracks in the forward direction
- Begin to study the effects of various technological options

- Understand the physics capabilities of the detector.

Summary

- Maintain coherence between developing the concept design and R&D efforts
  - Develop physics simulation with pattern recognition
    - Initial aim would be for internal studies
    - Use it to motivate decisions
    - Depends on full simulation package with beam backgrounds, pattern recognition, and charge deposition
  - Increase participation in tracking/vertex meetings
  - Integrate R&D groups in simulation and system design
  - Find groups to study
    - Interconnection
    - Power engineering (serial, DC/DC, pulsed)
- Different sensor requirements for different VD subsystems offer additional freedom to optimize the design
  - Helps strengthen links with generic R&D collaborations

Backups

Service Material Model

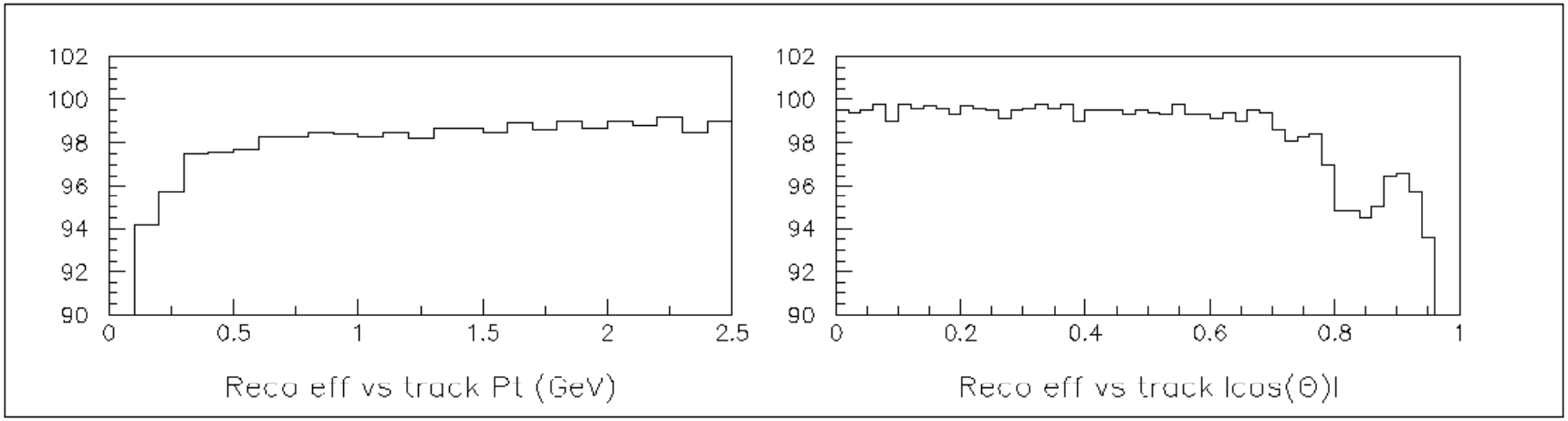
Due to the lack of a real design, this is unfortunately a very crude toy model in GEANT:

1) Readout/service connection at each barrel layer end is represented by a solid ring of G10 5mm wide in Z and 2mm high in radius.
2) The power and signal cables are represented by a 300μm diameter copper wire (leading to DC-DC on coned beam pipe) and 250μm diameter fiber at each end of a ladder. The cables all focus down to the beampipe to exit from there to be out of fiducial volume, but this causes a significant clumping of material at lower radius which may not work mechanically. It suffers Lorentz force at ~1 Newton at peak current in anyway. The eventual real design is more likely through serial power or local DC-DC.

Simulation and Reconstruction

- GEANT simulation In LCsim framework
- Digitization model based on SLD VXD3 CCD data.
- Full tracking reconstruction starting from VXD alone tracking followed by matching to outer tracker.

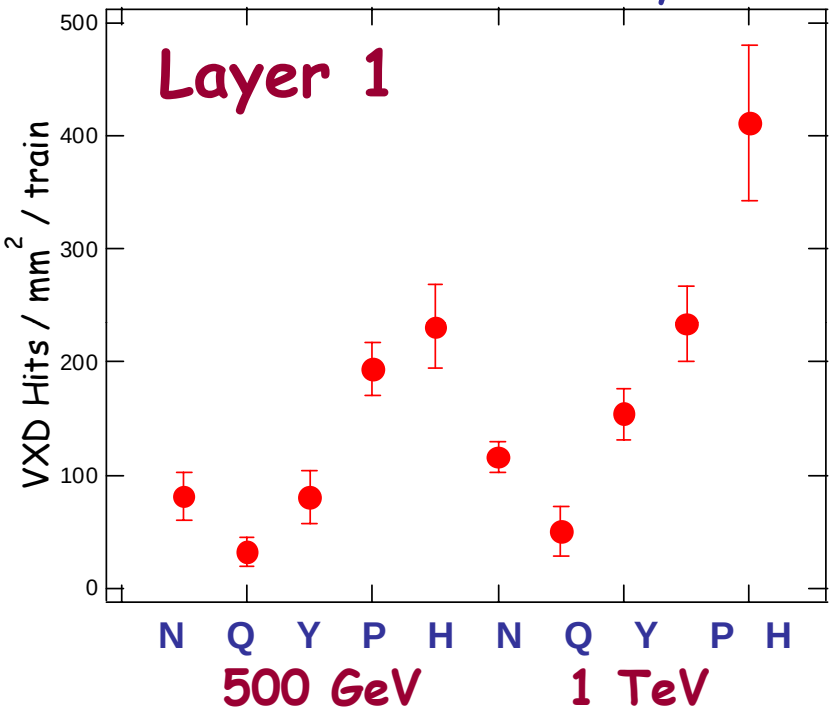
Nick Sinev



VXD Background Rate Variations

Takashi Maruyama

Radius (cm)	Hit density/train/mm^2 (Mean/RMS)
1.4	80.2 / 16.2
2.2	16.1 / 7.9
3.5	2.3 / 1.7
4.8	1.0 / 0.8
6.0	0.2 / 0.2



Layer 1's problem is in its own league (Revised estimated based on new RDR design).

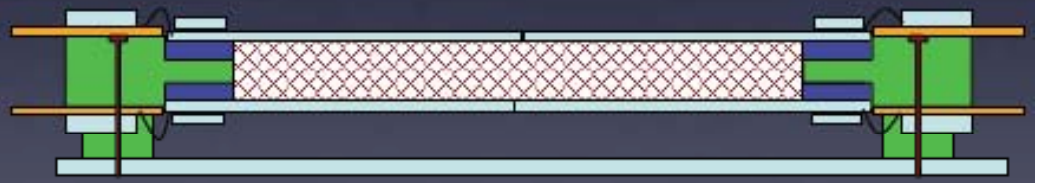
Need to be able to deal with ~200 hits/mm^2/train –

Tracking studies by Nick Sinev for NLC and by Richard Hawkings for TESLA both point to performance problem at Layer 1 density of ~1-2 hits/mm^2. Can only get there with time stamping !

Mechanical Studies

- 25 micron silicon on 1.5mm 8% SiC
  - Very rigid
  - Achieved 0.14% X_0

- 20 micron silicon sandwiching 1.5mm 2% carbon
  - Could be double-sided
  - Achieved 0.07% X_0



Mechanical Studies

- Foams!

- SiC Foam substrate ladder cooled
- Negligible thermal distortion over 70°C