DEPFET Active Pixel Sensors for the ILC

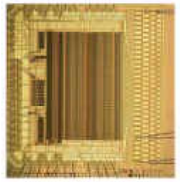
- Status Report -

Laci Andricek

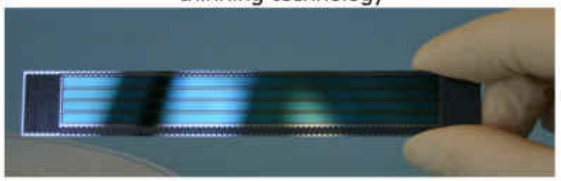
for the DEPFET Collaboration
(www.depfet.org)

The DEPFET ILC VTX Project

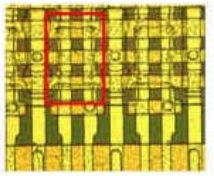
✓ steering chips Switcher



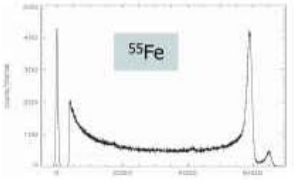
✓ thinning technology

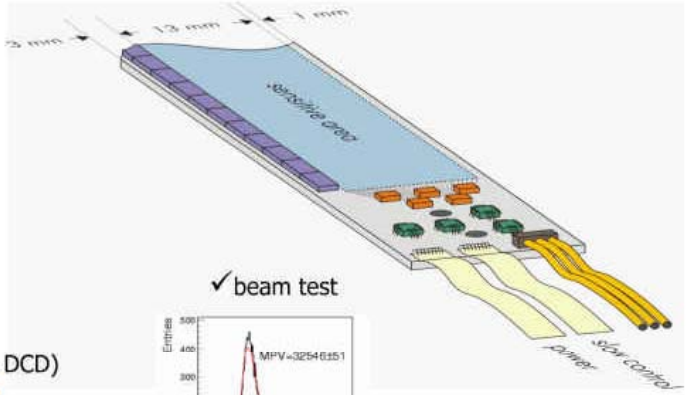


✓ sensor development

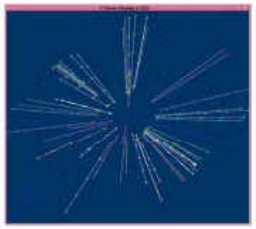


✓ radiation tolerance

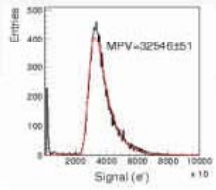




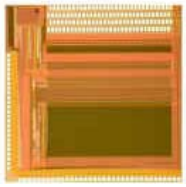
✓ Simulation



✓ beam test



✓ r/o chips (CURO & DCD)



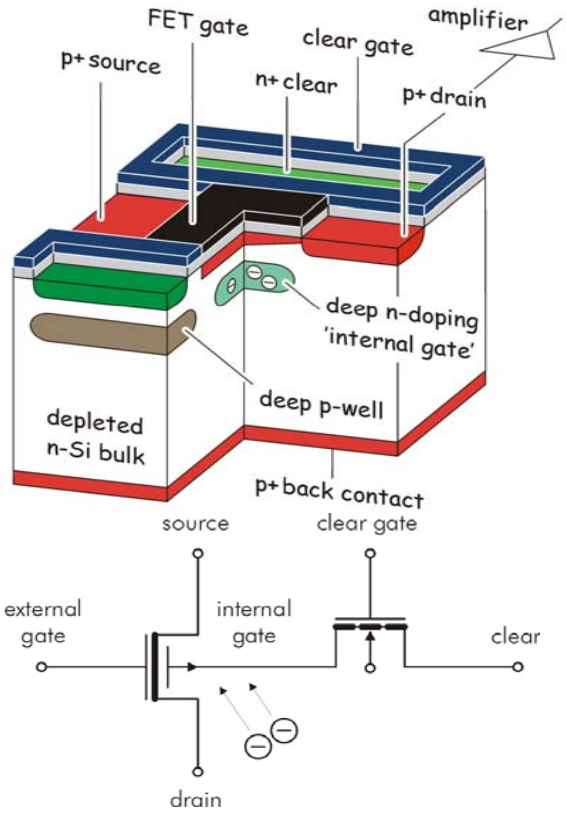
See DEPFET Backup Document at www.depfet.org

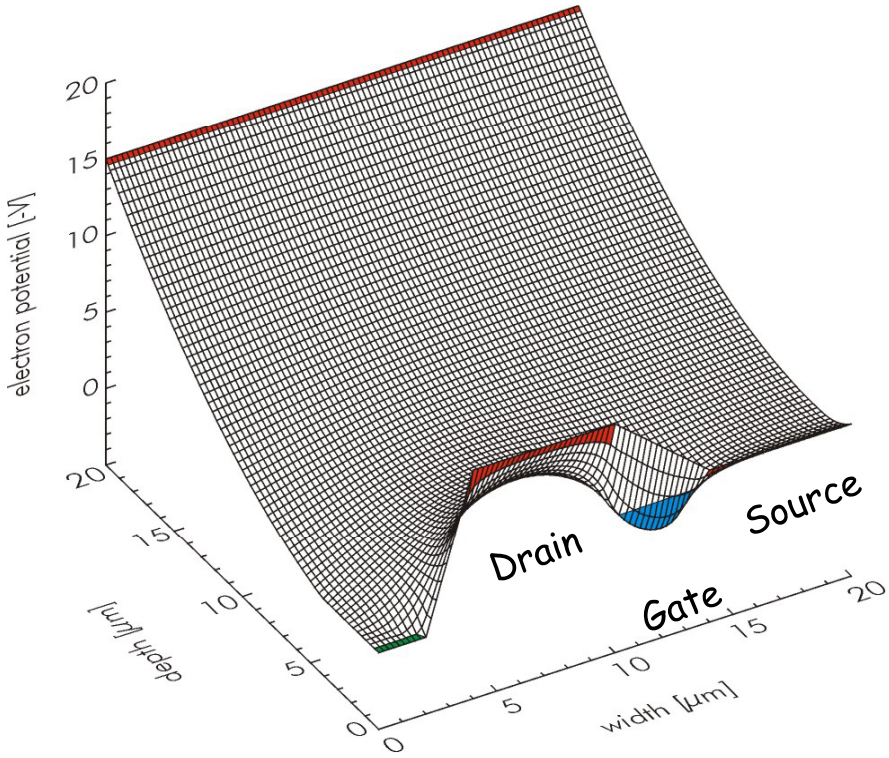
- DEPFET in a nutshell
- Summary of the current achievements
- Some news from PXD5
- News on thinning/ladder design

DEPFET Principle

J. Kemmer & G. Lutz, 1987

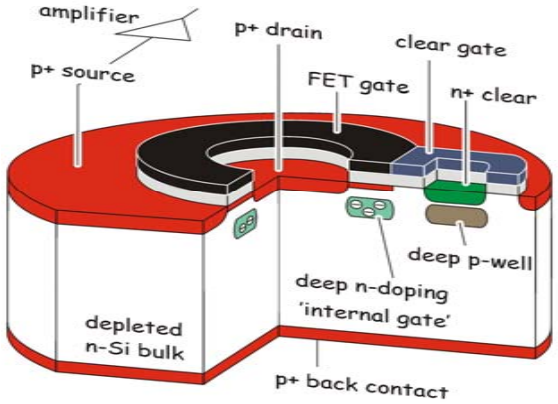
DEpleted P-channel FET





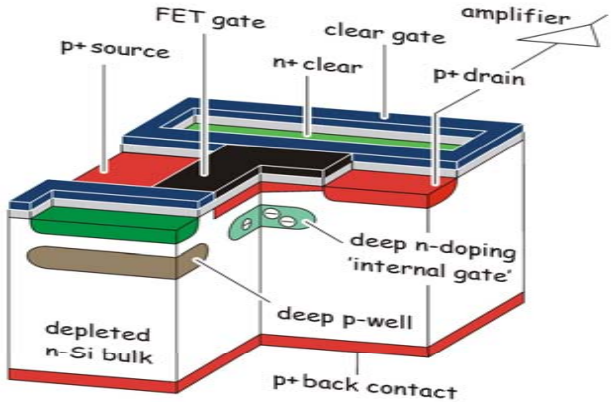
- fully depleted sensitive volume, charge collection by drift
- internal amplification → q-I conversion: 0.5 nA/e, scales with gate length and bias current
- Charge collection in "off" state, read out on demand

Overview: Types and Applications



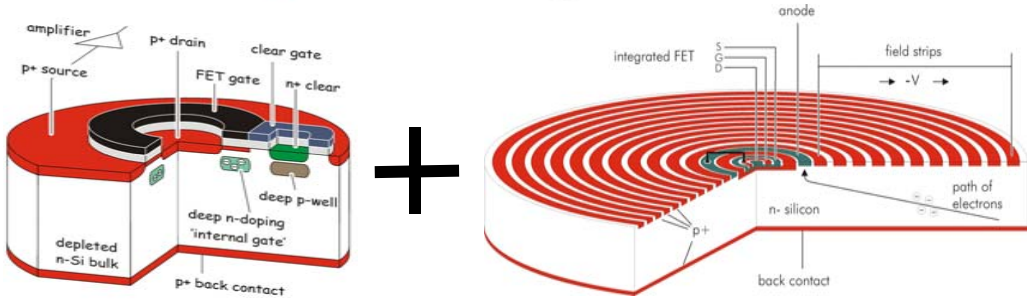
X-ray imaging spectroscopy → XEUS

- pixel size: 100µm
- r/o time per row: 2.5 µs
- Noise: ≈4 el ENC



Particle tracking → vertex detector at ILC

- pixel size: 24µm
- r/o time per row: 25
- Noise: ≈100 el ENC
- thin detectors: ≈50µm

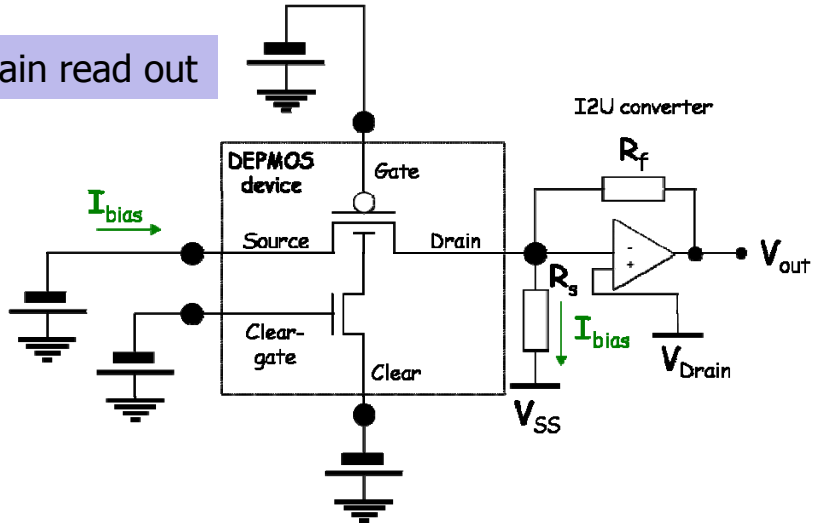


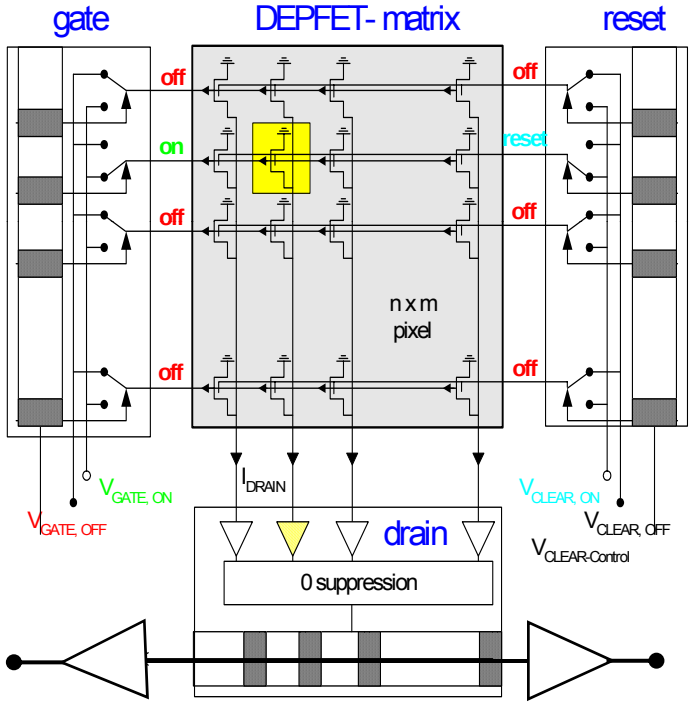
DEPFET MacroPixel
X-ray (imaging) spectroscopy
→ BepiColombo, SimbolX

- pixel size: 100s of µm

DEPFET Array - read-out at the ILC

Drain read out

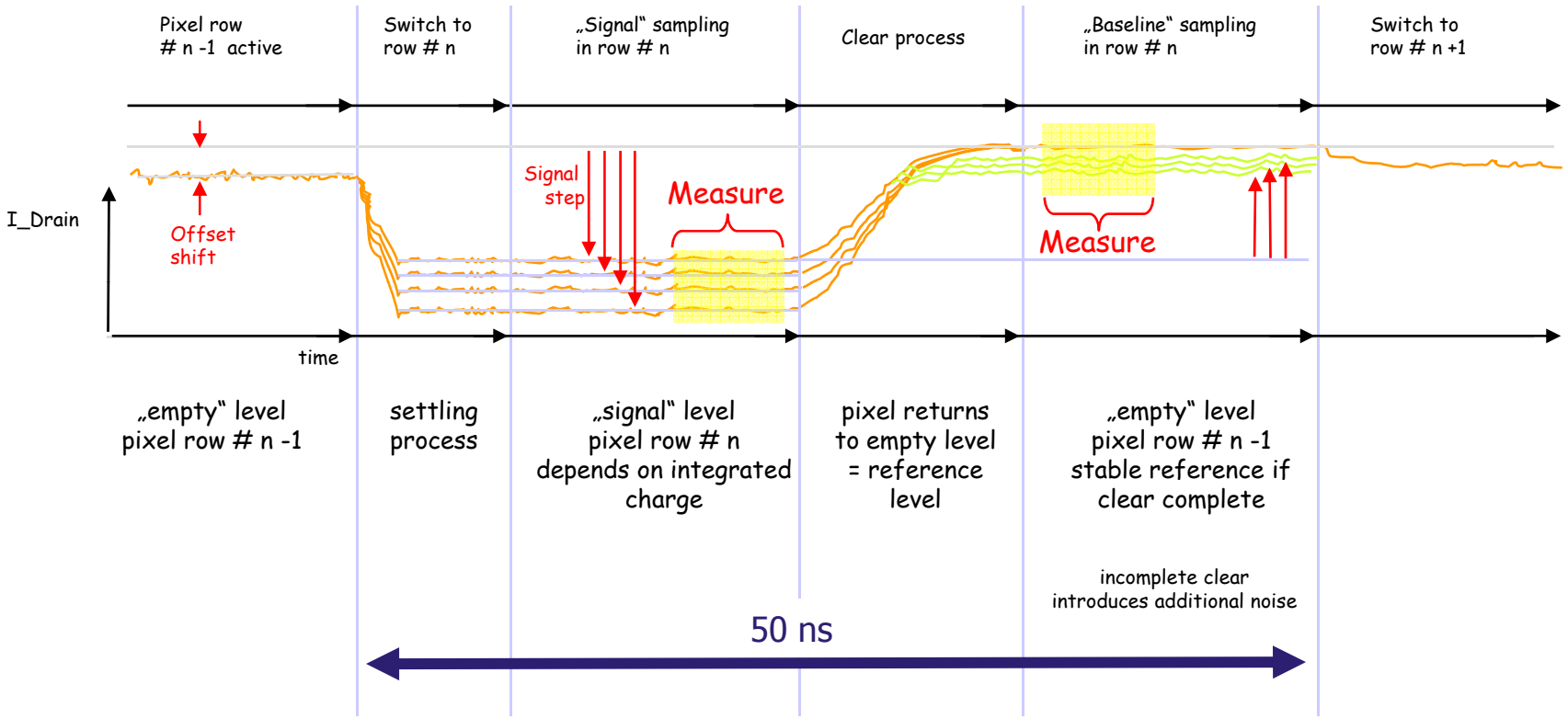




Row wise read-out ("rolling shutter")

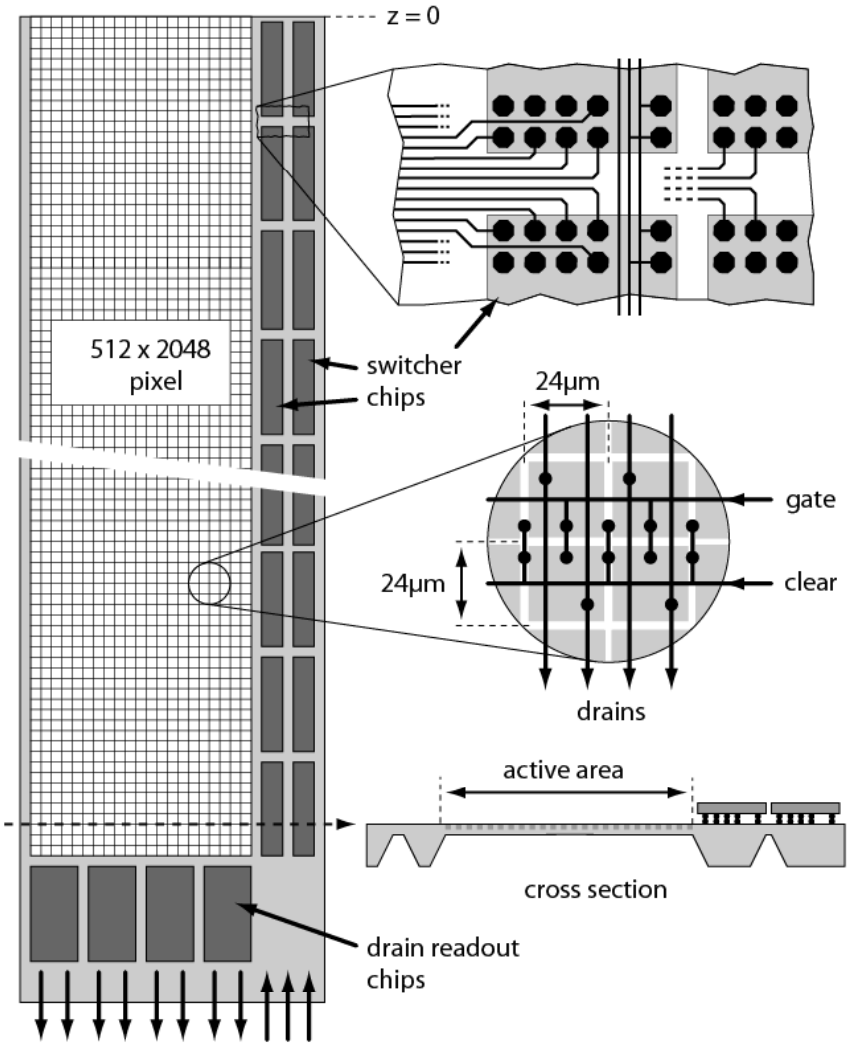
- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal
- Low power consumption
- two different auxiliary ASICs needed
- limited frame rate
- cap. load at the f/e adds noise

Row wise read-out → matrix signal



- Row wise CDS, time between the two samples ~10 ns!
- However, we need (almost..) complete clear
- and … it's a luxury which costs a lot of time!

ILC VXD baseline design



Just as a starting point for the R&D!

- 5 layer, old TESLA layout
- 10 and 25 cm long ladders read out at the ends
- 24 micron pixel
- design goal 0.1% X_0 per layer in the sens. region

Strategy to cope with the background:

- read ~20 times per train
- store data on ladder
- transfer the data off ladder in the train pause

  → row rate of 40 MHz
- read two rows in parallel, doubles # r/o channels but:

  → row rate 20 MHz ☺

The ILC DEPFET Collaboration

www.depfet.org

	DEPFET/Ladder Sim. and Irrad.	Auxiliary ASICs Development	System Development	System Tests and Test Beams
Bonn		X	X	X
Karlsruhe	X			
Heidelberg		X	X	X
Munich	X			X
Prague			X	X
Valencia			X	X

…and growing! Three new groups from Spain joined DEPFET

→ USC (Universidad de Santiago de Compostela)

→ UB (Universidad de Barcelona)

→ URL (Universidad Ramon Lull, Barcelona)

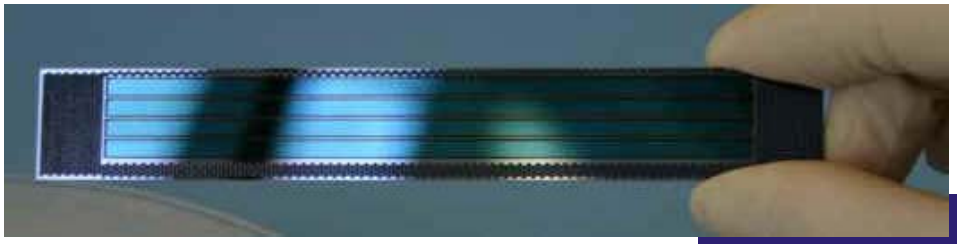
Experience in

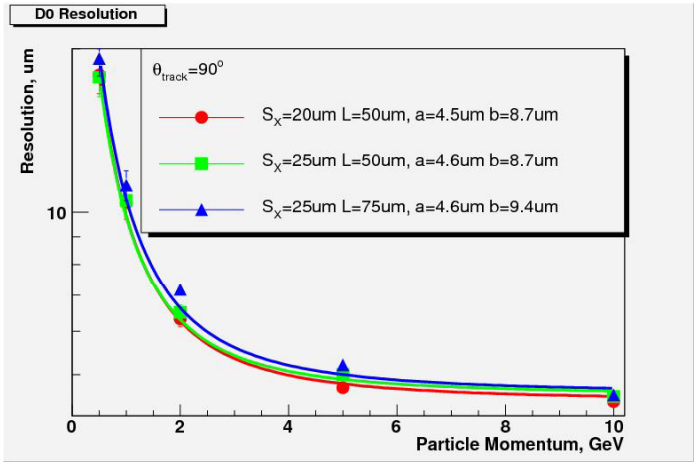
→ front and back end electronics

→ system and ladder design

→ System Test

In Summary: Achievements and status





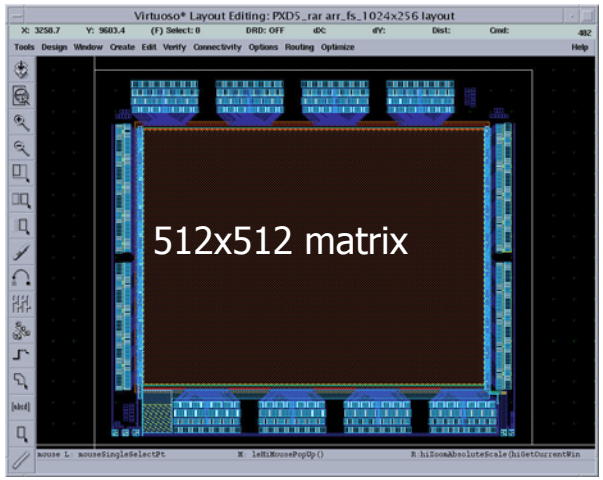
- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
  - ✓ S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2
- ✓ Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.

In this talk:

- **PXD5: Internal amplification and laser tests**
- **Update on thinning**
- **Christian's talk: DCD2 and Bump Bonding**

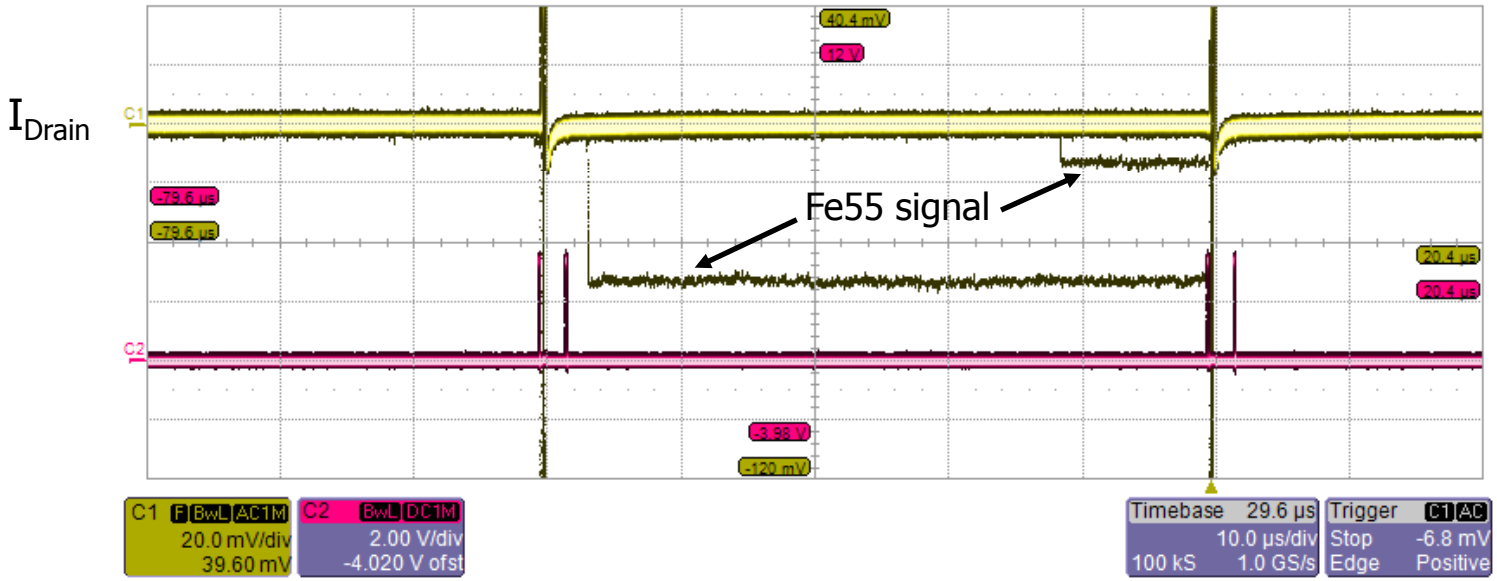
New DEPFET Generation 'PXD5'

- Mostly use 'baseline' linear DEPFET geometry
- Build **larger matrices**
  - Long matrices (full ILC drain length)
  - Wide matrices (full Load for Switcher Gate / Clear chips)
- Try new DEPFET variants:
  - reduce **clear voltages**
  - Very **small** pixels (20µm x 20µm)
    - Increase internal **amplification** (g_q)

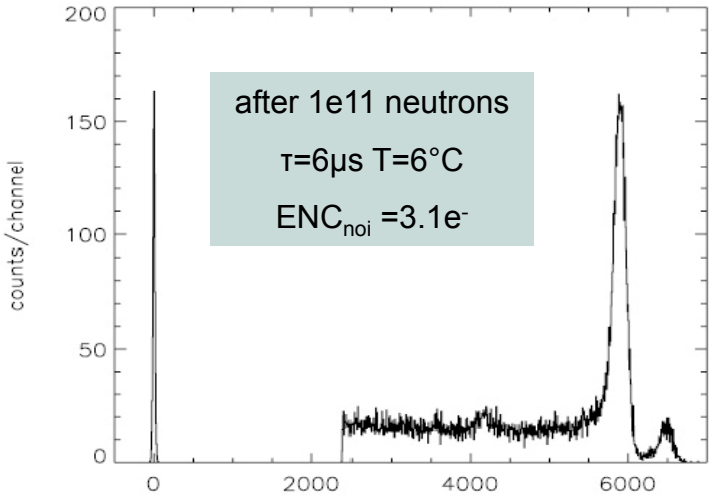


- Production finished
- Currently under test and evaluation
- beam test in July and August a PS and SPS (stand-alone and EUDET)
- expect first results from Lab tests at the Warsaw meeting

Single Pixel Setup

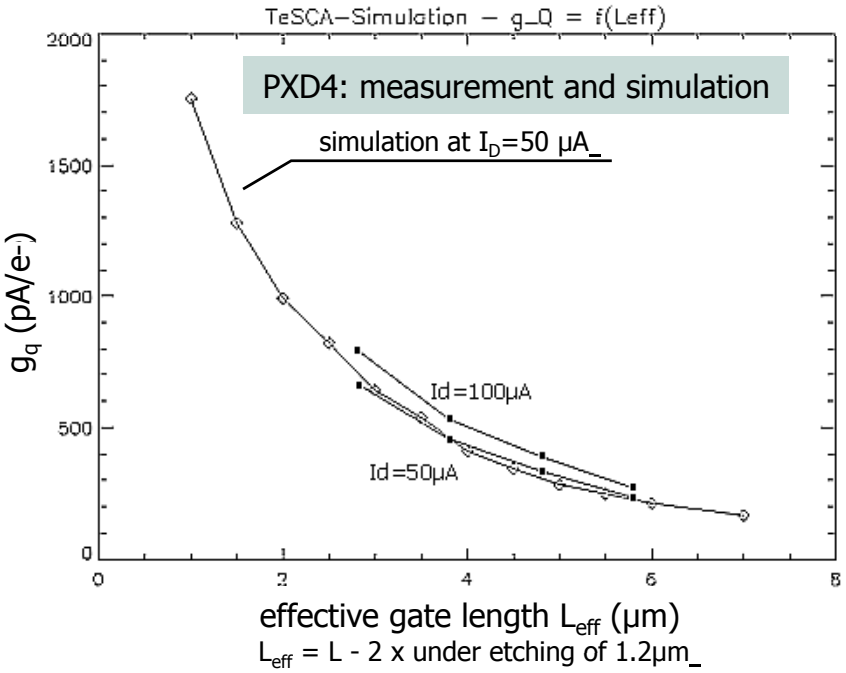


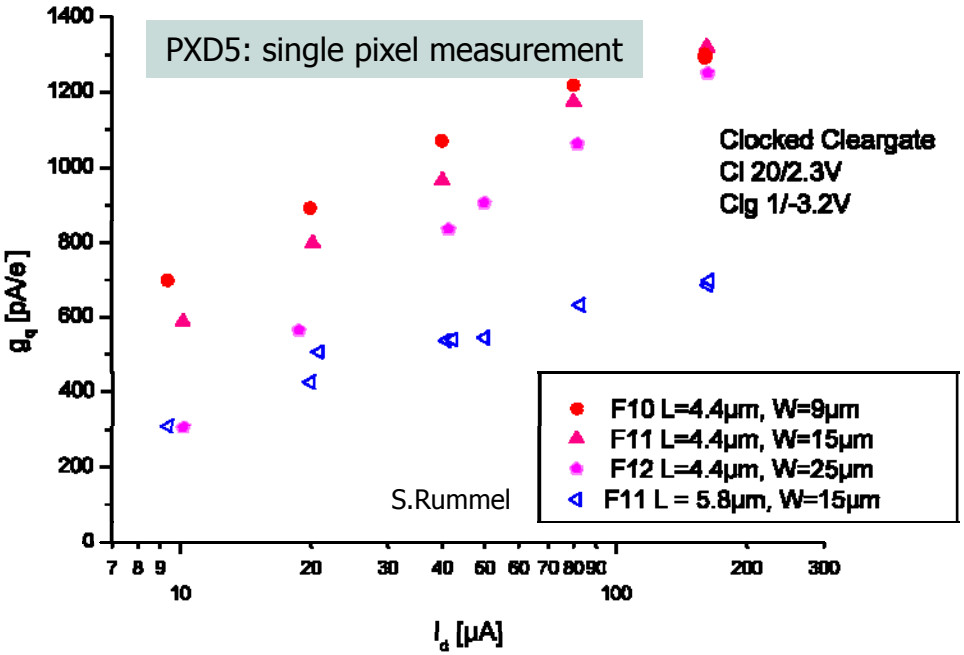
- → Noise measurements
  (CDS and peak sensing amp.)
- → Fe55 spectra
- → internal amplification g_q
- → …



Internal amplification g_q

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)



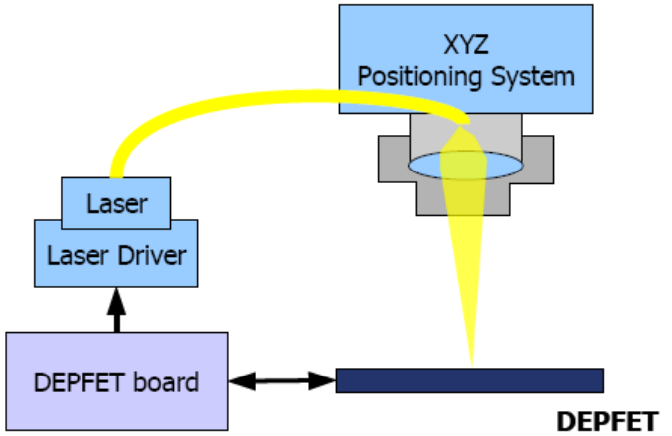


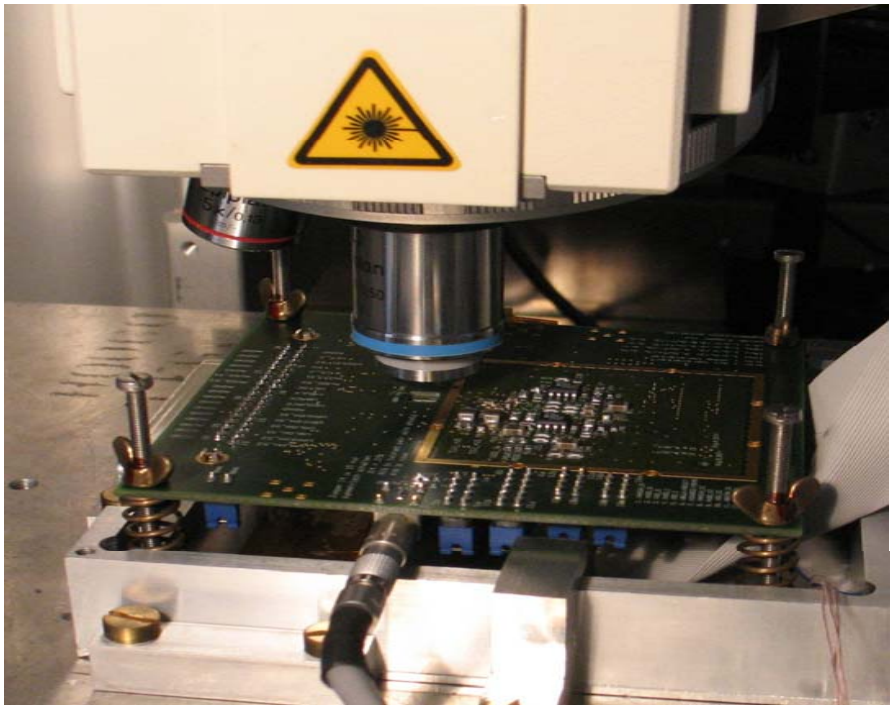
As long as noise is dominated by r/o chip → S/N linear with g_q

PXD4 has L=6µm, some matrices in PXD5 have now L=4µm → expect factor 2 better S/N

Laser Tests

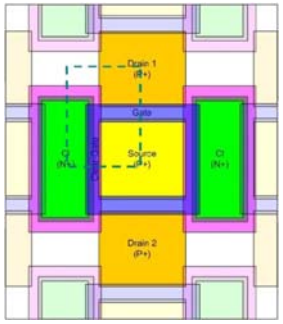
- ✔ Laser setup in several institutes
- ✔ Different wave lengths:
  - ➔ 682nm, 810nm, 1055nm
- ✔ Laser triggered by
  - ➔ Signal generated by DEPFET DAQ sequence
  - ➔ External pulse generator. DEPFET DAQ sequence started by internal trigger
- ✔ Laser focused on matrix backplane
- ✔ Laser spot: 2.5 – 5 µm
- ✔ Laser mounted on a XY-stage with 1µm steps
- ✔ 5x5 clusters
- ✔ Pixel-to-pixel variations on Mean signal height are of ~5%



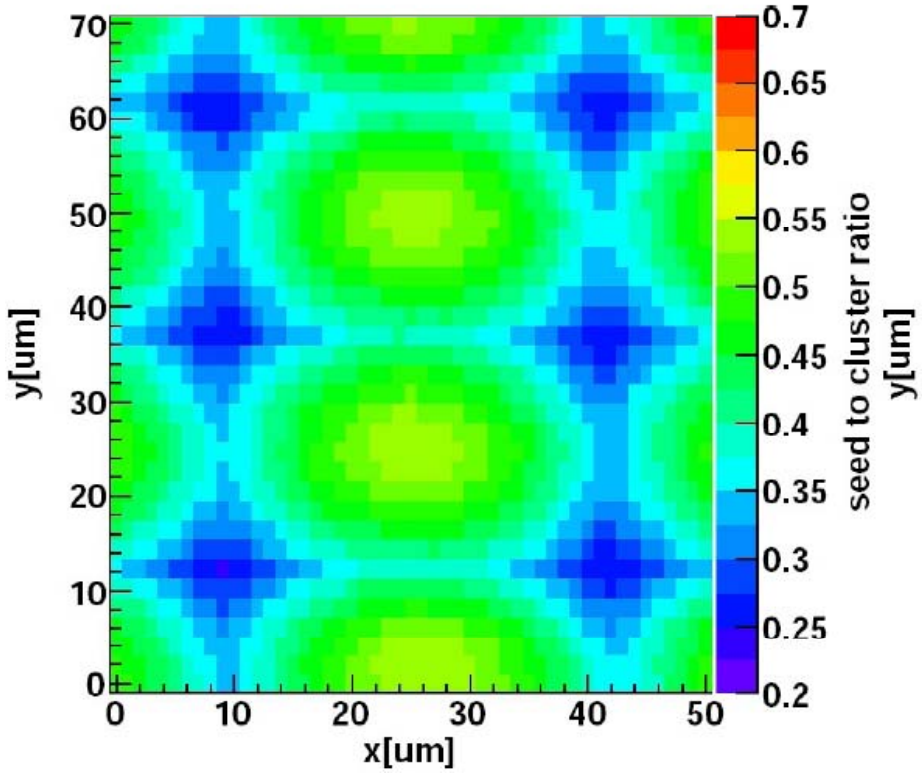


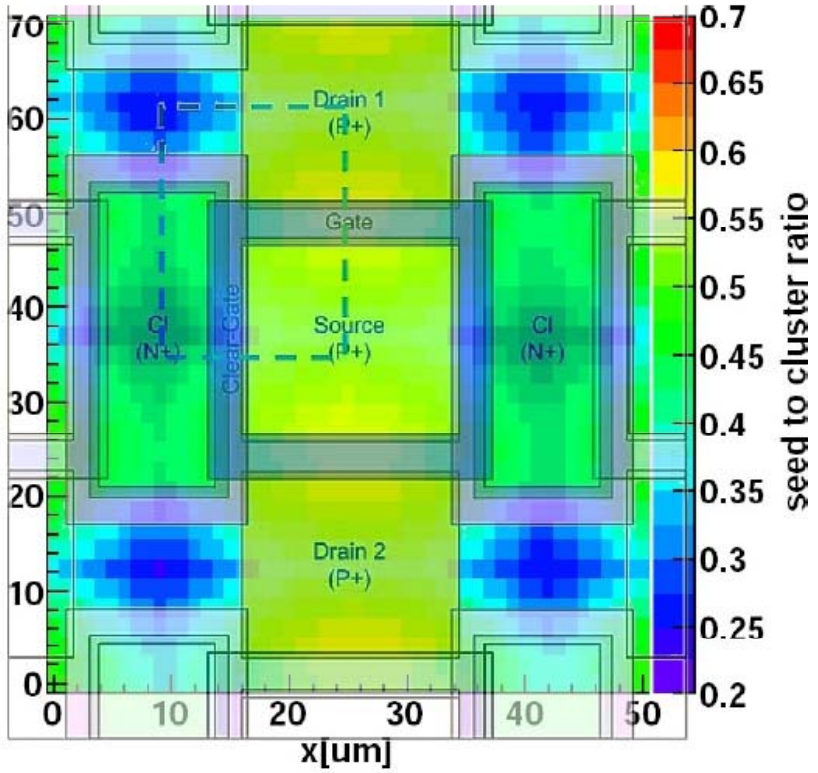
PXD4 - seed/cluster charge

- ✔ Scan with the laser a DEPFET double pixel structure.
- ✔ Figure below shows the seed to cluster signal ratio



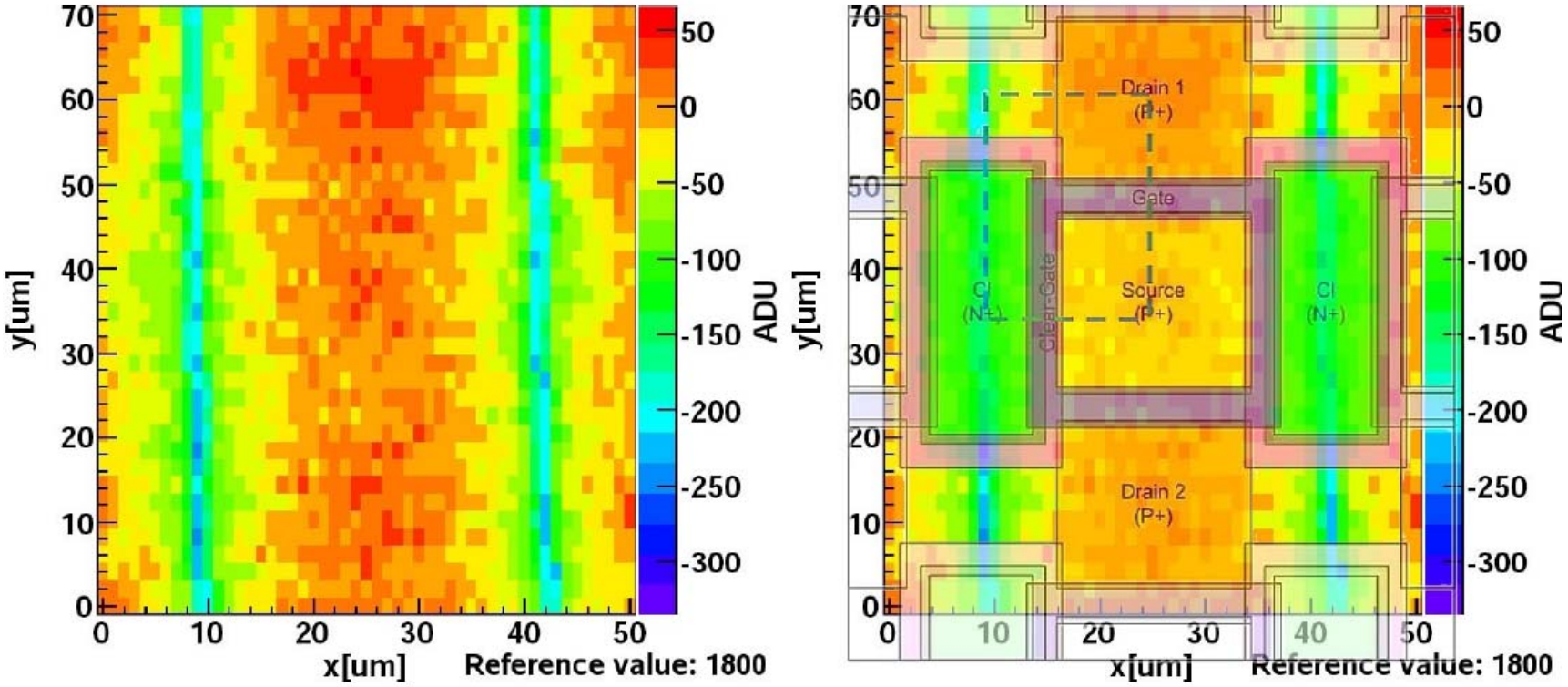
- ✔ Maximum seed fraction happens in the middle of the pixel and decreases in the region between pixels.



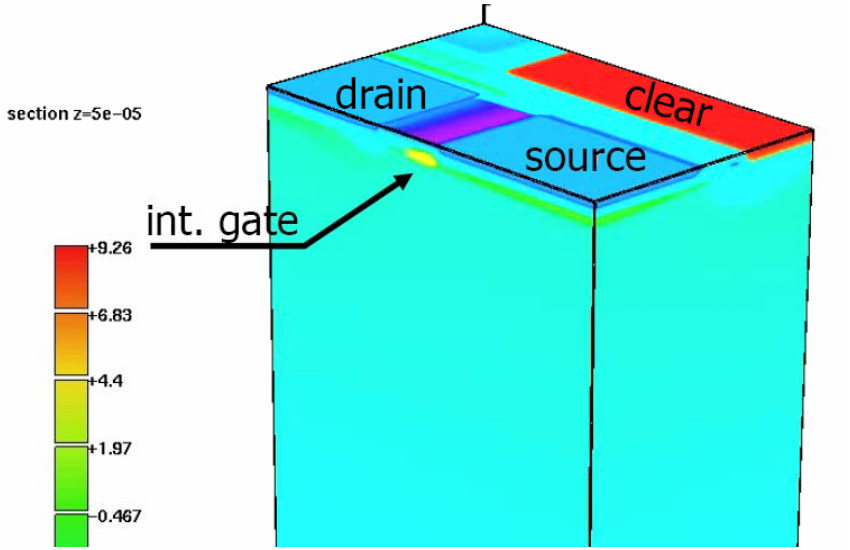


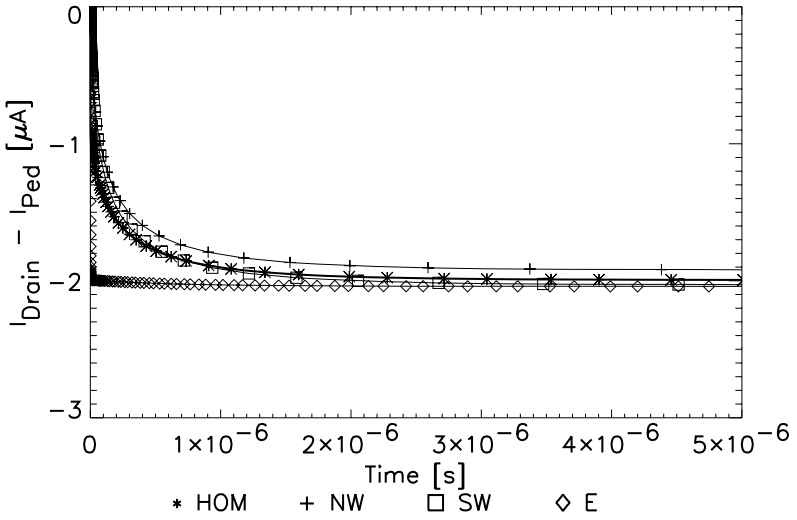
PXD4 - 5x5 cluster charge

- ✔ Total cluster signal shows charge losses which correspond to the n^+ clear implants
- ✔ Also observed in detailed 3D device simulations.



Improvements for PXD5



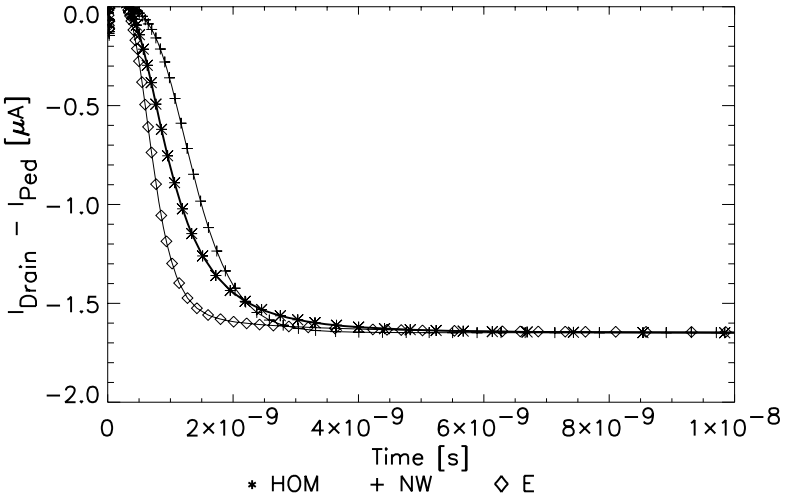


Low drift field underneath Clear!!

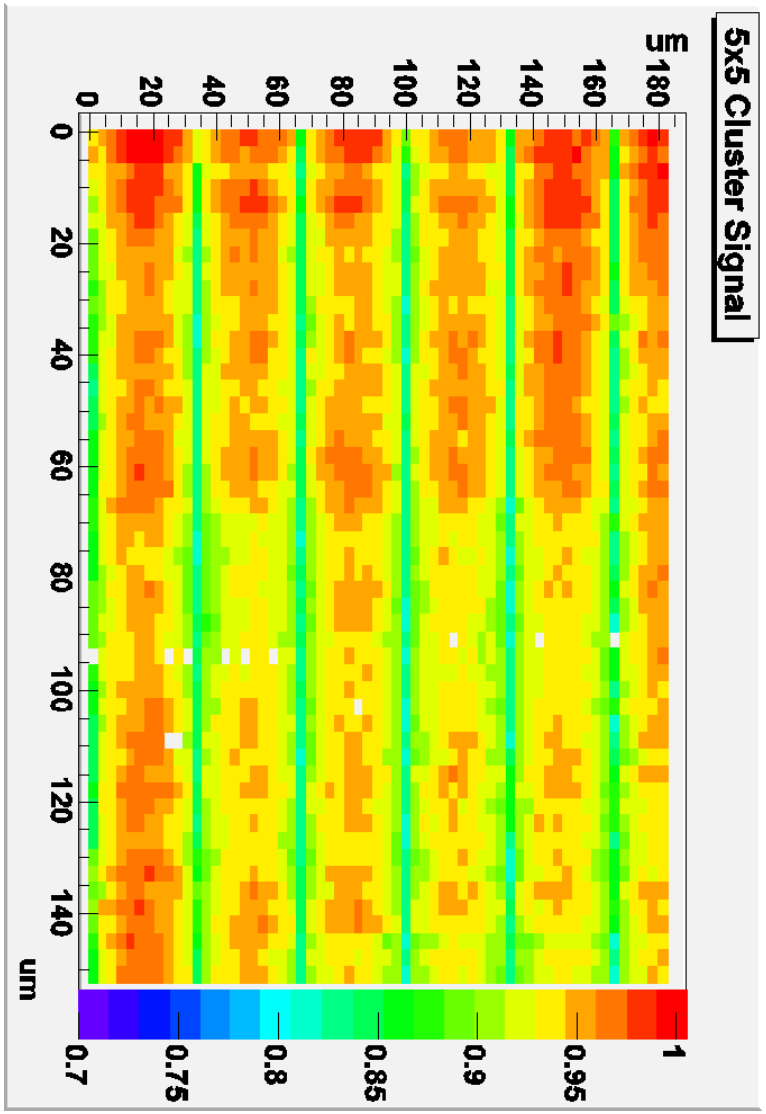
→ slow charge drift into internal gate

→ charge loss at high frame rates

→ PXD5: additional implant, "field shaping"



PXD5 under Laser Test



☹

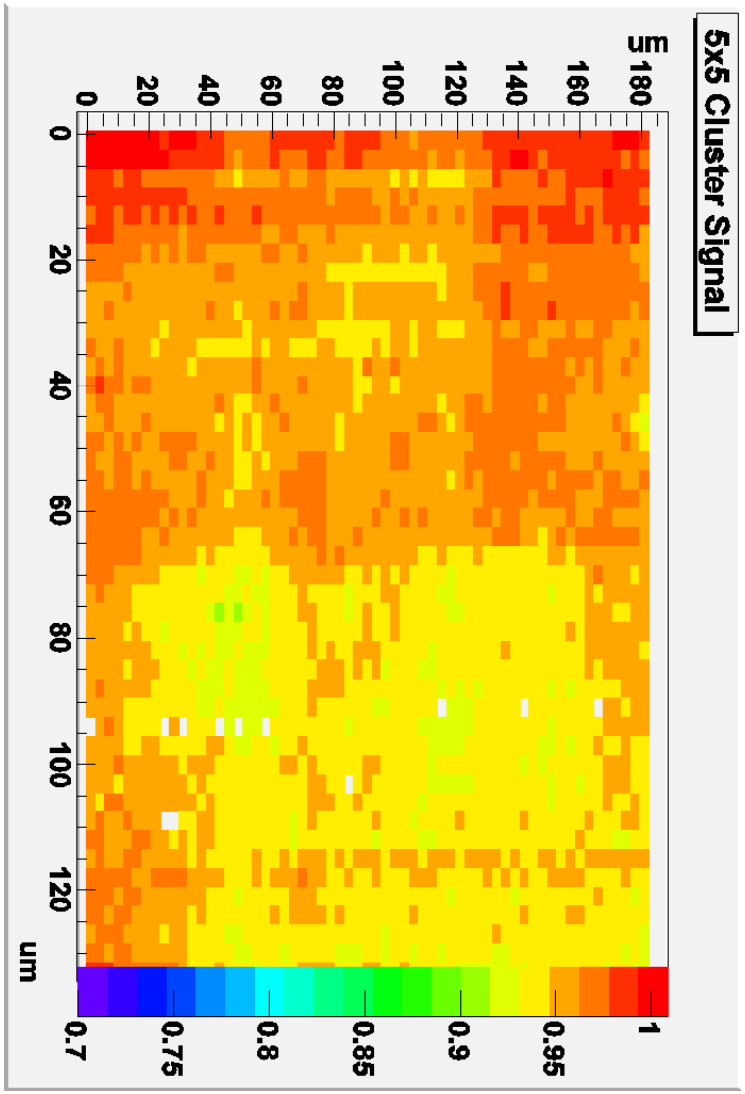
But then Kristof Schmieden from Bonn started to think!

And to look at the CM correction procedure…

1. Remove Laser signal → +/- 4 σ cut
2. Mean of the remaining pixels is CM value
3. Subtract …

In particular where signal charge is spread over more pixels, CM is overcorrected!!

PXD5 under Laser Test



The solution is simple:

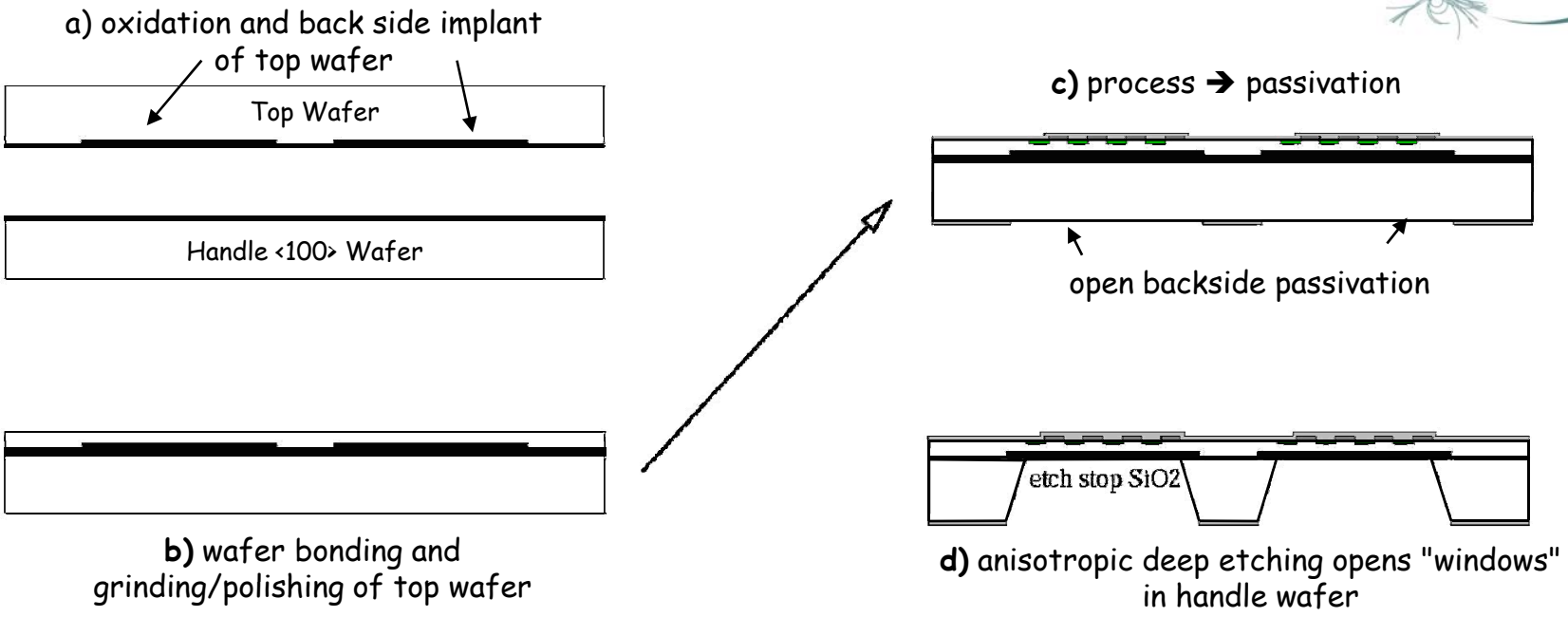
1. Find seed
2. Mask a 5x5 cluster around seed
3. And calculate CM Value

☺

-: Remaining small large area inhomogeneities (most likely) due to temp. effects.

-: Re-analyse PXD4 data …

Thinning Technology



Compatibility with the main production line tested

So far:

-: mechanical samples

-: test structures (diodes) on SOI wafers

The technology found its way into other projects:

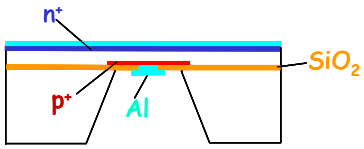
-: production of thin (75 and 150 µm) ATLAS pixel sensors for sLHC

-: first production of Geiger-mode APDs on 70 µm top layer

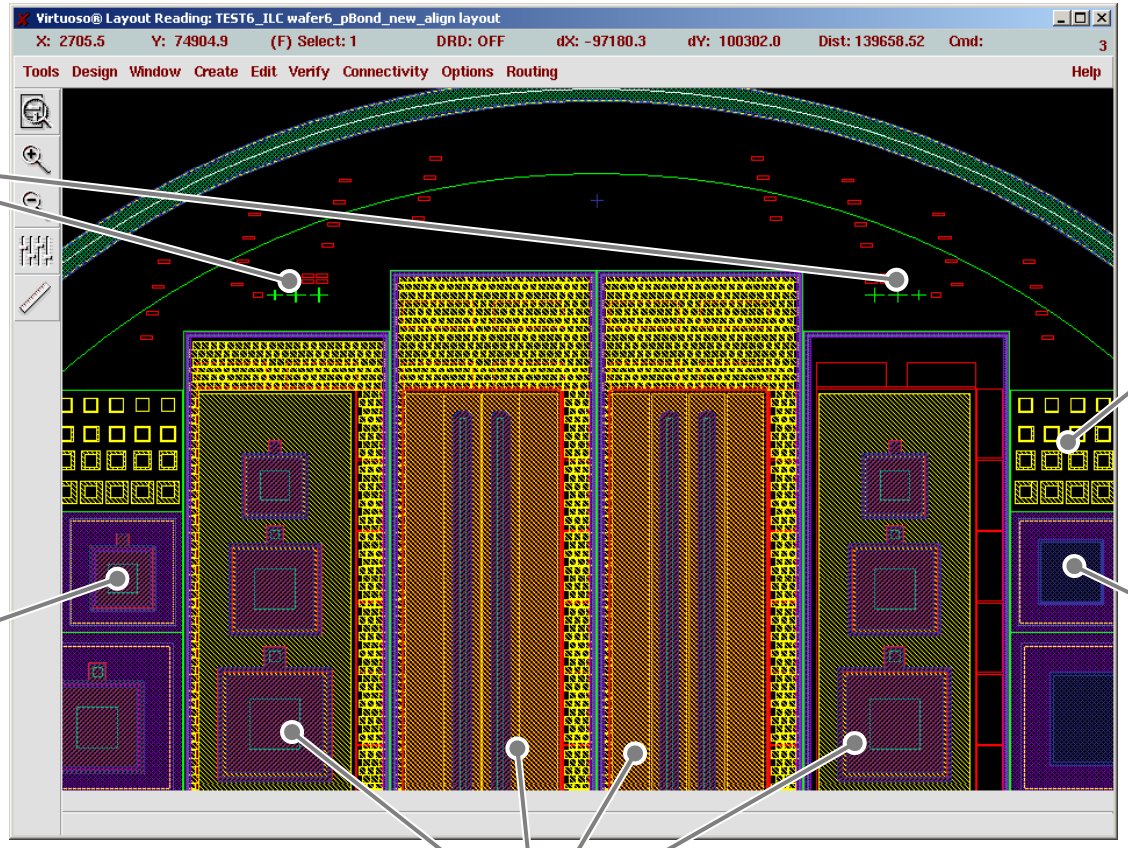
Large area Type II Diodes and mechanical samples

Alignment marks in BOX to find the partial p-implant after bonding

Implants like DEPFET config.



unstructured n+ on top
structured p+ in bond region



Some test structures

Diodes with various areas

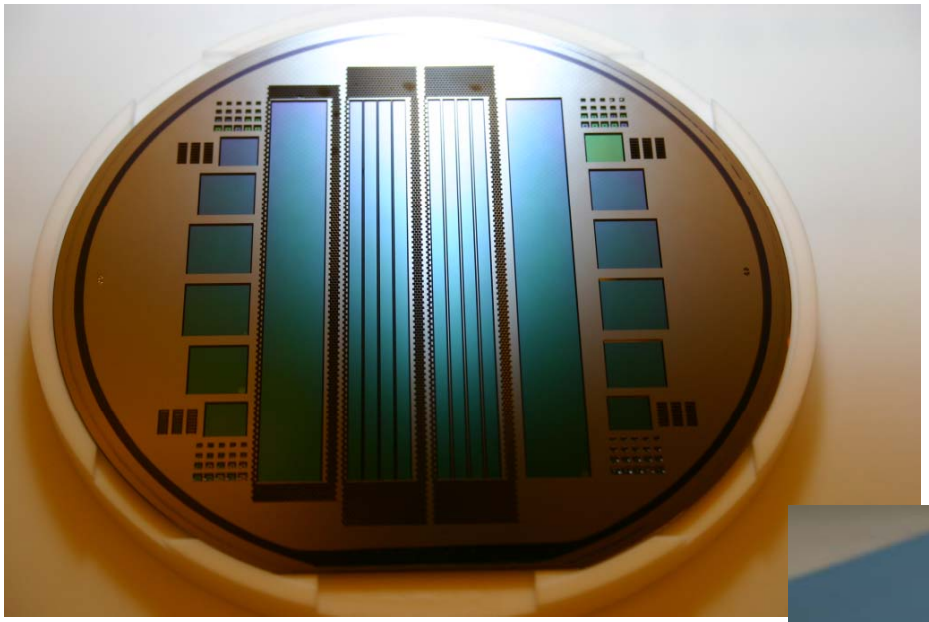
MOS-C with various areas

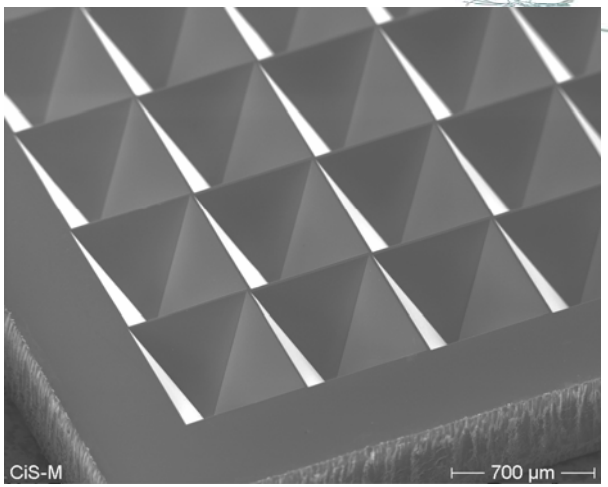
4 "full size" 1st layer ILC ladders 100x13 mm², 1 and 3 mm frame along the long side

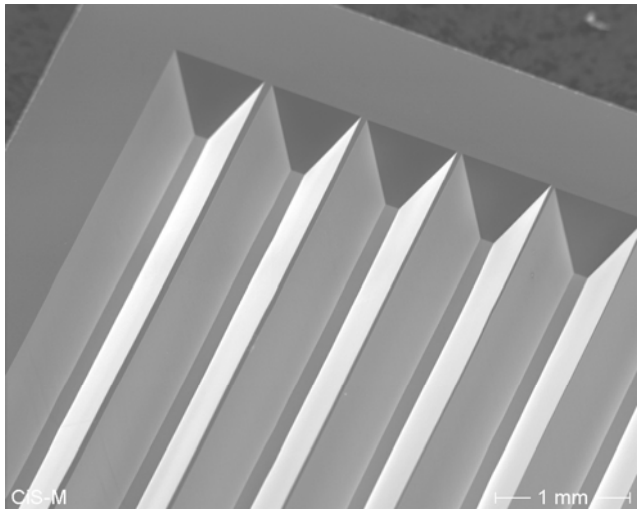
Just finished!!

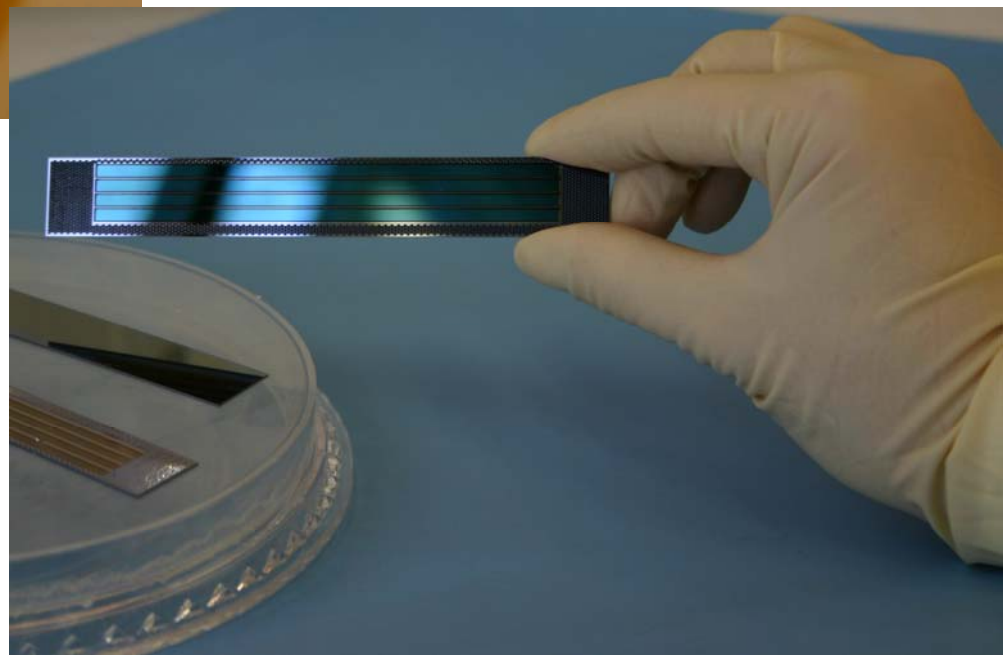
Evaluation as soon as I'm back...

Thinning : mechanical samples

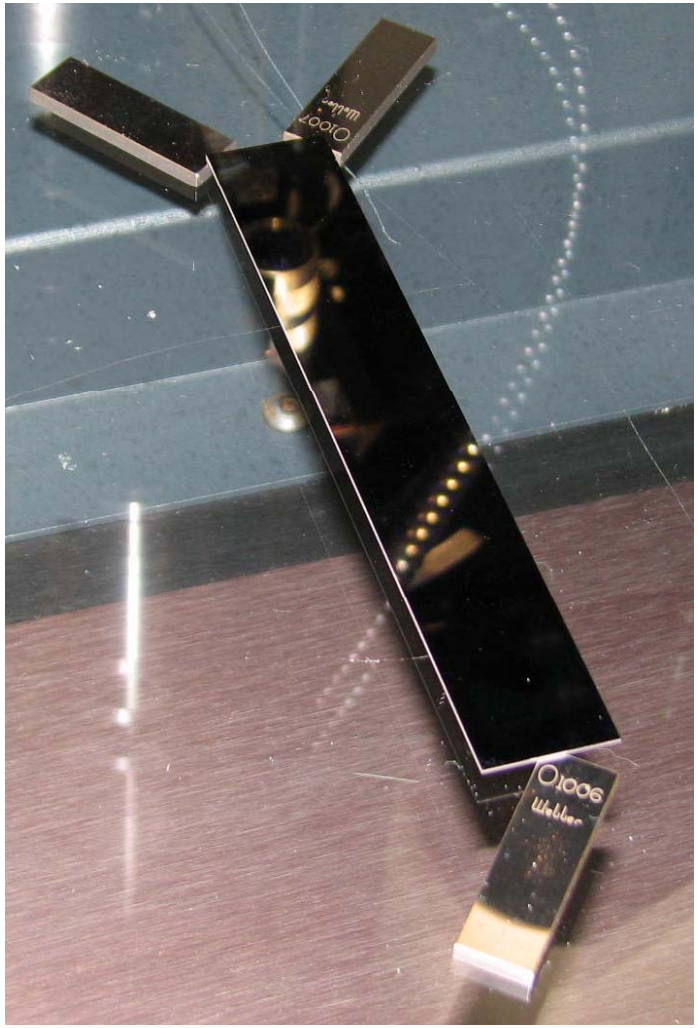




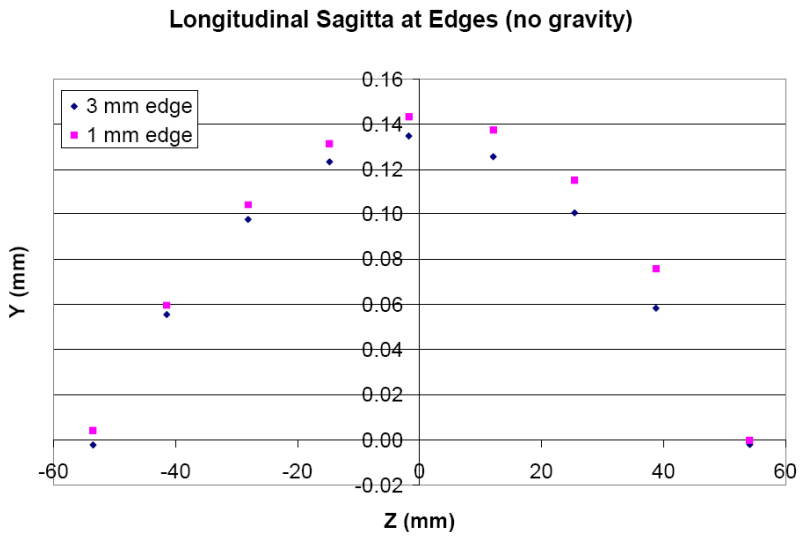


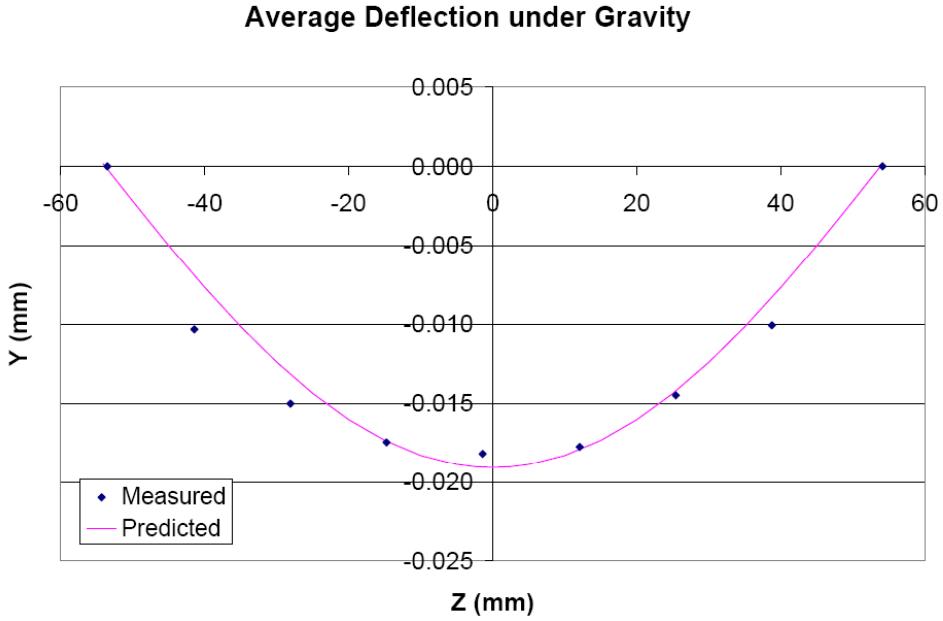


Bow under gravity



Bill Cooper, Fermilab





Flatness!!!??

→ "all-Silicon" module? - Not really..

Material	Si	SiO_2	Si_3N_4	Al
Thickness (µm)	50	0.1 .. 1	≈ 0.1	1 .. 2
CTE (ppm/K)	2.6	≈ 0.5	≈ 2.8 - 3.6	24

→ Build-in stress due to high temperature processes! → Wafer/Sensor bow!

1. Does it change with temperature (ΔT ≈ 40 K) after processing/dicing?
2. If it's stable, is it of concern at all?

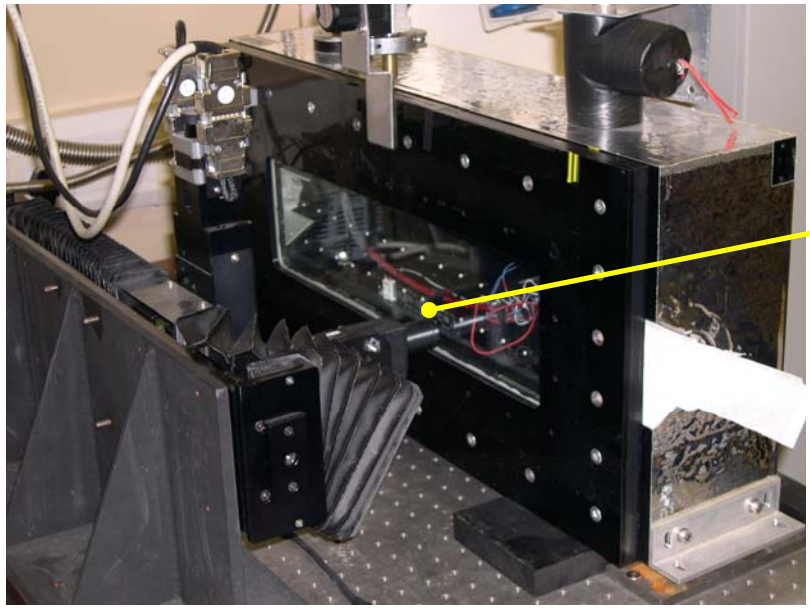
(3. Can the build-in stress (and bow) be adjusted with additional single sided layers?)

→ First assessment:

-: 1st layer ladder with single sided double metal (Al-600nm SiO_2-Al on front side) diced!

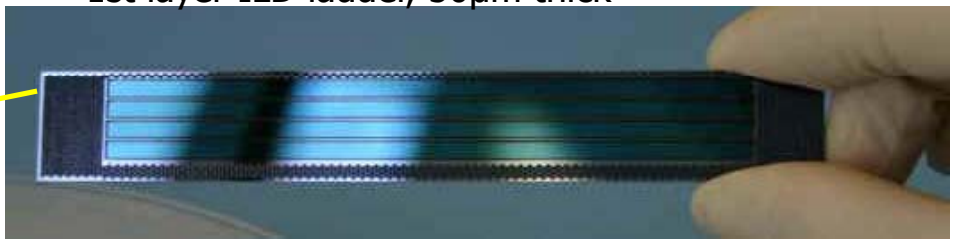
→ Measure bow and temp. dependence at RAL (Erik Johnson)

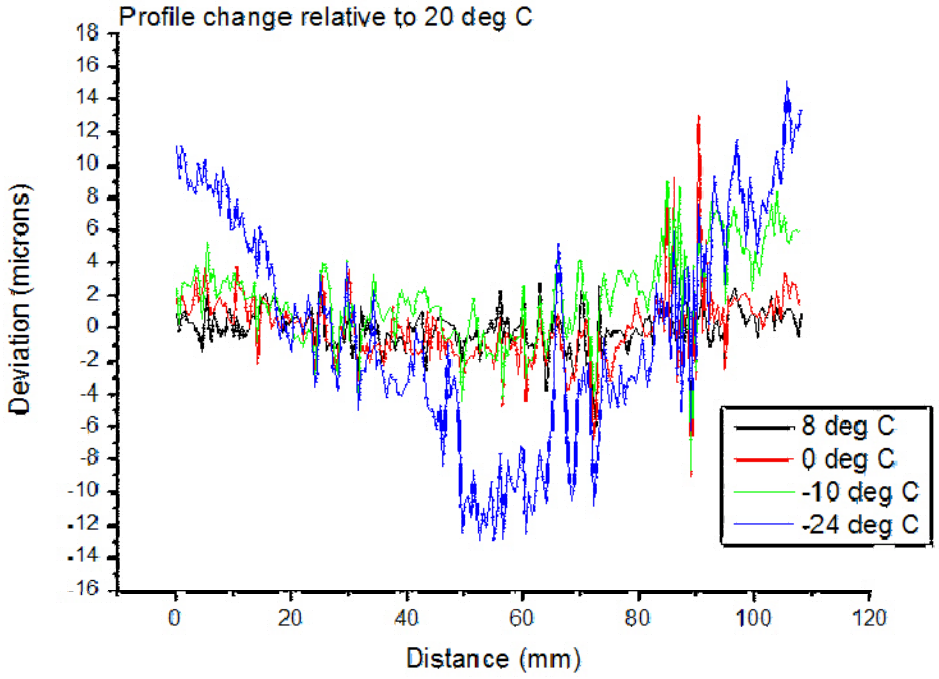
Bow vs. Temperature (at RAL)



double metal sample,

1st layer ILD ladder, 50µm thick





measure flatness down to -24 degC:

-: max. +/- 12 µm at ΔT=44K

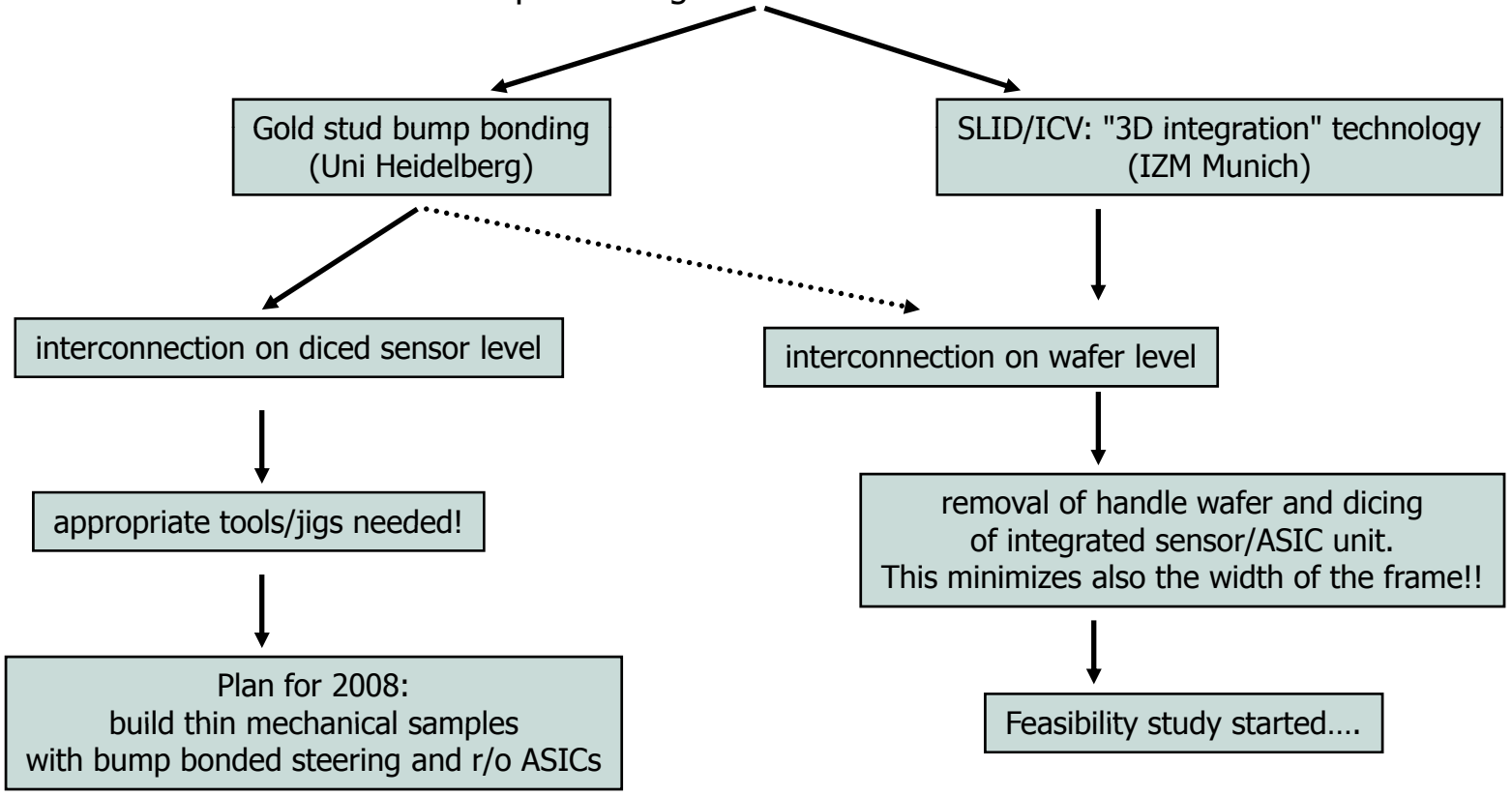
-: small effect at 20degC→-10degC

-: these are just first results, more tests underway (many thanks to Erik and RAL!)

Open questions, next steps → ladder assembly/interconnections

→ So far it looks feasible, from the processing point of view, to produce fully depleted sensors of almost any desired thickness without degradation of the sensor properties.

→ The next step is to work on the integration of sensor and auxiliary ASICs (steering and r/o chips)
→ "bump" bonding of thin ASICs to thin Silicon!



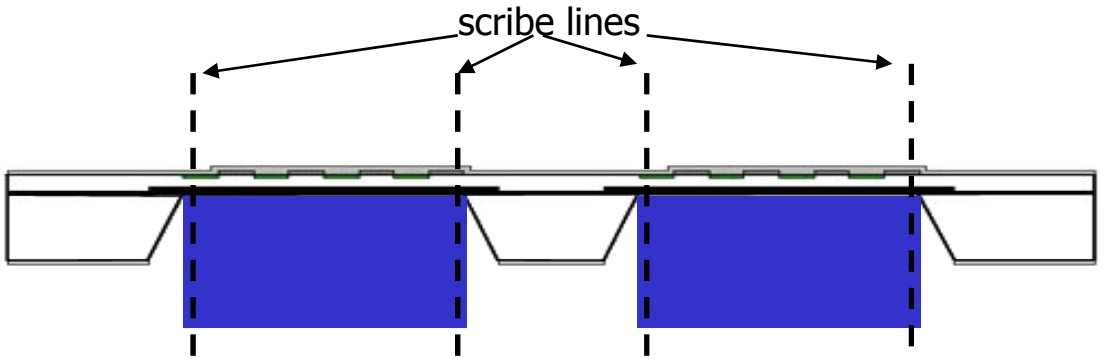
A final remark…

If it turns out that the approach of the "all-silicon" module is too risky or has too much material…

…we probably don't have to make use of the integrated frame and still have a **save handling of thin sensors**

Possible Process flow could be:

1. Finish top side of the sensor
2. remove handle wafer in the sensitive area
3. finish back side processing
4. attach/glue low mass material (foam a la LCFI: SiC, RVC…) to the open back side
5. dicing (laser cutter? saw?), only thin sensor area, supported by (rigid??) foam material



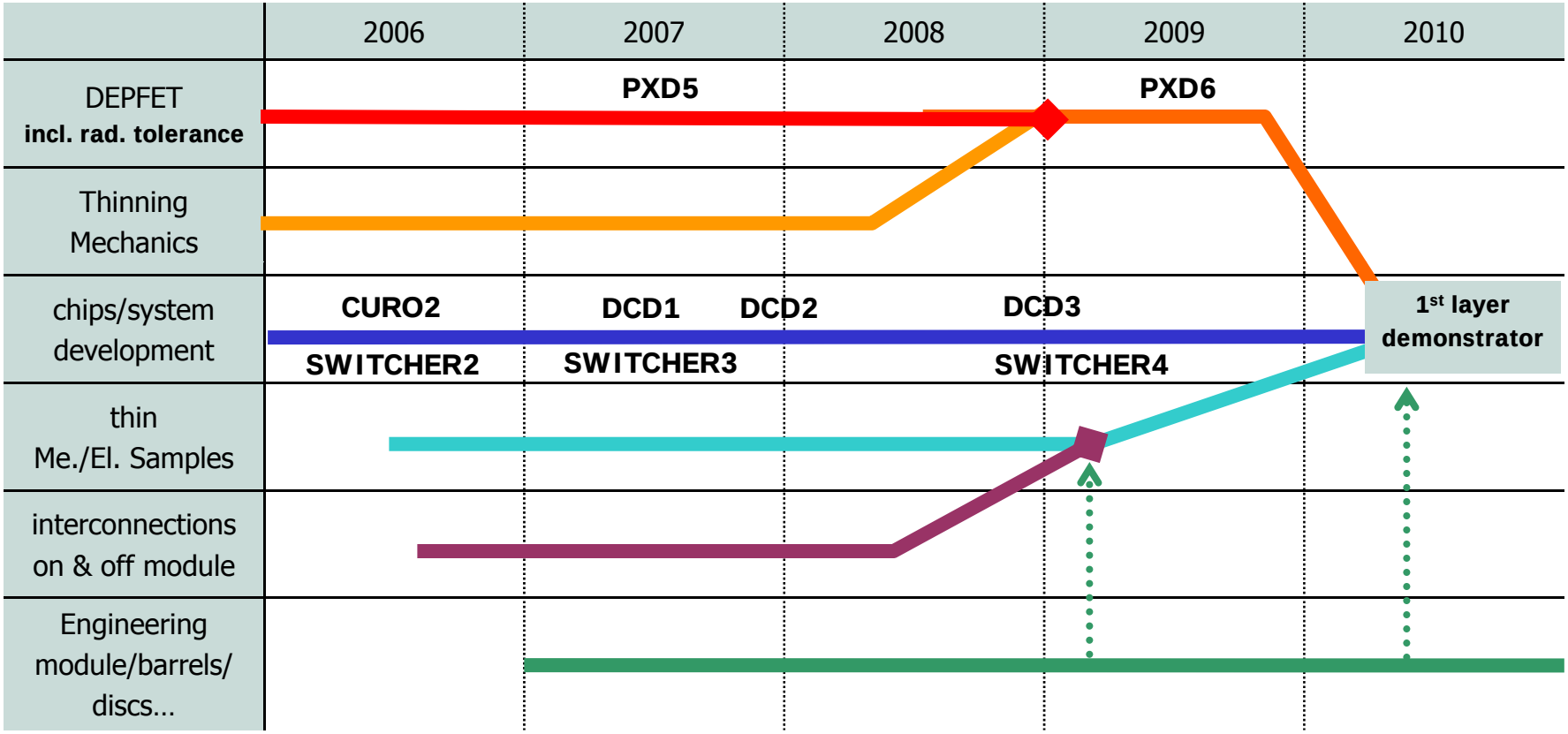
Summary

- ✓ Evaluation of the **new DEPFET generation** is in full swing:
  - ✓ New Sensors, larger matrices, with improved gain under test
  - ✓ New r/o chip operational
- ✓ **Thinning** technology at the door step to migrate to the **production line**. Excellent results using a commercial supplier for the engineered SOI wafers.
- ✓ Next Production PXD6 on custom made SOI Wafers → Thin DEPFETs end 2009!

It remains a challenging task but we don't see any show stoppers and are on schedule for a thin "full size" demonstrator by ~2010 - 2012!

- Backup slides follow….

….towards a thin demonstrator (in baseline design)



- ✓ ASIC production: UMC, AMS, IBM, TSMC…. use the best available process
- ✓ DEPFET prototyping and series production of the sensors at the MPI Halbleiterlabor

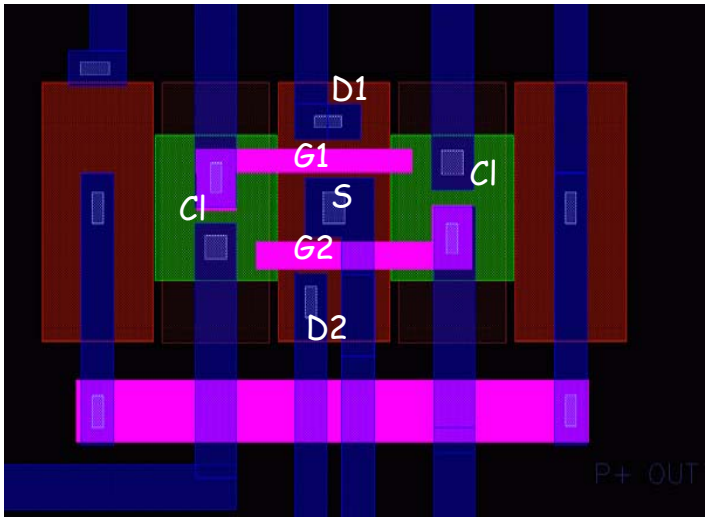
Irradiations - Overview

-: Irradiations with ^{60}Co gammas, protons and neutrons

-: Single pixel structures with 6 and 7 µm gate length

-: Look for degradation in:

- Electric characteristics (V_{th} shifts, g_m and g_q)
- Leakage current
- noise spectrum (1/f noise)
- Spectroscopic performance

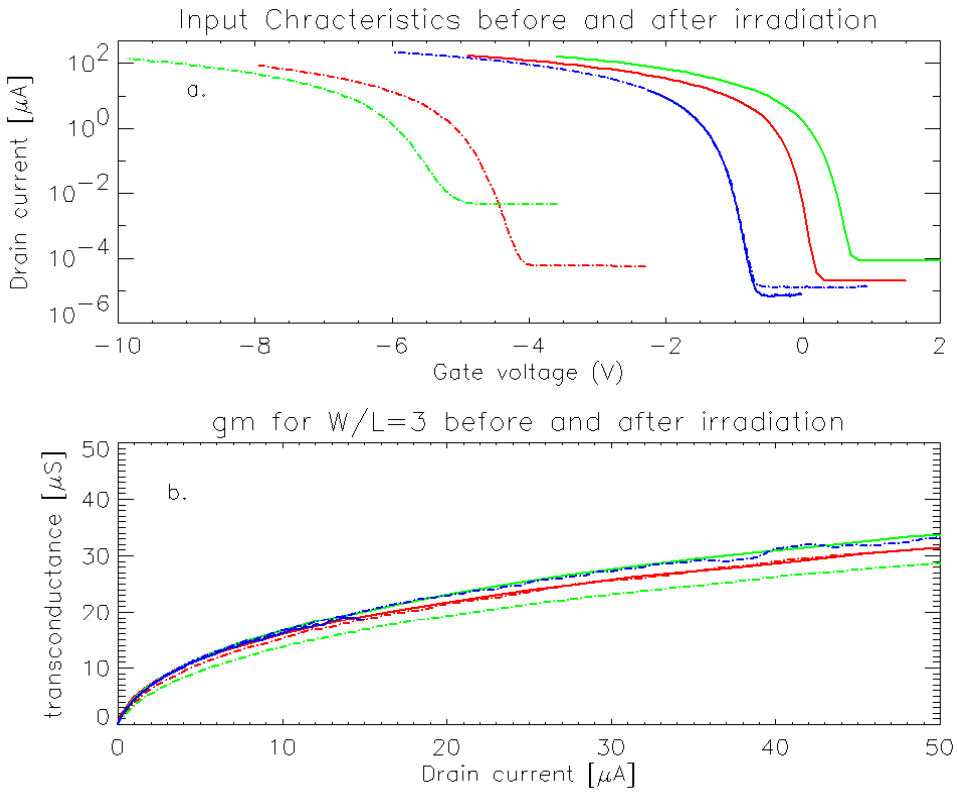


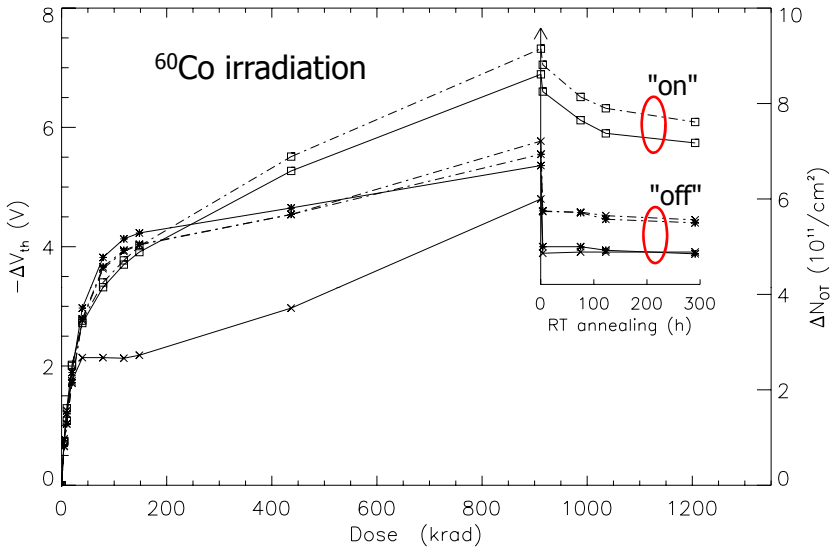
	PXD4-10 MO2	PXD4-5 M05	PXD4-2 J14
Type	Protons, 30MeV	Neutrons, 1-20MeV	Gammas - ^{60}Co
Fluence / Dose	$1.2 \cdot 10^{12}$ p/cm²	$1.6 \cdot 10^{11}$ n/cm²	913kRad
1MeV n equivalent	$3 \cdot 10^{12}$ n_{eq}/cm²	$2.4 \cdot 10^{11}$ n_{eq}/cm²	n/a

LBNL Cyclotron

GSF Munich

Basic Characteristics: ΔV_T, g_m, I_{Leak}

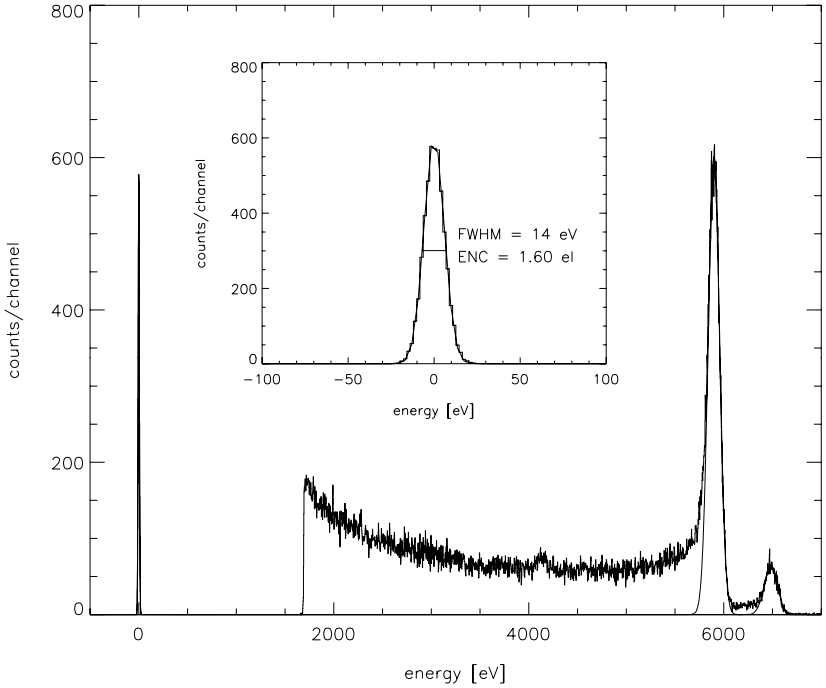


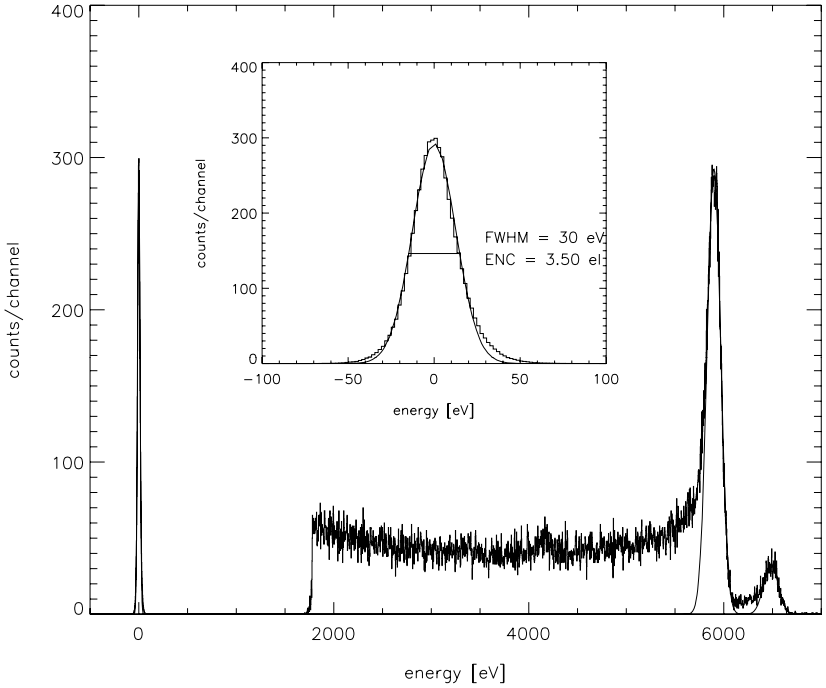


irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3x10^{12} n/cm^2	~-5V	~ -15%	26 pA

(*) 5..22 fA non irrad.

Spectroscopic Performance - ^{60}Co irradiation





non-irradiated

V_{thresh}≈-0.2V, V_{gate}=-2V

I_{drain}=41 µA

time cont. shaping τ=10 µs

Noise ENC=1.6 e^- (rms)

at T>23 degC

913 krad ^{60}Co

V_{thresh}≈-4.0V, V_{gate}=-6.0V

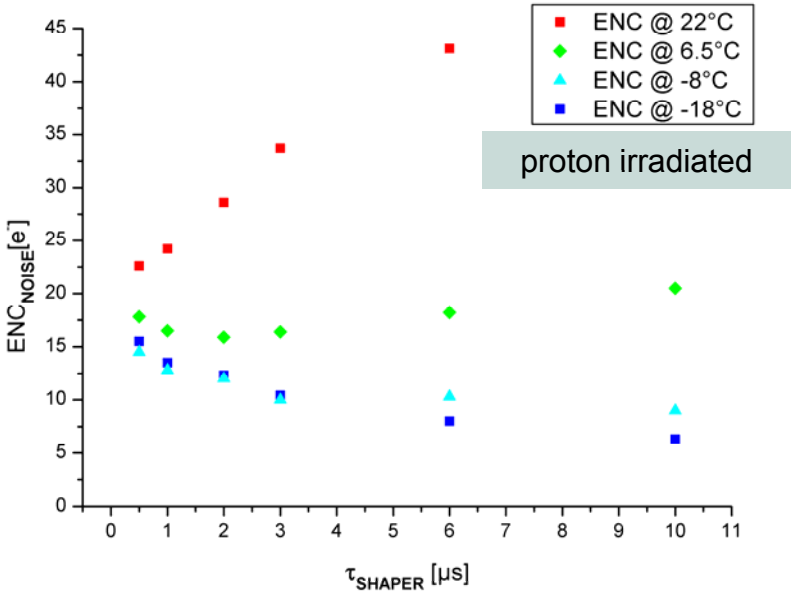
I_{drain}=40 µA

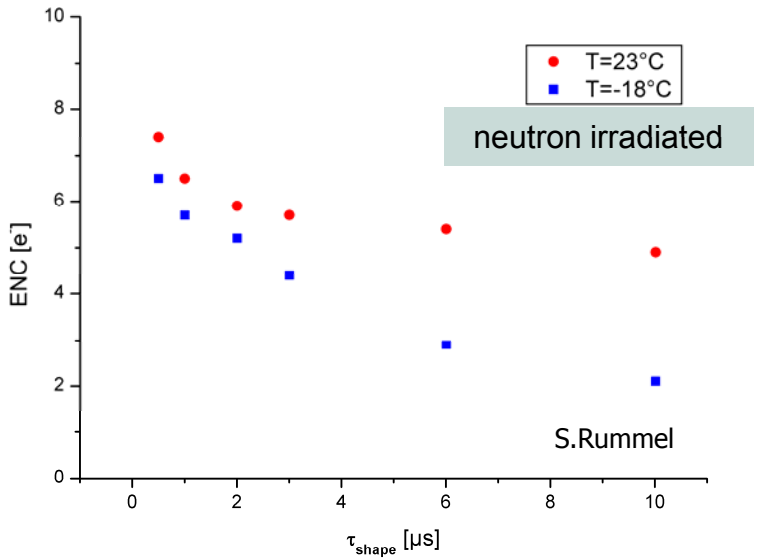
time cont. shaping τ=10 µs

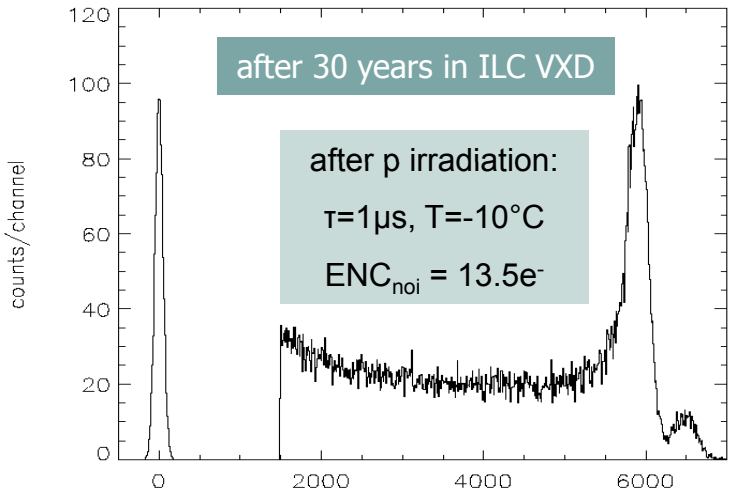
Noise ENC=3.5 e^- (rms)

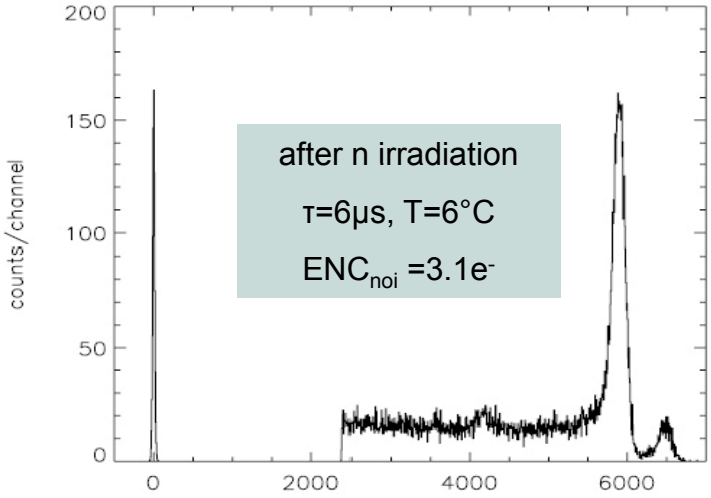
at T>23 degC

Spectroscopic Performance - p and n irradiation

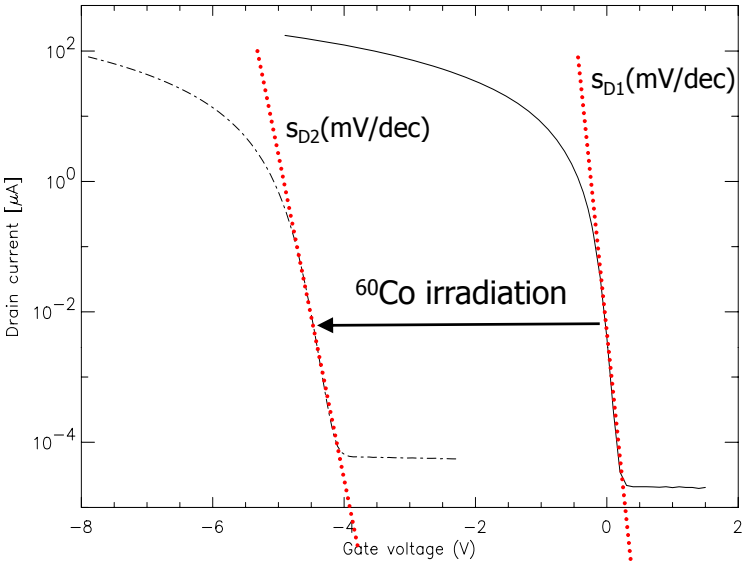


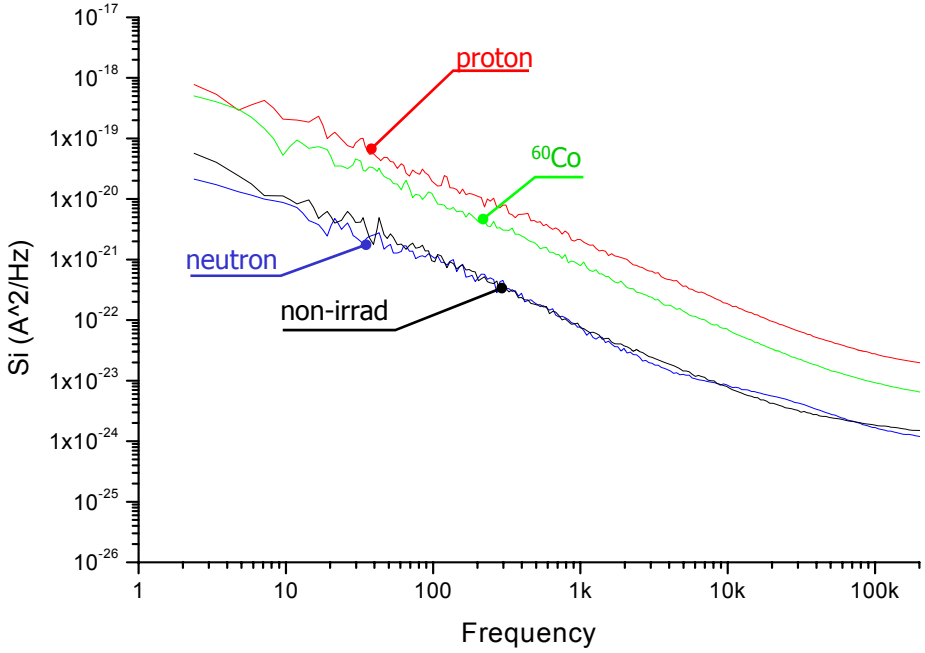






Subtreshold current → Interface trap density → 1/f noise



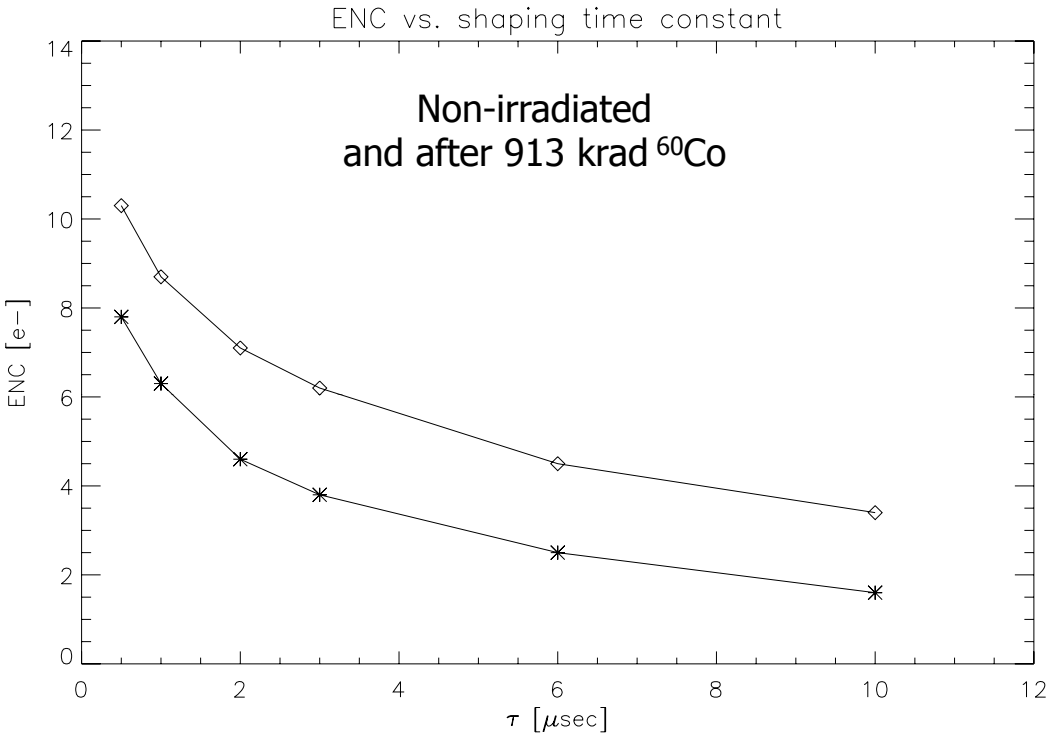


$$\Delta N_{it} = \frac{C_{ox}}{kT \cdot \ln(10)} \cdot (s_{D2} - s_{D1})$$

irradiation	TID / NIEL fluence	Δs (mV/dec)	ΔN_{it} ($cm^{-2} \cdot eV^{-1}$)
gamma ^{60}Co	913 krad / ~ 0	88	$1.6 \cdot 10^{11}$
neutron	~ 0 / 2.4×10^{11} n/cm^2	~ 0	~ 0
proton	283krad / 3×10^{12} n/cm^2	230	$4.2 \cdot 10^{11}$

Lit: ~ 10^{12}-10^{13} $cm^{-2} \cdot eV^{-1}$ for 200nm gate oxide

Noise vs. shaping time τ - ^{60}Co irradiation



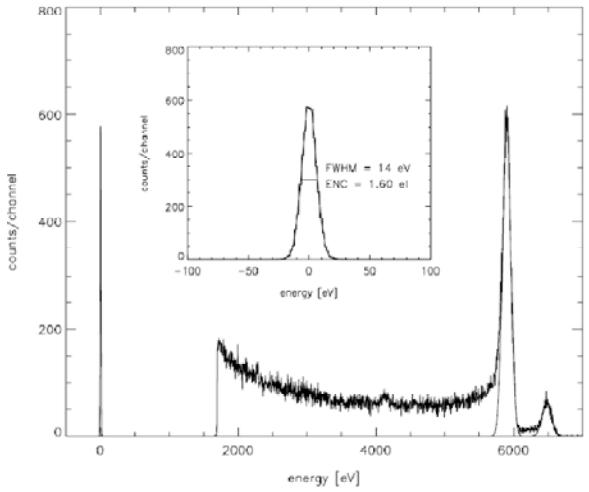
$$ENC = \sqrt{\underbrace{\alpha \frac{8kTg_m}{3g_q^2}\frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2}_{1/f} + \underbrace{qI_{Leak}\tau}_{I_L}}$$

Bandwidth and Noise

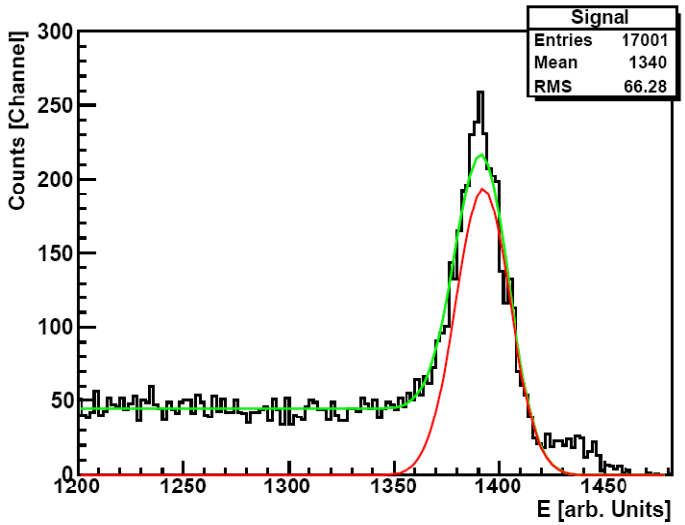
High readout speed → high bandwidth → short shaping times

$$ENC = \sqrt{\alpha \frac{8kT}{3g_q^2} g_m \frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau}$$

Measurements of a single pixel with an external high bandwidth amplifier



1.6 e ENC at t=10 µs



40 e ENC at t=20ns (50MHz)

Intrinsic DEPFET noise sufficiently low for high speed operation at ILC

In Summary: Prospects

- ✓ Production of 2nd iteration DEPFETs was finished summer 2007,
- ✓ higher internal amplification demonstrated (g_q=0.4nA/e → almost 1 nA/e), better S/N
- ✓ New Switcher3 chips tested and functional
- ✓ New r/o chips DCD designed for read-out of large matrices are under test

Power Consumption for the ILC VXD (baseline design) with these new chips

layer 1: 8 ladders, 4096x512 pix./ladder → ~ 12W/ladder → ~100 W/layer

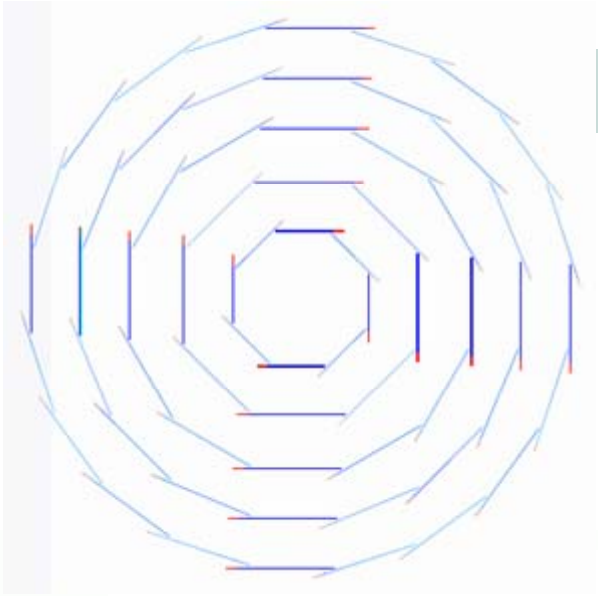
layer 2-5: 56 ladders, 10496x928 pix./ladder → ~ 21W/ladder → ~1200 W/ 4 layers

→ 1300 W → **6.5 ... 13 W** with pulsed power operation 1/200 - 1/100

About 90% of the power is dissipated at the ladder ends (r/o chips DCD)

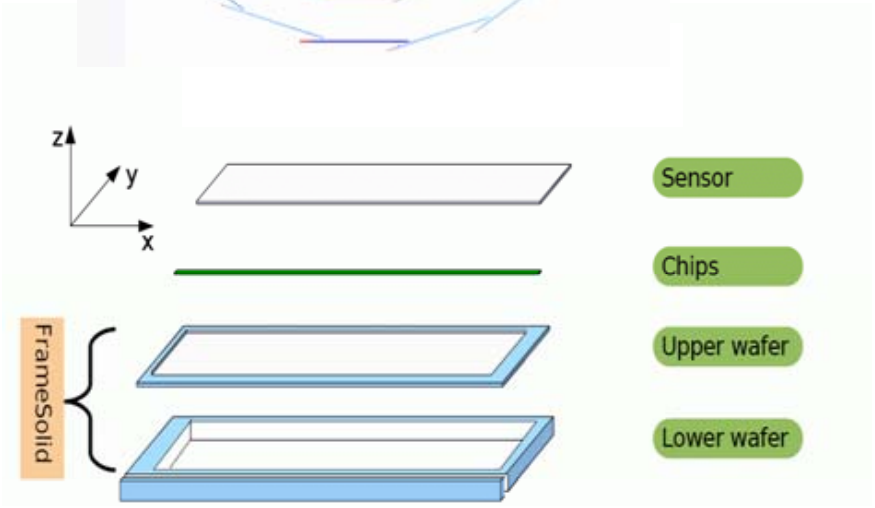
Based on the experience made with the prototype system, we are confident that the DEPFET in the **present baseline design** can meet the requirements at the ILC VXD. In this concept, with the read out at the end of the ladders, the biggest challenge is the required row rate and the capacitive load at the f/e inputs. There are several ideas how to increase the "head room" in this respect, one of those being the use of the emerging 3D technologies. This will be one of the future R&D directions.

Simulation: LDC Geometry description

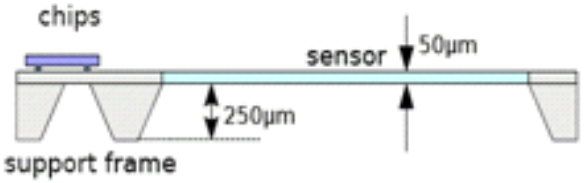


Sensitive layer thickness = 50 μm
Pixel size = 25×25 μm^2

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2×12.5
3	3.8	12	2×12.5
4	4.9	16	2×12.5
5	6.0	20	2×12.5



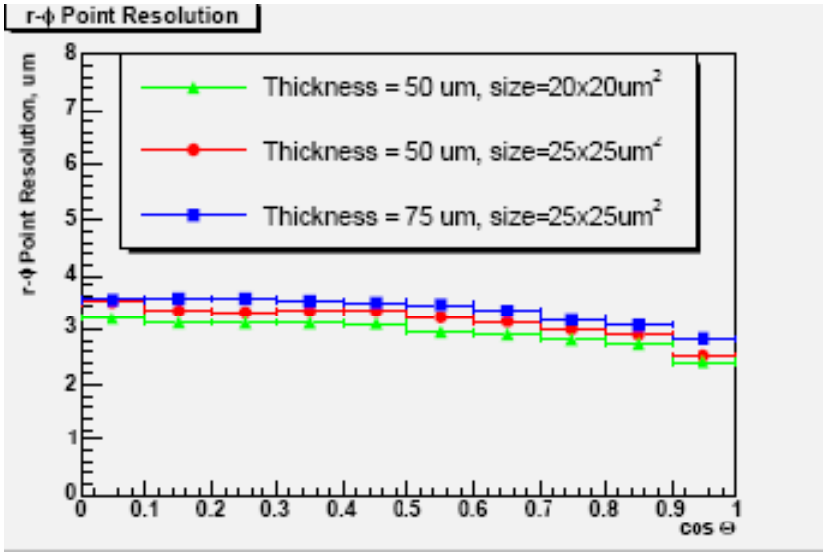
→ LDC ladders with support frames

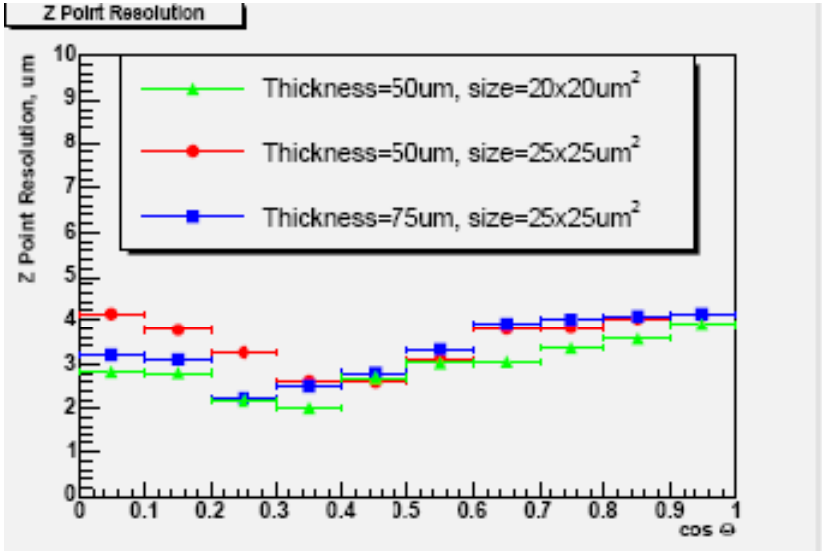


Material up to first layer : beam pipe (500 μm beryllium)

MC Studies

Spatial resolution for 50 mm thick 25 x 25 mm^2 pixels: <3.5 mm (r-φ), <4.0 mm (z)

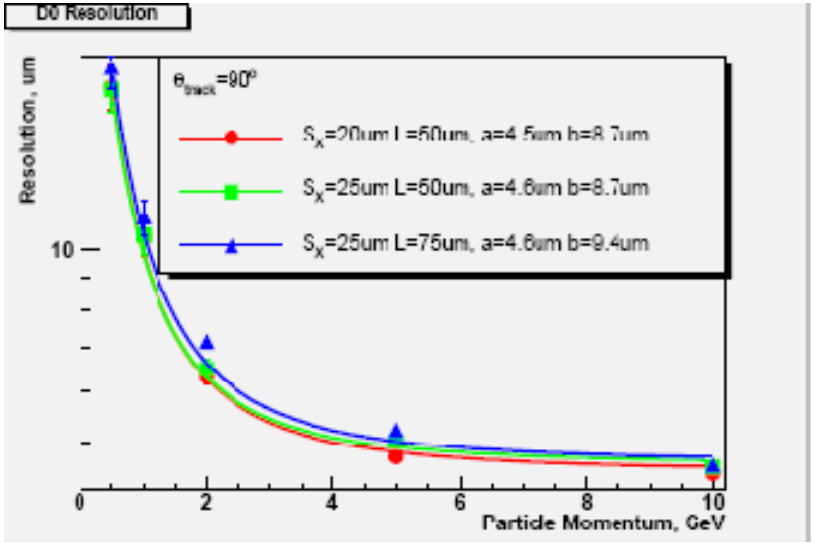




Impact parameter resolution
(5 layers, frames, 500 mm Be beam pipe)

$$\sigma(IP)_{r\text{-}\phi} = 4.5\ \mu m \oplus \frac{8.7\ \mu m}{p(GeV/c)\ \sin^{3/2}\theta}$$

ILC requirements fulfilled



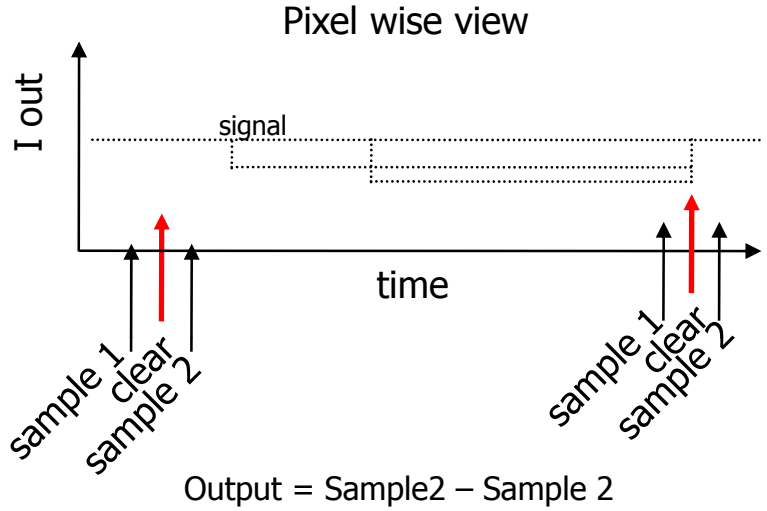
Correlated Double Sampling

Why CDS?

- Subtraction of pedestals
- Strong suppression of 1/f noise

Drawbacks:

- Long readout time per row
- Signal loss in presence of incomplete Clear
- White noise is increased by sqrt(2)



Output = Sample2 – Sample 2

$$T_{integration} = T_{Frame} = \frac{n_{row}}{2} * \left(2 * T_{Sampling} + T_{Clear}\right)$$

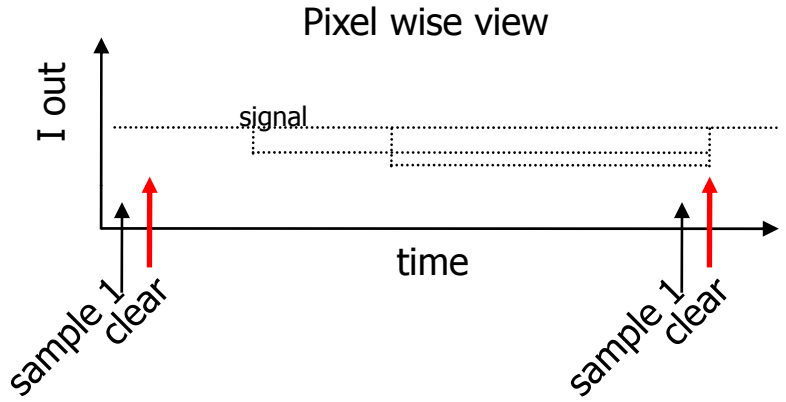
Subtraction of pedestals could be done by a current source at the input of the front-end (see CARLOS chip)

1/f noise is not an issue at high bandwidth - ENC is limited by white noise

Scheme S-C-S-C-S-C

Sample only once per clear
Speed increase about 30%
Incomplete clear leads to problems

$$T_{integration} = T_{Frame} = \frac{n_{row}}{2} * \left(T_{Sampling} + T_{Clear}\right)$$



$$Signal_n = S_n - Pedestal$$

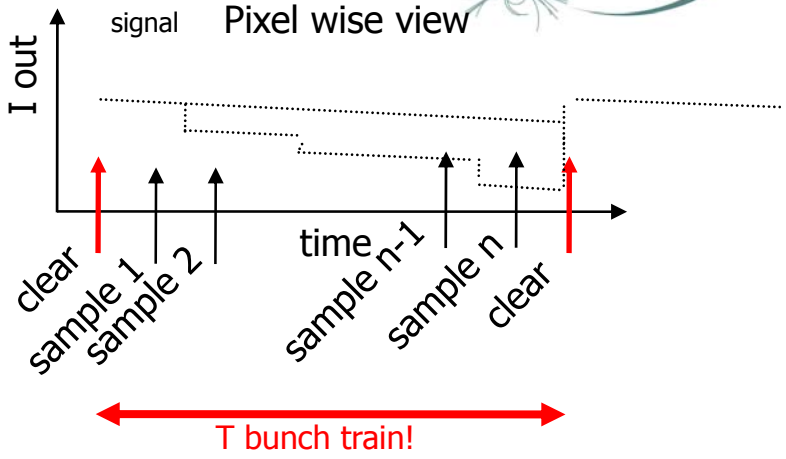
Schemes C-S-S-S … S-S-S-C

Clear while quite phase (outside bunch train)

- Utilize the CCG for clear process over whole matrice
- CG could be optimized for charge collection
- No Clearswitchers – reduced complexity
- **Full Clear** will be possible

Increase in speed 66% compared to CDS

Signal = difference of two consecutive samples



$$T_{integration} = T_{Frame} = \frac{n_{row}}{2} * T_{Sampling}$$

$$Signal_n = S_n - S_{n-1}$$

$$Signal_n = S_n - \frac{1}{k}\sum_{i=1}^{k} S_{n-i}$$

Related questions:

- 1/f noise contribution?
- Increase of shot noise?
- Charge handling capacity of the DEPFET sufficient?
  - Occupancy?
  - Leakage current due to long period between two clears?

PiN Diodes on thin Silicon