# A custom 12-bit cyclic ADC for the electromagnetic calorimeter of the International Linear Collider

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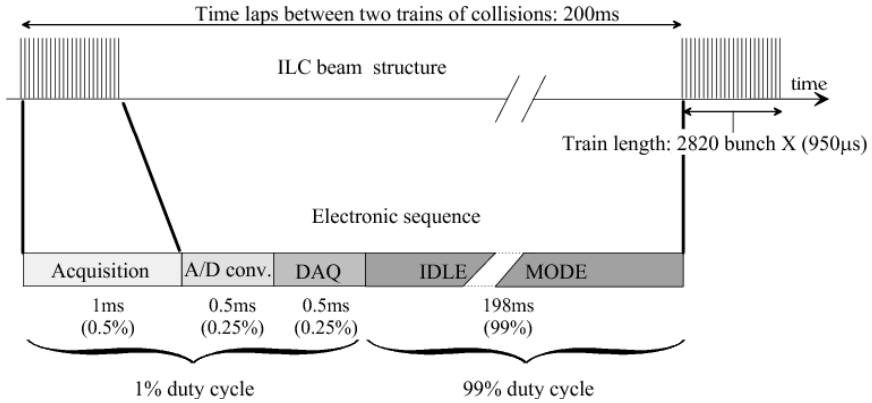
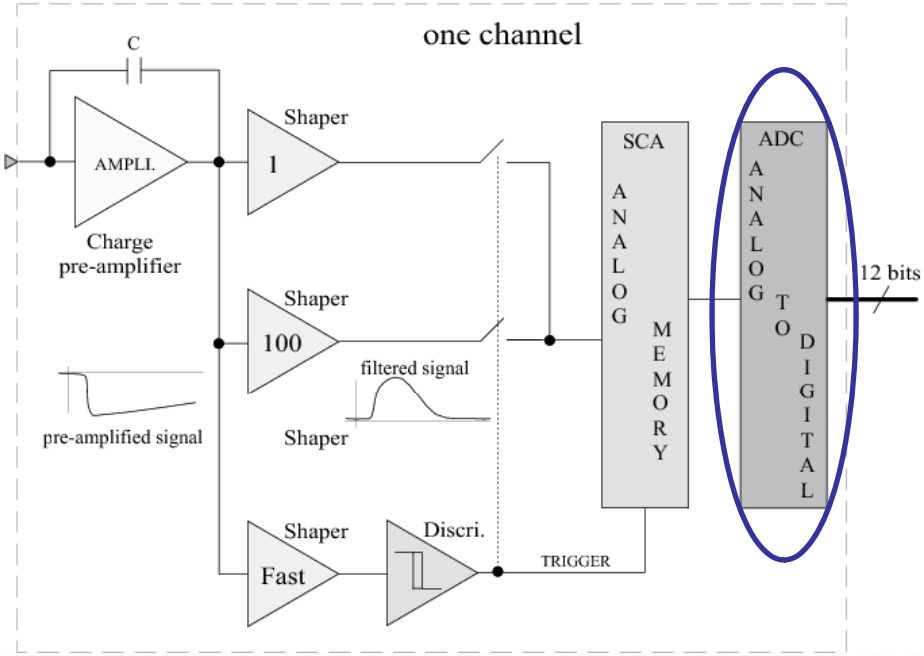
CALICE Calorimeter for ILC

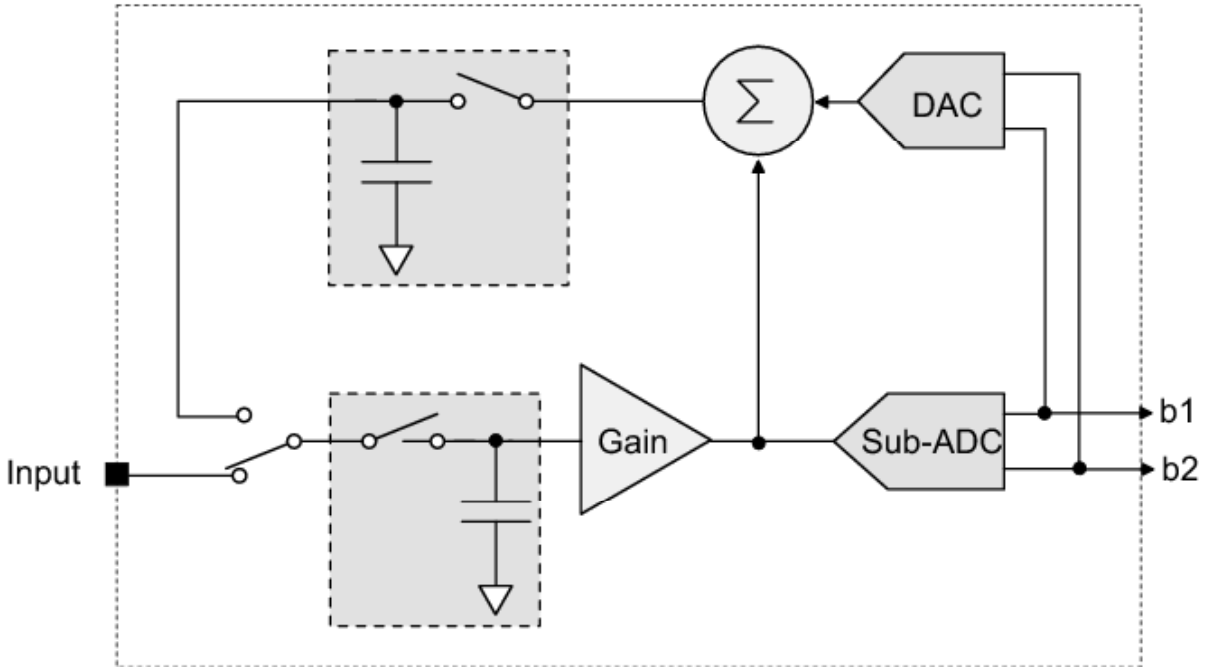
# VFE electronics of the Ecal




- **Main requirements for the ADC:**
  - 100 Millions channels
  - ULTRA LOW power is the key issue:
    - **25 µW/channel**
    - **2.5 µW** for the ADC with one ADC per channel
      - **Power pulsing needed**
    - **Advantages with one ADC/ch**
      - **No "fast" ADC required**
      - **Integrity of analog signals saved**
      - **Power saved**
  - Resolution:
    - **12 bits if 2-gain shaping**
  - Time of conversion: 500 µs for 5 data
    - **T_conversion = 100 µs**
  - Die area:
    - **As small as possible…**

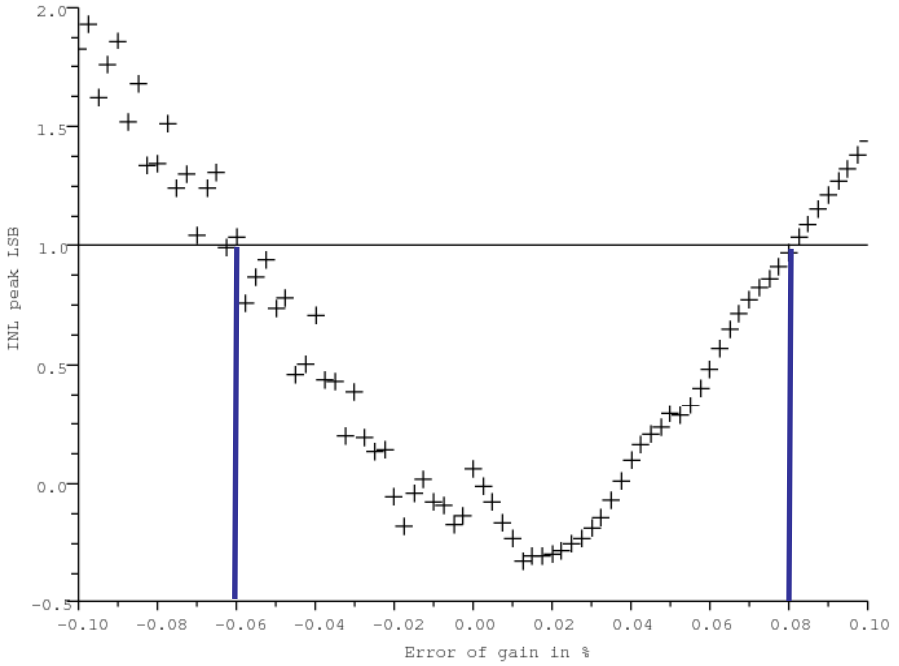
# Architecture of the ADC



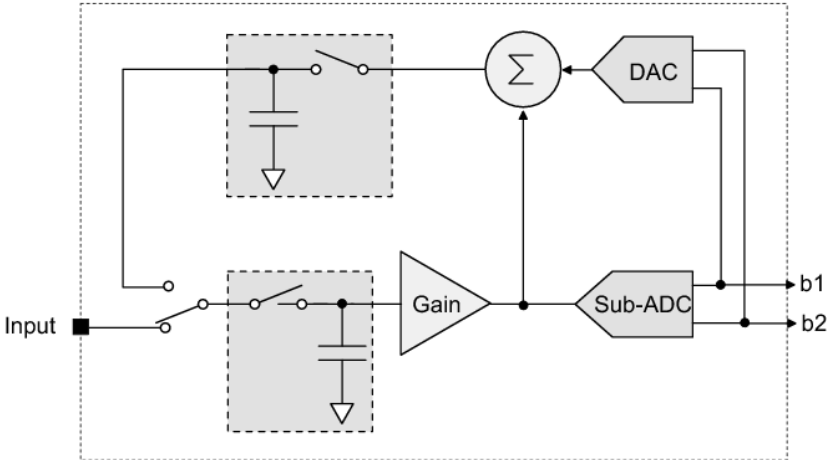

- 1.5 bit per stage architecture
  - Insensitive to the offset of the comparator, ± 1/8 of the dynamic range
- Silicon area and consumption limited due to the structure of the ADC
- Fully differential Input, reference, clock…
- Clock frequency 1MHz, Technology, 0,35µm CMOS AMS

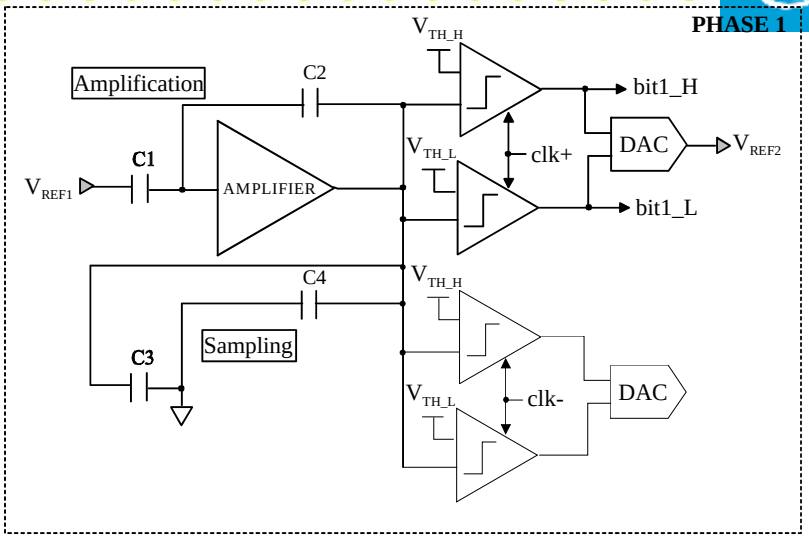
# Enhanced ADC and requirements

- Resolution 12 bits
  - **Open loop gain amplifier, A≥ 16484**
  - **Size capacitance, C ≥ 834 fF**
- Conversion rate T<100µs
  - **Bandwidth of the amplifier, $f_\mu$≥2.86MHz**
- Scilab description of the ADC
- Error of gain tolerated 0.8‰



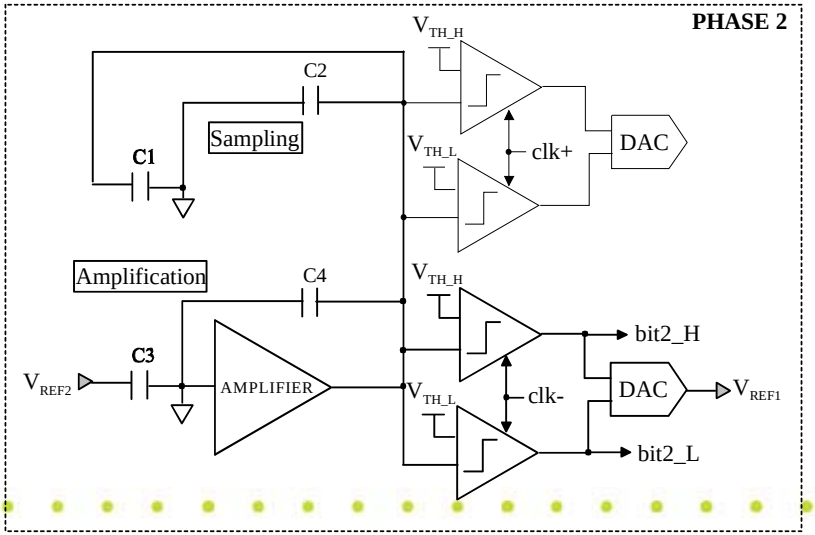
# Design of the ADC




Two conversion phases with a single amplifier

- Gain and Σ, gain 2 amplifier
- Sub ADC, 2 comparators
- DAC, switch array



# Classical cyclic versus optimized

✓ Clock frequency: 1MHz
✓ Supply voltage : 3.5V

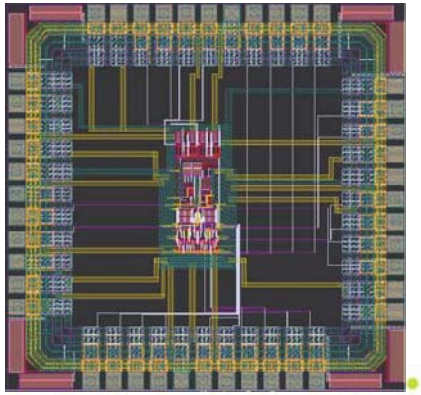
✓ Sent to fabrication in March 08 via CMP, 10 chips delivered with delay in July

✓ Technology: 0.35 µm CMOS Austriamicrosystems.

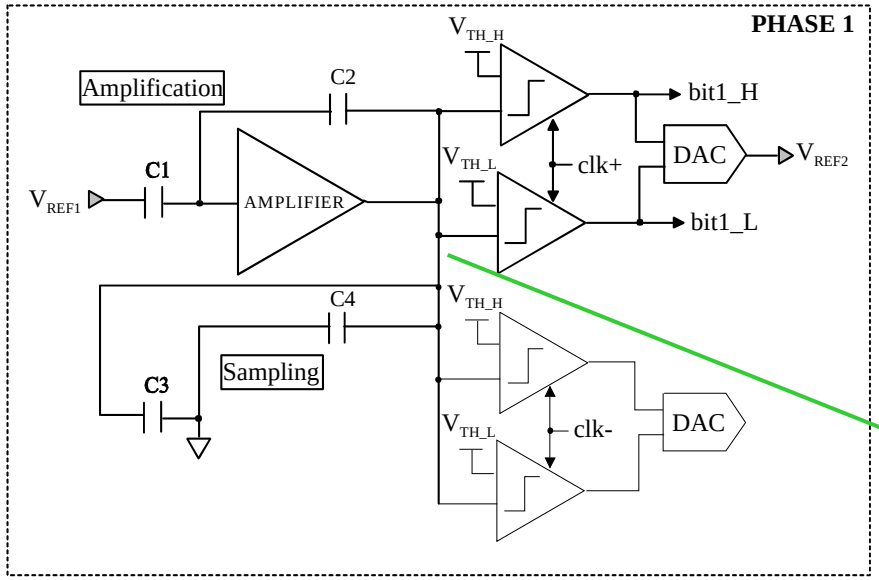
✓ ADC designed with the validated building blocks (Amplifier & Comparator) of our 10-bit pipeline ADC (published in IEEE NSS in June 08) but optimized for the 12-bit precision requirement

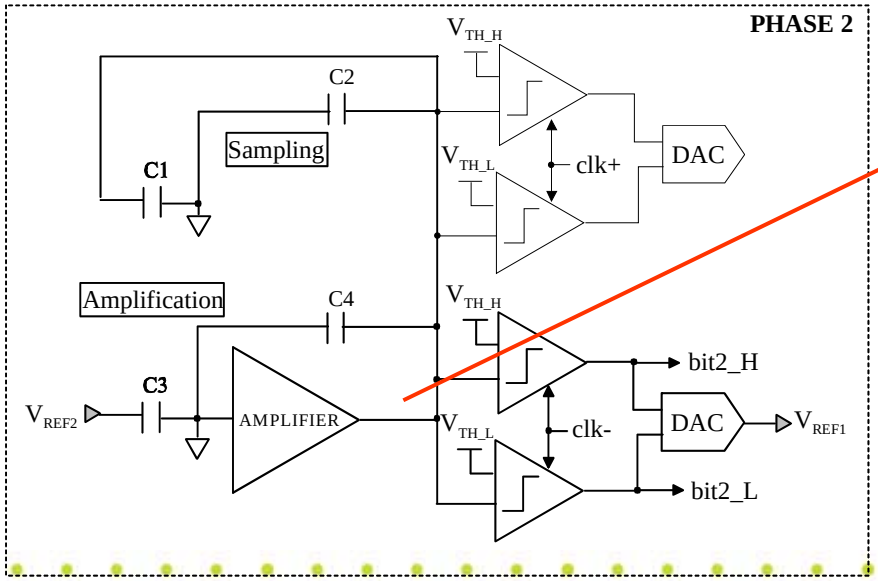
✓ Power pulsing system implemented

| | "Classical" Cyclic | "Optimized" Cyclic |
|---|---|---|
| Resolution | 12 bits | 12 bits |
| Number of elements | 1 amplifier<br>2 comparators<br>1 capacitors array | 1 amplifier<br>4 comparators<br>2 capacitors array |
| Time for one conversion | 12 µs | 7 µs |
| Power consumption | 3.6mW | 4mW |
| Integrated consumption | **1.1µW** | **0.7µW** |
| Area | 0.145mm$^2$ | 0.175mm$^2$ |

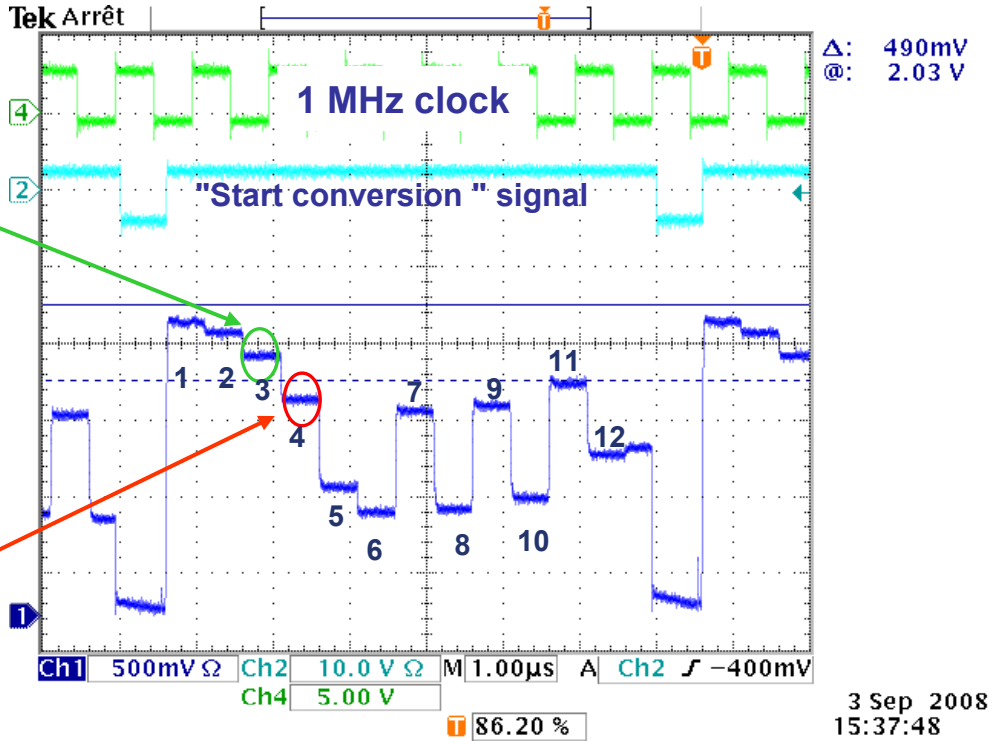


# Results of measurement

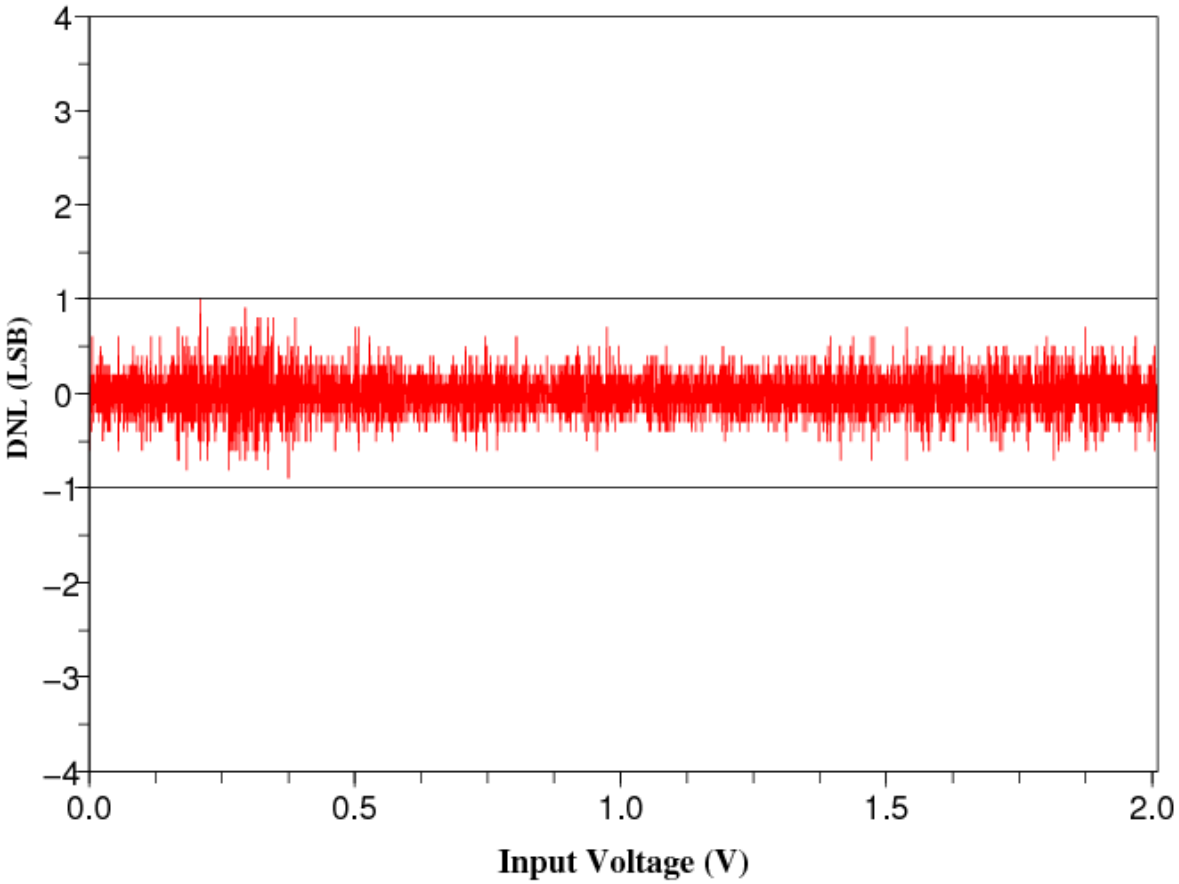



**Oscillogram of the chip under test**

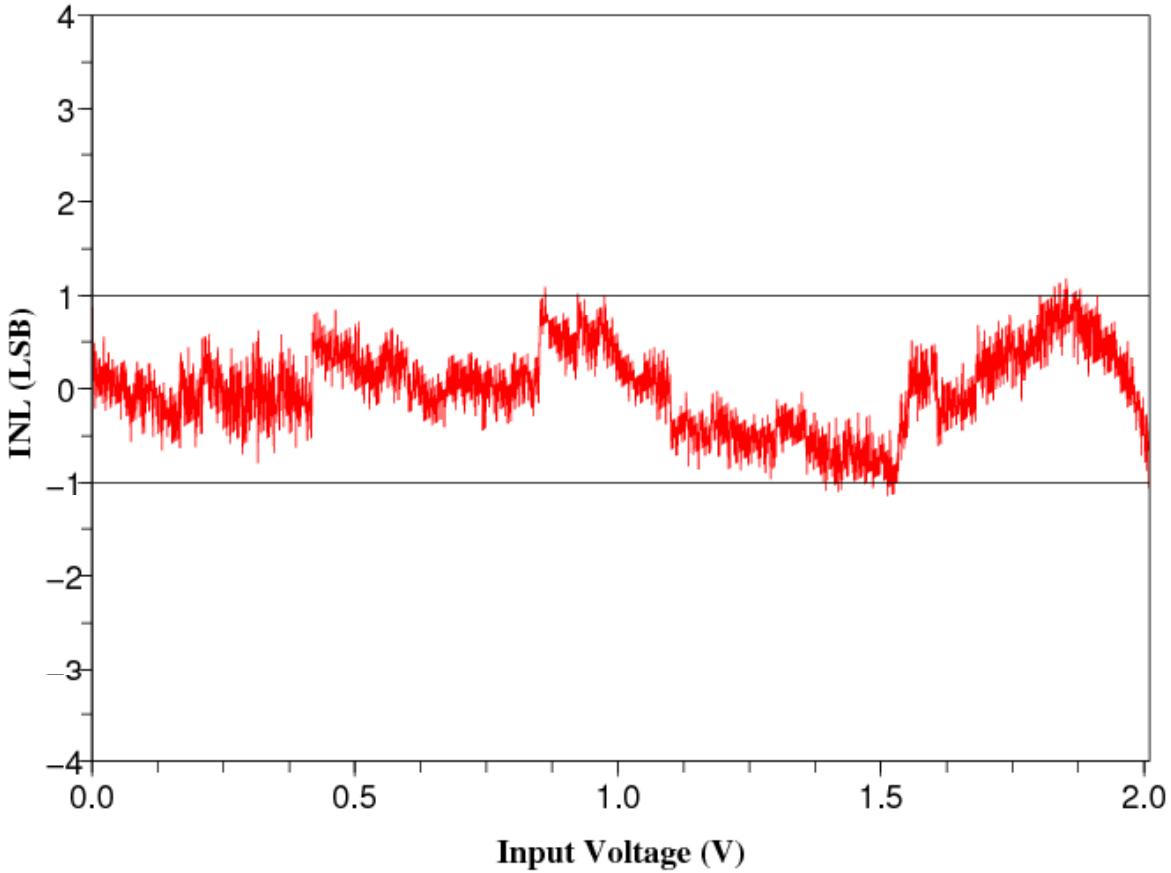


# DNL Measurement




- DNL<+/-1 LSB
- No missing code

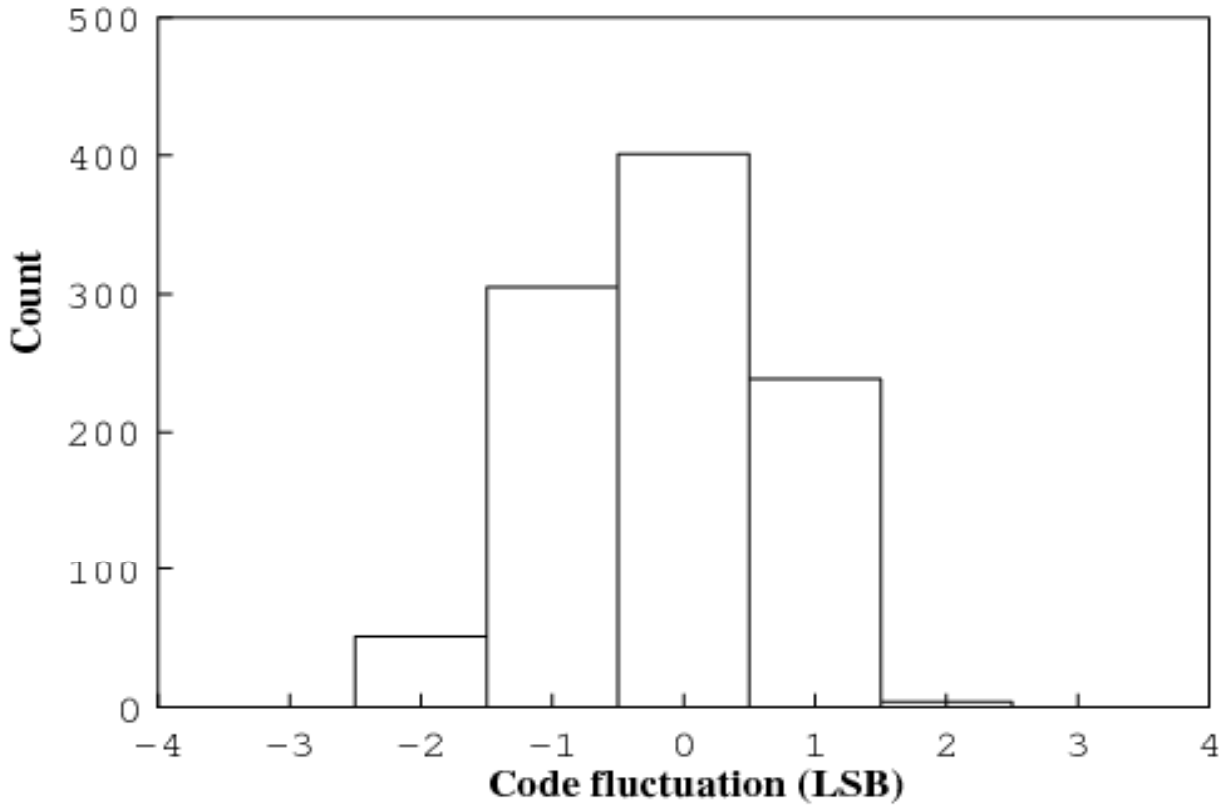
# INL Measurement




- ✓ INL<+/-1.2 LSB
- ✓ Technology limitation due to polysilicon capacitors

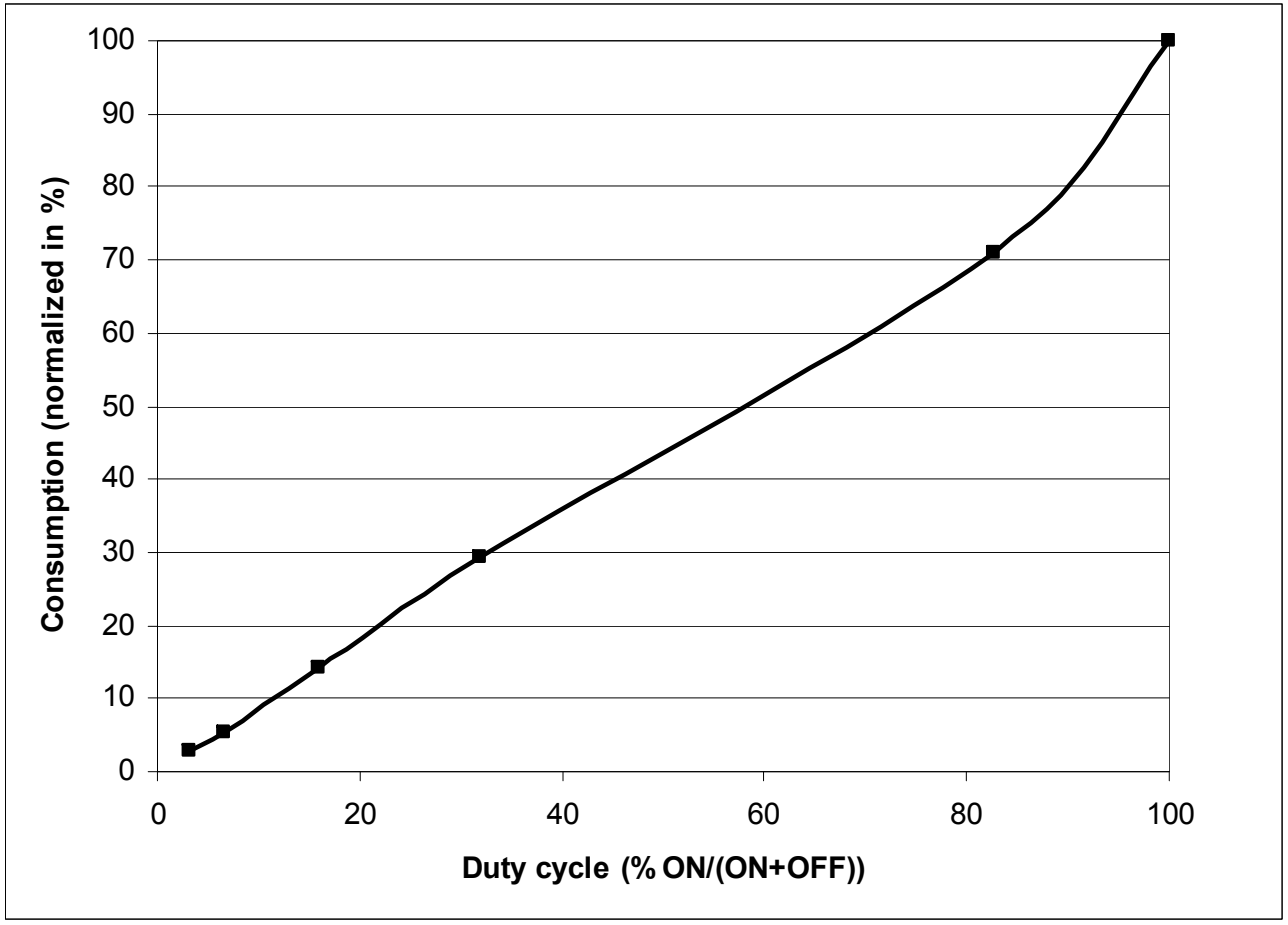
# Noise measurement

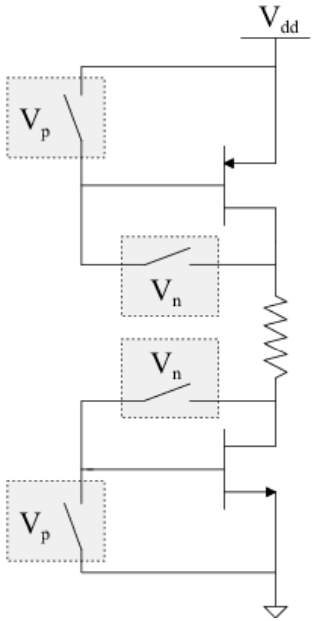
## Code fluctuation @ 1V




## Standard deviation = 0.84 LSB (420µV)

# Power pulsing, measurement




- Switch off the master current sources
- Recovery time of the biasing of the ADC is 1µs after 7µs latency

# Summary

- A 12-bit cyclic ADC prototype, dedicated to ECAL of ILC, has been fabricated in 0.35µm CMOS and is under test
- First measured performance are in accordance with simulations
  - **Time conversion: 7µs**
  - **Consumption: 4 mW/3.5V, integrated consumption: 0.7µW**
  - **DNL<+/-1 LSB**
  - **INL<+/-1.2 LSB**
  - **Noise standard deviation: 0.84LSB**
- Next measurements have to evaluate:
  - Dependence of performance with clock frequency
  - Dynamic performance, SNR, SFDR…
- Improvements of the yield (60%), CMFB