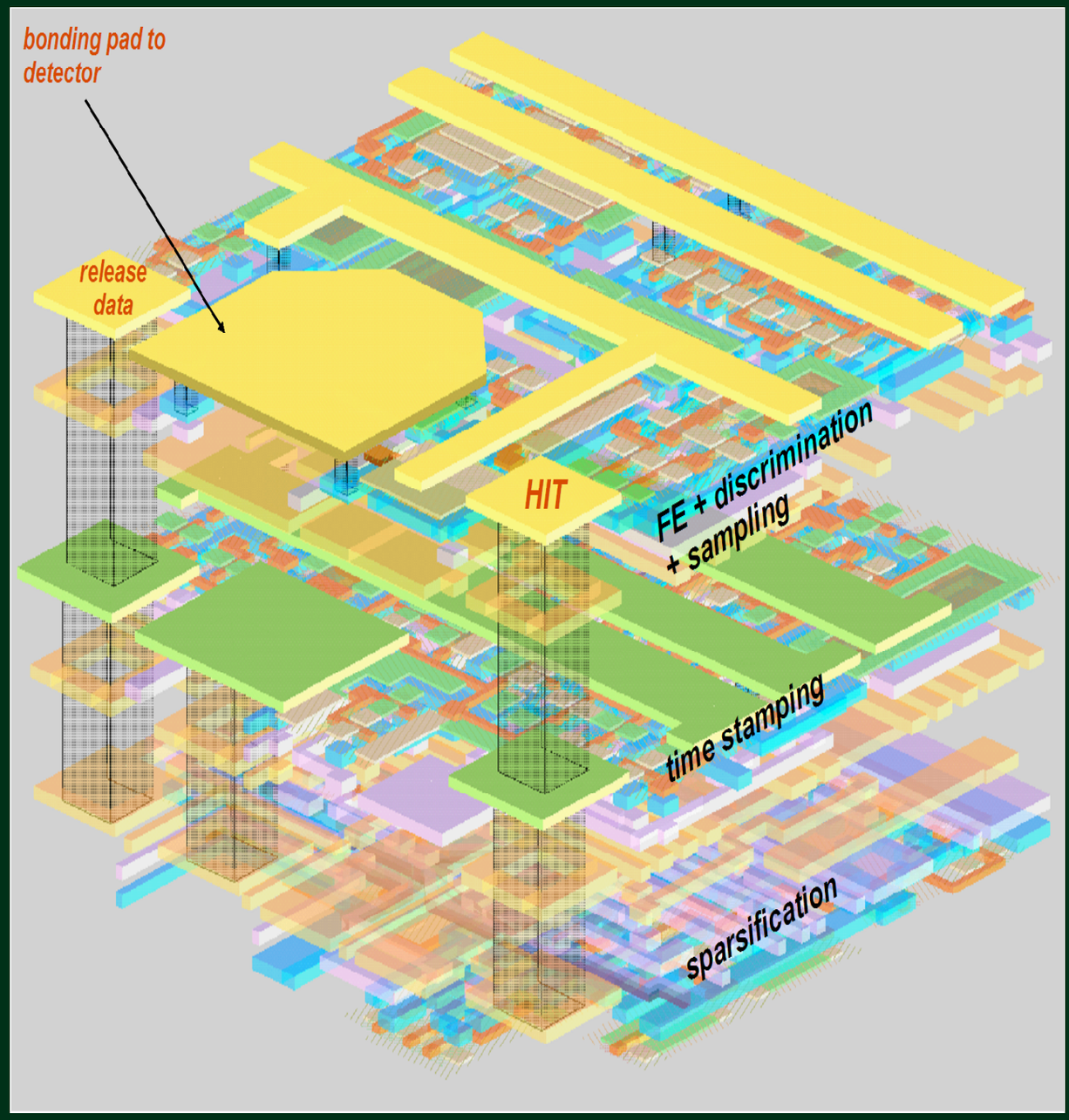
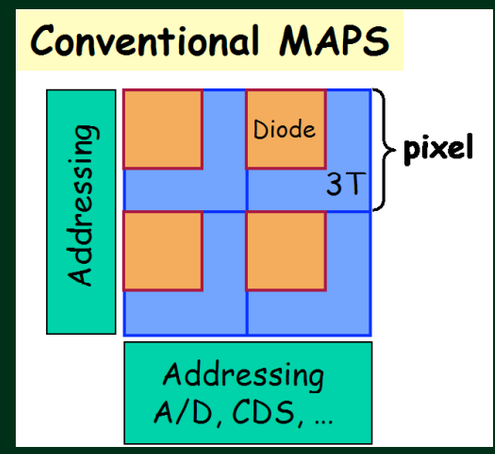
Development of Vertically Integrated Circuits for ILC Vertex Detectors

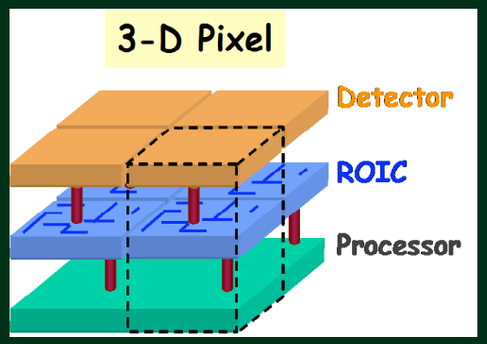
- This talk will be an overview of the work done over the past two years to investigate the application of vertically integrated electronics to HEP
- Contents
  - Overview of 3D
  - The VIP chip for ILC Vertex
  - VIPII
  - Sensor integration
  - Conclusions
- **Other talks today**
  - **Direct oxide bonding - Zhenyu Ye**
  - **SOI R&D - Marcel Trimpl**

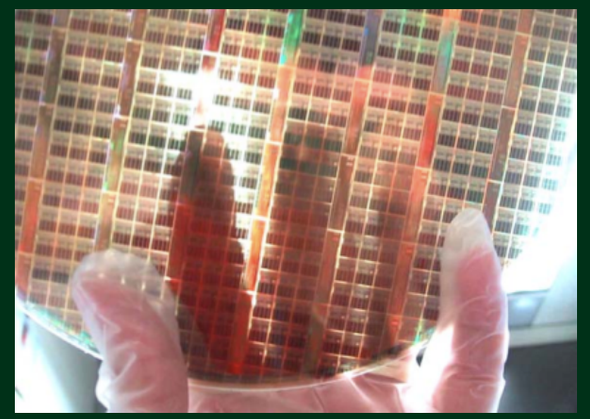


3D Technology

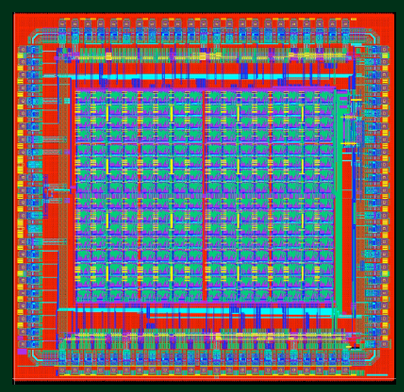
- 3DIC - vertical integration of electronics
- 3D IC technology is likely to become an important component of future electronics
  - Reduces length and R,C of interconnects
  - Allows for heterogeneous device integration
  - Improves processing density/pixel
  - Increases circuit density without billions of investment in new fab facilities
  - Multicore processors are at the memory access limit - more bandwith is crucial to continue Moore's Law performance
- This is a opportunity for HEP to build detectors with significantly improved performance







IBM SOI on Glass Wafer

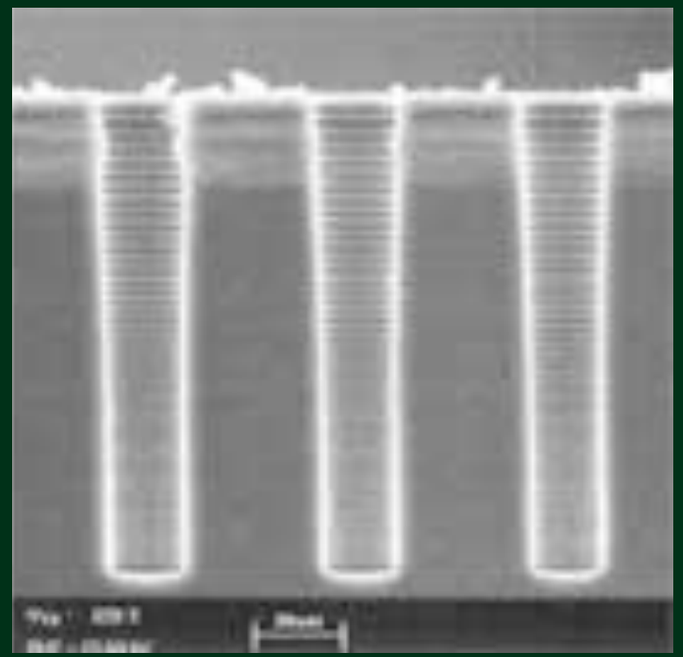


Tezzaron 3D FPGA

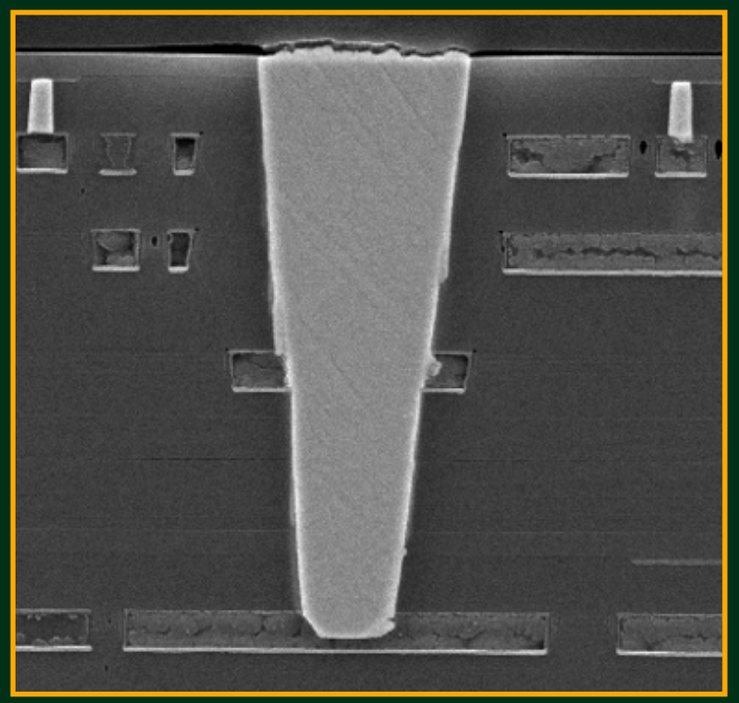
3D Basics

Technology based on:

1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Copper/copper
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation (SOI)
4) High precision alignment



SEM of 3 vias using Bosch process

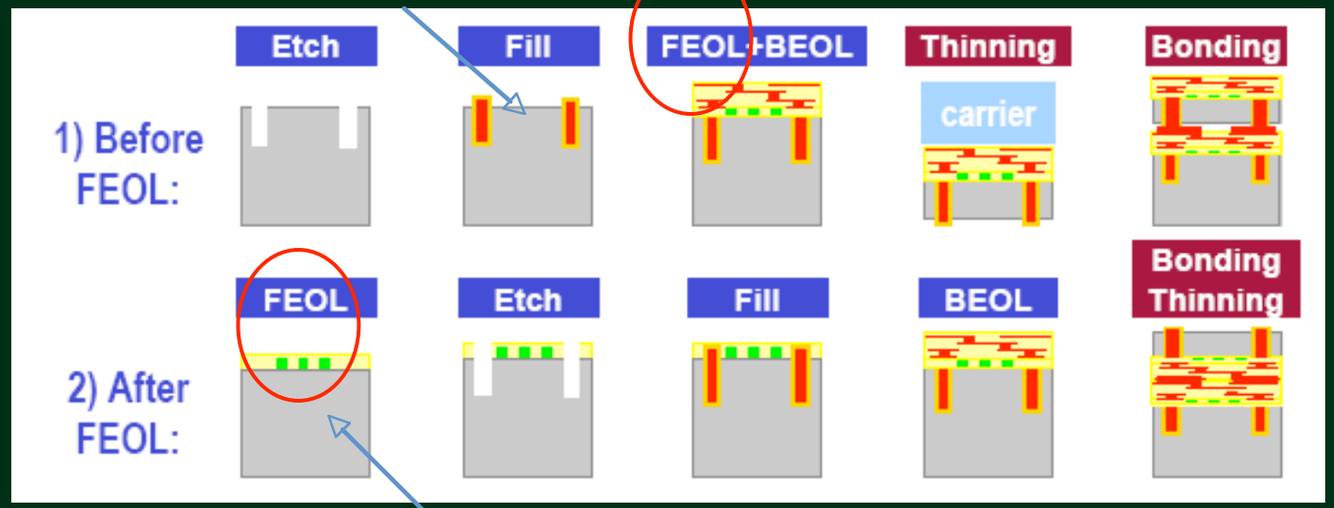


Via using oxide etch process (Lincoln Labs)

Via Formation Strategies

Via First

Form vias before transistors

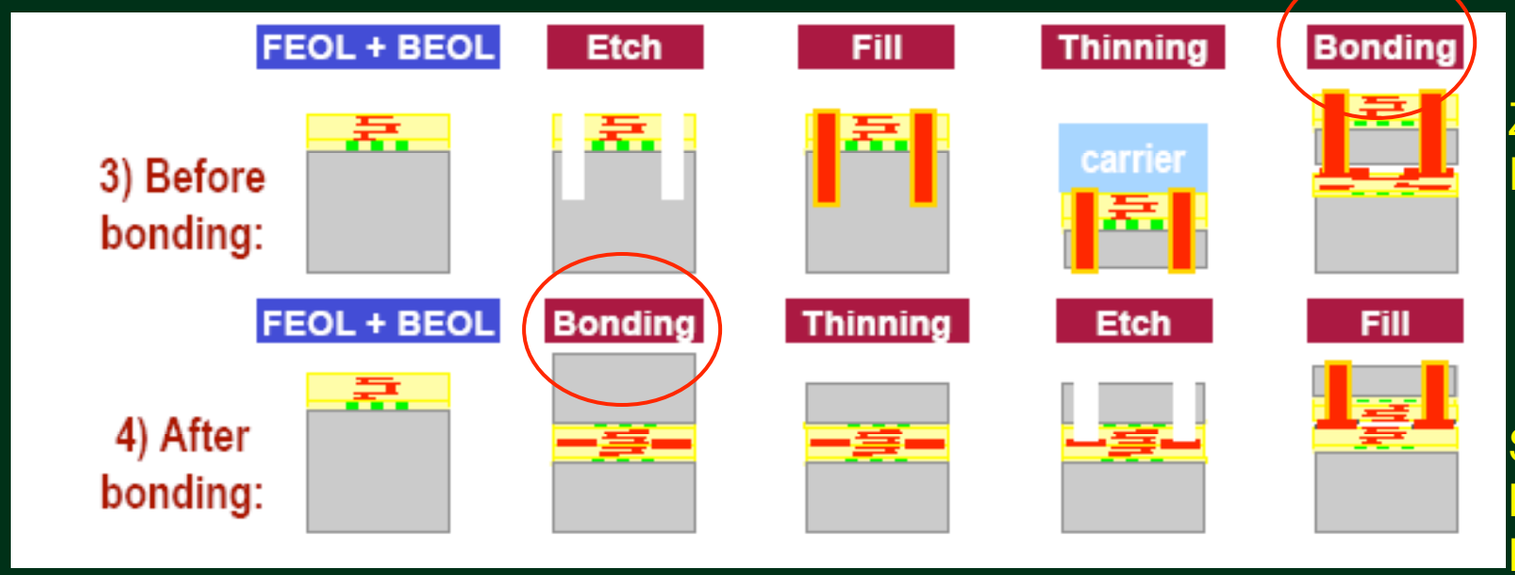


Form transistors before vias

IBM, NEC, Elpida, OKI, Tohoku, DALSA….

Tezzaron, Ziptronix Chartered, TSMC, RPI, IMEC……..

Via Last



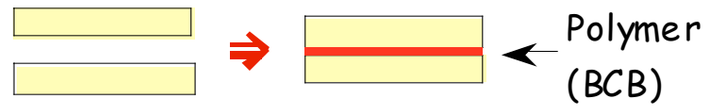
Zycube, IZM, Infineon, ASET…

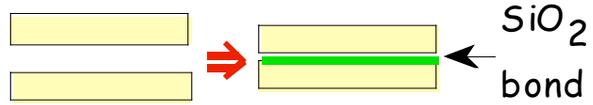
Samsung, IBM, MIT LL, RTI, RPI….

Bonding Technologies

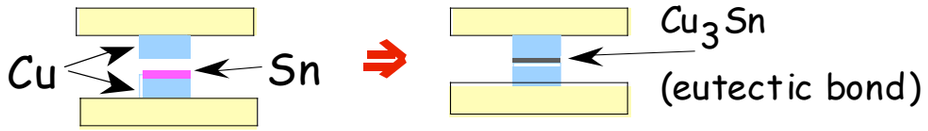
1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation
4) High precision alignment

Electrical and Mechanical Bonds

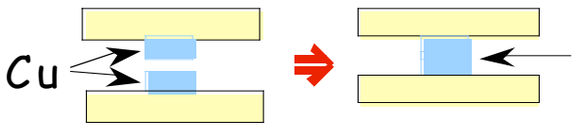
a) Adhesive bond 

b) Oxide bond (SiO2 to SiO2) 

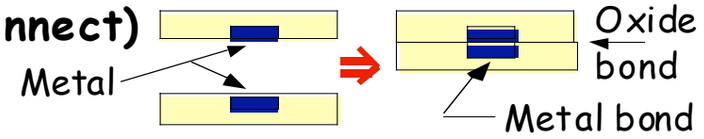
(MIT LL)

c) CuSn Eutectic 

(RTI)

d) Cu thermocompression 

(Tezzaron)

e) DBI (Direct Bond Interconnect) 

(Ziptronix)

For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

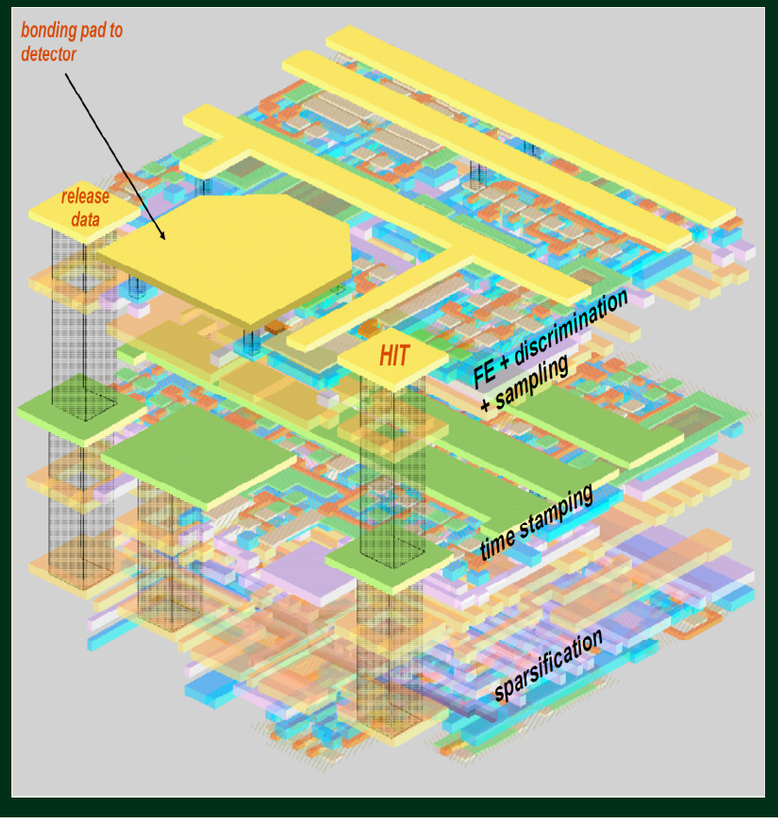
VIP Chip

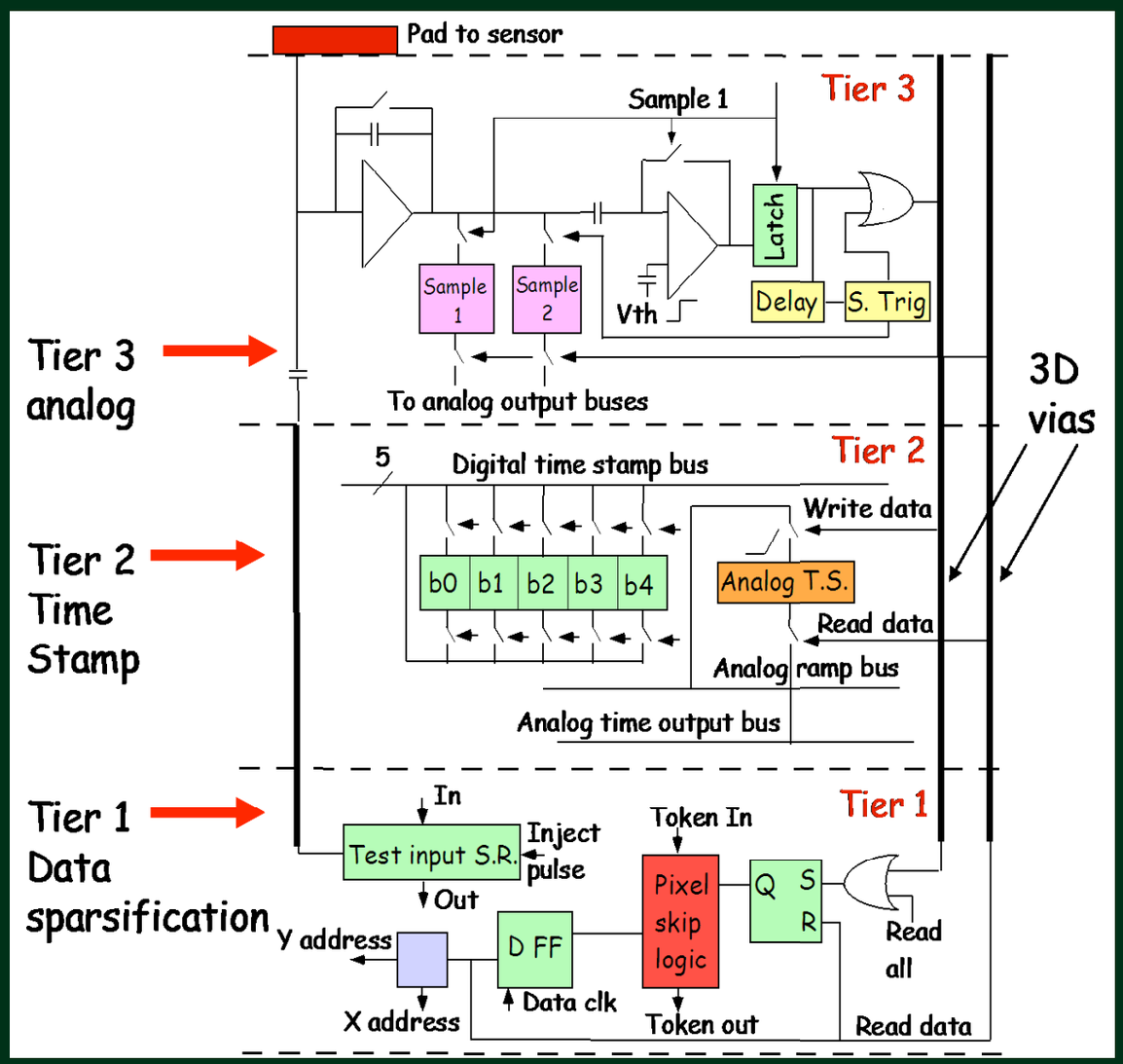
Goal - demonstrate ability to implement a complex 3D pixel design with all required ILC properties in a 20 micron square pixel

Previous technologies limited to simple circuitry or larger pixels - 3D density allows analog pulse height, sparse readout, high resolution time stamp in a 20 micron pitch pixel.

- **Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.**
- **64 x 64 pixel demonstrator version of 1k x 1K array.**
- **Submitted to 3 tier DARPA-sponsored multi project run. Sensor to be added later.**

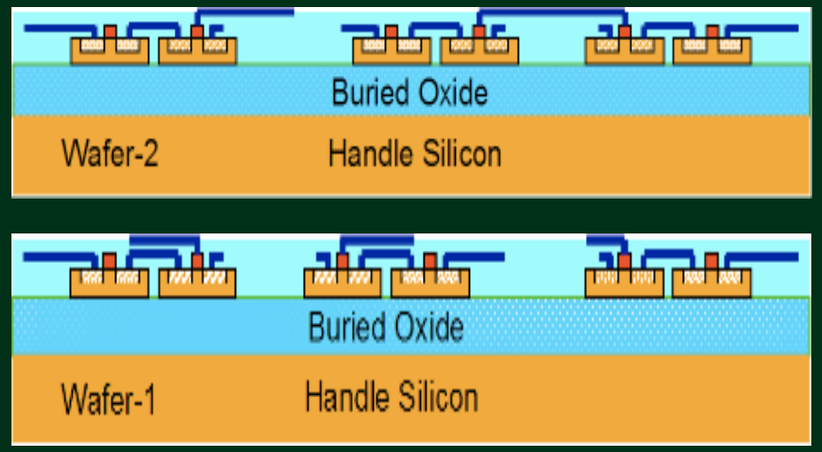
- **Low power front end 1875 μW/mm2 x Duty Factor**



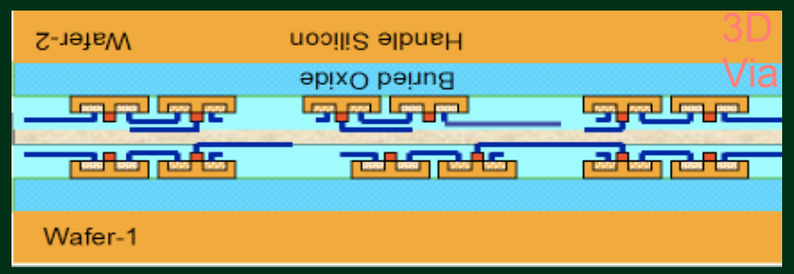


MIT-LL 3D Process

1) Fabricate individual tiers

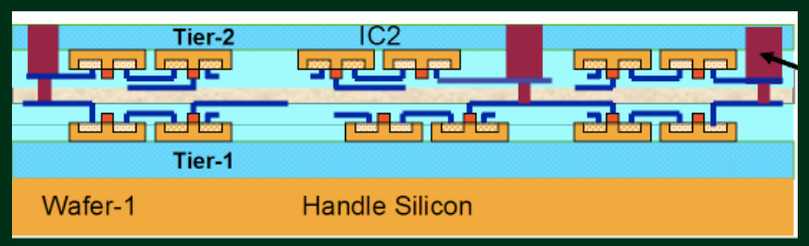


2) Invert, align, and bond wafer 2 to wafer 1

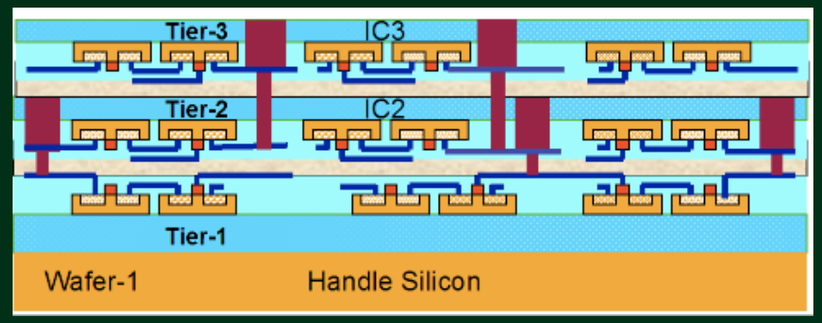


Oxide bond

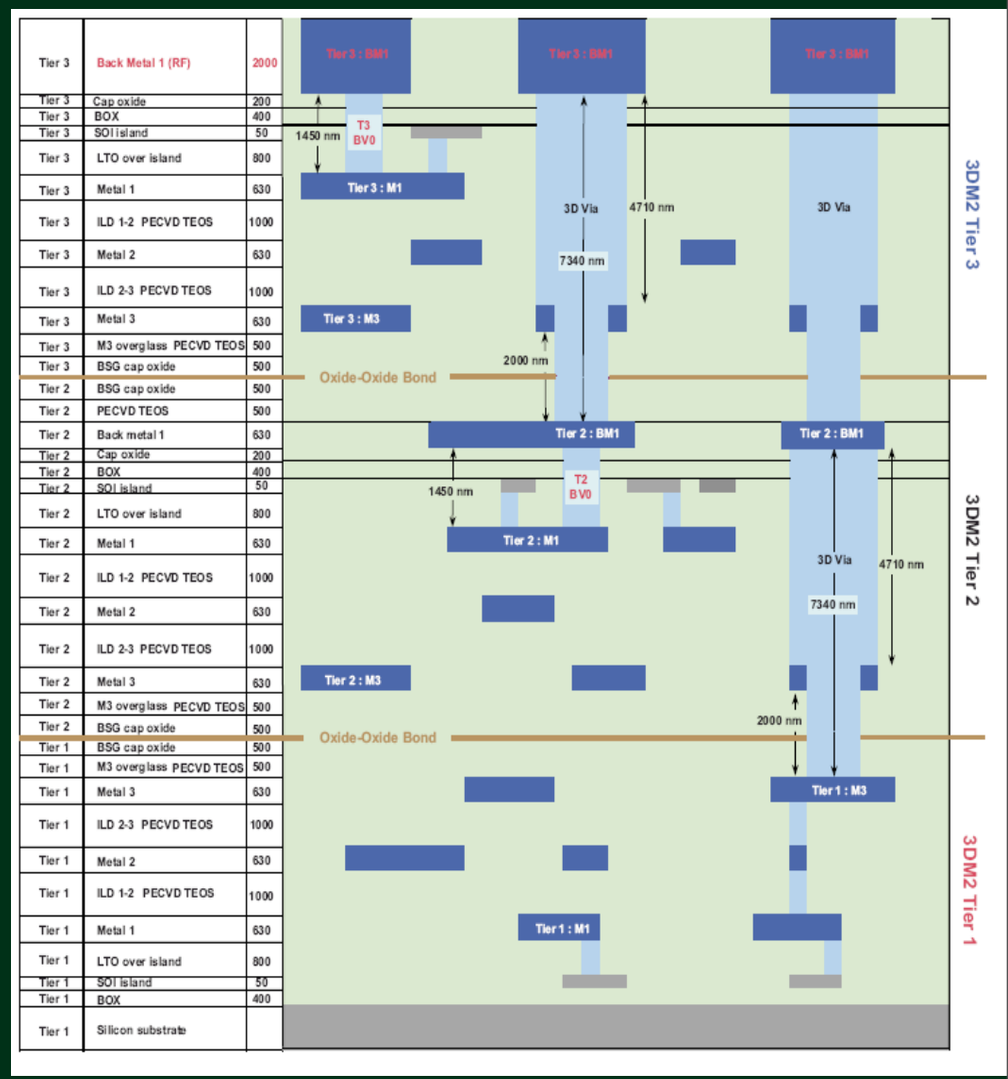
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3

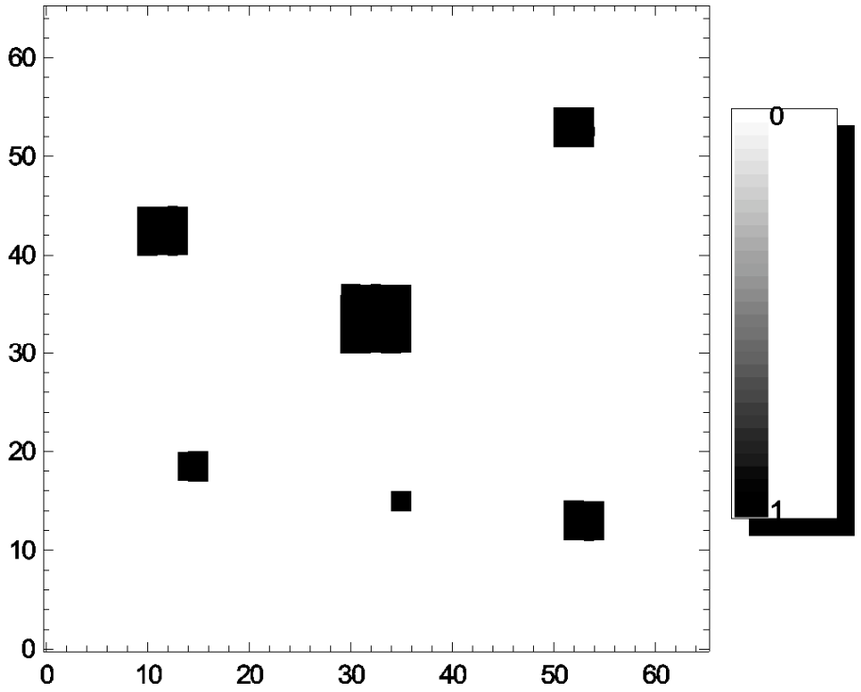


Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

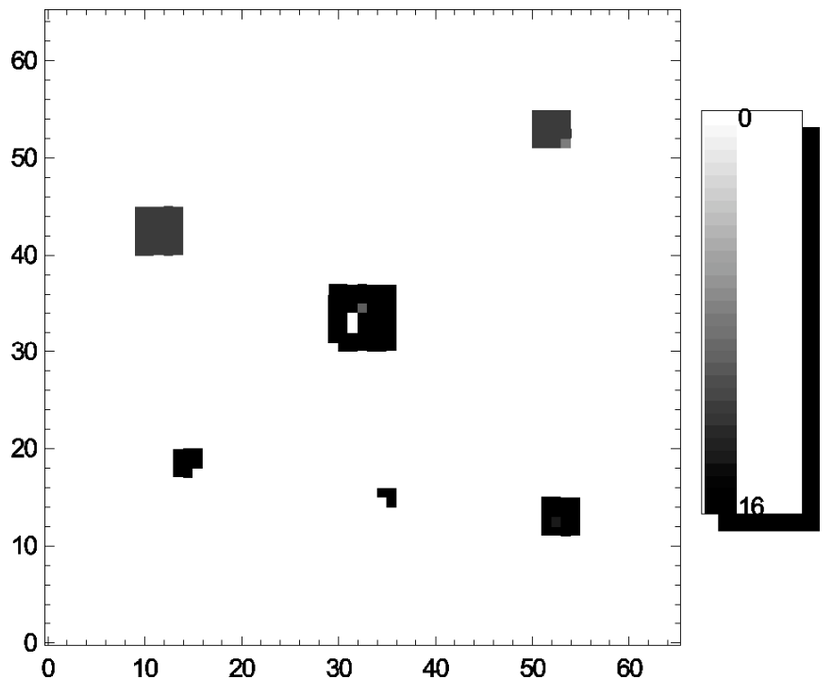


VIP Test results

- Basic functionality of the chip has been demonstrated
  - Propagation of readout token
  - Threshold scan
  - Input test charge scan
  - Digital and analog time stamping
  - Full sparsified data readout
- Fixed pattern and temporal noise measurements
- No problems could be found associated with the 3D vias between tiers.
- Chip performance compromised by:
  - Poor transistor models
  - Large leakage currents in transistors and diodes
  - Poor current mirror matching
  - Vdd sensitivity
  - low yield



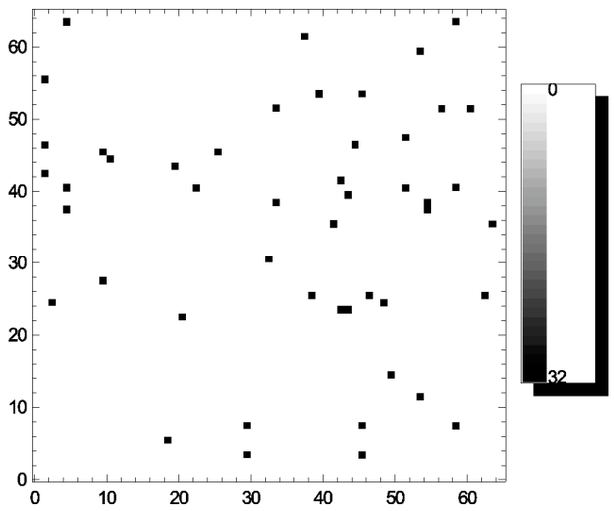
Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal



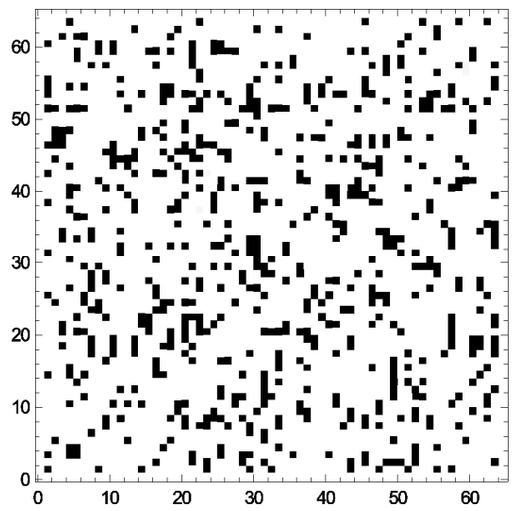
Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

Injection of Test Charge into 119 Integrator Inputs of 64 x 64 Array

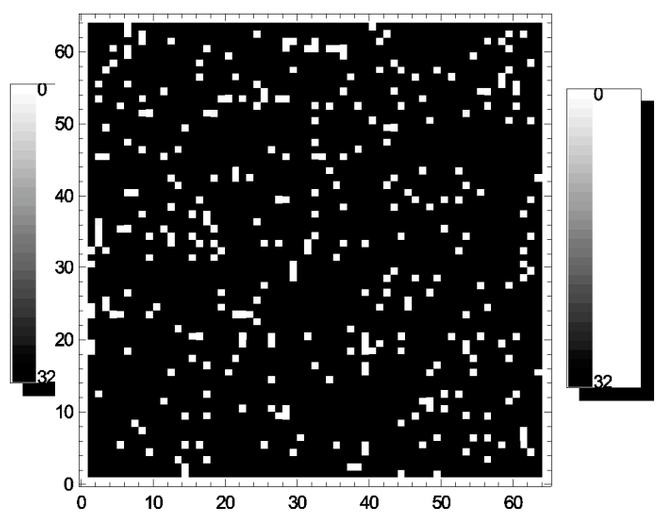
Data readout out using data sparsification scheme.



Maximum threshold



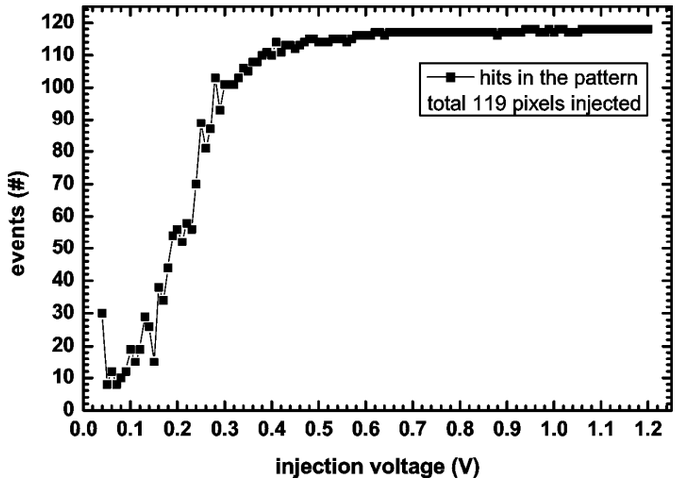
Intermediate Threshold



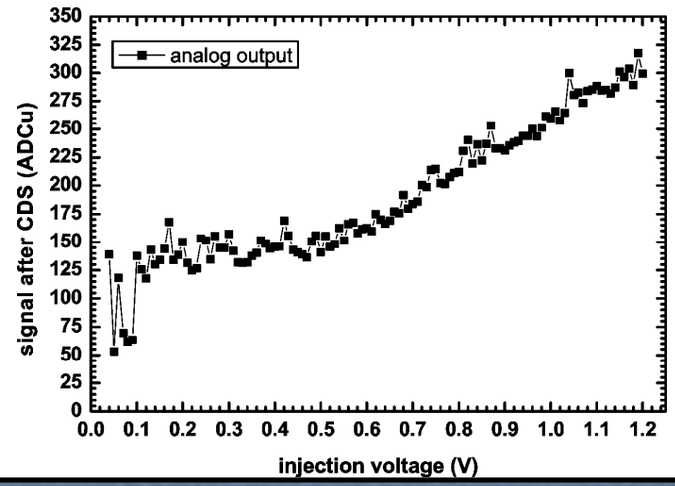
Minimum Threshold

Hit Pixels in Full Array as a Function of Threshold

As level of test charge through test capacitor (located between tier 2 and 3) is increased, more pixels exceed the threshold up to the maximum of 119 pixels

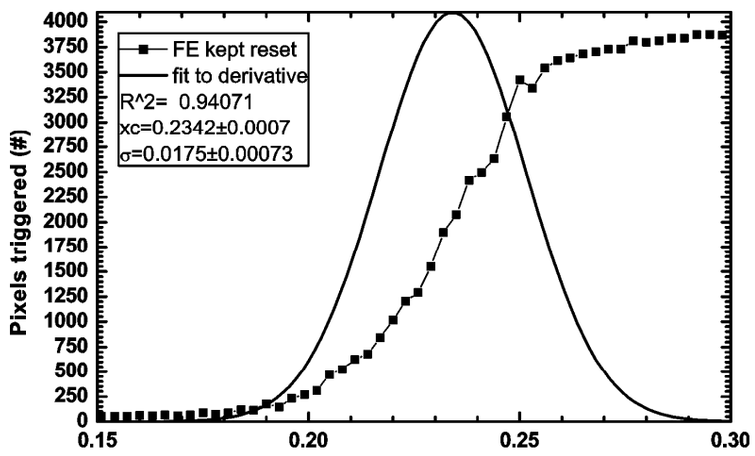


Mean analog signal level of pixels exceeding the threshold voltage. The red line is an indication of the linearity of the analog output signal (100 ADC units= 35 mv).
charge injection capacitor = 0.2 fF



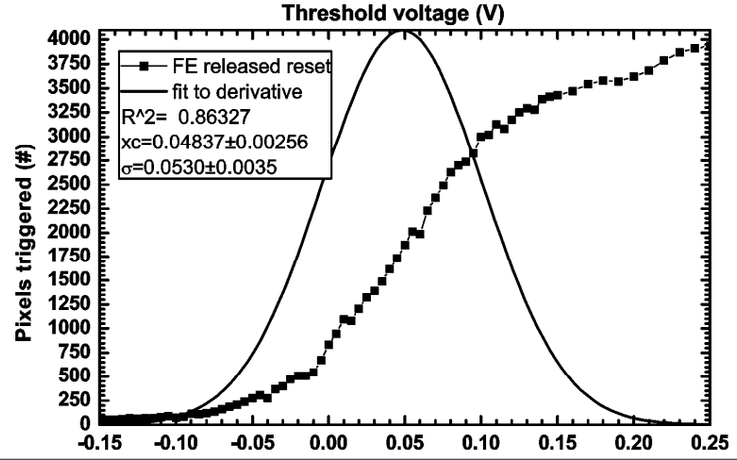
Analog response for 119 pixels in preselected pattern using sparsified readout.

A) With integrator held reset, threshold dispersion has a sigma of 1.6 mv or about 25e-.



Pixel to Pixel Threshold Dispersion

B) With integrator reset and released, discriminator reset (autozeroed), threshold dispersion has a sigma of 4.9 mv or about 75 e-.



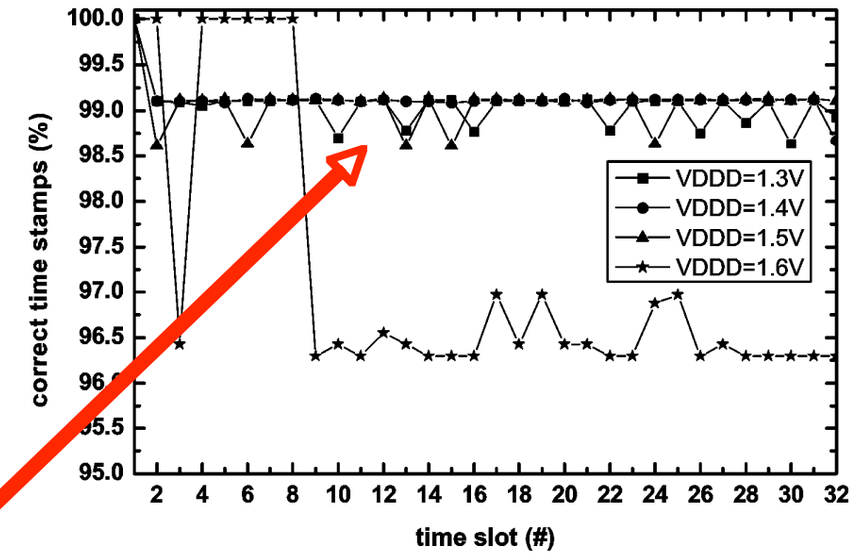
Threshold set at increasing levels and all pixels over threshold read out using data sparsification scheme.

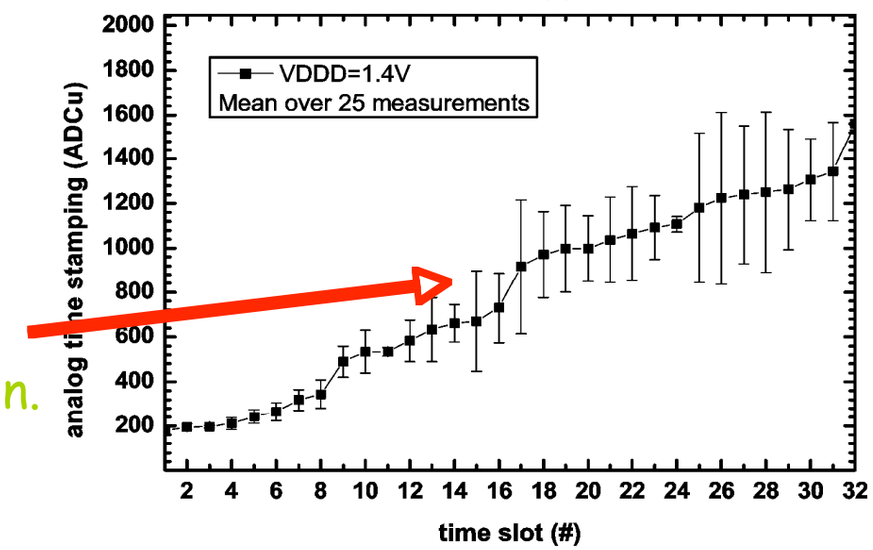
Time Stamping Performance

Time stamping studied for 119 pixels in preselected pattern using sparsified readout. Digital time stamping uses inverted Gray code. External ADC used for analog time stamp

Charge is injected at a specific time, and time is compared to the digital time stamp. The readout shows a dependence on VDDD. Data shows that 118 of 119 pixels have correct time stamp for VDDD = 1.4V.

Analog time stamping suffers from high leakage current in sample and hold circuit. Problem to be corrected in next submission.





VIP Lessons Learned

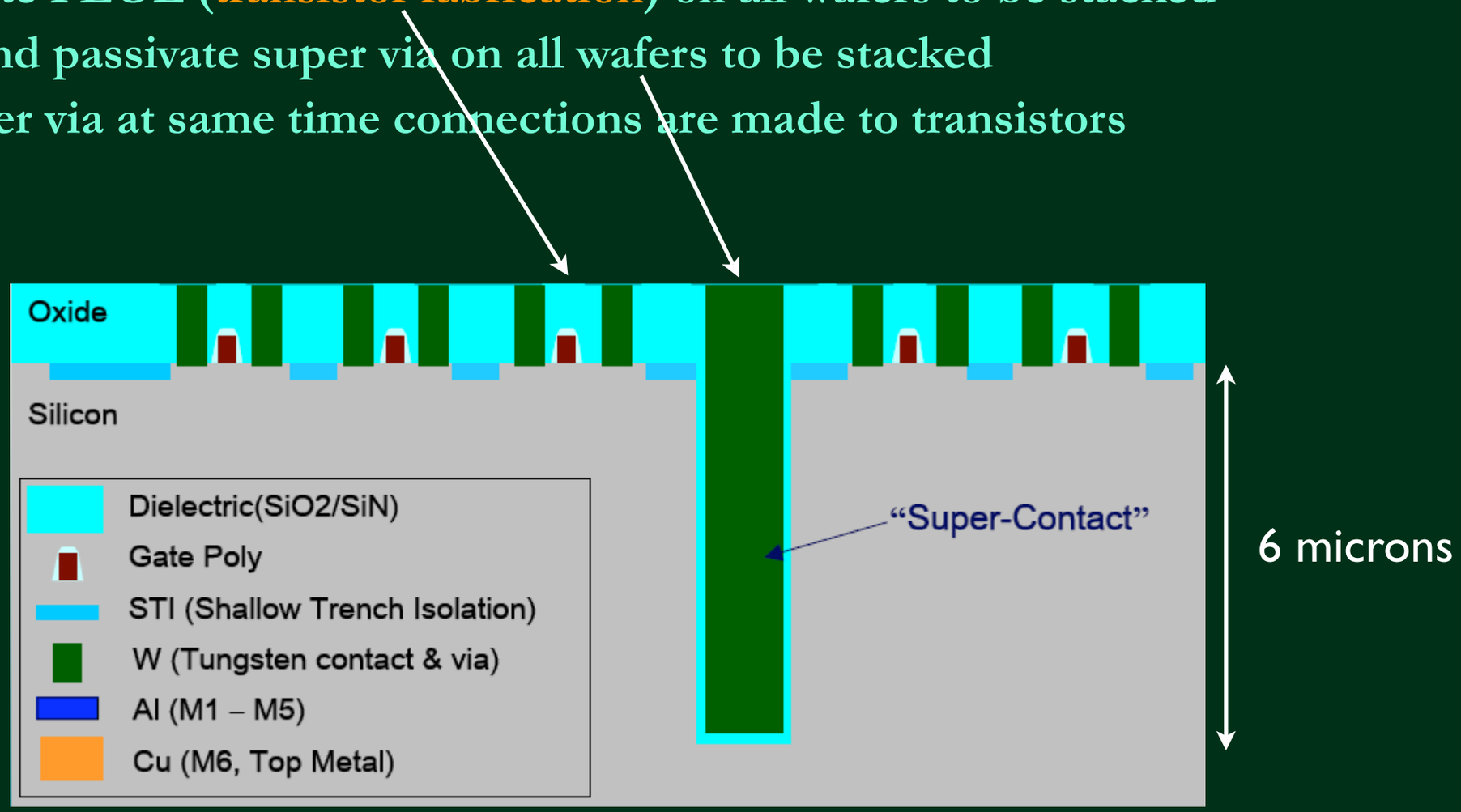
- Difficult to design complex devices in an R&D process
  - Long turn-around
  - Unreliable models
  - low yields
- SOI has particular analog design issues
  - Differential heating of “island” silicon and mobile contamination in oxide can cause mismatch of current mirrors
  - MIT-LL had high leakage in protection diodes
  - Short “hold” time in dynamic logic due to leakage

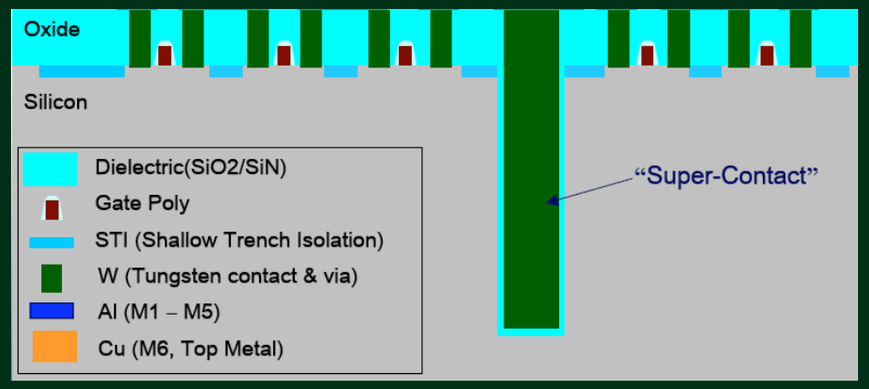
VIPII

- An improved version of the VIP was submitted to MIT LL in October. The new chip is called VIP2
  - Different power and grounding layout
  - Larger transistor sizes (0.18 → 0.5 micron)
  - Larger pixels (30 x 30 microns)
  - Redundant vias and larger traces in critical paths
  - On chip ADC
  - More bits in digital time stamp (7 bits)
  - Redesign of current mirrors
  - Removal of dynamic logic due to leakage current problems
- Very useful interaction with MIT-LL on SOI should improve overall quality of the design

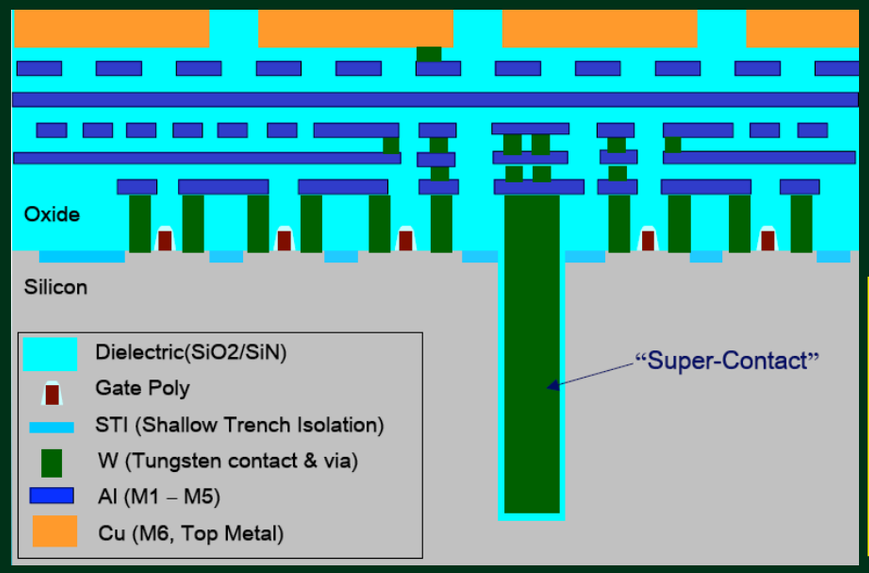
Tezzaron Process

- **Tezzaron (Naperville Ill) has developed a 3D technology implemented in the high volume 0.13 micron Chartered (singapore) process**
  - **Through silicon vias are fabricated as a part of the foundry process. "Via first" approach.**
  - **Complete FEOL (transistor fabrication) on all wafers to be stacked**
  - **Form and passivate super via on all wafers to be stacked**
  - **Fill super via at same time connections are made to transistors**

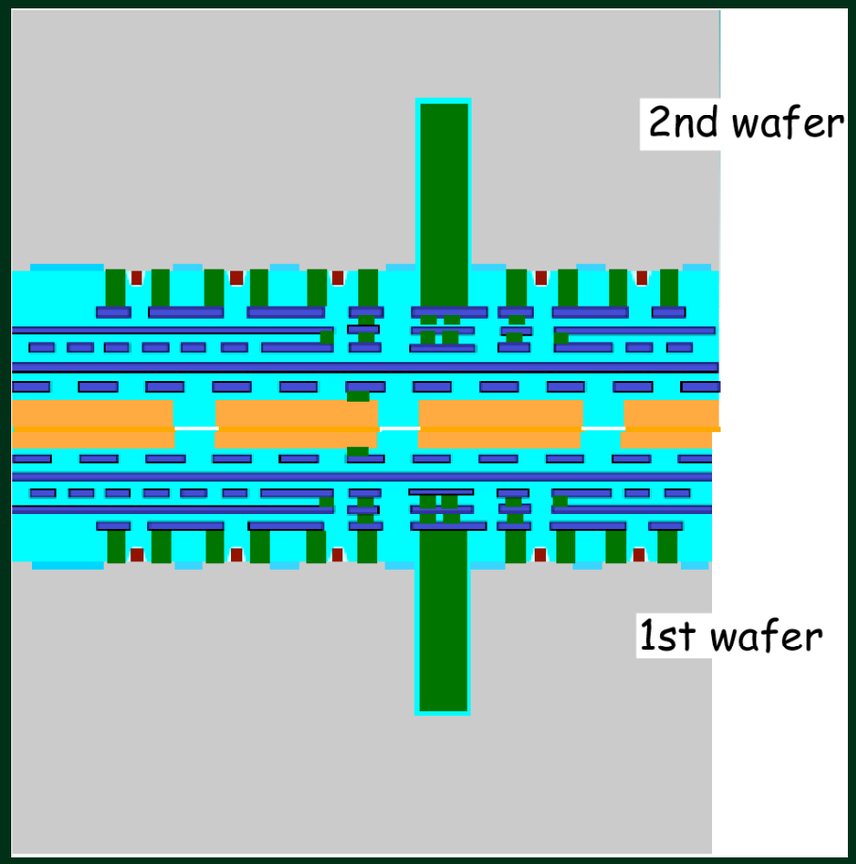




Transistor fabrication
Form super via
Fill super via



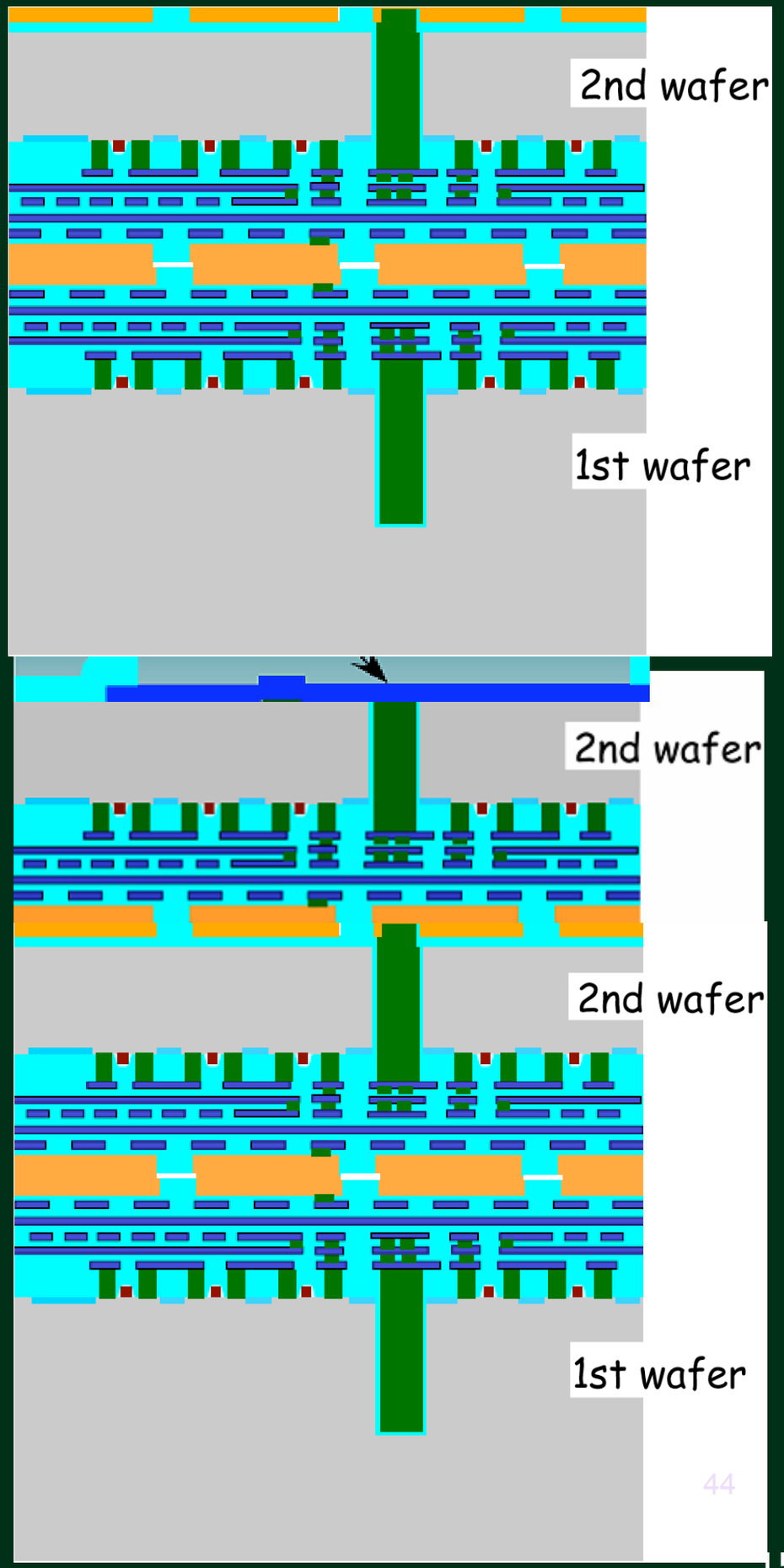
Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal



Bond second wafer to first wafer using Cu-Cu thermo-compression bond

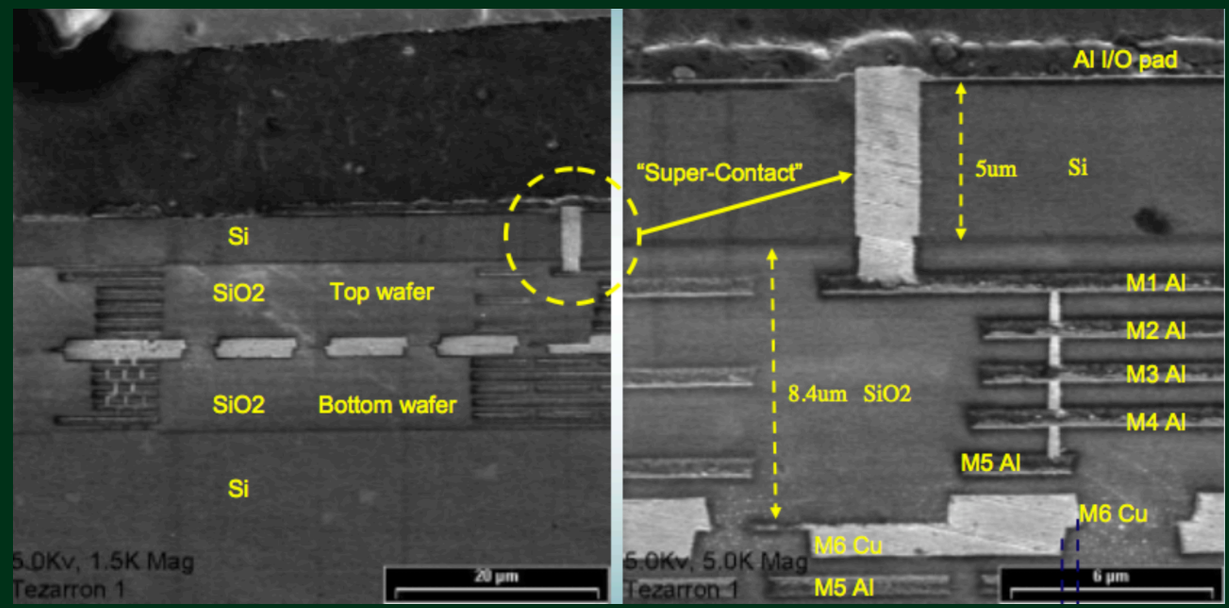
Stack 3rd wafer
Thin 3rd wafer
Add final passivation and metal for bond pads

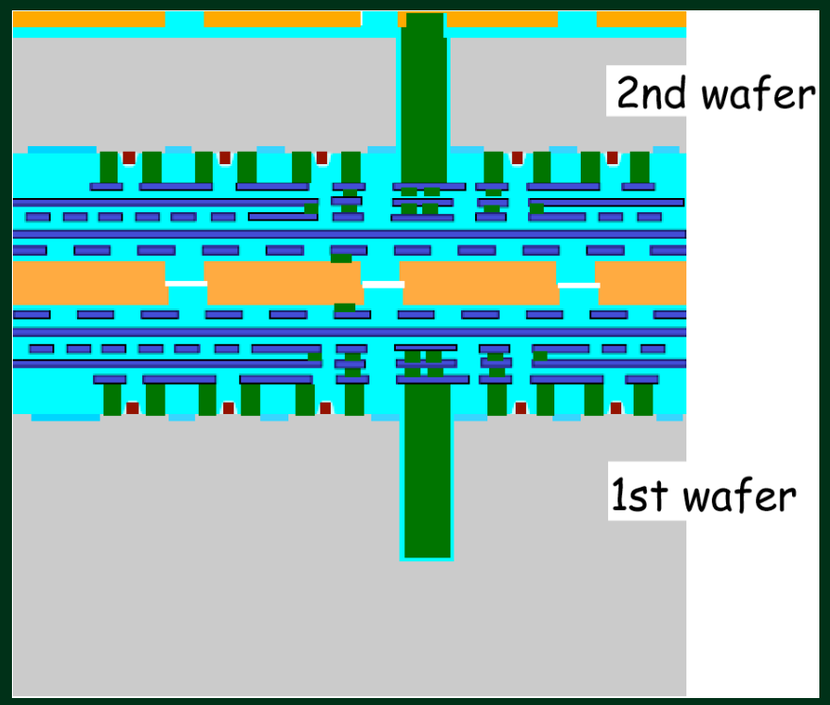
Thin the second wafer to about 12 um to expose super via.
Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd



Tezzaron Multiproject run, VIPIIb

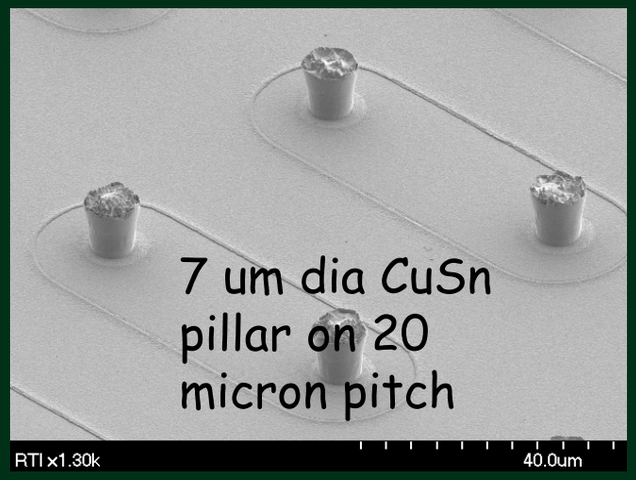
- **Fermilab is organizing a multiproject run which will include a two tier version of the VIP**
- **Process can include MAPS option**
- **Submission this spring**
- **Labs with NDAs:**
  - **Fermilab, Batavia**
  - **University at Bergamo (3D MAPs)**
  - **University at Pavia**
  - **University at Perugia**
  - **INFN Bologna**
  - **INFN at Pisa**
  - **INFN at Rome**
  - **CPPM, Marseilles**
  - **IPHC, Strasbourg**
  - **IRFU Saclay**
  - **LAL, Orsay**
  - **LPNHE, Paris**
  - **CMP, Grenoble**
- **VIP2b in *standard commercial CMOS*, more dependable models, better rad hardness, faster turn-around, availability of full wafers for sensor integration, less wasted area - expect much better performance**

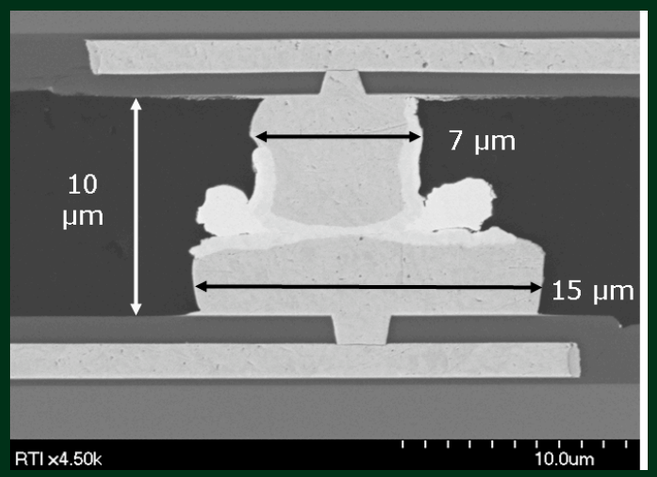




Sensor Integration

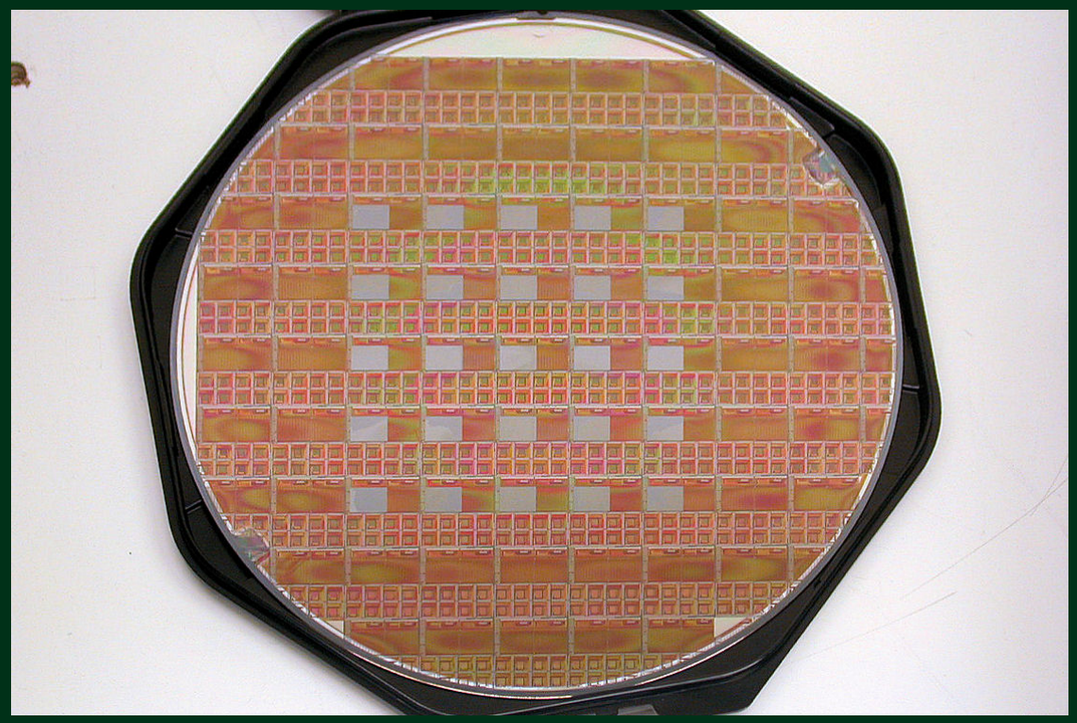
- 3D techniques can also be applied to sensor integration with readout
- We have tried two techniques: Cu-Sn and DBI oxide bonding
- DBI provides a robust bond with low capacitance and very fine pitch - results of first tests in Zhenyu Ye talk





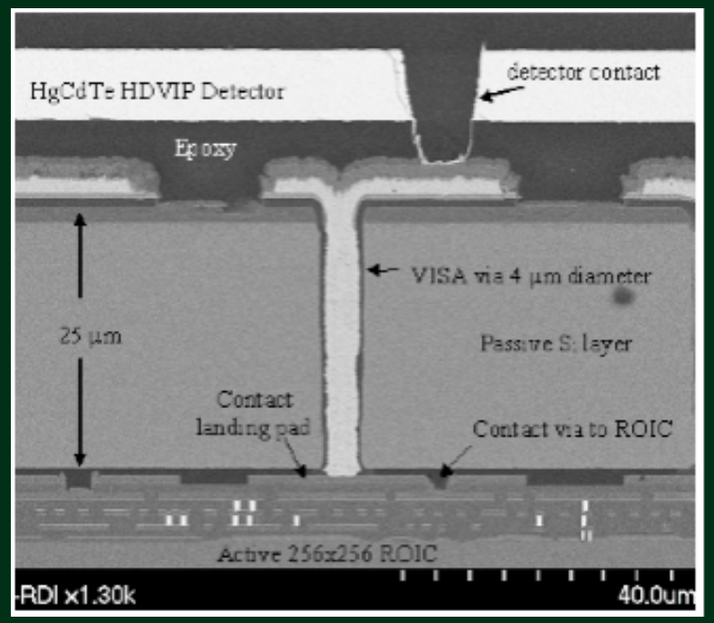
CuSn bond cross section

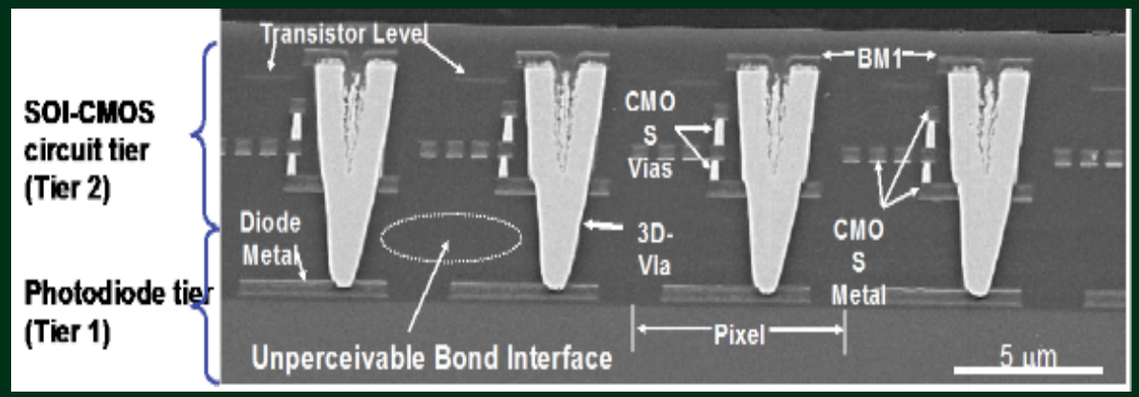
Fermilab sponsored study of sparse Cu-Sn bonding by RTI



MIT-LL BTeV sensors bonded to FPIX2 wafer, tinned to 100 microns after bonding (would be better to bond ROIC to sensor)

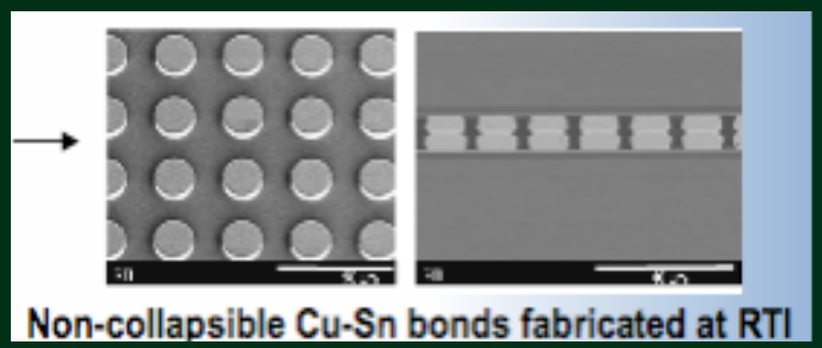
Examples of sensor Integration

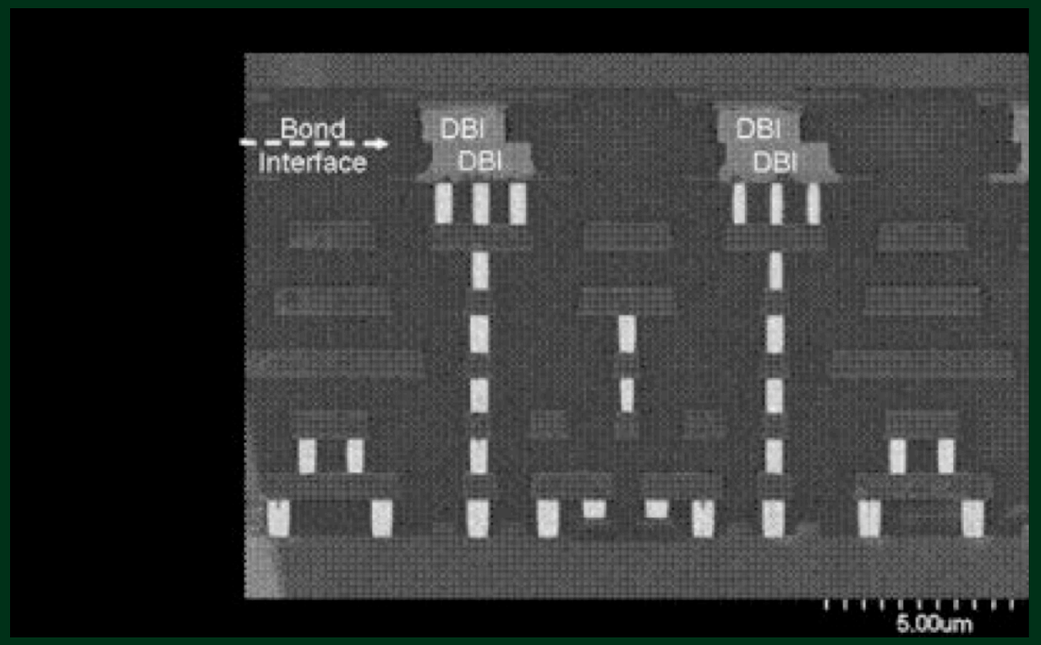




8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)

Epoxy bonded 3D connected imager (RTI/DRS) with through silicon vias

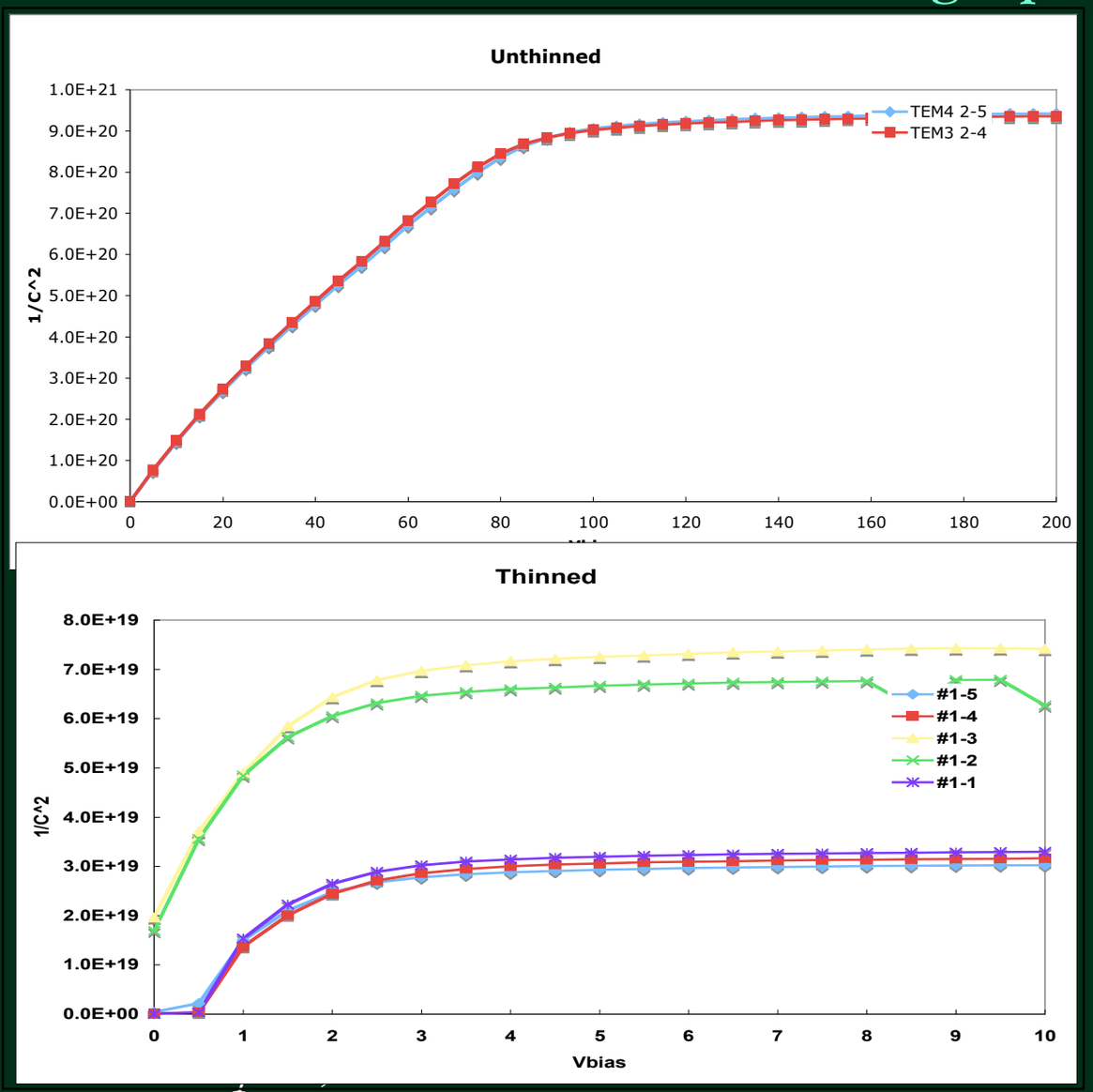




8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

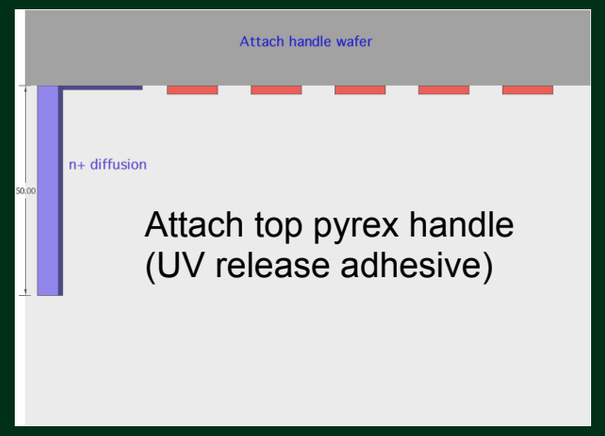
Thinning and Laser Annealing

- **We have developed a thinning/implantation/annealing process based on a 3M bonded pyrex carrier**
  - Bond to pyrex carrier
  - Thin, chemical mechanical polish
  - Implant
  - Laser anneal
  - Remove from carrier to dicing tape



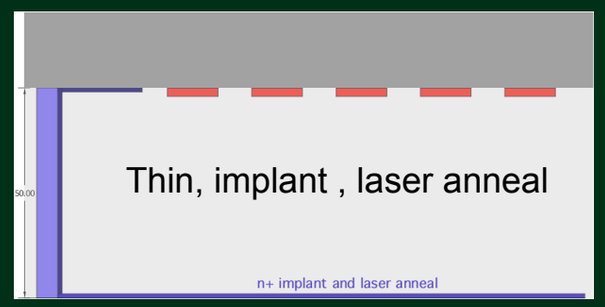
Initial 6" wafer

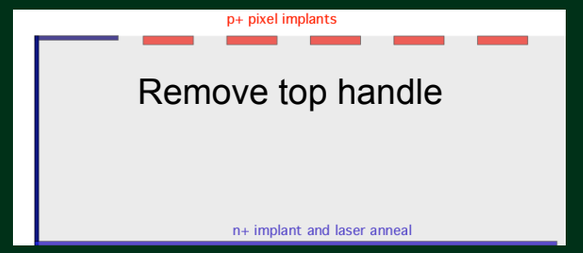
pixel implants



Pilot wafers obtained from Micron Semicondcutor

- Mounted on pyrex, thinned to 50 microns
- Chemical Mechanical Polish
- Implant back side contacy
- Laser anneal contact





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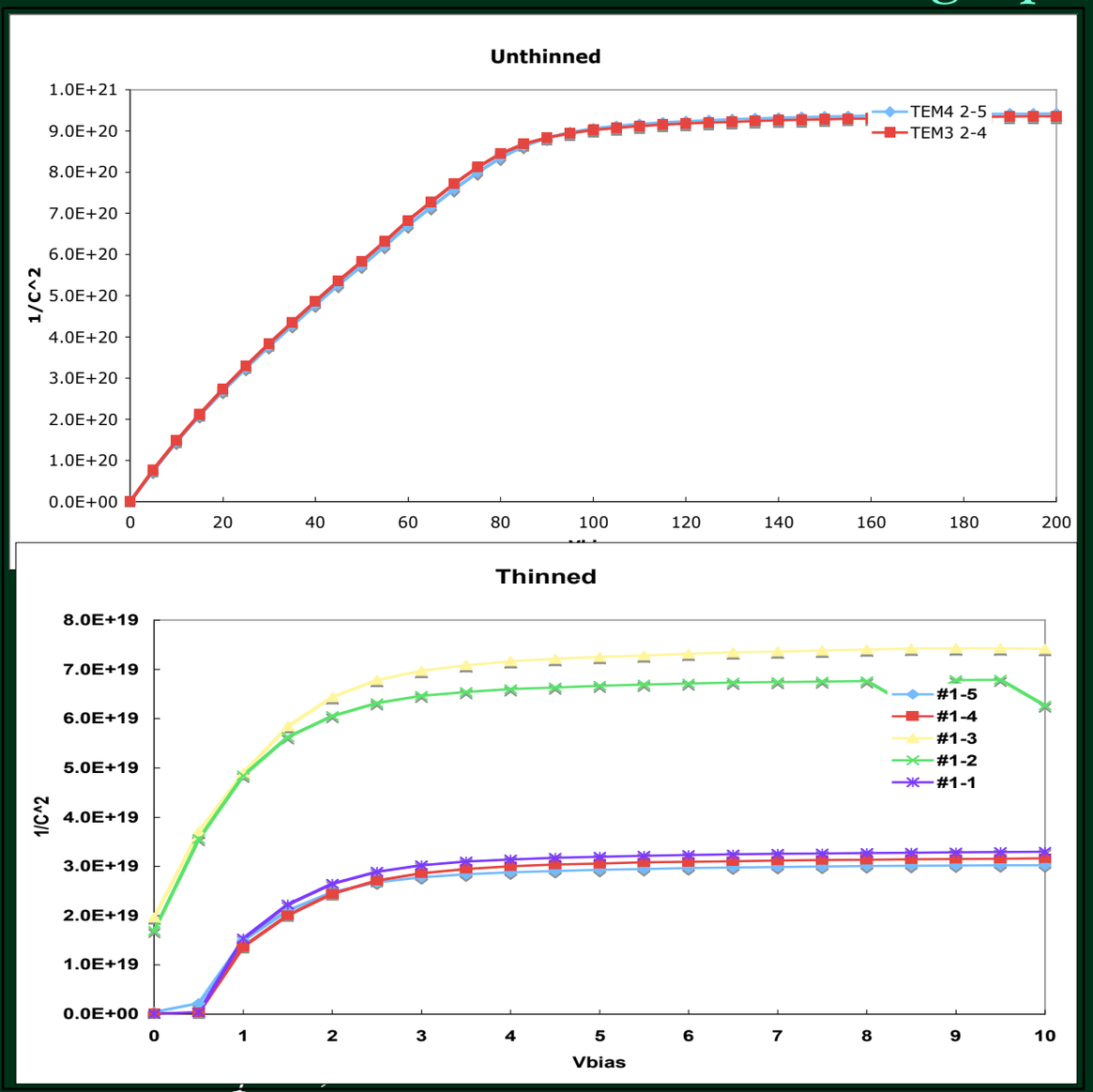

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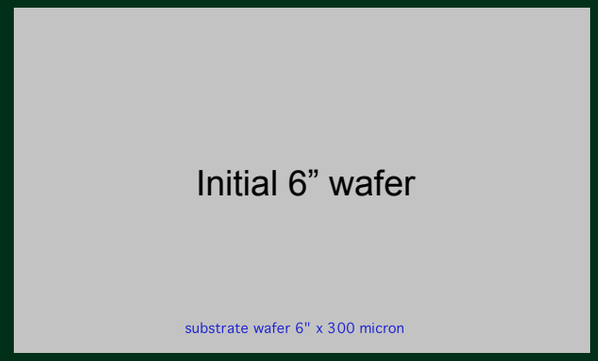
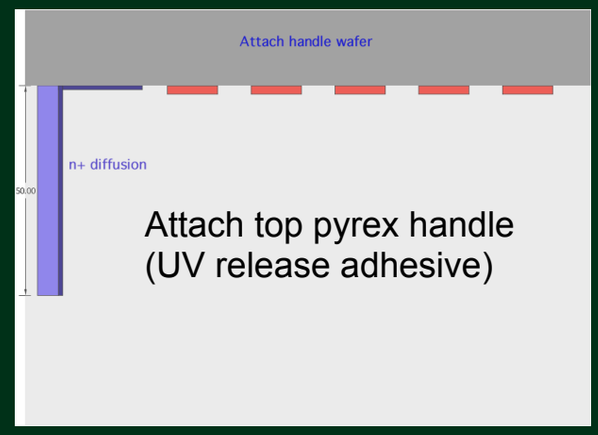
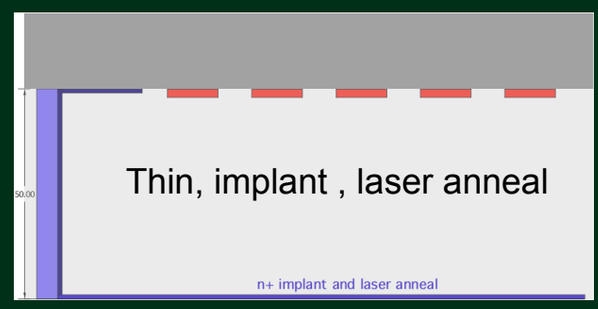
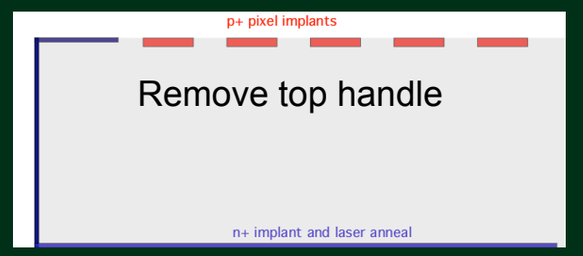


pixel implants







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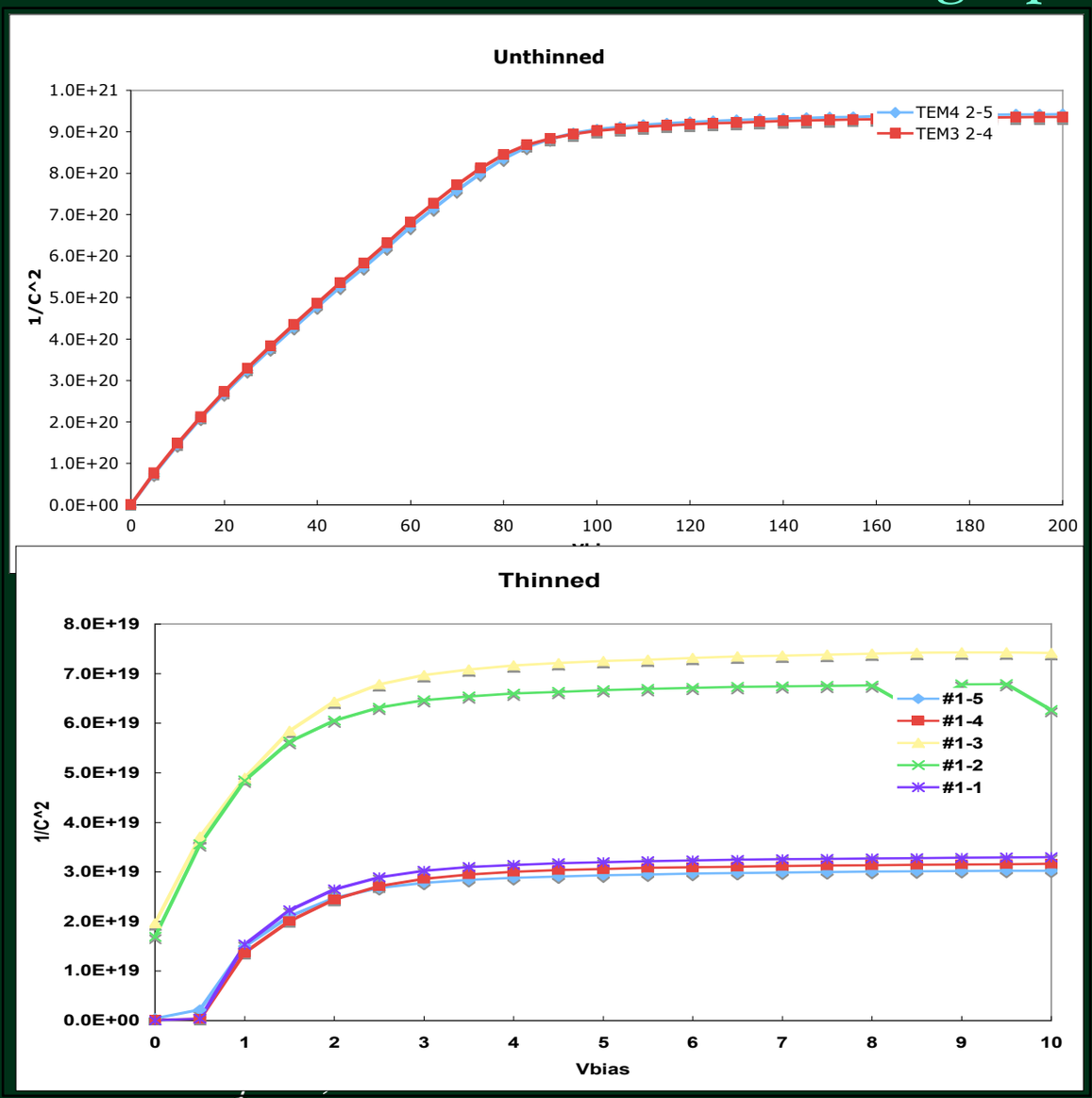

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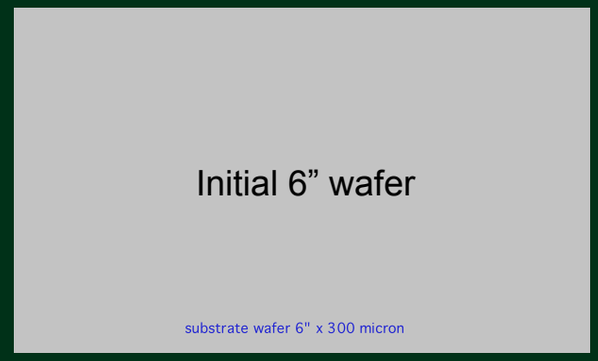
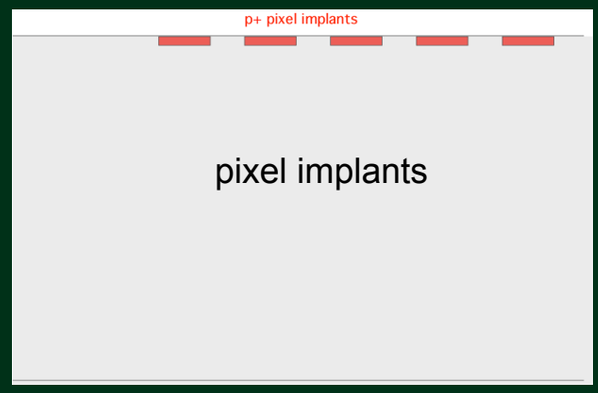
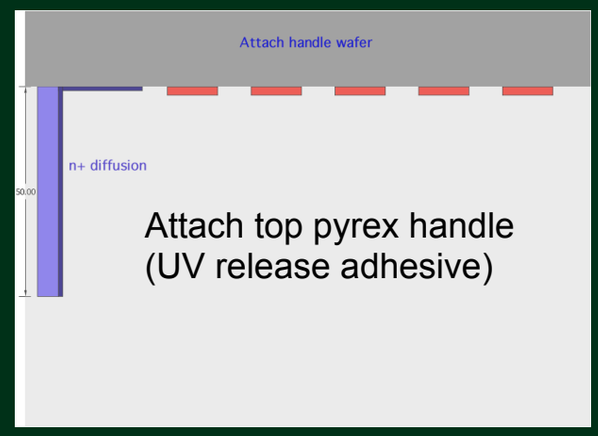
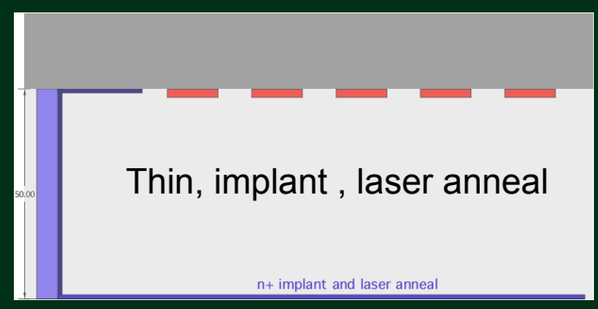
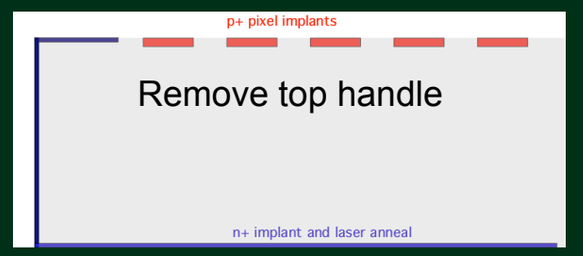




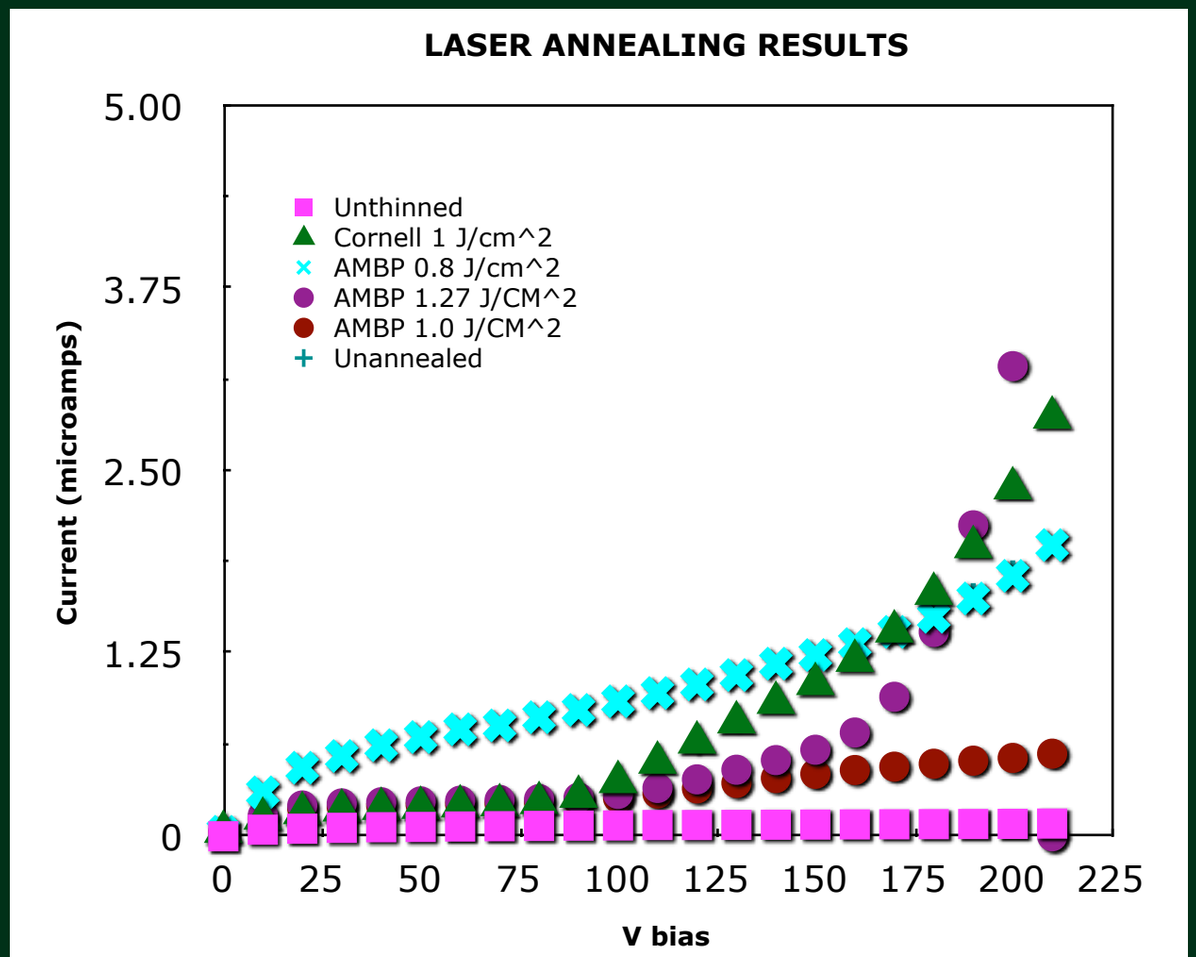


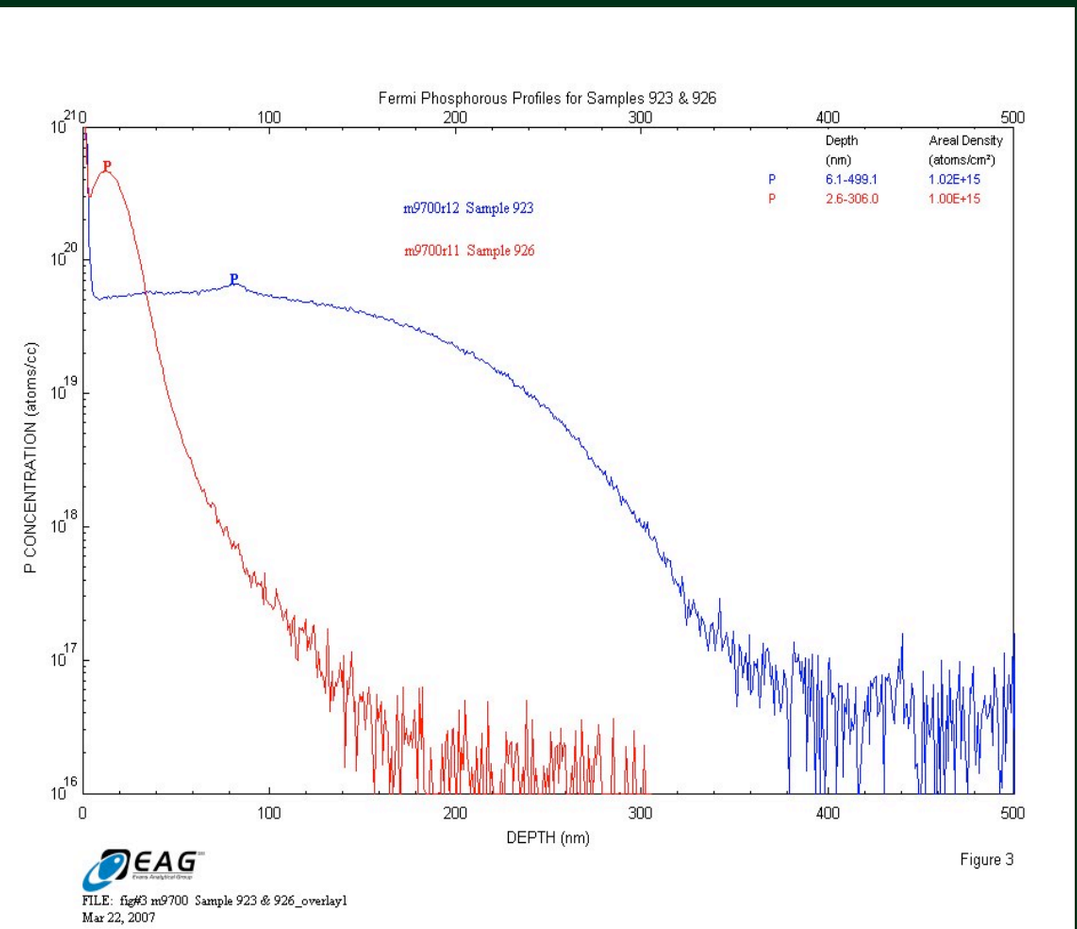




Laser Annealing

- For some technologies sensors need to be thinned after the top side circuitry has been processed - this limits the process temperature to <400 deg C. This makes backside ohmic contacts difficult to form. We are developing a laser annealing process which limits the frontside temperature
- Cornell group is continuing to optimize laser parameters.
- We will use the process to thin and anneal OKI SOI wafers.

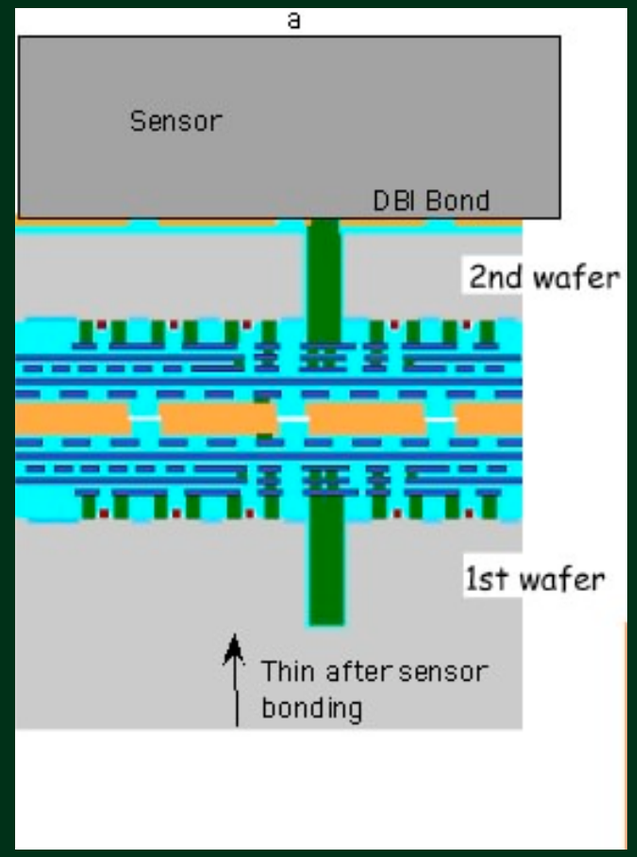


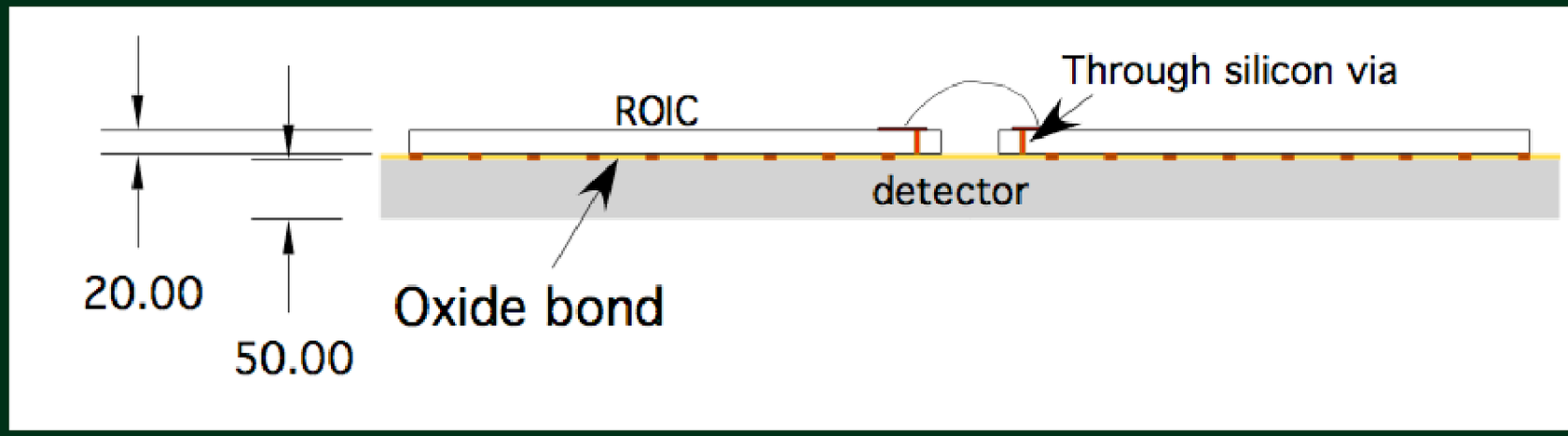


Possible ILC Vertex Design

- A bonded Tezzaron wafer provides “supercontacts” above and below the substrate. The bottom contacts can be used to provide 4-side buttabiliy
  - Produce sensor wafer thinned and bonded to silicon substrate
  - DBI bond ROIC to sensor wafer using top supervias to contact sensor pixels to ROIC
  - After bonding to sensor grind ROIC to ~ 24 microns to reveal top super vias
  - Contacts to readout are made by lithography to top pads
  - Remove bottom side handle wafer to produced thinned ladder
  - This process will be tested in upcoming Tezzaron run
- Alternative could use cu-sn bonds and polyimide bonded wafers - would allow all thinning on full wafers
- Use 6” sensor wafers - full length ladders
- no stitching

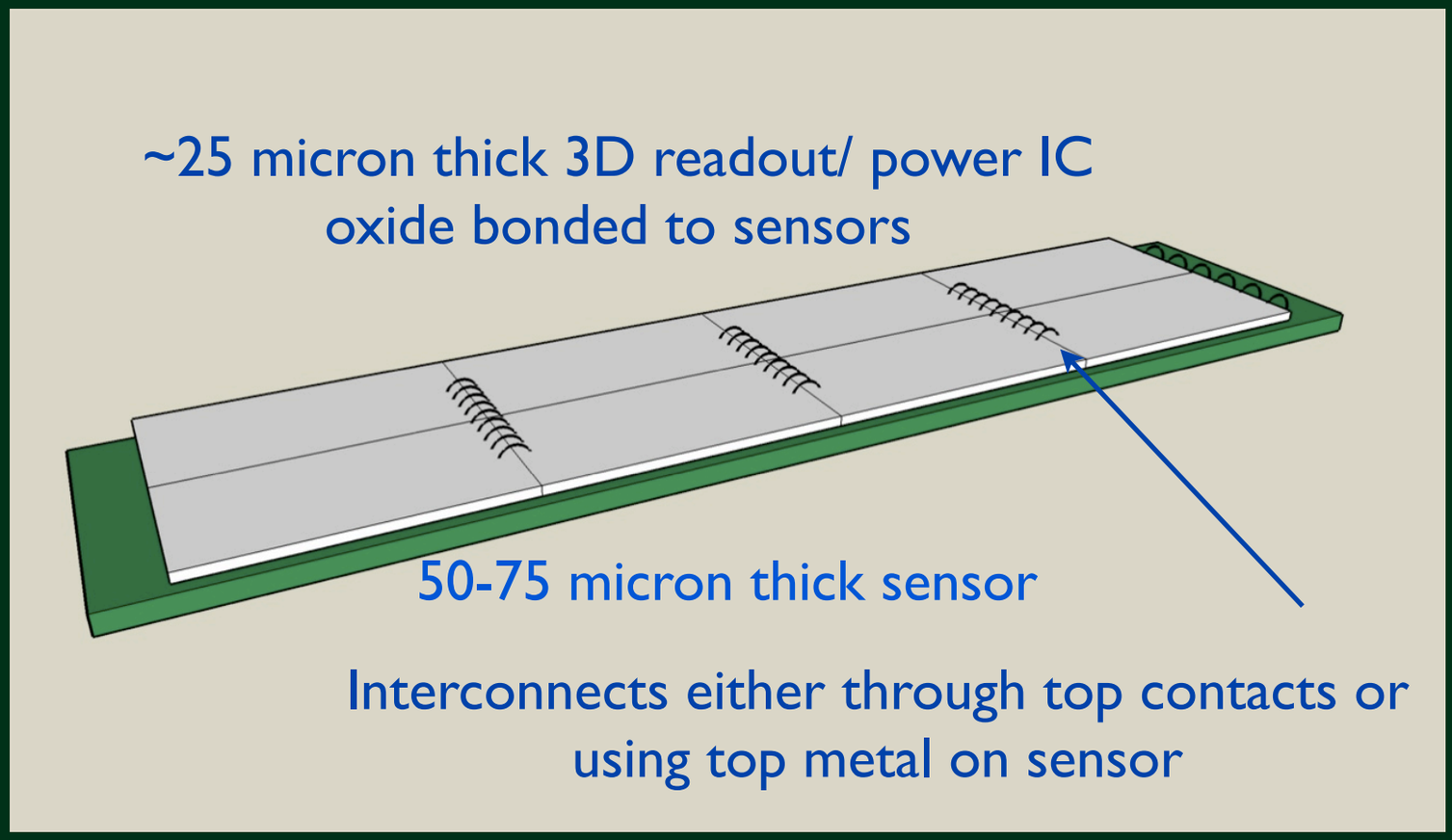
DBI bond ROIC
to sensor wafer, thin
fabricate topside pads





3D Based VXD

- Toy model of a 3D based vertex detector
  - Normal p-on-n sensors with 20-25 micron pitch pixels
  - Chip-on-wafer bond to readout ICs
    - Thin ICs to 25 microns after bonding to expose through-silicon vias and pattern topside interconnects
    - Thin base silicon if necessary



Conclusions

- First 3D chip for HEP (VIP) produced and tested
  - Functional, but low yield and high leakage currents
    - Postponed detector integration efforts for VIP
  - Second version has been submitted to MIT-LL
- Moving to commercial 3D technologies
  - VIP in two-tier 0.13 micron CMOS
  - Expect increasing commercial availability of other technologies. This is just the beginning.
- Developing sensor integration technologies
  - Thinning and laser annealing techiques
  - Received Direct bond Interconnect BTeV ICs bonded to thinned sensors
  - Shown robust fine pitch cu-sn bonding
- Conceptual design for a 3D integrated ladder