M.i.p. detection performances of a 100 μs read-out CMOS pixel sensor with digitised outputs

Marc Winter (IPHC-Strasbourg)

on behalf of IPHC and IRFU/Saclay

OUTLINE

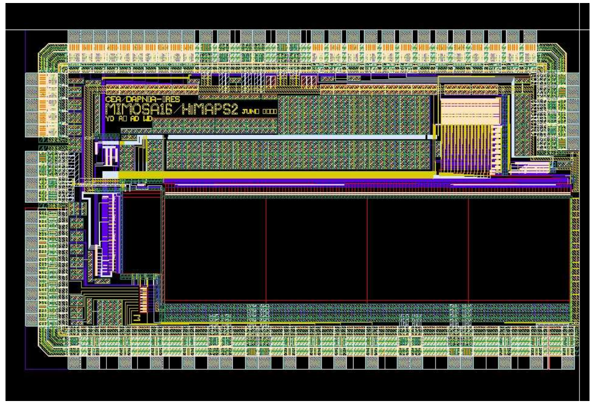
- **Strategy of the chip development (reminder)**
- **Column parallel sensor prototyping :** *Objectives of MIMOSA-22 prototyping – Lab & beam test results*
- **The question of radiation tolerance**
- **SUZE-01 zero suppression μcircuit :** *Established performances*
- **Fist chip with integrated zero suppression: status and plans**
- **Summary - Outlook**

- **Specific goals of MIMOSA-22 :**
  - *validate the fast read-out architecture developed in MIMOSA-16 (next slide) at* **Real Scale**
  - *extract an optimal pixel design (sensing diode and signal processing μcircuits)*
  - *improve the chip testability (JTAG, analog outputs, pads, ...)*

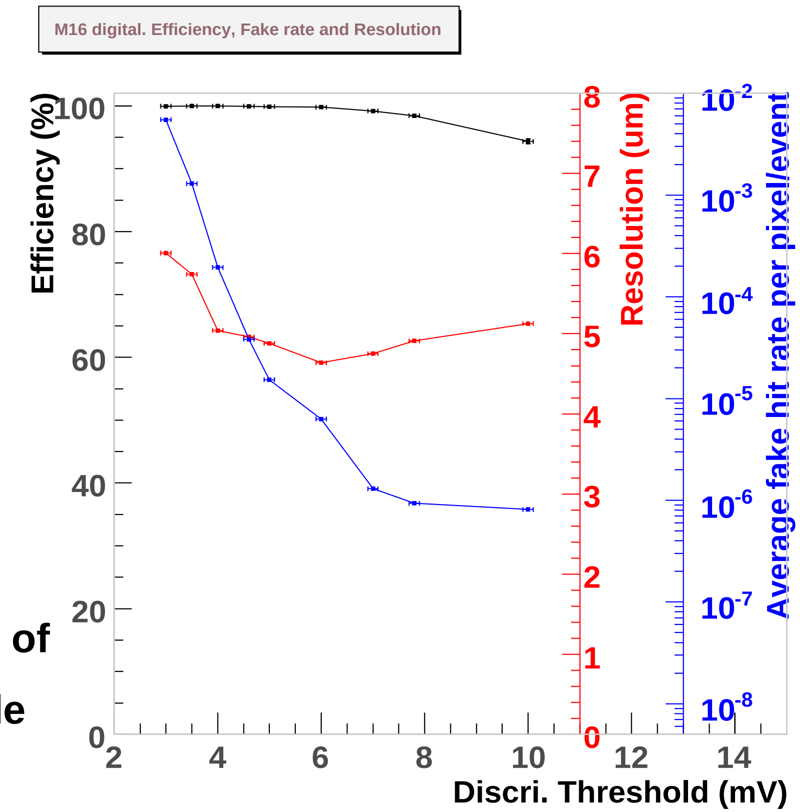
- **2 sensor versions designed and fabricated :**
  - *MIMOSA-22 : mainly for overall pixel architecture definition*
  - *MIMOSA-22bis : robustness, fine tuned optimisation, radiation tolerance*

- **Objectives beyond MIMOSA-22:**
  - *Variant (MIMOSA-23) with 640 x 640 pixels (30 μm pitch), 640 μs r.o. time, for STAR HFT 1st upgrade*
    - $\Rrightarrow$ *sent for fabrication in November '08* $\Rrightarrow$ *expected to produce (charm) physics in 2010*
  - *Merge MIMOSA-22 architecture with $\emptyset$ μcircuit (SUZE-01)*
    1) *Final sensor (MIMOSA-26) for EUDET BT* $\Rrightarrow$ *to be sent for fabrication on Friday 21st*
       - $\hookrightarrow$ *Will equip the EUDET beam telescope (6 planes) in Spring 2009*
    2) *Final sensor for STAR Vx Det. (suited to VXD outer layers)* $\Rrightarrow$ *fab. end of 2009*
       - $\hookrightarrow$ *expected to produce (charm) physics in 2011*

- *MIMOSA-16 :* ◇ *fabricated in 2006 (coll. with IRFU/Saclay)*
  - ◇ *32 col. of 128 pixels (25 μm pitch, integrated CDS)*
  - ◇ *24 col. ended with an integrated discriminator*
  - ◇ *4 different pixels (i.e. 4 sub-arrays)*



- *Tests at CERN-SPS ($\sim$ 180 GeV π^-) in Summer 2007*
  - $\rightarrowtail$ *results of one sub-array (S4)*



Discri. threshold	*Detection eff.*	*Fake rate*	*Resolution*
4 m V	*99.96 $\pm$ 0.03 (stat) %*	$\sim$ *2·10^{-4}*	$\sim$ *4.8 – 5.0 μm*
6 m V	*99.88 $\pm$ 0.05 (stat) %*	*<10^{-5}*	$\sim$ *4.6 μm*

▷▷▷ **Architectures of pixel (integrated CDS) and of full chain made of ”columns ended with integrated discri.” validated at small scale**

Main Characteristics of the MIMOSA-22 Sensor

♣ **Extension of MIMOSA-16 ⟶ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

Pixel characteristics (*optimal charge coll. diode size ?*) :

- **pitch : 18.4 μm** (compromise resolution/pixel layout)
- diode surface : $\sim$ 10 – 20 μm^2 to optimise charge coll. & gain
- **128 columns ended with discriminator**
- **576 pixels per column ($\equiv$ final column length)**
- 8 columns with analog output for test purposes
- 9 sub-matrices of 64 rows :

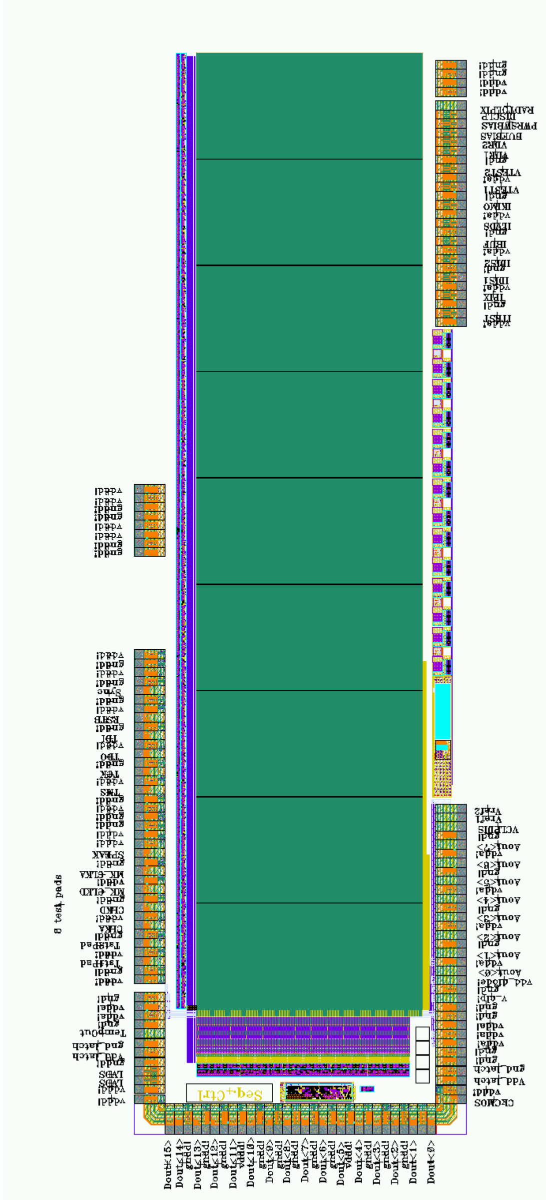
  17 pixel designs w/o ionising rad. tol. diode

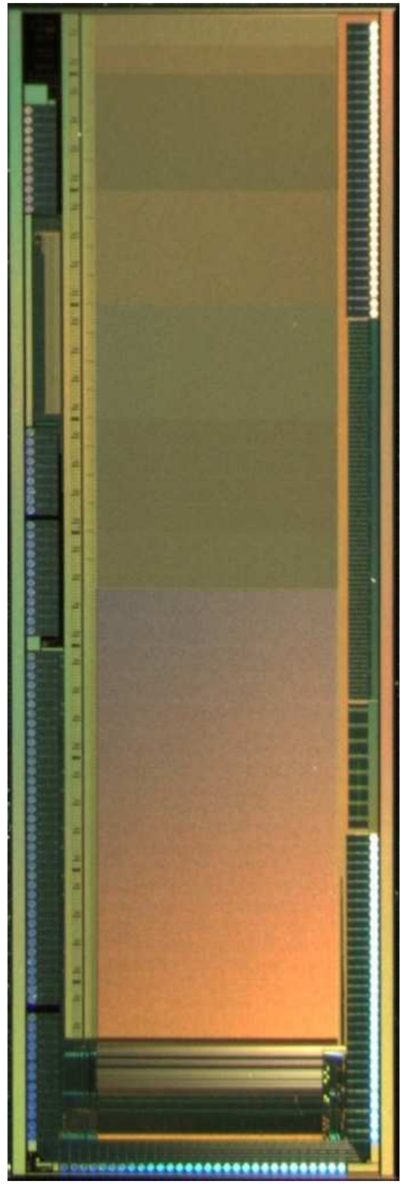
  $\Rightarrow$ **active digital area $\sim$ 25 mm^2** (128 x 576 pixels)
- **read-out time $\sim$ 100 μs ($\sim$ 10^4 frames/s)**

Testability :

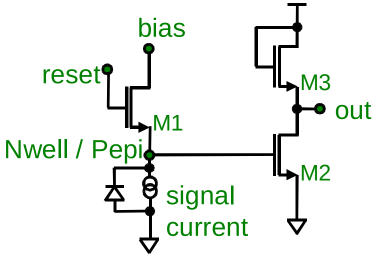
- JTAG + bias DAC ⟶ **programmable chip steering**
- 2 additionnal DC voltages to emulate pixel's output

  for independent discriminator performance assessment
- output frequency $\leq$ 40 MHz

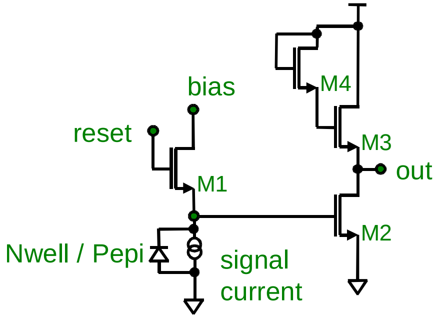




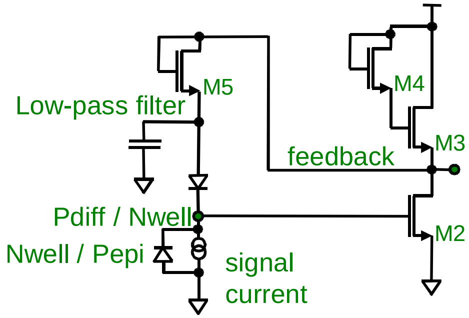
- **Various pixel designs (rad. tol. and standard) :**
  - *reset diode (improved gain)*
  - *self-biased diode with feedback (improved gain)*



(S13)



(S10)

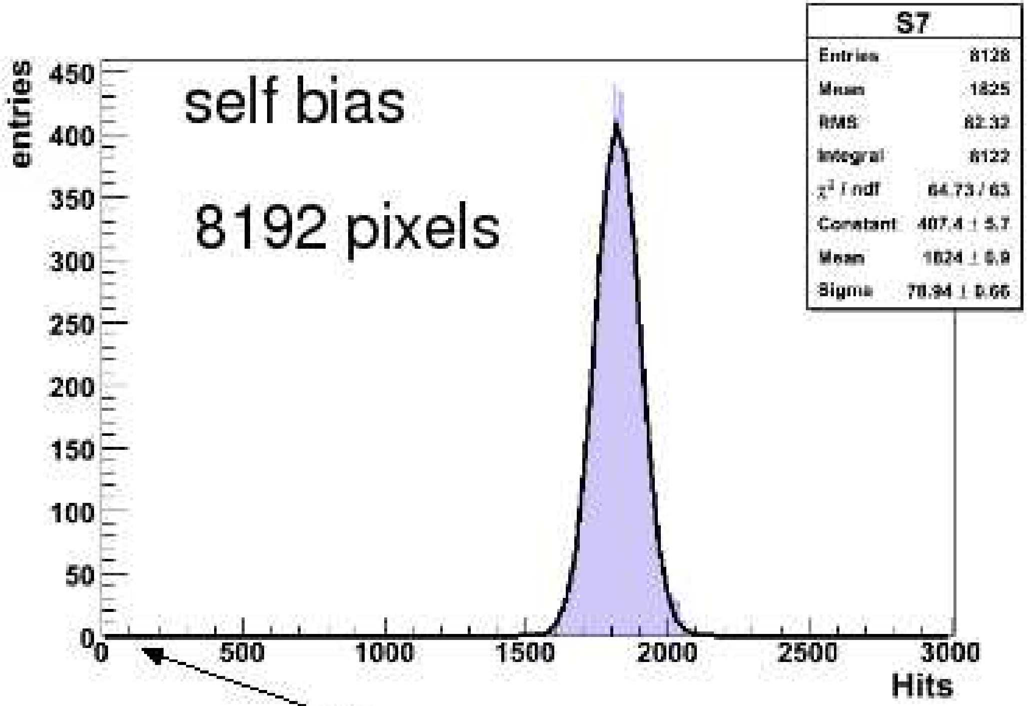


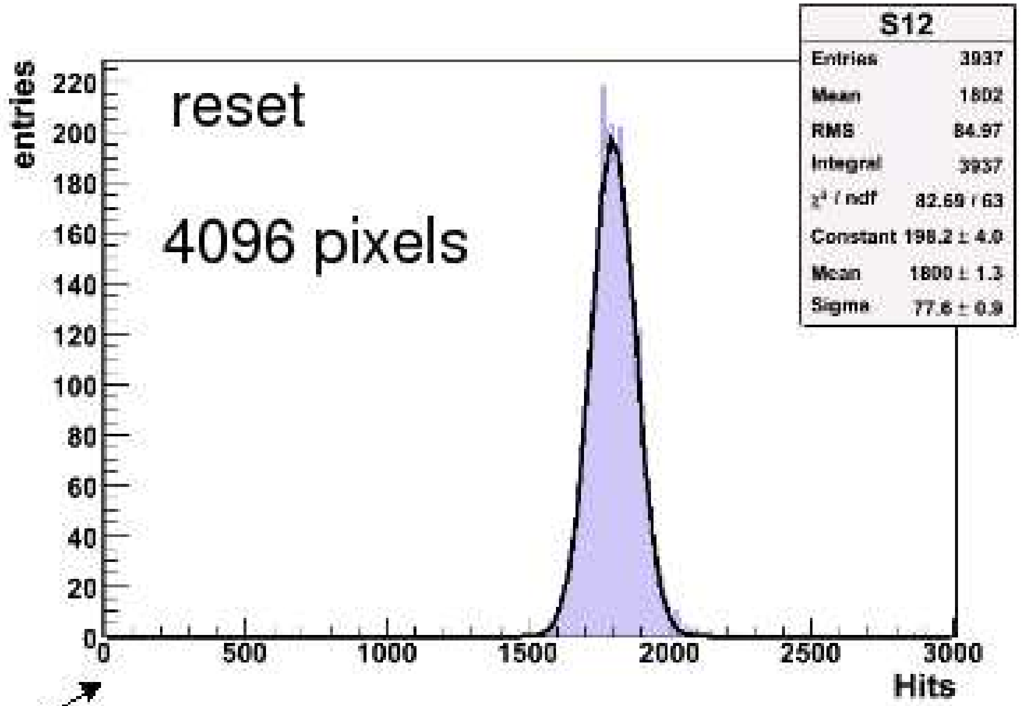
(S6)

- **Main results obtained with exposure to ^{55}Fe source (t$_{r.o.}$ = 92.5 μs) :**
  - *Noise :*
    - *Temporal (pixel) Noise $\sim$ 0.5 – 0.7 mV (10 $<$ N $<$ 14 e$^-$ ENC)*
    - *FPN $\sim$ 0.25 mV*
    - *N (rad. tol. pixels) $\sim$ N (standard pixels) + 1 e$^-$ ENC*
  - *Cluster CCE :*
    - *3x3 pixels : 70 – 80 %*
    - *5x5 pixels : 80 – 90 %*
  - *modest T dependence between $\sim$ 10°C and 35°C : $\lesssim$ 10 % noise variation*
  - *5 different chips characterised : identical performances within $\pm$ 5 %*

MIMOSA-22 Lab Tests : Digital Output Results

5 mV threshold with ^{55}Fe source





No dead pixel number

Good uniformity of discriminator response, within 4%

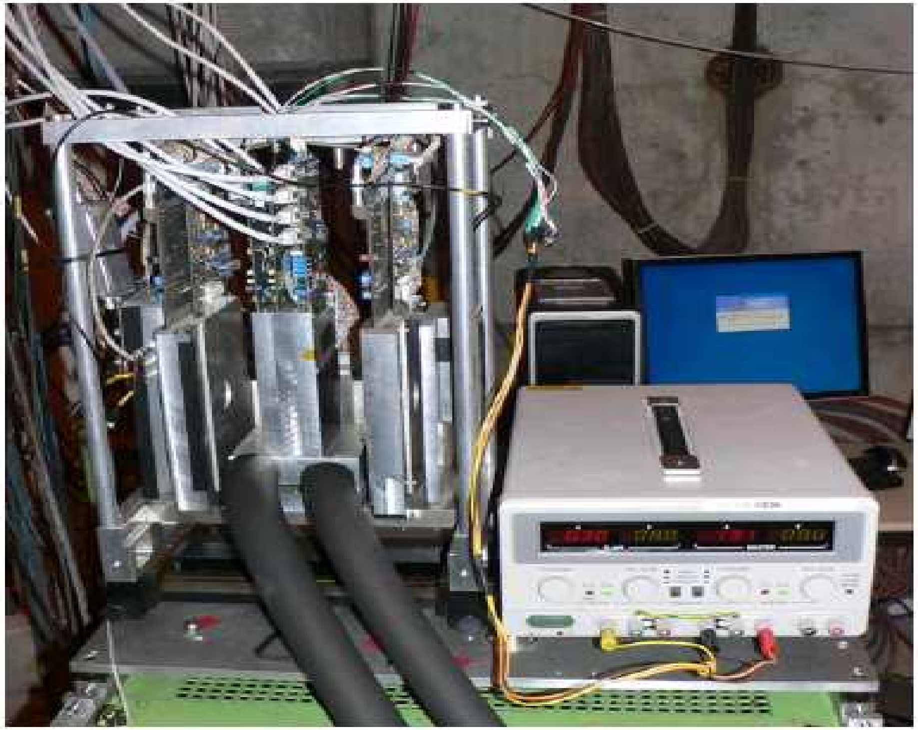
MIMOSA-22 Beam Tests : Data Taking Conditions

- **4 weeks of beam time at CERN-SPS :**
  - ▷ *∼ 2 weeks in August with MIMOSA-22 (EUDET period)*
  - ▷ *∼ 2 weeks in Sept.-Oct. with MIMOSA-22bis (SiLC period)*

- **T4-H6 beam line : ∼ 120 GeV π^- beam** ▷▷▷▷

- **Chips mounted at center of Si-strip telescope**

  (4 pairs of orthogonal strips) ▷▷▷▷



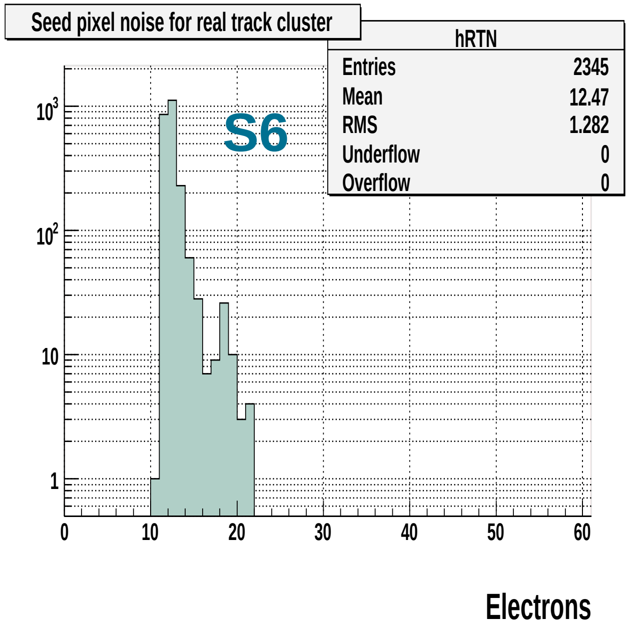
- **2 MIMOSA-22 and 4 MIMOSA-22bis chips tested**

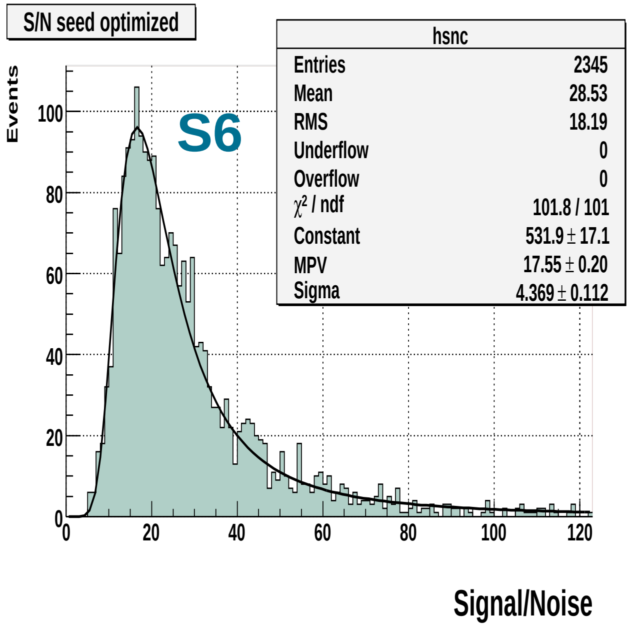
  at several values of discriminator threshold

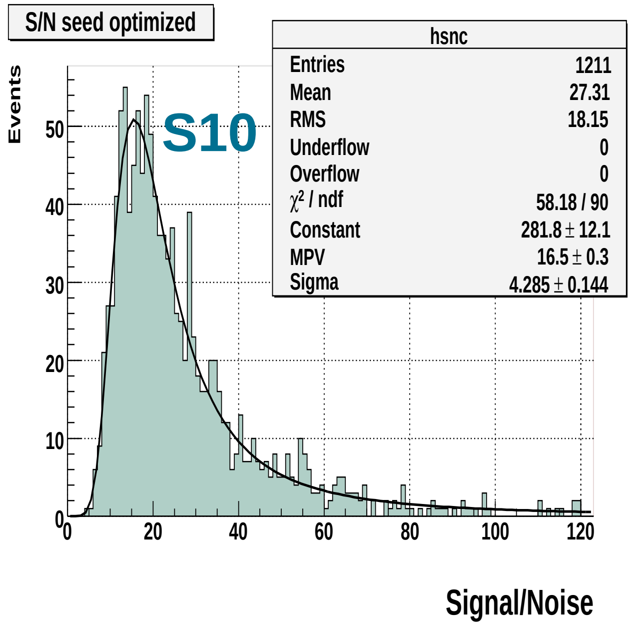
- **> 1 million tracks reconstructed in the sensors**

M-22 Beam Tests : Analog Output Performances

- Noise and S/N (seed pixel) distributions delivered by the 8 columns without discriminator







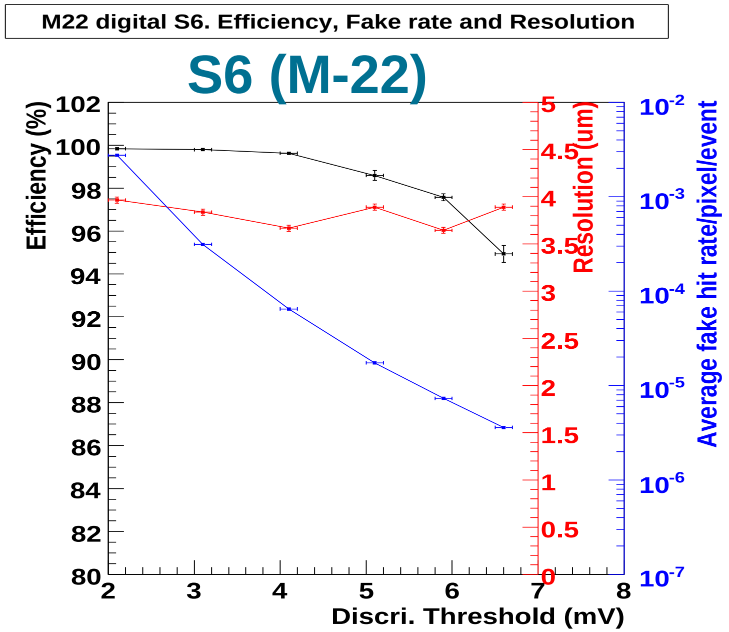
- **Detection performances (det. eff. , N and S/N for hits where the seed pixel exhibits S/N $>$ 4) :**

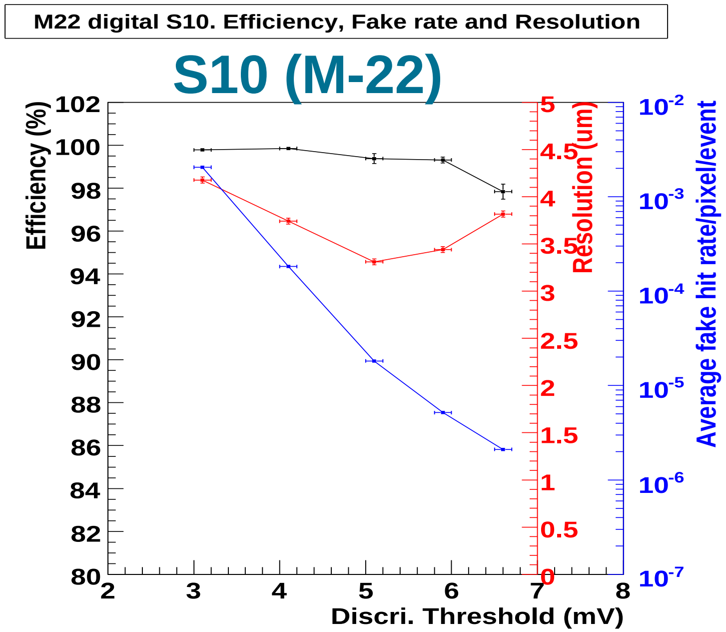
Sub-array	*S6*	*S7*	*S8*	*S9*	*S10*	*S12*	*S13*
Det. eff.	*99.93 % $\pm$ 0.05 %*	*99.95 % $\pm$ 0.04 %*	*100.00 % +0/-0.30 %*	*100.00 % +0/-0.14 %*	*99.87 % $\pm$ 0.09 %*	*100.00 % +0/-0.08 %*	*100.00 % +0/-0.07 %*
N (e^- ENC)	*12.5 $\pm$ 0.1*	*11.6 $\pm$ 0.1*	*12.3 $\pm$ 0.1*	*10.6 $\pm$ 0.1*	*13.6 $\pm$ 0.1*	*12.1 $\pm$ 0.1*	*14.0 $\pm$ 0.1*
S/N (seed, MPV)	*17.6 $\pm$ 0.2*	*18.5 $\pm$ 0.2*	*20.9 $\pm$ 1.1*	*19.5 $\pm$ 0.5*	*16.5 $\pm$ 0.3*	*18.2 $\pm$ 0.3*	*16.0 $\pm$ 0.3*

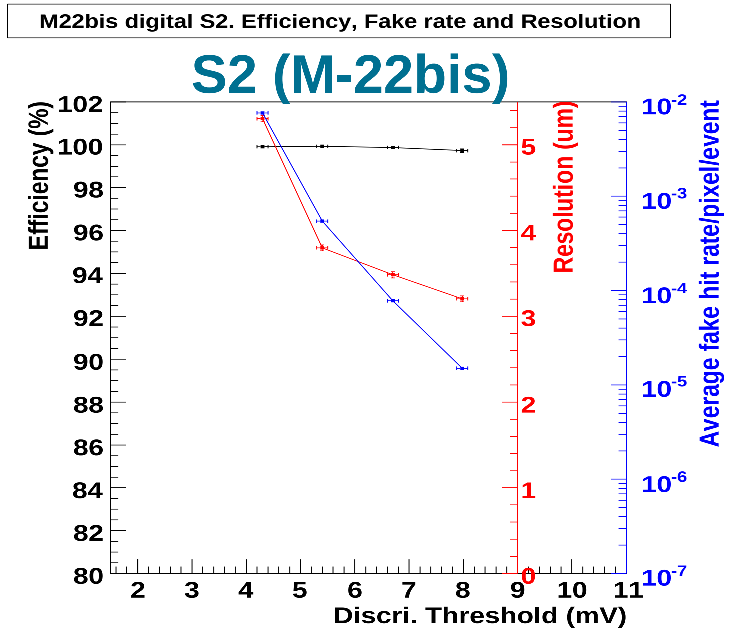
⋇ *very satisfactory performances (det. eff. $\sim$ 99.9 % and single pt resolution $\lesssim$ 1.5 μm)*

$\Rrightarrow$ **pixel architecture (diode size, rad. tol. diode design, amplification scheme) validated**

- **Det. eff., fake hit rate & spatial resolution for S6 & S10 (M-22) and S2 (M-22bis) vs discri. threshold :**







- **Main results:**

  - *rather marginal performance differences between $>$ 10 diff. pixels (e.g. rad. tol. vs standard)*
  - *det. eff. of analog output $\sim$ 99.9 % for all sub-arrays $\Rrightarrow$ pixel architecture validated*
  - *det. eff. of digital output $\gtrsim$ 99.8 % for almost all sub-arrays (agrees with MIMOSA-16)*
  - *fake hit rate very low (O(10^{-4} – 10^{-5})) while det. eff. still near 100 %*
  - *(binary) single point resolution $\gtrsim$ 3.5 μm (as expected)*
  - *no performance non-uniformity observed over the chip surface $\Rrightarrow$ real scale check validated*

Requirements:

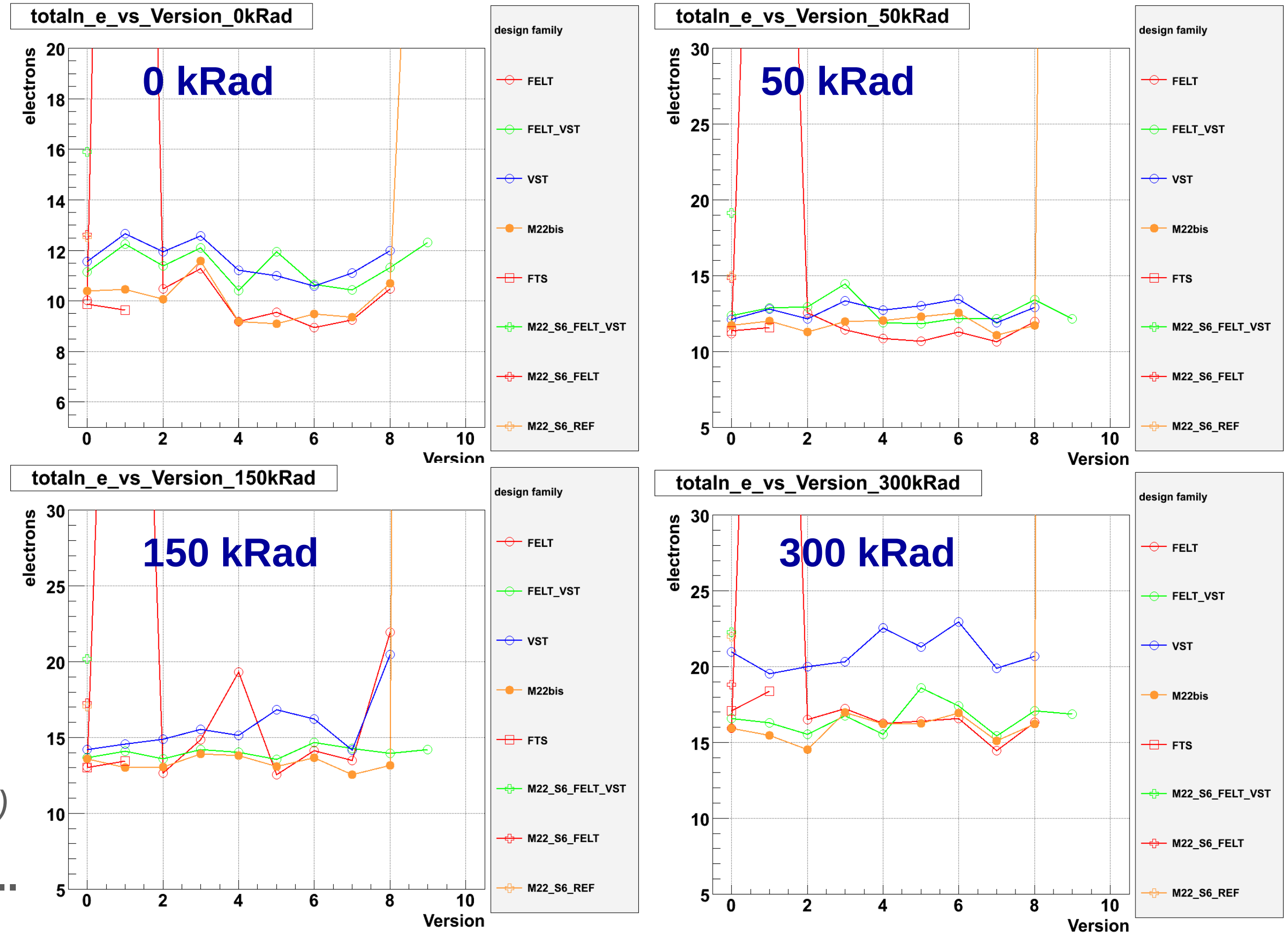
- **beamstrahlung (**GuineaPig X 2 **) :** $\lesssim$ **10**^{3} **e**$^{\pm}_{BS}$**/cm**^{2}**/25** μs $\rightarrowtail$ $\lesssim$ **2·10**^{12}**e**$^{\pm}_{BS}$**/cm**^{2}**/yr**

  $\hookrightarrow$ **O(100) kRad/yr – O(10**^{11}**) n**$_{eq}$**/cm**^{2}**/yr (**NIEL $\sim$ 1/30**)**

Assessing rad. tolerance (10 keV X-Rays) in lab.:

▷ *ex. of S6 (M22) variants at + 20*$^\circ$*C*

- **before irradiation** $\gtrsim$ **9.5 e**$^-$ **ENC**
- **after 50 kRad** $\gtrsim$ **11 e**$^-$ **ENC**
- **after 150 kRad** $\gtrsim$ **13 e**$^-$ **ENC**
- **after 300 kRad** $\gtrsim$ **15 e**$^-$ **ENC**



▷▷▷ **Excellent noise performance**

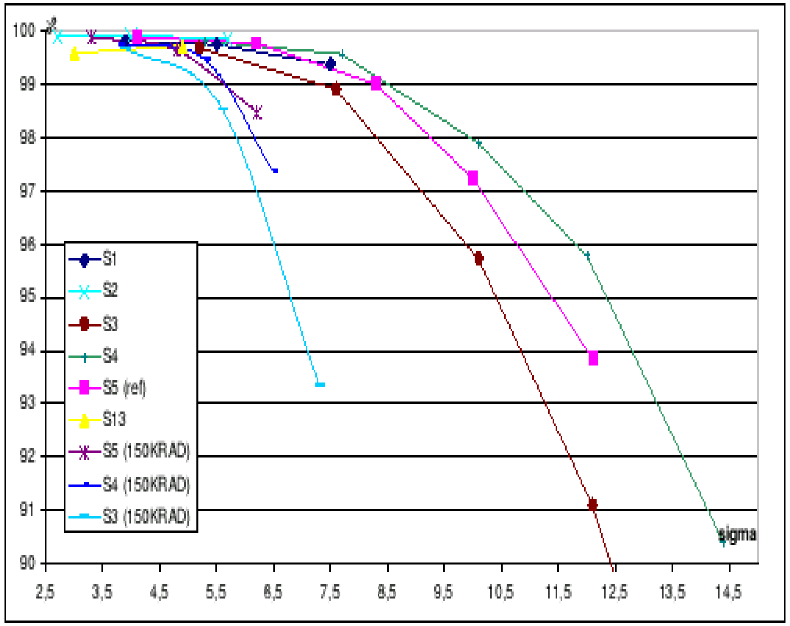
(but source of noise increase still under study)

... watch Charge Collection Efficiency ...

A. Dorokhov, IPHC, Strasbourg, 12

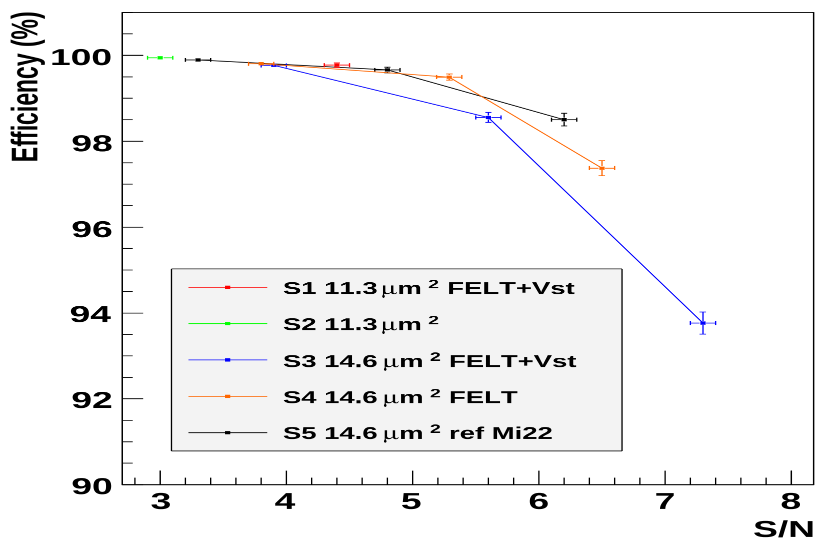
MIMOSA-22bis : Beam Test Results on Radiation Tolerance

- Beam test results with chips irradiated with 150 kRad :

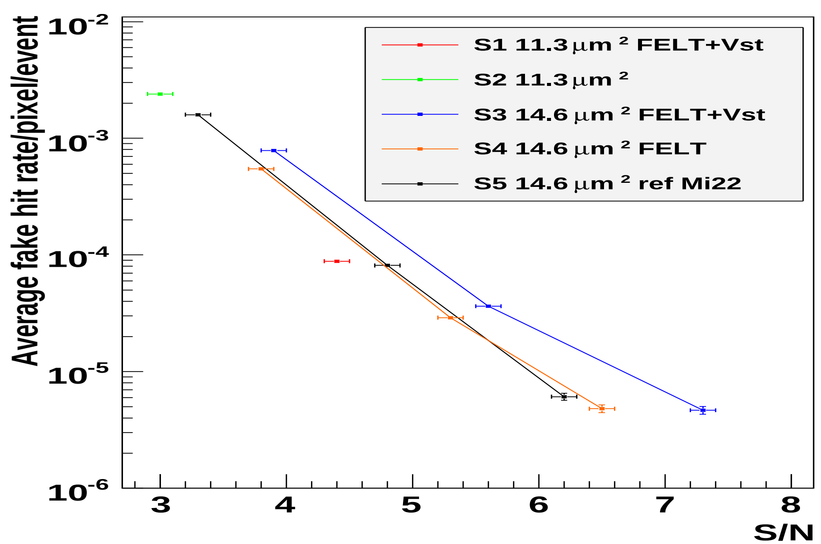


Det. eff. vs SNR before and after irradiation (150 kRad)

M22bis digital Efficiency after 150kRad



M22bis digital fake hit rate

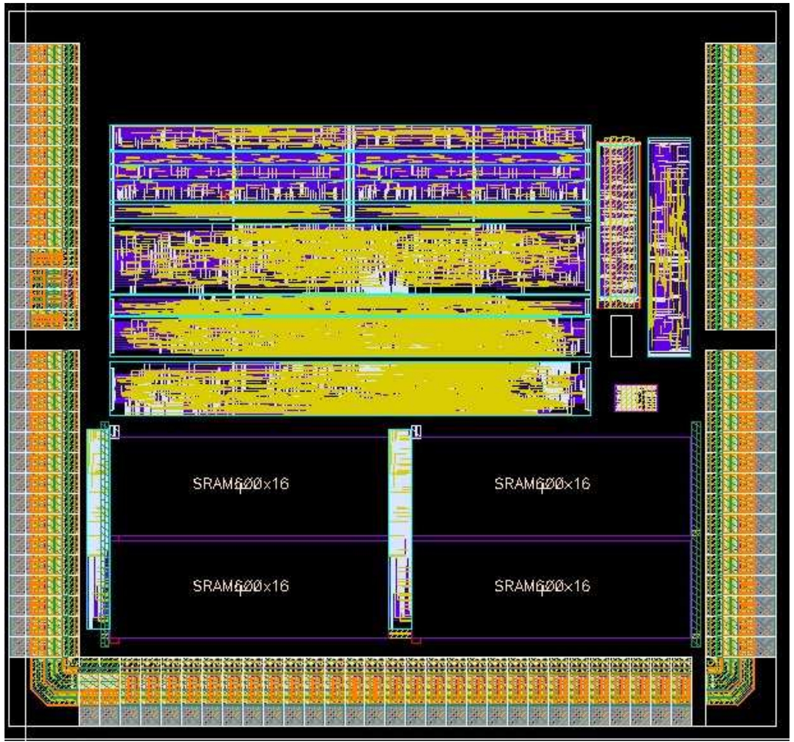


▷▷▷ **Pixel & column parallel architecture with integrated discriminators**

Fully Validated !!!

Zero Suppression Micro-Circuit : SUZE-01 Test Results

- **1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :**
  - *2 step, raw by raw, logic :*
    - *step-1 (inside blocks of 64 columns) :*
      identify up to 6 series of $\leq$ 4 neighbour pixels per raw
      delivering signal $>$ discriminator threshold
    - *step-2 : read-out outcome of step-1 in all blocks*
      and keep up to 9 series of $\leq$ 4 neighbour pixels
  - *4 output memories (512x16 bits) taken from AMS I.P. lib.*
  - *surface $\sim$ 3.9 $\times$ 3.6 mm^2*

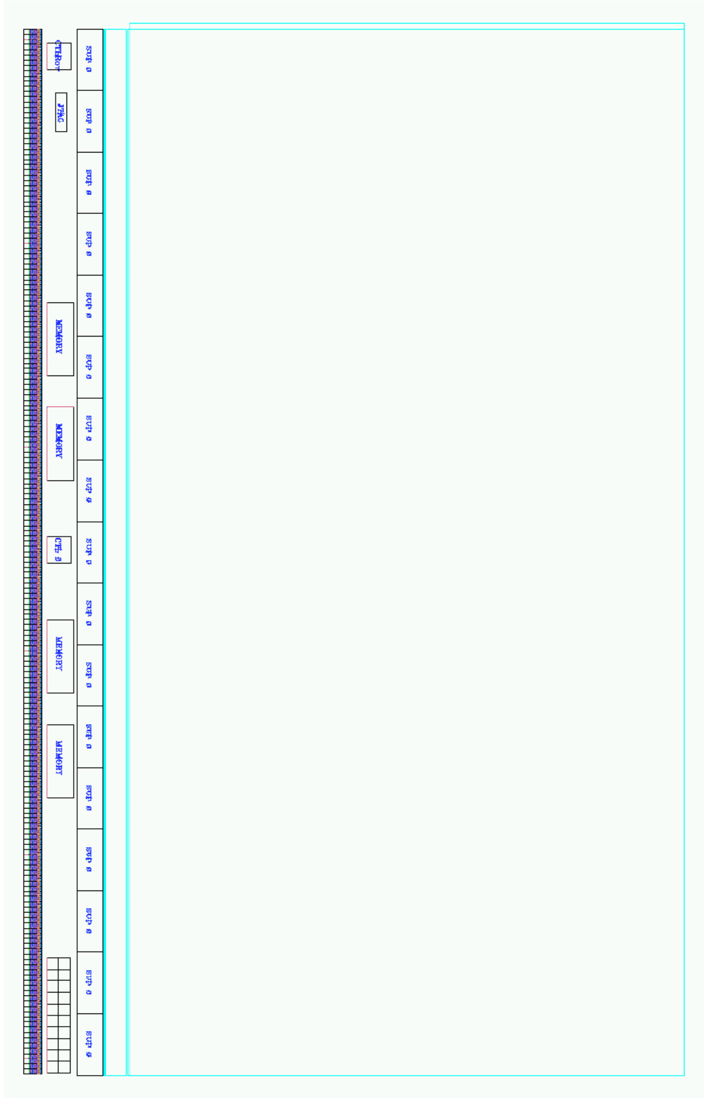


- **Test results summary :**
  - *back from foundry end of Sept. '07 $\rightarrowtail$ (lab) tests completed*
  - *design performances reproduced up to 1.15 $\times$ design read-out frequency (T_{room}) :*
    noise values as predicted, no pattern encoding error, can handle $>$ 100 hits/frame at rate $>$ 10^4 frames/s

- **Still to do :** *evaluate radiation tolerance (latch-up) of ouput memories*

Main Parameters of the Complete Sensor MIMOSA-26

- **Novembre 2008 : fabrication of MIMOSA-26 = Final Sensor for EUDET BT**



⋇ **M-22 (binary outputs) complemented with $\emptyset$ (SUZE-01)**

⋇ best performing (rad. tol.) pixel architecture of M-22(bis)

$\hookrightarrow$ S5 pixel of MIMOSA-22bis

⋇ **Active surface : 1152 columns of 576 pixels (21.2 x 10.6 mm^2)**

$\hookrightarrow$ **extension of M-22 & SUZE-01 from 128 col. to 9 x 128 col.**

⋇ **Pixel pitch : 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels**

$\hookrightarrow \sigma_{sp} \gtrsim$ **3.5** μm

⋇ **Integration time $\sim$ 110 $\mu s \rightarrowtail \sim$ 10^4 frames / second**

⋇ $\emptyset$ based on 18 groups of 64 columns and assuming $\leq$ 9 "clusters" per row

⋇ Chip dimensions : $\sim$ 21 x 12 mm^2

⋇ Data throughput: 1 output at $\geq$ 80 Mbits/s or 2 outputs at $\geq$ 40 Mbits/s

⋇ Engineering run : 2 (+ $\leq$ 4) wafers of $\gtrsim$ 30 chips expected (if yield $\sim$ 50 %)

⋇ **Design nearly completed $\Rrightarrow$ submission this Friday ....**

- **Col. // architecture with discri. outputs validated for m.i.p. detection on real scale (*128 col. of 576 pix.*) :**
  - *read-out frequency* $\sim 10^4$ *frames/s* ✓
  - *pixel noise* $\sim$ *10–13* e^- *ENC* ⇛ *S/N* $\sim$ *17–22 (MPV)* ✓
  - $\epsilon_{det} >$ *99.5 % with fake rate* $\sim$ *O(*10^{-4} *-* 10^{-5}*), similar to MIMOSA-16* ✓
  - $\sigma_{sp} \gtrsim 3.5\ \mu m$ ⇛ *14* μm *pitch would be sufficient for 3* μm *resolution demanded for VXD* ✓
  - *ionising rad. tol.* $\sim$ *sufficient for VXD innermost layer (3 yrs ???)* ✓

⇛ **2x2 cm^2 variant (30 μm pitch, 640 μs r.o.time) for STAR Vx Det. 1st upgrade**

⇛ *Being fabricated* ⇛ *(charm) physics in 2010*

⇛ **MIMOSA-26 $\equiv$ final sensor for EUDET BT ((combining col. // architecture with $\emptyset$ μ-circuit) :**

- *design* $\sim$ *completed* ⇛ *submission on Friday Nov. 21st '08*

↪ **tests expected to start in January 2009 ⇛ sensors mounted on BT in Spring '09**

⇛ **Extension of MIMOSA-26: final sensor for STAR Vx Det. upgrade (OK for VXD out layers)**

⇛ *Fabrication end of 2009* ⇛ *(charm) physics in 2011*

⇛ **New step in 2009 (coll. with FNAL & INFN): 1st prototypes in 3D technology**

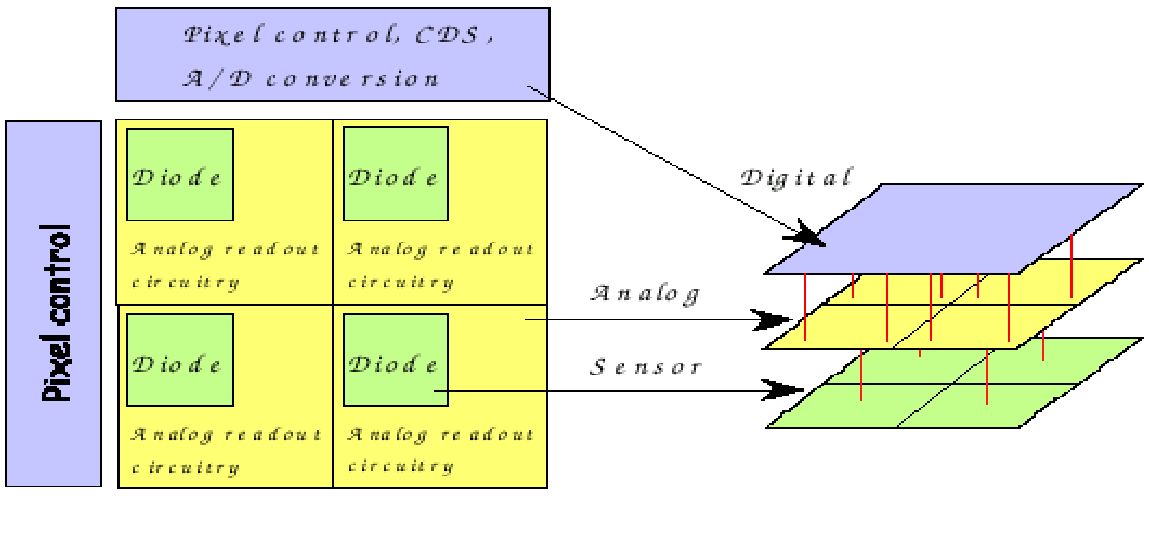
↪ **2-tier & 3-tier devices, single & mixed CMOS techno., continuous & delayed r.o.**

Using 3DIT to Improve CMOS Sensor Performances

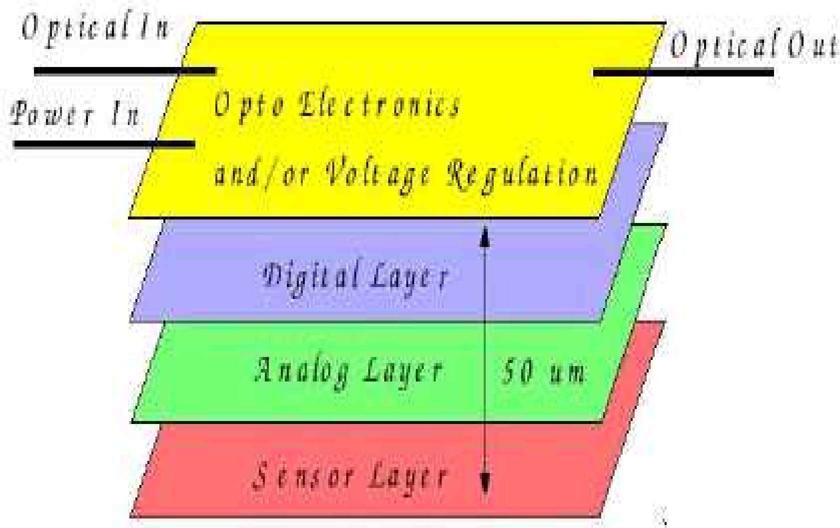
- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - *combine different fab. processes*
  - *alleviate constraints on transistor type inside pixel*

- **Split signal collection and processing functionnalities :**
  - *Tier-1: charge collection system*
  - *Tier-2: analog signal processing*
  - *Tier-3: mixed and digital signal processing*
  - *Tier-4: data formatting (electro-optical conversion ?)*

- **Use best suited technology for each Tier :**
  - *Tier-1: epitaxy, deep N-well ?*
  - *Tier-2: analog, low leakage current, process (nb of metal layers)*
  - *Tier-3 & -4 : digital process (nb of metal layers), feature size ⟼ fast laser (VOCSEL) driver, etc.*



Conventional MAPS 4 Pixel Layout   3D 4 Pixel Layout



- **2009 : 1st MIMOSA sensors in 3DIT**
  - *fab. technology : Chartered - Tezzaron*
  - *130 nm – 2 Tiers*
  - *Several collaborators sharing the reticule, coordinated by FNAL :*
    - *FNAL*
    - *INFN labs*
    - *IN2P3 labs*
    - *IRFU/Saclay*
  - *2 types of devices :*
    - *2-Tier single CMOS*
    - *3-Tier mixed CMOS*

- **combine MIMOSA design (IPHC) with VIP (FNAL)**