Column Parallel CCD and Raw Charge Storage Pixels by LCFI

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for LCFI collaboration

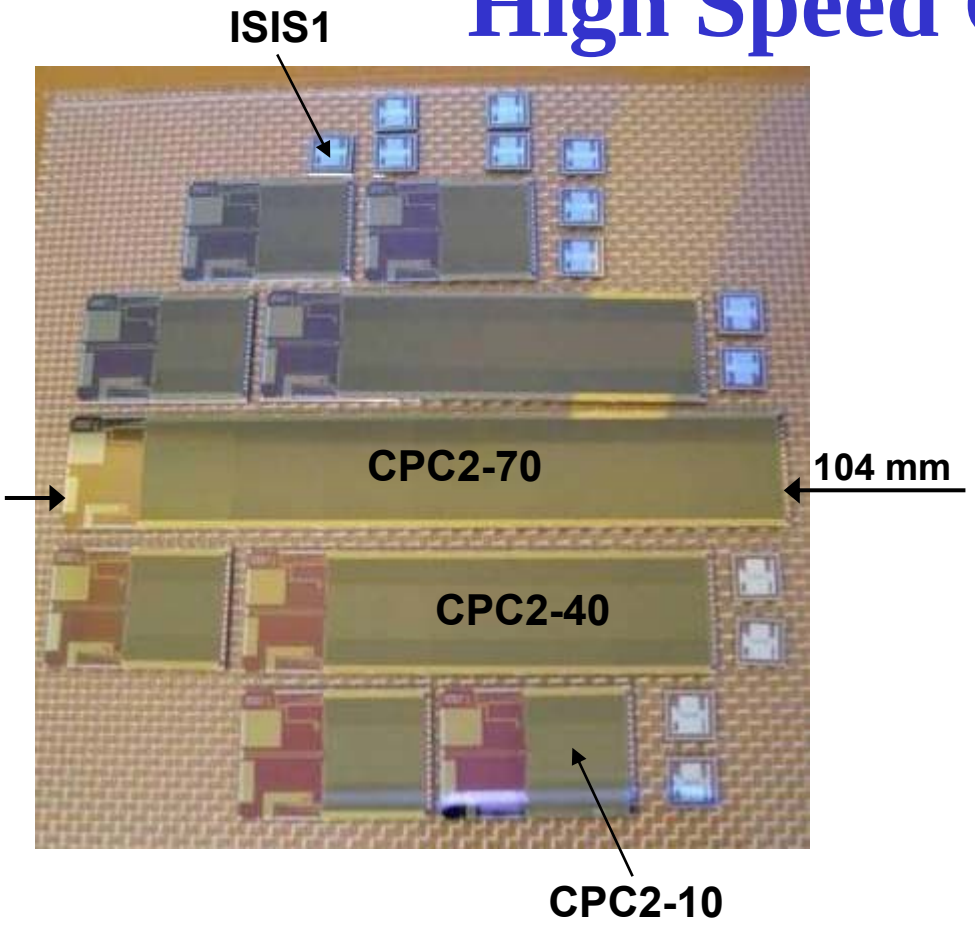
LCWS2008, 17 November 2008

Outline

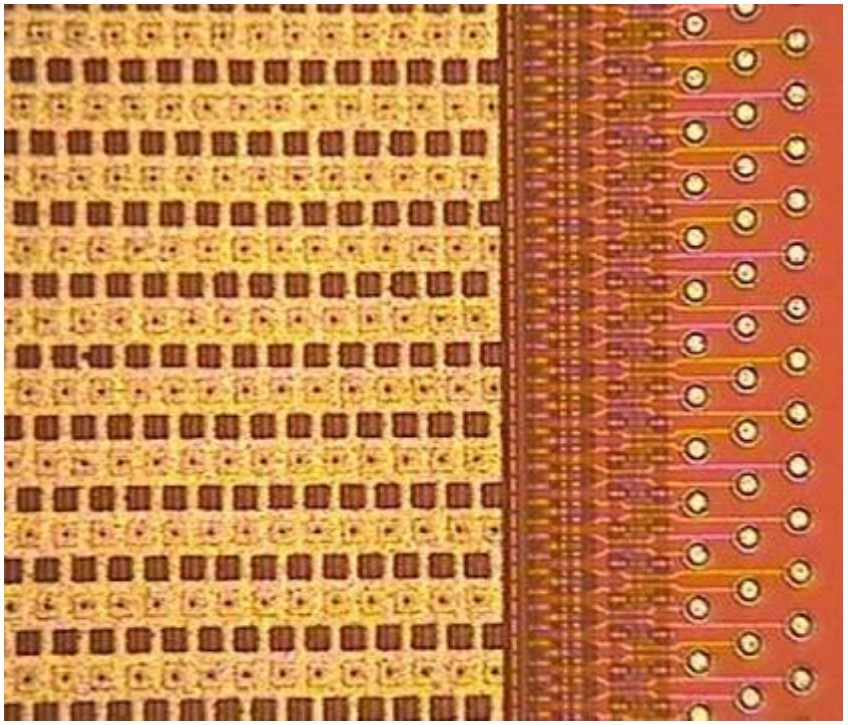
- Column Parallel CCD
  - Sensor: CPC2
  - Readout ASIC : CPR2A
  - CPCCD with reduced capacitance : CPC-T
- Raw charge storage pixels: ISIS2

CPCCD Sensor: CPC2

High Speed CPCCD



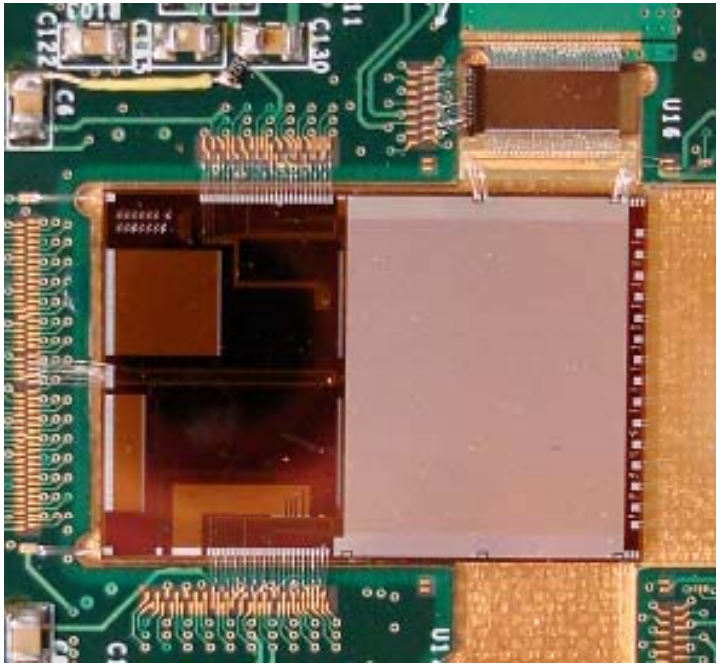
Busline-free CPC2

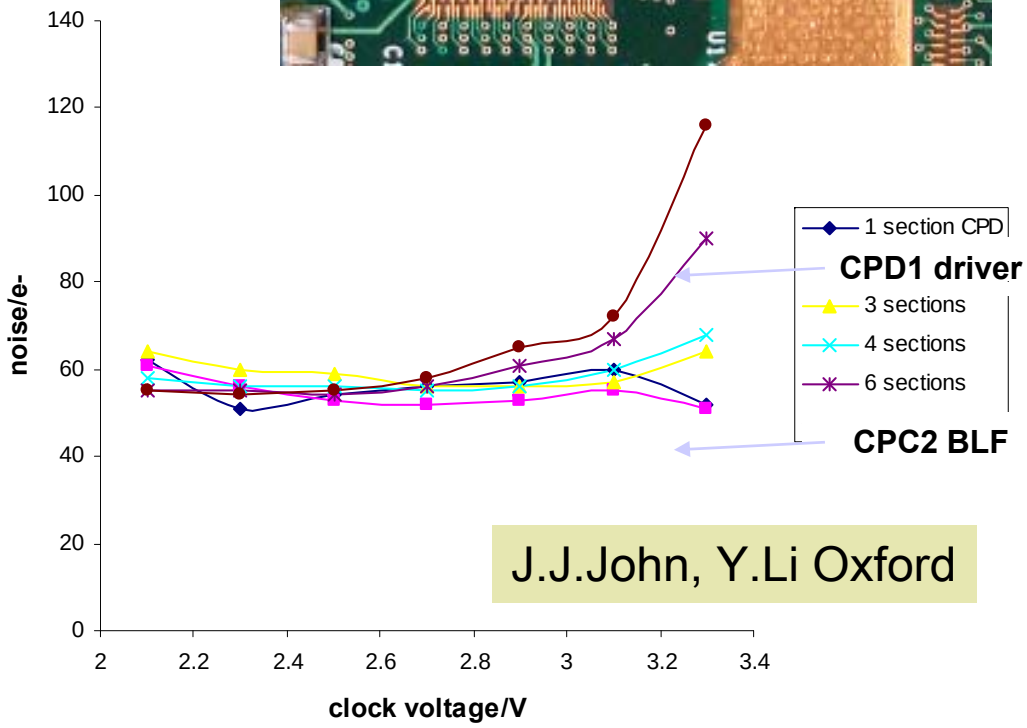


- High speed (busline-free) devices with 2-level metal clock distribution
- Whole image area serves as a distributed busline
- Designed to reach 50 MHz operation

Tests of high speed CPC2

- Need CPD1 driver chip to drive high speed CPC2
- Assembled several CPC2-10 and CPC2-40 with CPD1
- CPC2 noise performance optimized using CPD1 handles
  - # CPD1 sections
  - Clock voltage

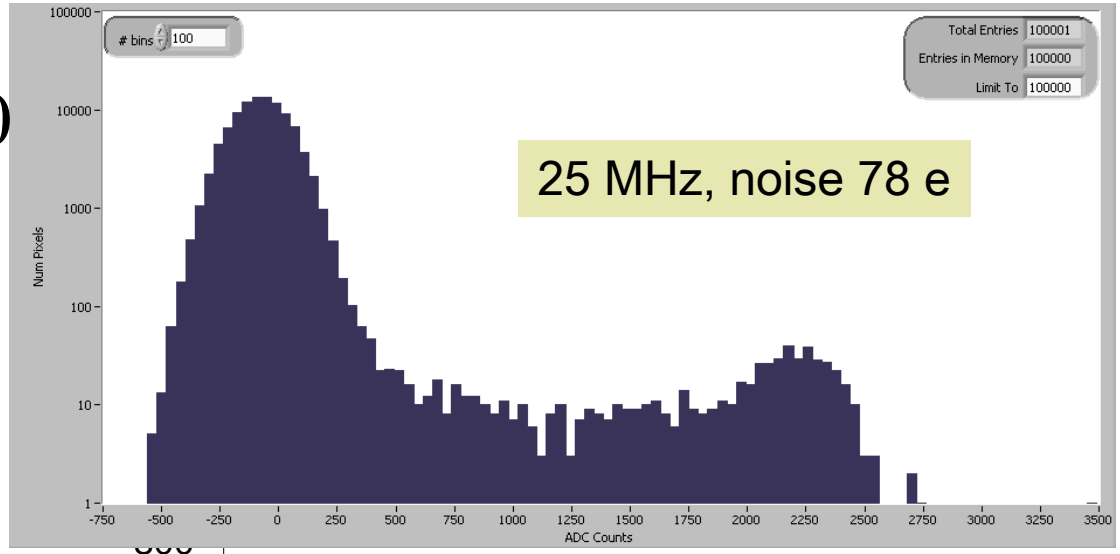


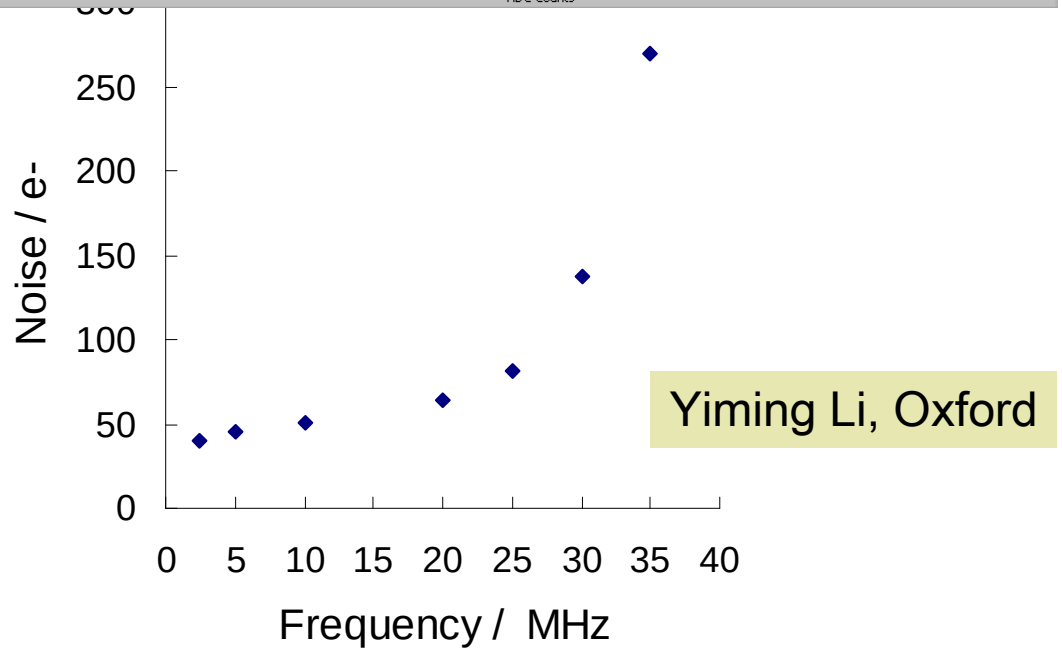


J.J.John, Y.Li Oxford

Maximum Frequency

- Low noise operation up to 30 MHz for CPC2-10
  - 50 MHz within reach
- Limited by substrate bounce effects
  - Clock pickup at analogue outputs, need to measure amplitude on fast transients
  - Happens inside CPC2

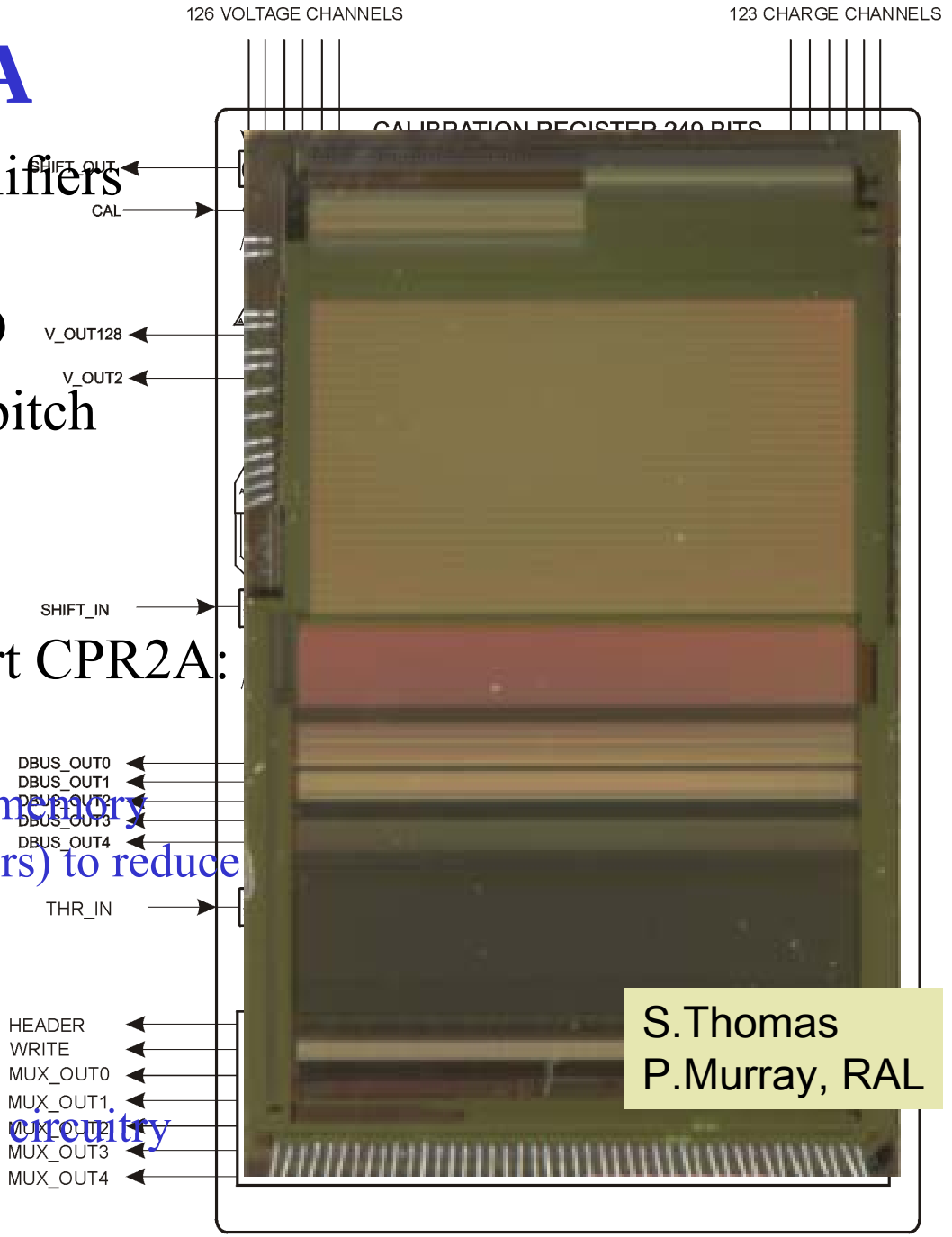




Readout Chip for CPCCD: CPR2A

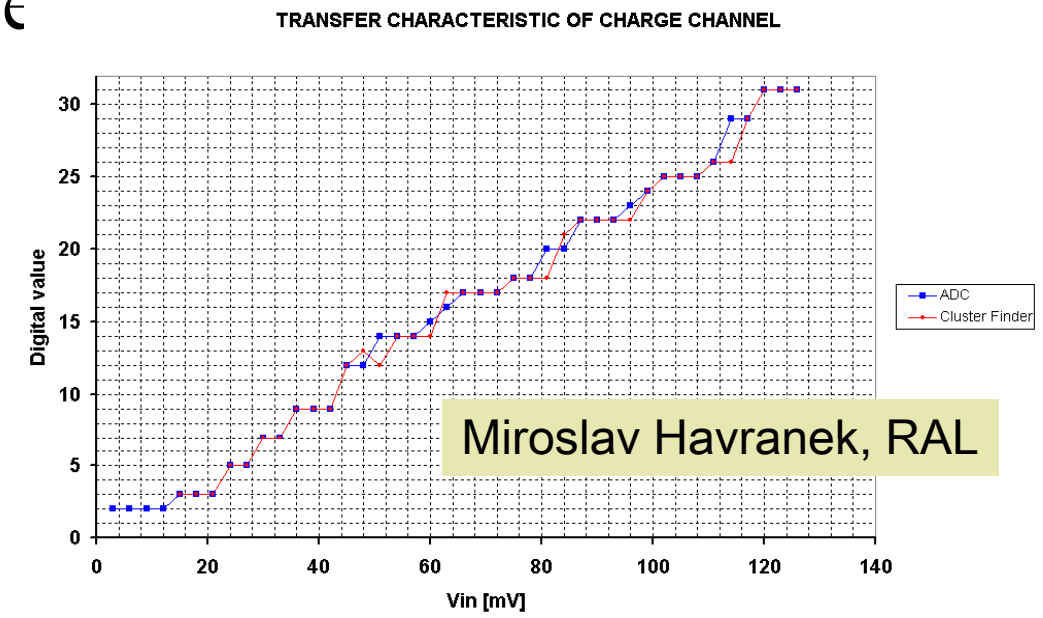
CPR2A

- 125 voltage and charge amplifiers channels
- Analogue and digital test I/O
- 5-bit flash ADCs on 20 μm pitch
- Cluster finding logic
- Sparse readout circuitry
- A range of improvements wrt CPR2A:
  - Cluster size reduced to 4×6
  - 3-fold increase in the column memory buffer (can store up to 3 clusters) to reduce dead time
  - Individual column threshold
  - Analogue calibration circuit
  - Improvements to the analogue circuitry



CPR2A Tests

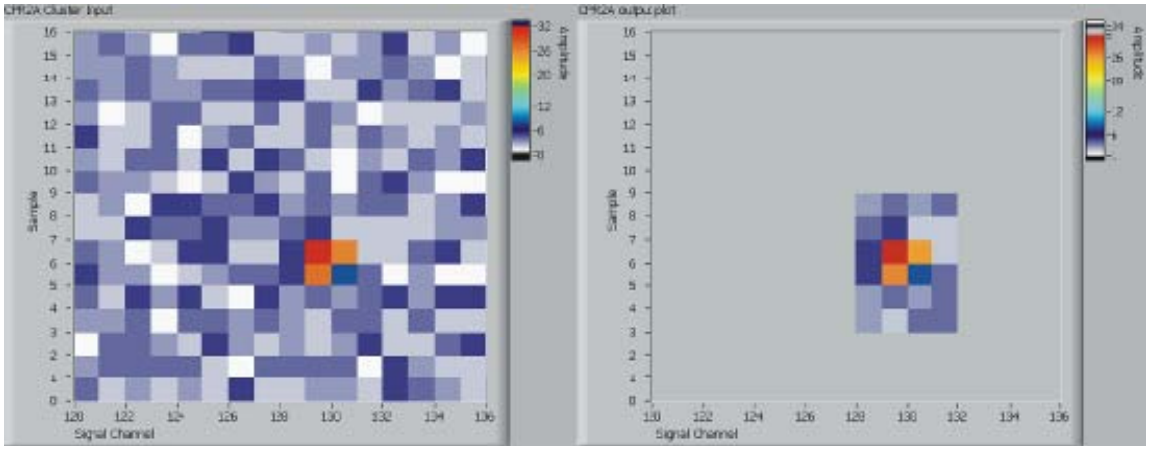
- Tests started in March 2008
- Simultaneous operation of analogue inputs and cluster finder demonstrated for both voltage and charge amplifiers
- Plot: analogue performance with and without asynchronous cluster finding
  - Charge amplifiers did not work in CPR2

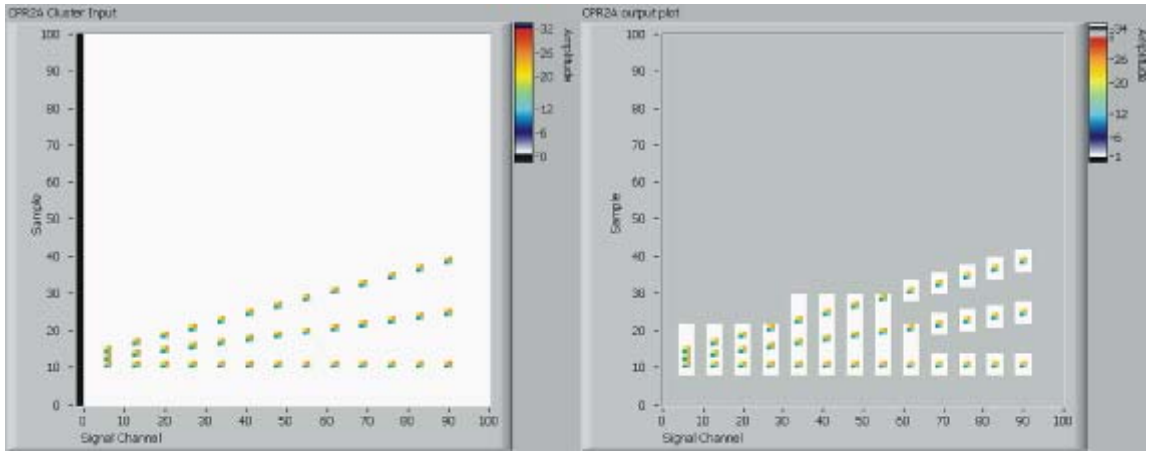


Miroslav Havranek, RAL

CPR2A Cluster Finding

- 2x2 seed cluster
- 4x6 (min size) clusters buffered inside CPR2A
- Cluster finding can be tested both with digital and analogue inputs
  - Software/firmware effort to code input calibration clusters and analyse data
- Performs up to specs

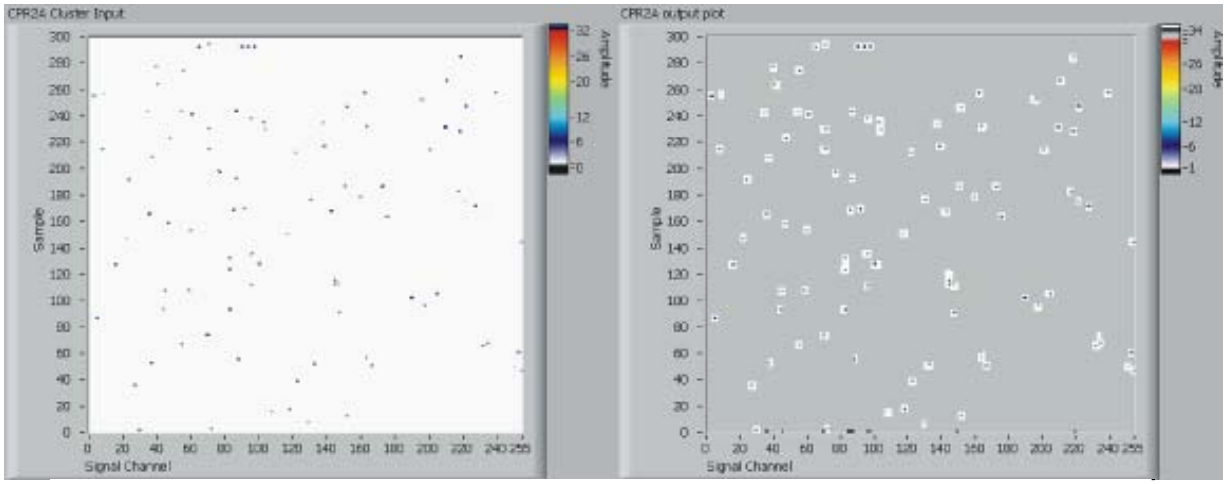




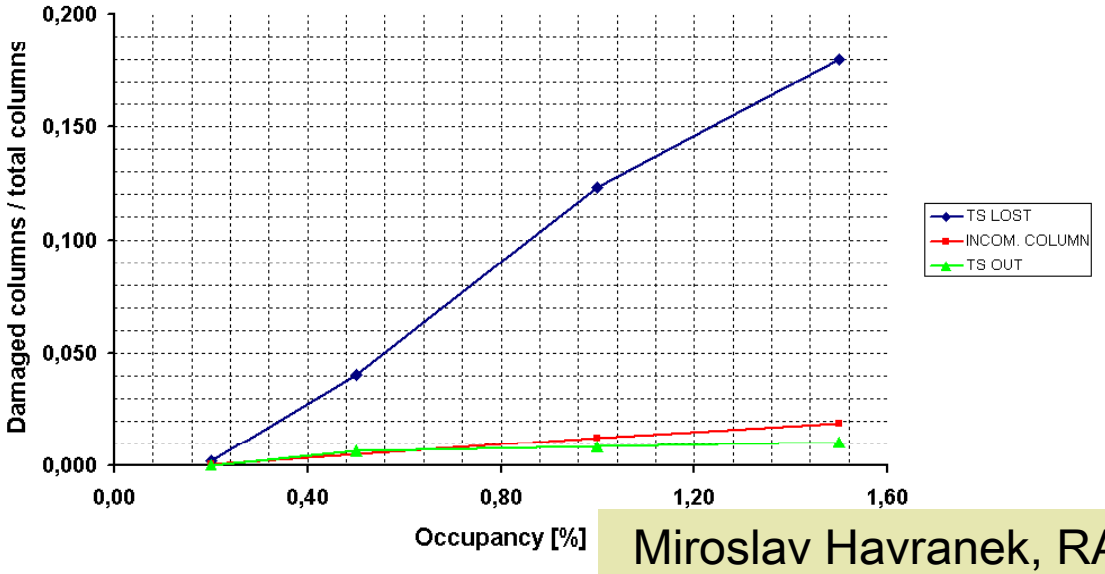
Miroslav Havranek, RAL

CPR2A Cluster Finding

- Errors analysed for random distribution of cluster locations
  - No errors till 0.2% occupancy
  - Most frequent error is loss of time stamp



ERRORS VS OCCUPANCY



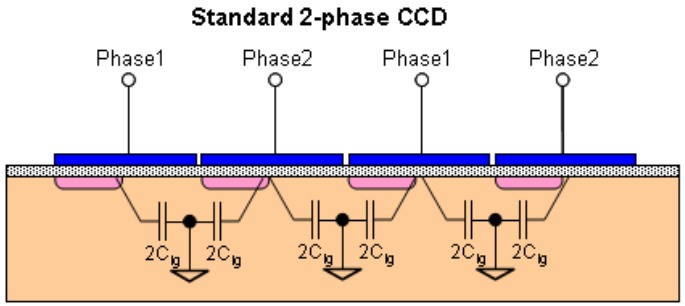
- Overall CPR2A performance is quite impressive and it is ready for CPC2

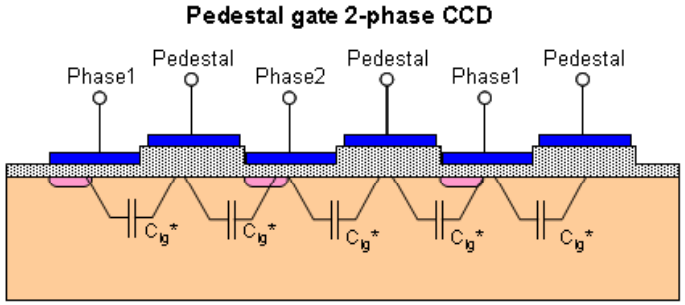
Miroslav Havranek, RAL

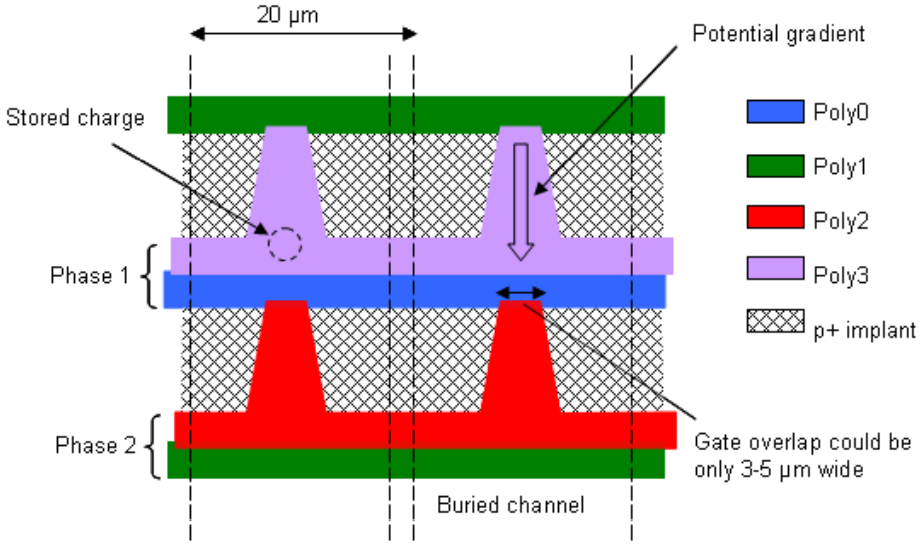
CPCCD with reduced capacitance and reduced clock voltage: CPC-T

CPC-T

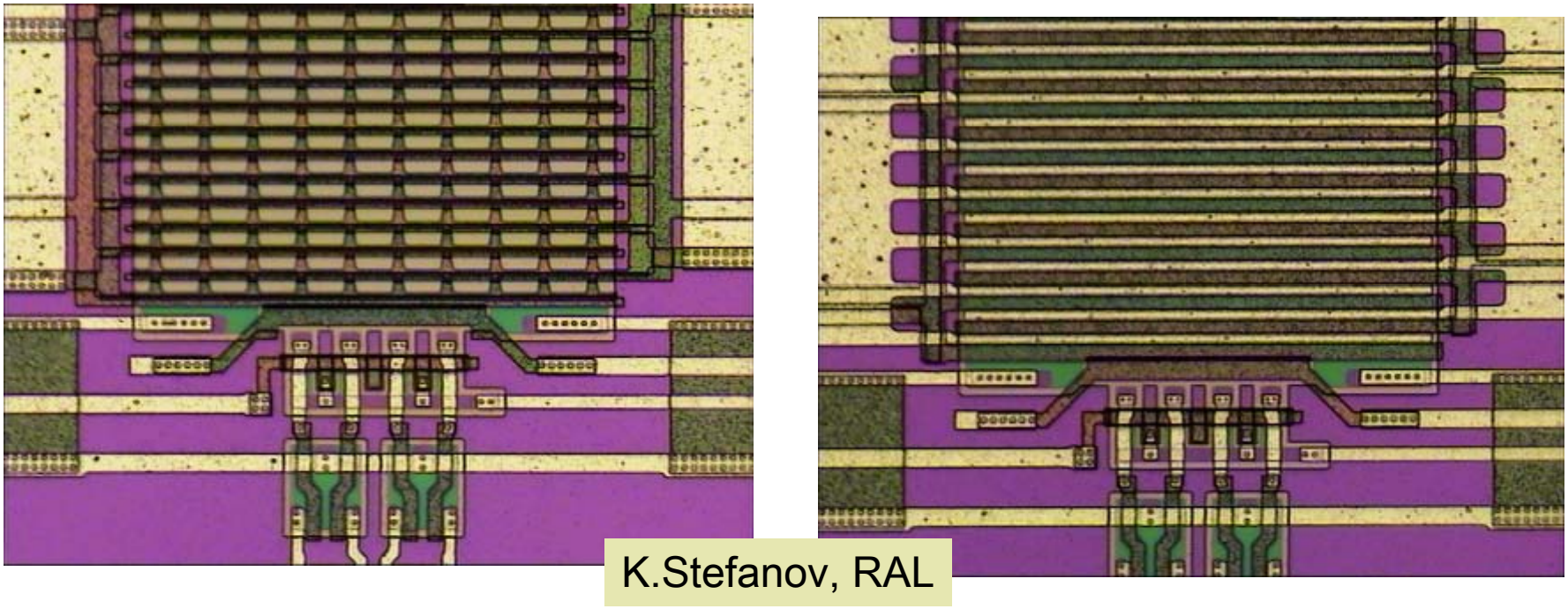
- Two-fold goal : lower V and lower C
- Two designs based on CPC2 to study very low inter-gate barriers and clock amplitudes
- Six designs for reduction of the inter-gate capacitance:
  - Pedestal CCD (on 20 µm and 24 µm pitch)
  - Shaped Channel CCD (variant of the Pedestal CCD), on 20 µm and 24 µm pitch
  - Open Phase CCD
  - "Inter-channel gap" CCD
- Pedestal designs could reduce Cig by a factor of 2-4, open phase by ≈2







CPC-T

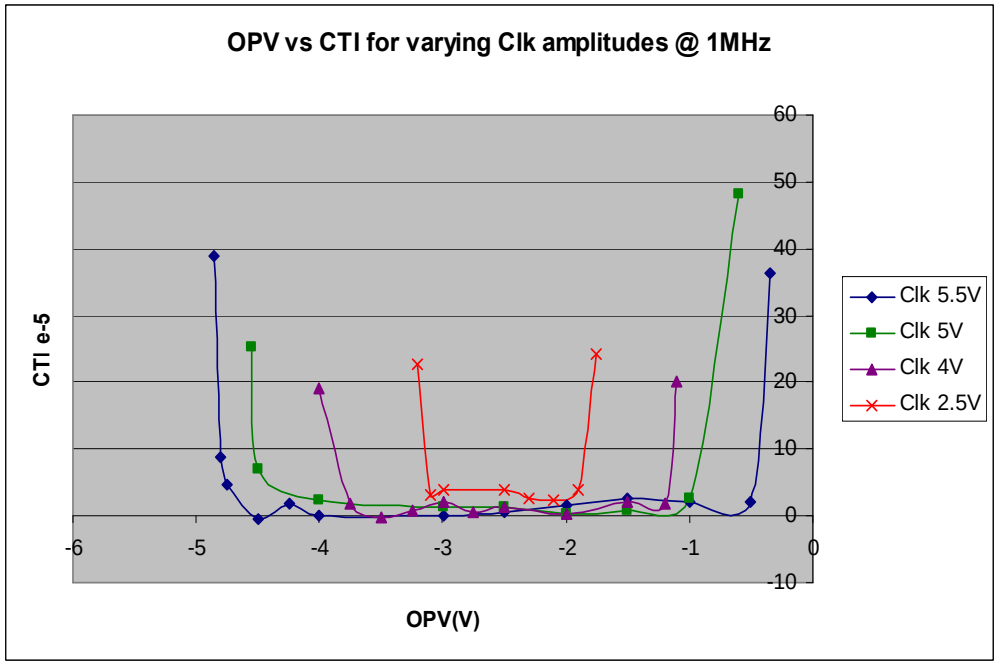


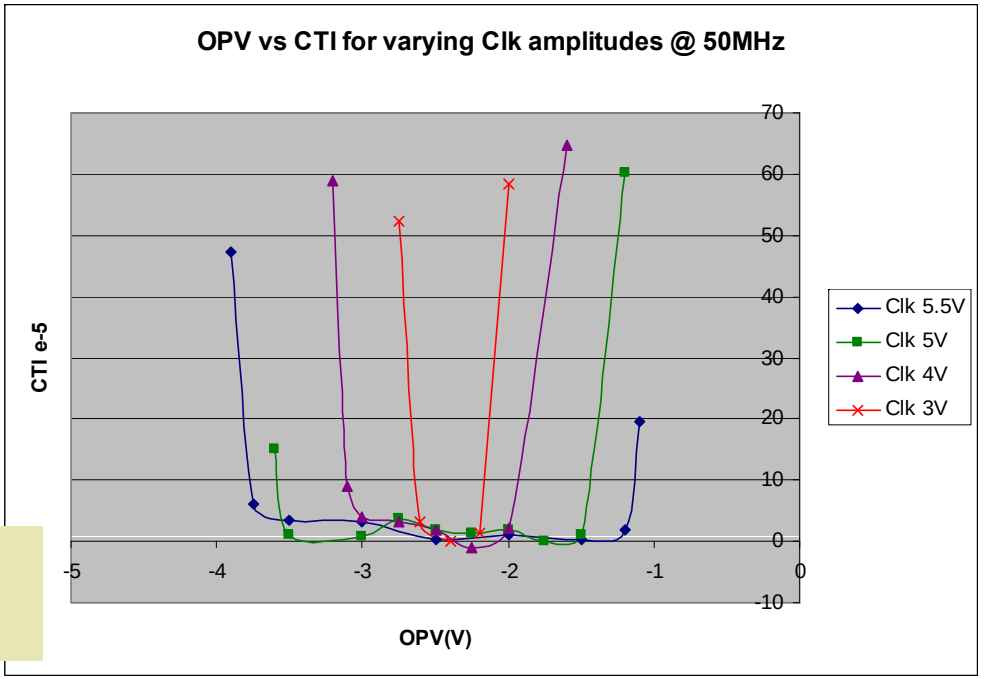
K.Stefanov, RAL

- 6 CPC-T wafers delivered in March 2008, one of each type
  - One type (stepped nitride barrier) failed for complete wafer

CPC-T Tests

- 24 variants to test – a lot of work
- 4-phase CCD used to determine the minimal clock amplitude
  - Look at CTI as function of gate potentials
  - OPV is voltage difference between two gates of the same phase, emulates implant for 2-phase devices
- 50 MHz operation is no problem
  - Small device – small C
  - But need higher clock voltage
  - Smaller operational OPV range





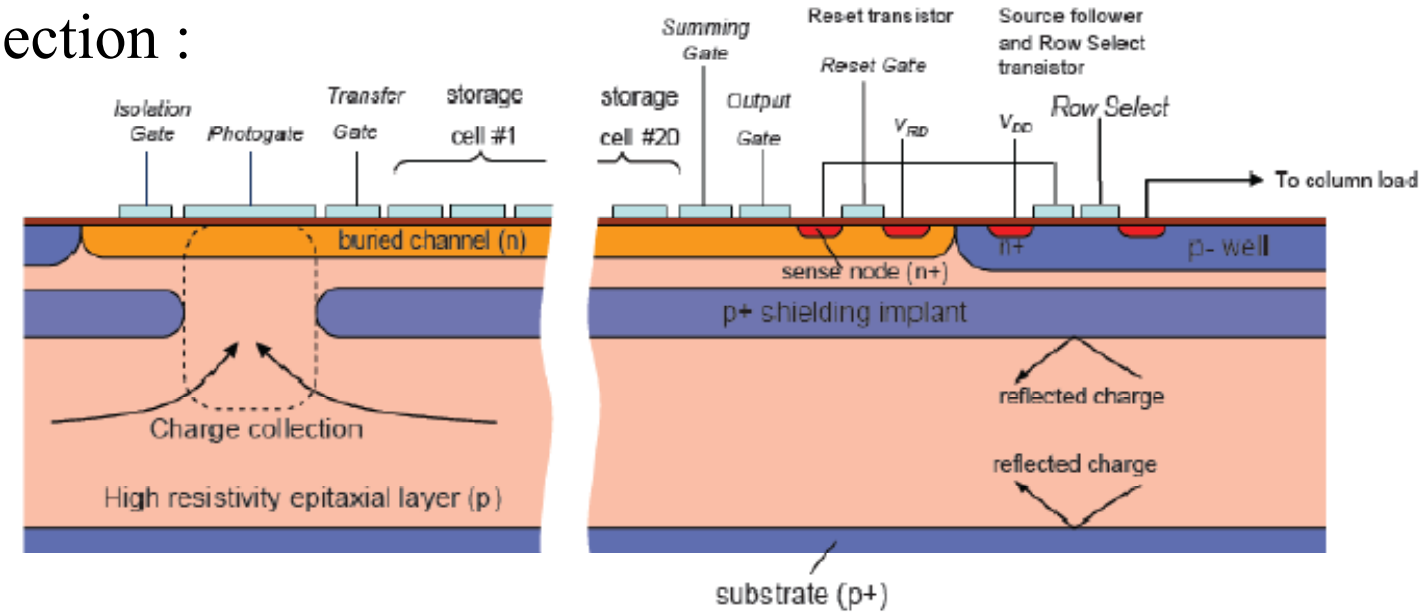
G.Zhang,
T.Jayawardena, RAL

ISIS2

Next generation ISIS: ISIS2

- ISIS2 manufactured by Jazz Semiconductor

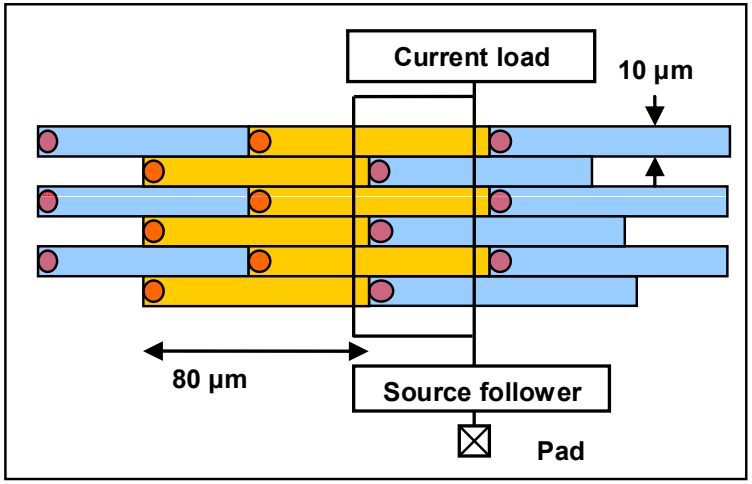
- Process: 0.18 µm with dual gate oxide
  - p++ wafers with 25 µm epi layer ρ > 100 Ohm cm
- Process enhancement for LCFI: buried channel and deep p+ implant
  - Buried channel is necessary for raw charge storage
  - Deep p+ protects buried channel from parasitic charge collection
- Cross section :

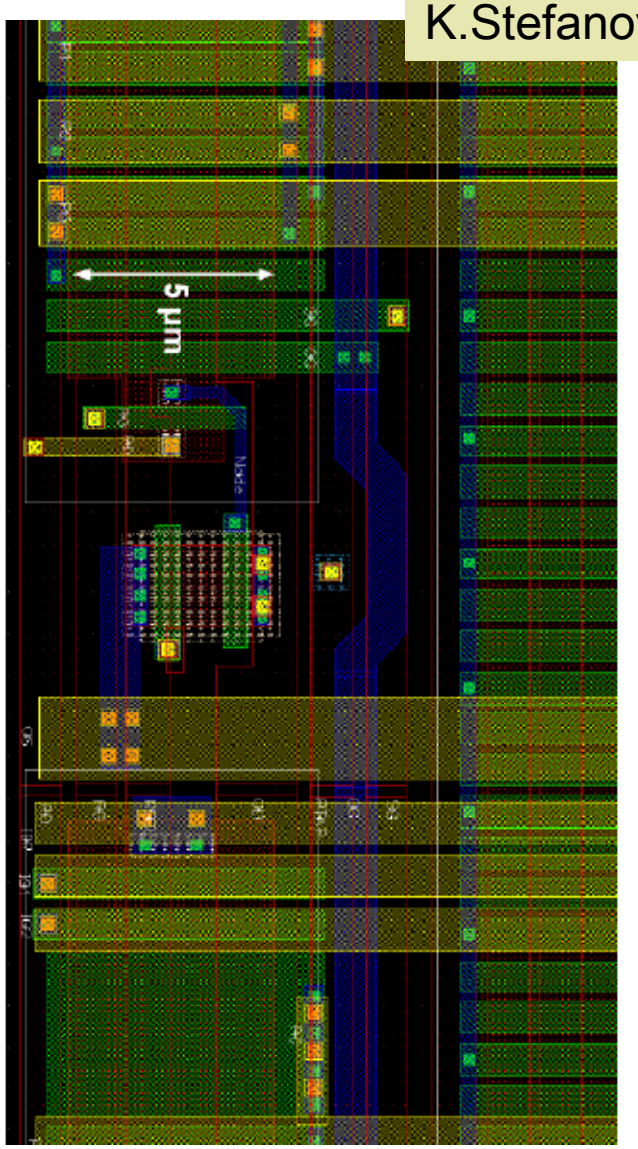


ISIS2 Design

S.Thomas,
P.Murray,
K.Stefanov, RAL

- Pixels 80 x 10 μm^2
- Imaging pixels 40 x 20 μm^2
- Buried channel 5 µm wide
- CCD gates: doped polysilicon, non-overlapping
- Logic, source followers use 5V custom logic gates, 3 metal layers

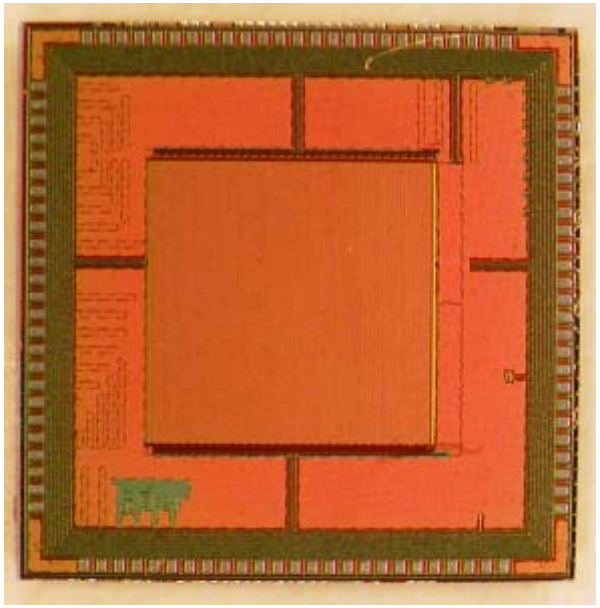


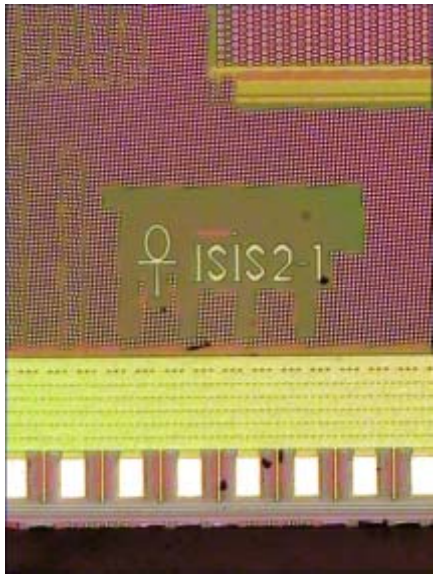


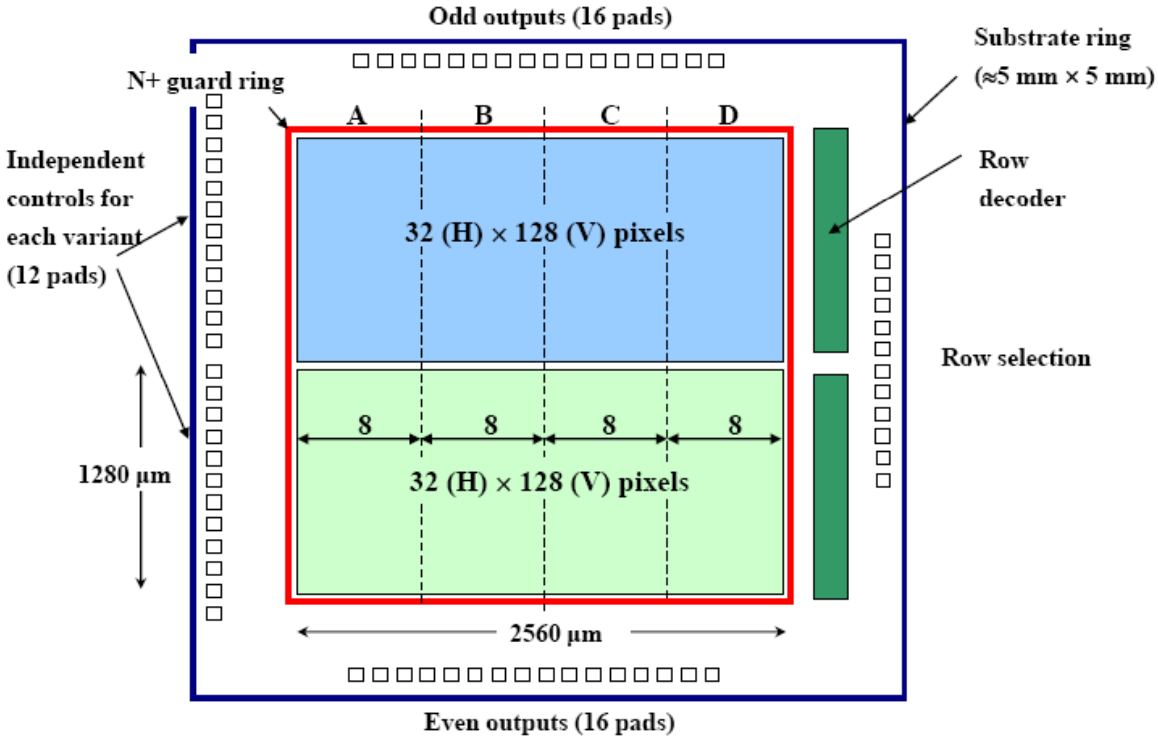
ISIS2 Design

- One chip will have several variants of ISIS2
  - Each has independent control
- Row select and decoder edge logic
- Area 1 cm^2 (four 5x5 mm^2 tiles)

- Submitted in May 2008, delivered last week, being packaged







Summary

- CPCCD demonstrated
  - Operation at 45 MHz, low noise operation at 30 MHz
  - Operation with readout chip CPR2 at 9 MHz, new chip CPR2A is a success
  - Improved CPCCD, CPC-T, are under test

- Raw charge storage demonstrated
  - Proof of concept ISIS1 tested in beam
  - Started testing of ISIS2 based on 0.18 um CMOS process

- Future of UK silicon pixel R&D :

  New proposal SPIDER (Silicon Pixel DEtector R&D)
  - Continue ISIS program
  - Develop MAPS based on 4T process and INMAPS process (deep p+ protective layer)