SiD ECAL/HCAL/Muon/Tracker System Using KPIX

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Overview Of KPIX Front End



- * KPIX ASIC electrically connected to sensor
 - Die bump bonded directly to Si based sensors (ECAL & Tracker) Packaged die with short cables for other sensor types (HCAL & Muon)
- * Level 1 concentrator provides services required by KPIX
 - Configurable clock generation
 - External trigger generation (diagnostics)
 - Outgoing serial command stream generation
 - Incoming data stream processing including zero suppression & timestamp sorting
 - Power conversion
 - Interfaces to level 2 or ATCA crate via high speed fiber optic link
- * Level 2 concentrator combines data streams from multiple level 1 concentrators
 - Required when level 1 output does not fully saturate fiber optic link
 - Provide second level of timestamp sorting
- * ATCA based processor board to process and switch data packets
 - Interface to control system & online storage

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- * KPiX is a multi-channel system-on-chip, for self triggered detection and processing of low level charge signals. Motivated by the Silicon Detector (SiD) for the International Linear Collider (ILC).
- * A common external trigger can be enabled for test-beam and other applications.
- * A digital core controls all operations according to parameters stored during set-up. This allows to match the chip to signals from a variety of sources.
- * Digital core allows for reduced signal count to/from KPIX
 - 3 LVCMOS lines idle during noise sensitive acquisition: Command, Reset, Data Out
 - 2 LVDS pairs active during acquisition: clock & trigger input (trigger inactive for most applications)
- * Low average power consumption (<20 μW per channel) for ILC operation is obtained by powering down between beam spills.
- * Designed to be bump bonded to a Si-sensor, or to a hybrid for large area detectors (RPC's, GEM's). This avoids an extensive cable plant for the detector signals, resulting in significant savings in cost for large systems.
- * Full sized chip is an array $32 \times 32 = 1024$ channels. Current prototypes are 2x32 = 64 channels, laid out in 0.25μ m TSMC technology.
- * Range- and Noise-Specifications:

Peak Signal (Dual Range) 10 pC.

Range Switching (selectable) ~400 fC.

Noise Floor 0.15 fC (1000 electrons).

KPIX Charge Amplifier Block

- * The incoming signal is picked up by the charge amplifier and stored in the feedback capacitor (default ranges 200 fF and 400 fF).
- * If the default range is exceeded, a 10 pF capacitor is automatically added to the feedback to extend the range to 10 pC.
- * For negative-polarity signals, an inverter is inserted after the charge amplifier. The polarity of the calibration signal is reversed too.
- * For DC-coupled signals, the leakage is compensated by a servo circuit. The amount of leakage is determined with no signal present and held during the signal period.
- * A precision calibrator sends up to four signals with amplitudes and timings as defined during the set-up cycle.
- * Digital reset during power-up and after each triggered event. Can be executed before each beam bunch for ILC operation.
- * Option for DC reset for non-bunched signals, e.g. cosmic rays, radioactive source data.
- * Periodic and digital resets are inhibited immediately after each trigger (controlled by the acquisition block)..



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KPIX Data Acquisition Logic

- * The charge amplifier signal is amplified, shaped and sent to the trigger stage.
- * For signals above trigger threshold, the digitally controlled acquisition cycle is started. After a wait period, the signal is acquired in the storage capacitor. The coupling elements form a low pass filter (0.5 us time constant).
- * One of two threshold levels is selectable in each cell. High-low discrimination system to catch potential triggers early to inhibit digital and DC resets.
- * For the tracker application, the trigger is carried over to the neighboring cells to catch low level spill-over signals below trigger threshold.
- * After a programmable time interval, the signal amplitude is held in the capacitor and control passed to the next storage capacitor.
- * The integration interval is thus precisely controlled, resulting in a stored amplitude proportional to the signal, even if the asymptotic value is not reached.
- * A strobe signal is sent to the memory block to record event time.
- * Amplitude and time information for up to four events can be stored for each data cycle.



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KPIX ADC and Digital Storage

- * The analog information previously stored in 4x1024 capacitors is digitized in four cycles, each for 1024 capacitors in parallel.
- * The Wilkinson method is used for the conversion, with a current mirrored into each cell running down the charge in the storage capacitor. A rampthreshold discriminator detects the transition through zero and causes the content of a common Gray counter to be stored in memory.
- * The ADC has 13 bits resolution.
- * This method of digitization could proceed independently in each cell, offering the possibility of DC operation. The four buffers in each cell could be filled and read out on a rotating basis. This would require a major upgrade of the digital core.



KPIX Measurement Results



- * Measured noise in 64 cells set to high gain mode. ADC branch high-lighted in yellow, trigger branch open boxes.
- * The noise in the trigger branch is determined by recording the trigger rate as function of threshold in each of 64 cells and fitting an error function to the data points.
- * Most cells are below the specification of 1000 electrons (0.15 fC).



Sid E-CAL Application



SiD Tracker Application

- * Two KPIX ASICS support each tile
- * Standard fixed length cable bonded to each sensor
- * Variable length cable routed between common cable and level 1



Si-Tracker and KPiX in SLAC Test-Beam

- * Three CDF sensors (128 channel) were arranged in layers of vertically oriented strips.
- * The data were taken in a SLAC test-beam of 10 GeV e-.
- * A synchronous trigger signal 1 ms before beam pulse was used to power-up KPiX.
- * An external forced trigger at the correct beam time served as a common data strobe.
- Plotted are double-coincidence clusters of strips (only 15% >1 strip).
- * The fitted curve is a Landau distribution convoluted with a Gaussian (noise).



Sid Muon Application



- Low input count allows for wire bonding
 Hybrid package can also be used
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- RPC strips electrically connected to traces on interface board Interface board contains additional protection circuitry Dual polarity feature of KPIX utilized to readout either side of RPC Cable provides command, clock, reset, test trigger, data readout & power Concentrators at the ends of the cables combining data from several RPC * interface boards

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Signals from Resistive Plate Chambers in KPiX SLAC

- The plot shows Cosmic Ray data in an RPC connected to KPiX.
- * Data taken by H. Band of the Univ. of Wisconsin.
- * The RPC's are running in avalanche mode.
- * The signal peaks at 3 pC.
- * The spike at zero is attributed to tracks missing the RPC.
- * The plot shows the noise distribution without a signal in the RPC.
- * The variance is 29 fC, to be compared to the expected noise of <10 fC.
- * The difference may be due to pick-up.





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SiD H-Cal Application



- GEM array board consists of 20 x 50 array of 1cm square pads Array board serves as low voltage side of GEM chamber 2 x 5 grid of array boards form 1 meter square array of 10K pads 1024 channel KPIX mounted on GEM array board in hybrid package Array board contains additional protection circuitry Negative polarity feature of KPIX utilized for GEM signals *
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- * Cable provides command, clock, reset, test trigger, data readout & power Concentrators at the ends of the cables combining data from several GEM array boards

SiD GEM Testing





KPIX Test Setup





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KPIX Test Setup Expansion



- Development board allows connection to multiple KPIX FPGA boards Fiber optic interface to control system Raw Ethernet for connection directly to PC PGP for connection to DAQ system in ATCA crate * *

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- * A 64-channel KPIX prototype of the projected 1024-channel device has been tested and found to meet specifications.
- * The transition to the full size KPIX chip is planned in two steps, 256 and then 1024 channels, mainly to save on prototype fabrication costs.
- Testing of KPIX 64 wire bonded to Tracker test sensor will be performed in the coming weeks.
- * Channel count of RPC test structure is currently being increased.
- Testing of KPIX 64 wire bonded to E-Cal sensor will be performed in the coming weeks.
- * Testing with new GEM chamber currently in progress.
- * Throughput of prototype DAQ system being improved in order to support 8-16 KPIX devices in test structure.