LCWS 2008 Data Acquisition and Global Detector Network

SiD ATCA DAQ System

Matt Weaver, weaver@slac.stanford.edu
SLAC National Accelerator Laboratory
November 18, 2008

Representing:
Mark Freytag
Gunther Haller
Ryan Herbst
Michael Huffer
Chris O'Grady
Amedeo Perazzo
Leonid Sapozhnikov
Eric Siskind

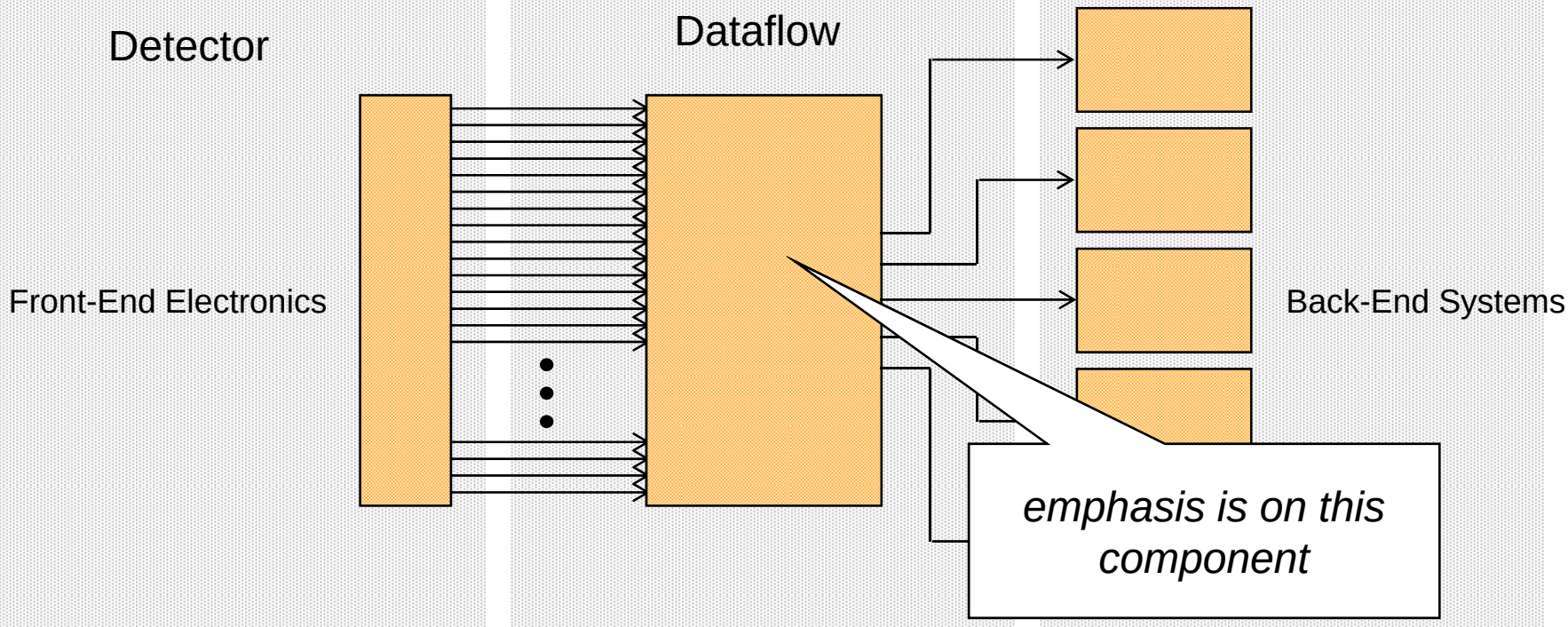
Talk based largely on
Huffer, et al., "A new proposal for the construction of high speed, massively parallel, ATCA based Data Acquisition Systems," *IEEE 2008 Nuclear Science Symposium.*

Represents development work done at SLAC for the following projects:
PetaCache, LCLS, LSST

Outline

- Modular DAQ design to address new projects
- ATCA demonstration boards
  - Reconfigurable Cluster Element
  - Cluster Interconnect Module
- Example application to SiD

Abstract HEP Data Acquisition System

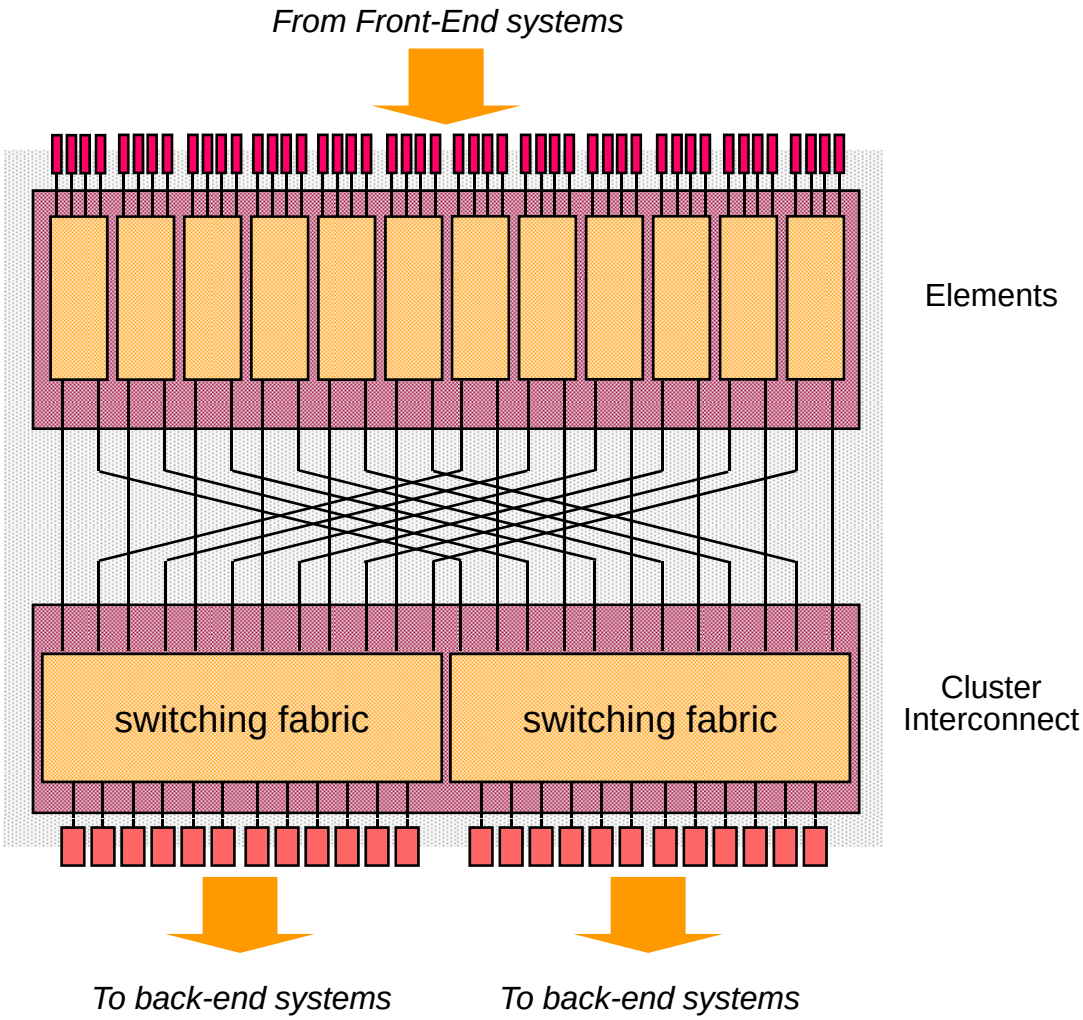


- Analog shaping
- Digitization
- Transmission
- Trigger pipeline buffering
- Charge injection

- Feature Extraction
- Compression
- Re-formatting
- Event buffering
- Aggregation
- Reception & Transmission
- Protocol conversion

- High-Level Triggering
- Event-Building
- Archival
- Data Quality Assurance

A *cluster* of 12 elements



Typical (5 slot) ATCA crate

Front

fans

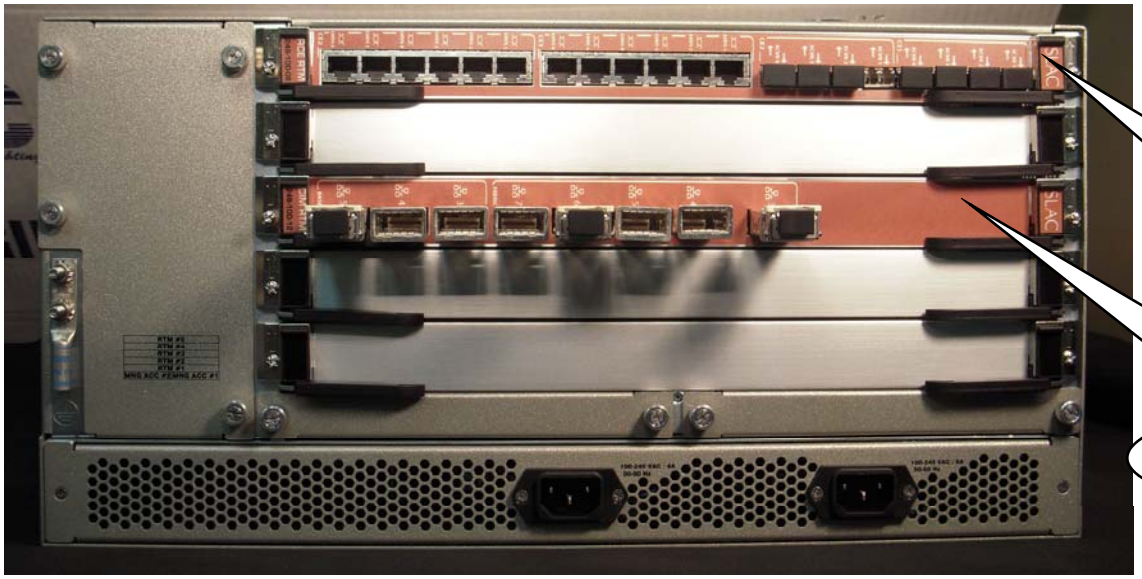
"element" board

Shelf manager

"interconnect" board

Power supplies

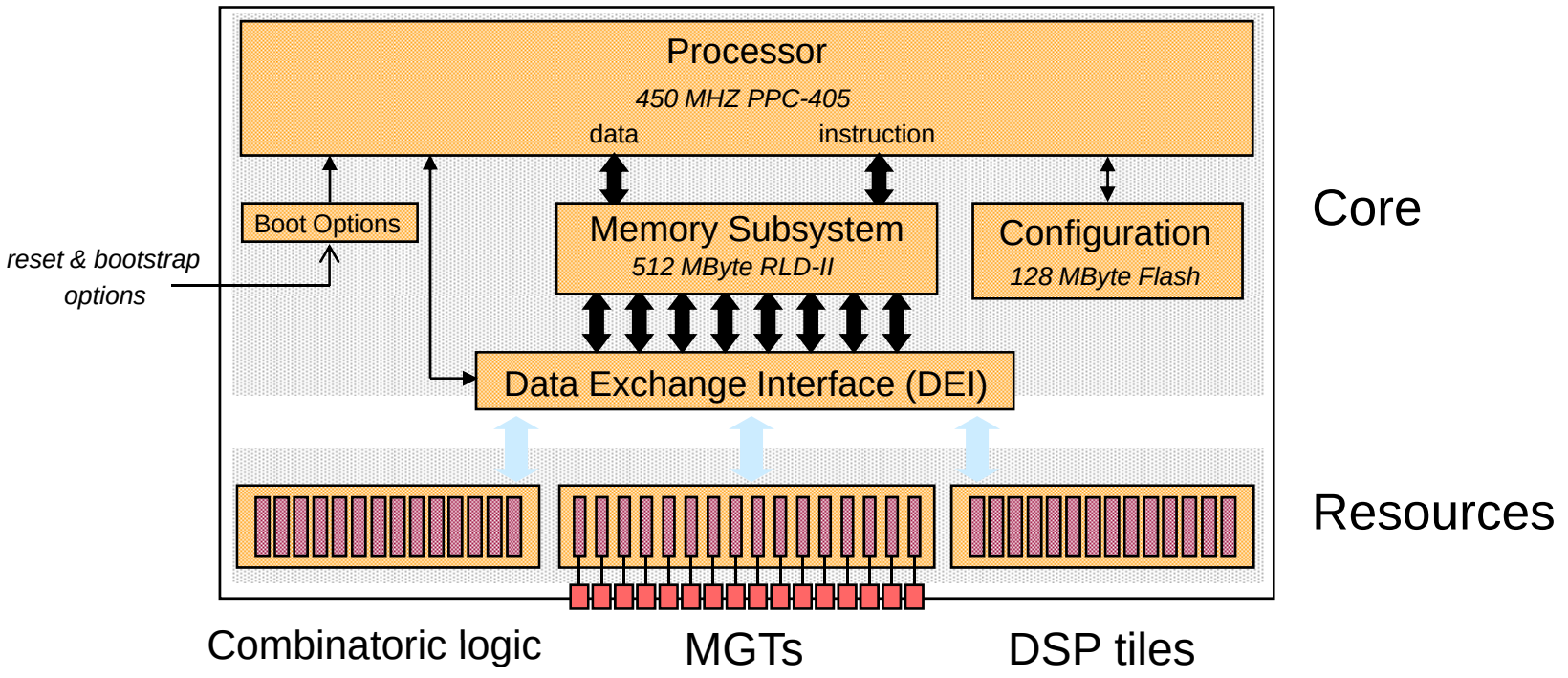
Rear



"front-end" I/O

"back-end" I/O

(Reconfigurable) Cluster Element (RCE)

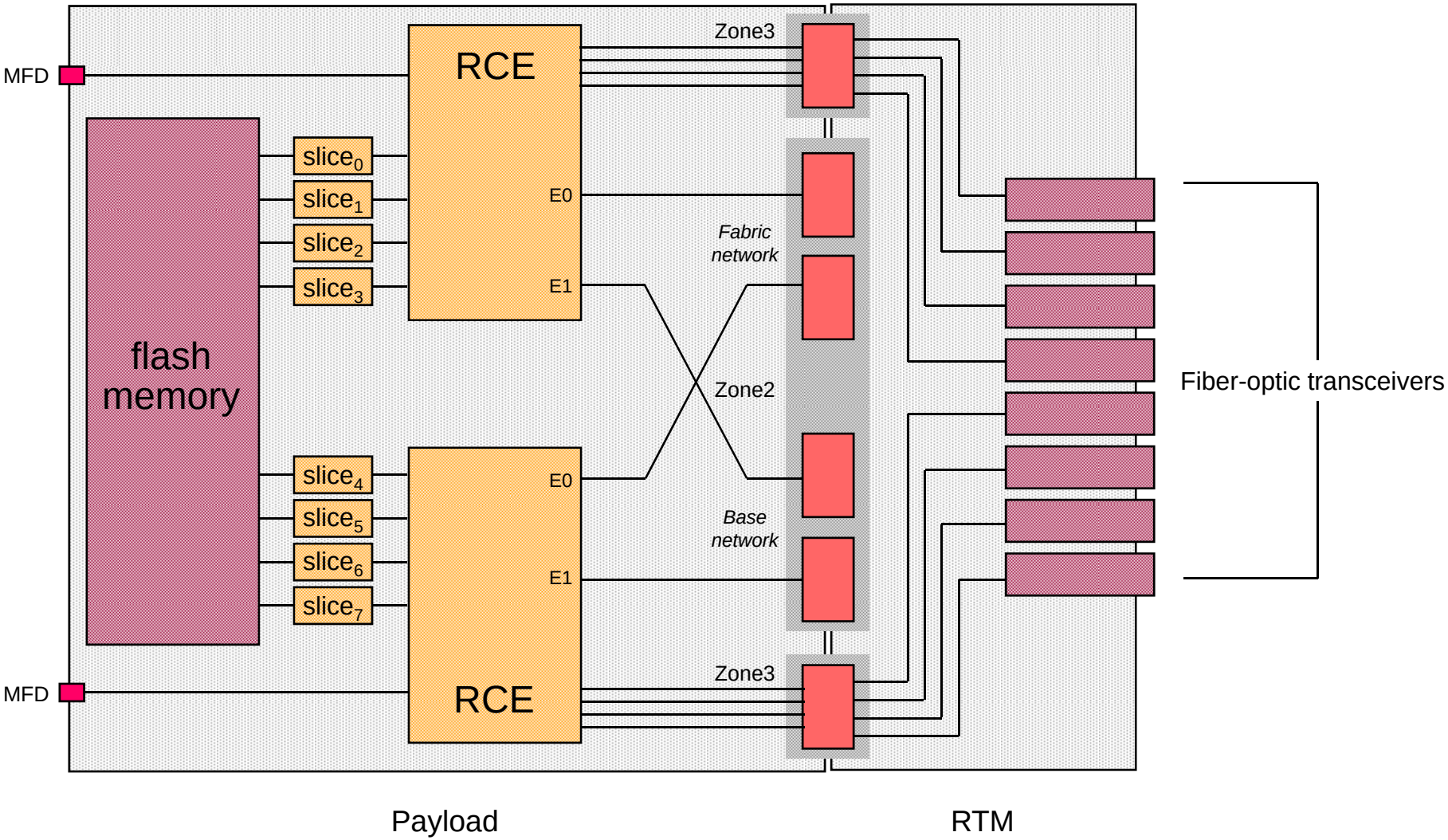


- Bundled software:
  - GNU cross-development environment (***C & C++***)
  - remote (network) GDB debugger
  - network console
- Bundled software:
  - bootstrap loader
  - ***Open Source*** kernel (RTEMS)
    - POSIX compliant interfaces
    - standard I/P network stack
  - exception handling support
- Class libraries (***C++***) provide:
  - DEI support
  - configuration interface

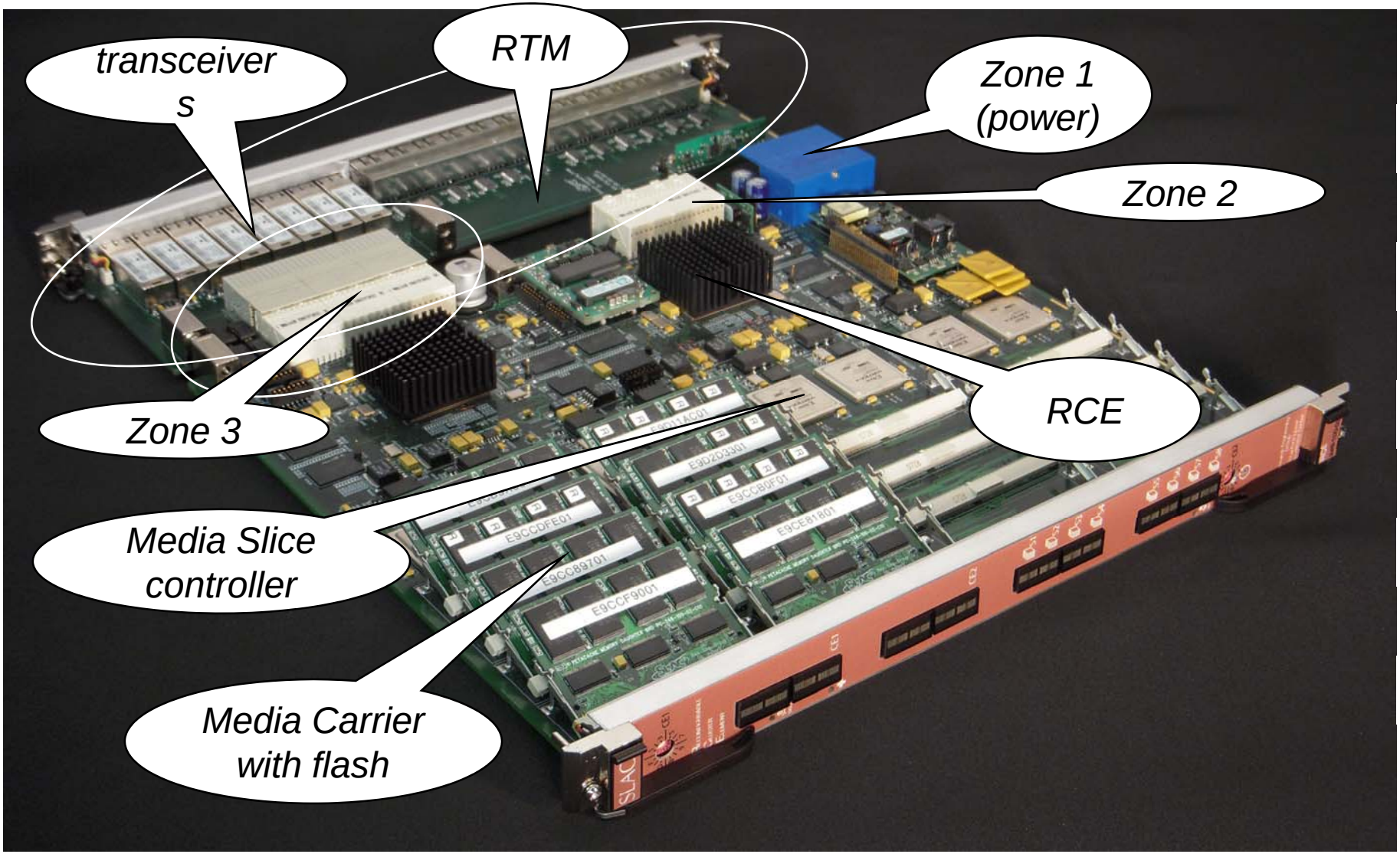
Resources

- Multi-Gigabit Transceivers (MGTs)
  - up to 24 channels of:
    - SER/DES
    - input/output buffering
    - clock recovery
    - 8b/10b encoder/decoder
    - 64b/66b encoder/decoder
  - each channel can operate up to 6.5 gb/s
  - channels may be bound together for greater aggregate speed
- Combinatoric logic
    - gates
    - flip-flops (block RAM)
    - I/O pins
- DSP support
  - contains up 192 Multiple-Accumulate-Add (MAC) units

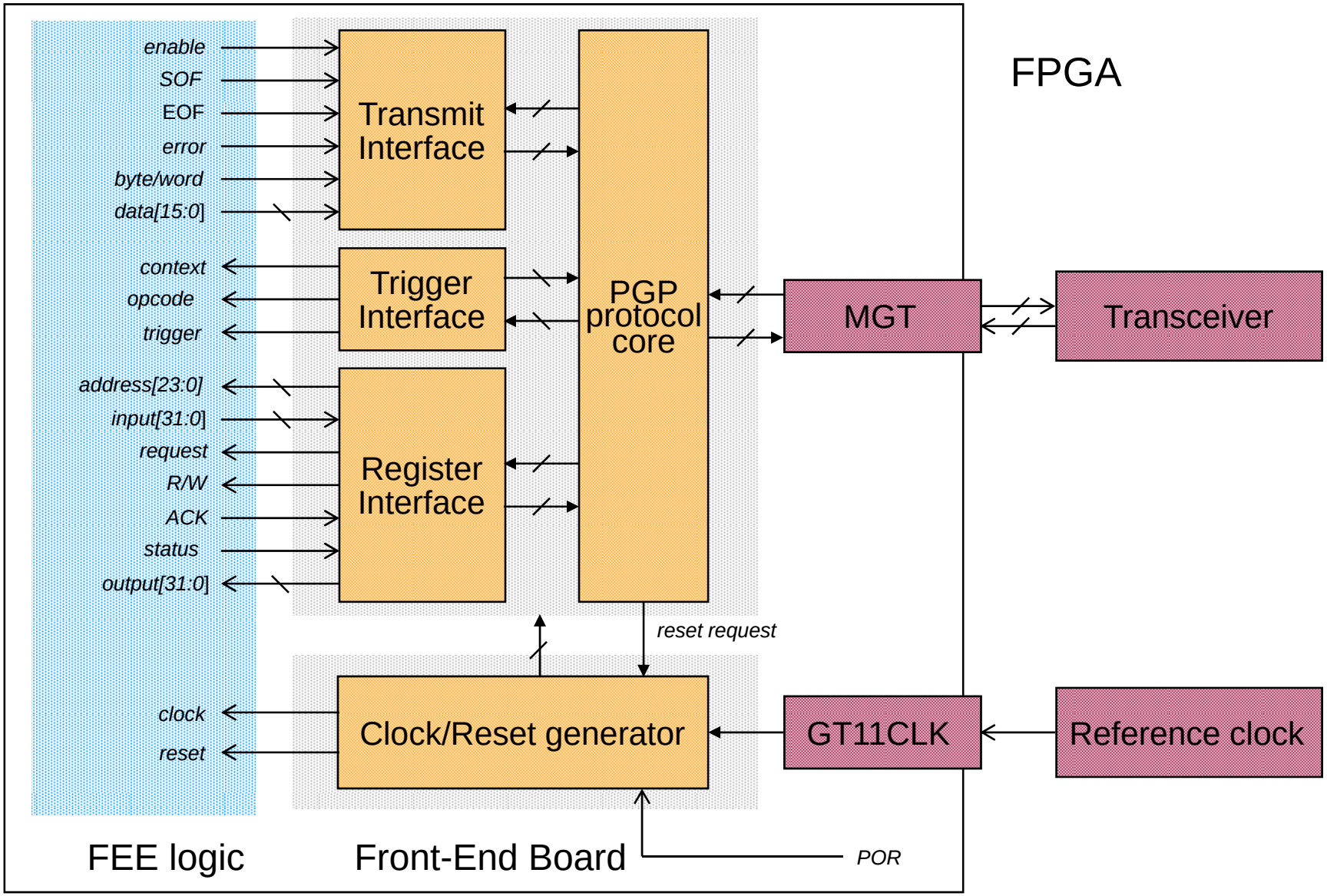
RCE board + RTM (Block diagram)



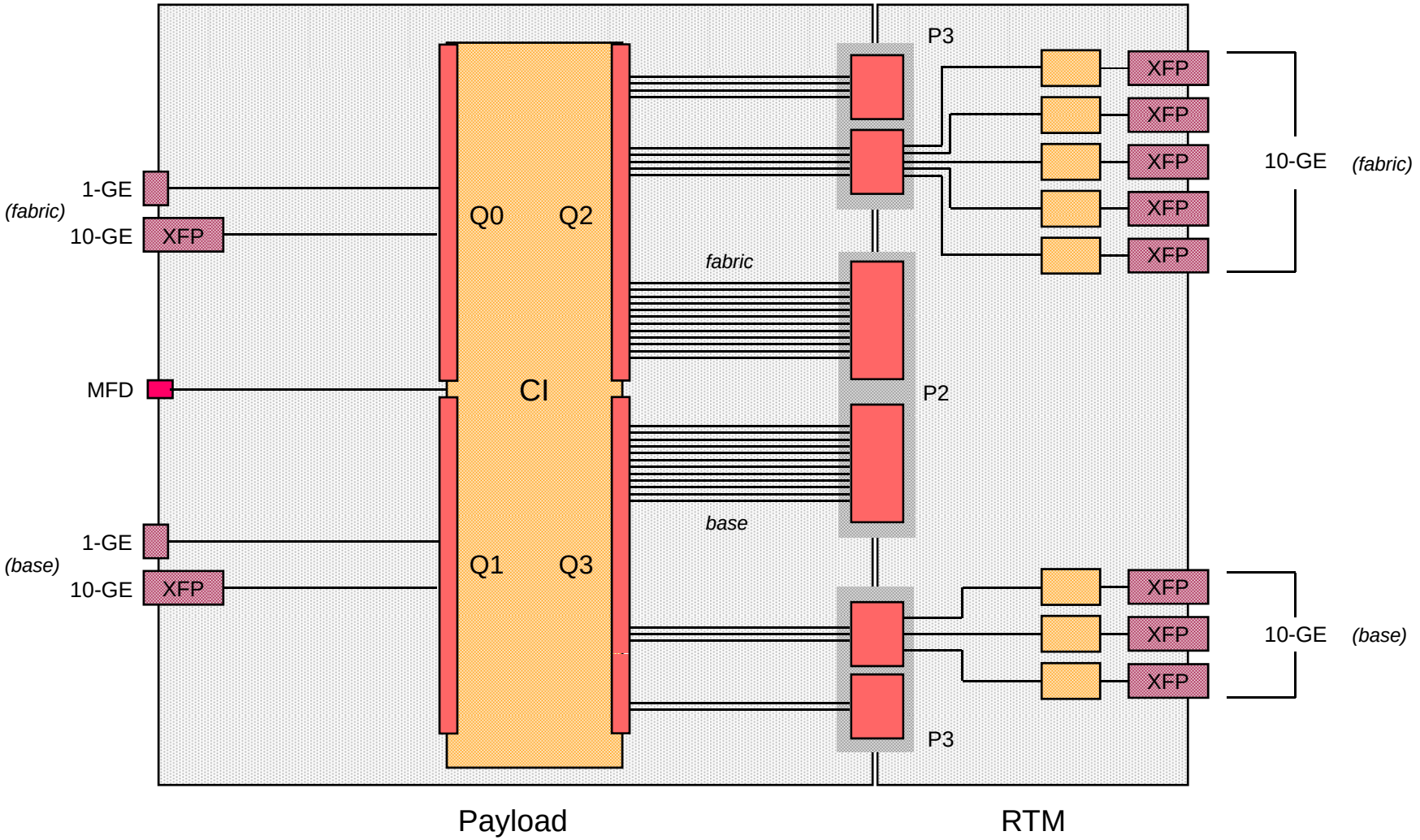
RCE board + RTM



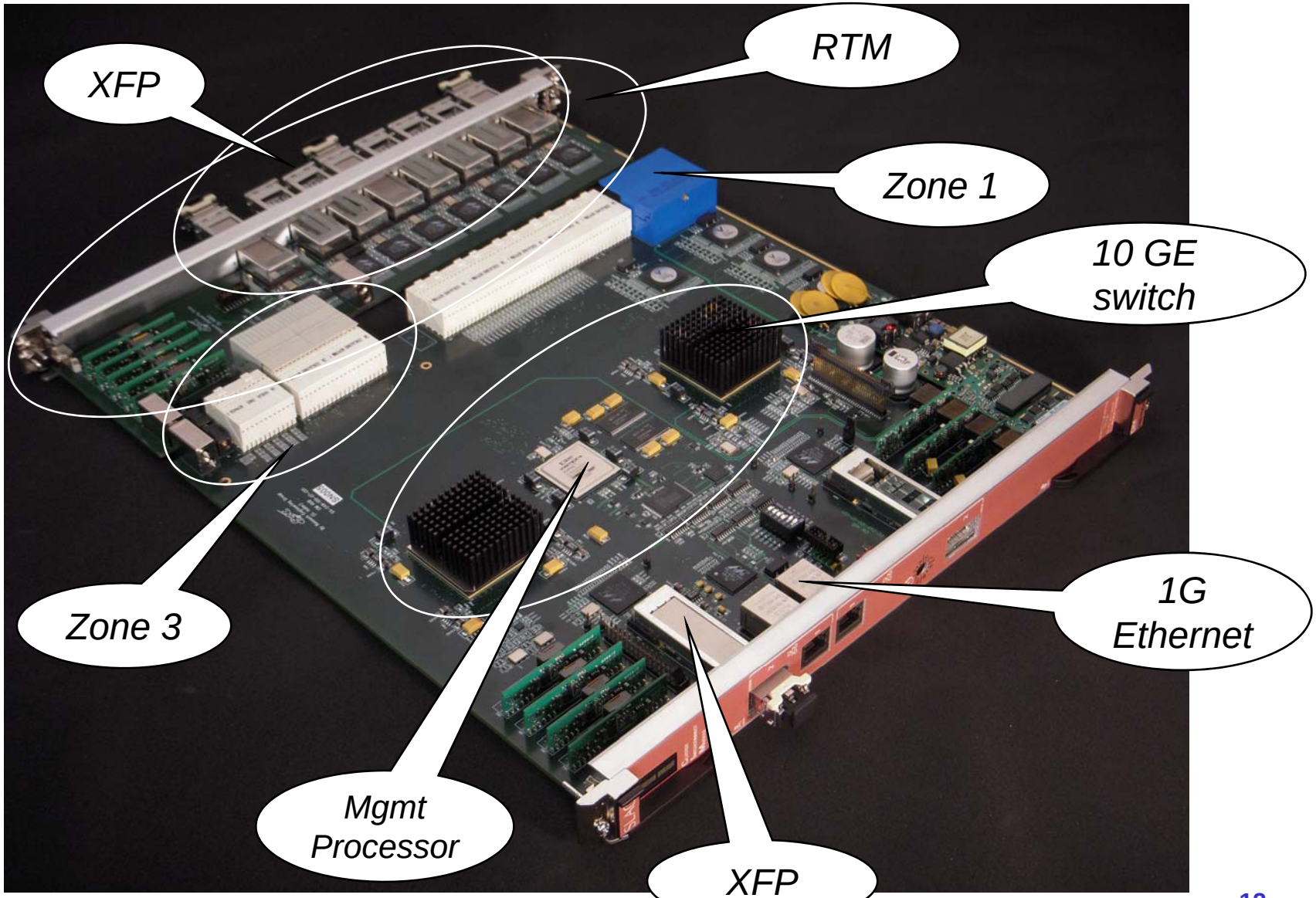
Front-end Interface Example



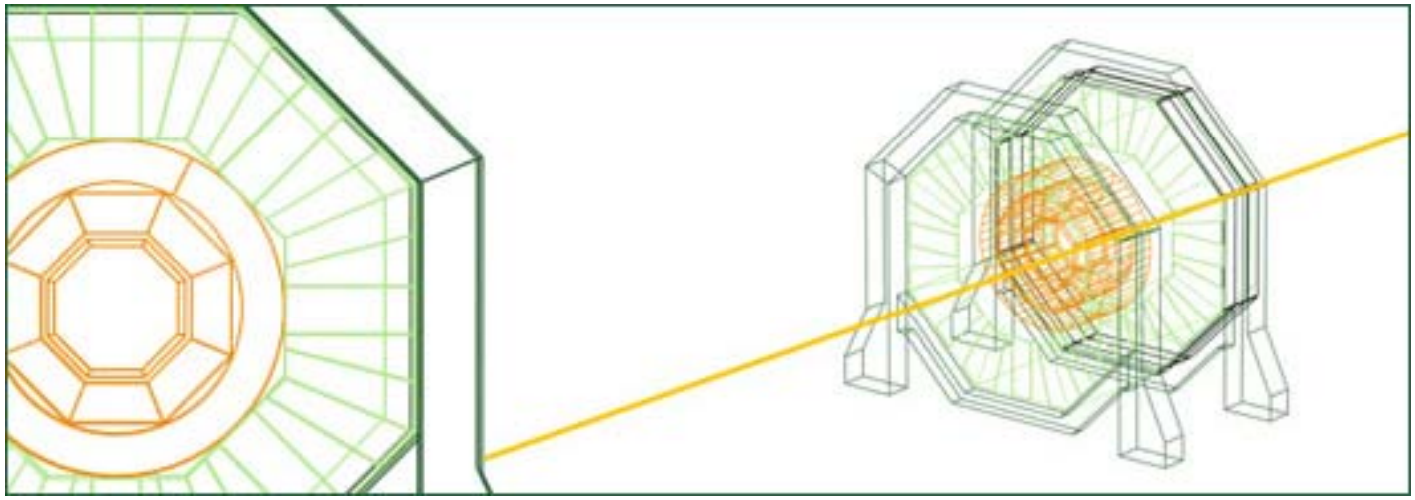
Cluster Interconnect board + RTM (Block diagram)



Cluster Interconnect board + RTM

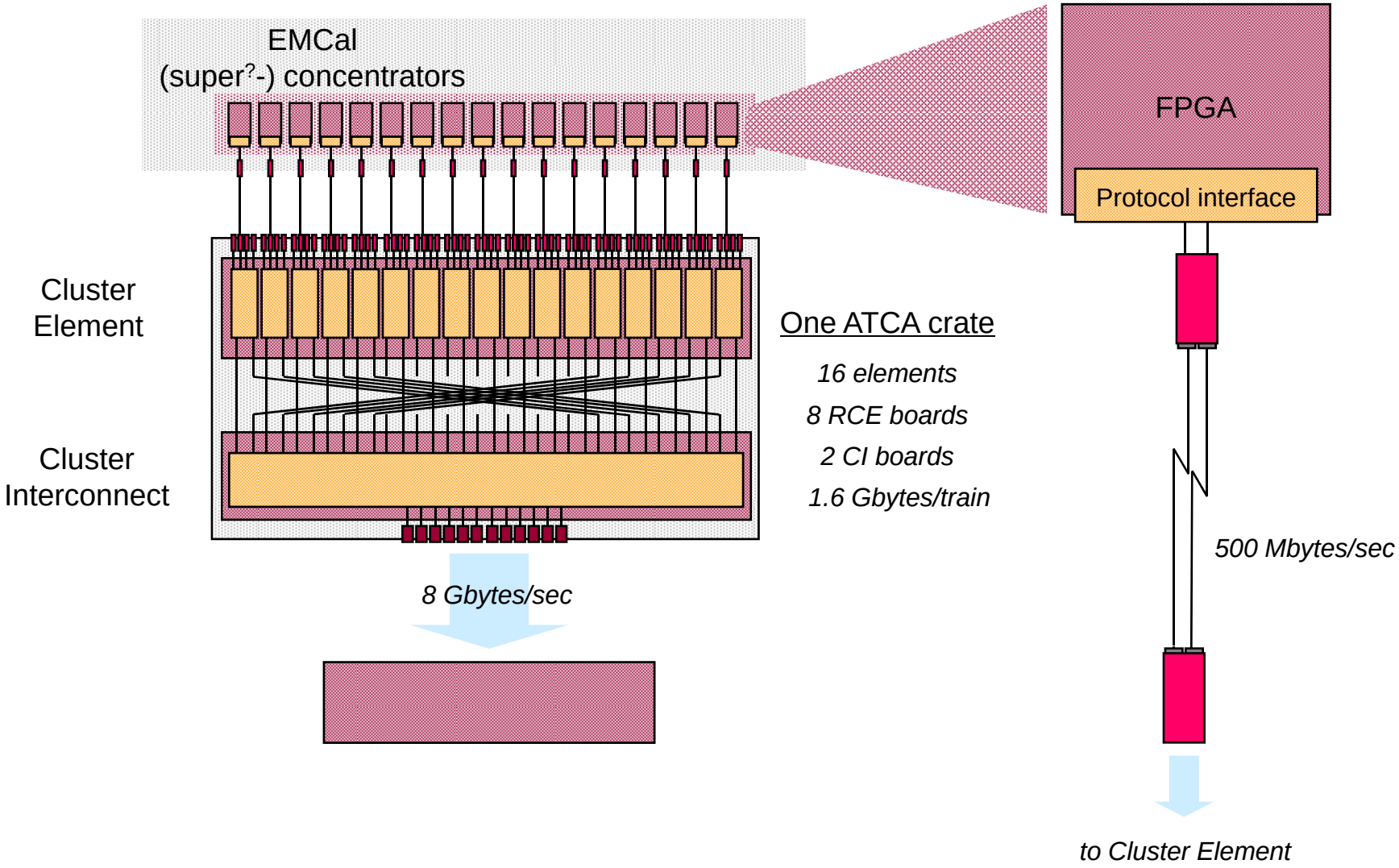


SiD Data Acquisition



- EMCal example
  - ~100M channels
  - 4bytes/hit x 4hits/train (KPiX)
  - readout in 100ms (1/2 of inter-train spacing)
  - EMCal total readout data rate ~ 128Gbps

SiD DAQ continued…



Status

- SLAC is positioning itself for the production of a new generation of DAQ systems
  - strategy is based on the idea of modular building blocks
    - inexpensive computational elements (the RCE)
    - interconnect mechanism (the CI)
    - industry standard packaging (ATCA)
- Architecture is now relatively mature
  - both demonstration boards (& their corresponding RTMs) are functional
    - RTEMS ported & operating
    - network stack fully tested and functional
  - performance and scaling have been demonstrated to meet expectations
- Current focus is on applications using these concepts…
  - LSST DAQ
  - LCLS DAQ
  - ***PetaCache*** project
- Application of same boards to SiD DAQ could yield a compact yet scalable system.