

# **Overview of the SiLC R&D activities**

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*LCWS08, University of Illinois at Chicago,  
November 19<sup>th</sup> 2008*

# Synopsis

- R&D on sensors
- R&D on Electronics
- R&D on Mechanics and Integration (LOIs)
- Simulation studies (LOIs)
- Lab test benches and test beams activities

***Latest results, highlights and where we go from there.***

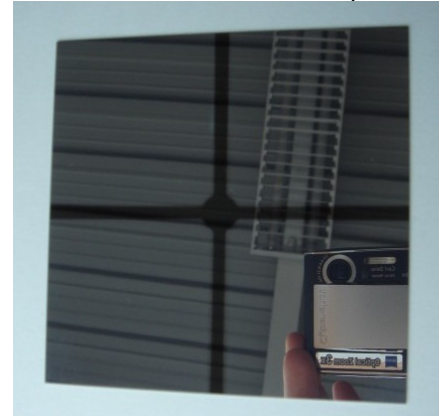
***SiLC is a generic R&D collaboration (transversality)***

***Thus it serves several detector cases: main involvement in ILD, starting to be contacted by 4<sup>th</sup> concept, “natural” interest in SiD.***

# R&D on sensors

## **Microstrips = the short term baseline**

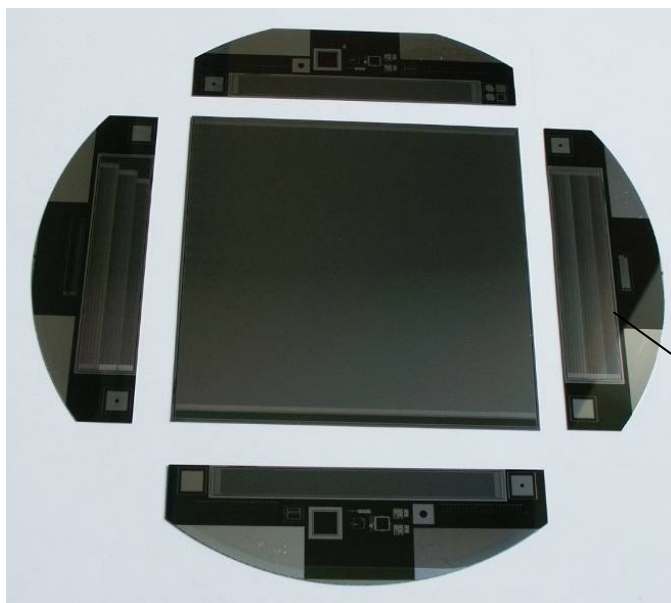
**Today:** HPK 6", 50  $\mu\text{m}$  pitch, 320  $\mu\text{m}$  thick, delivered end 2007, include sensors specially treated for alignment;  
Fully tested at Lab test bench and test beam  
(see S. Haensel talk)



**Short term:** Look for other vendors and even more performing strip detectors: edgeless (CANBERRA S.A.)  
Continuing with HPK for thinner large wafers  
And novel technology: 3D planar (VTT, IRST and CNM)

## **Go to pixel technology** (longer term)

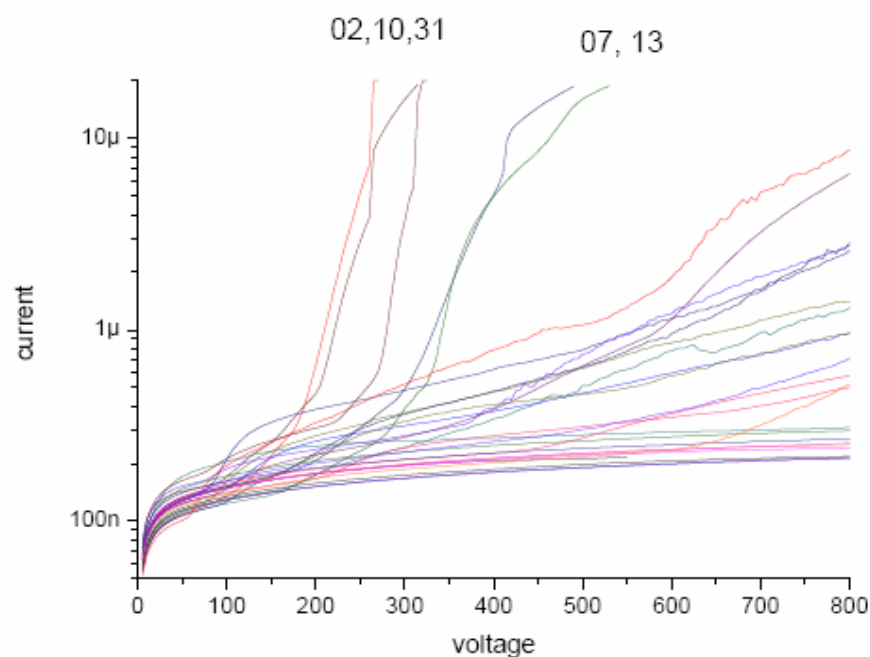
- => Presently DEPFET (IFIC-Valencia), LMB-pixels (Low Material Budget) also a 3D technology (OSU)
- => Pursue on 3D pixels and 3D vertical interconnect



# HPK strip sensors

*with test structures a la CMS*

*Fully tested on dedicated Lab test bench  
At HEPHY- Vienna and IEKP Karlsruhe*

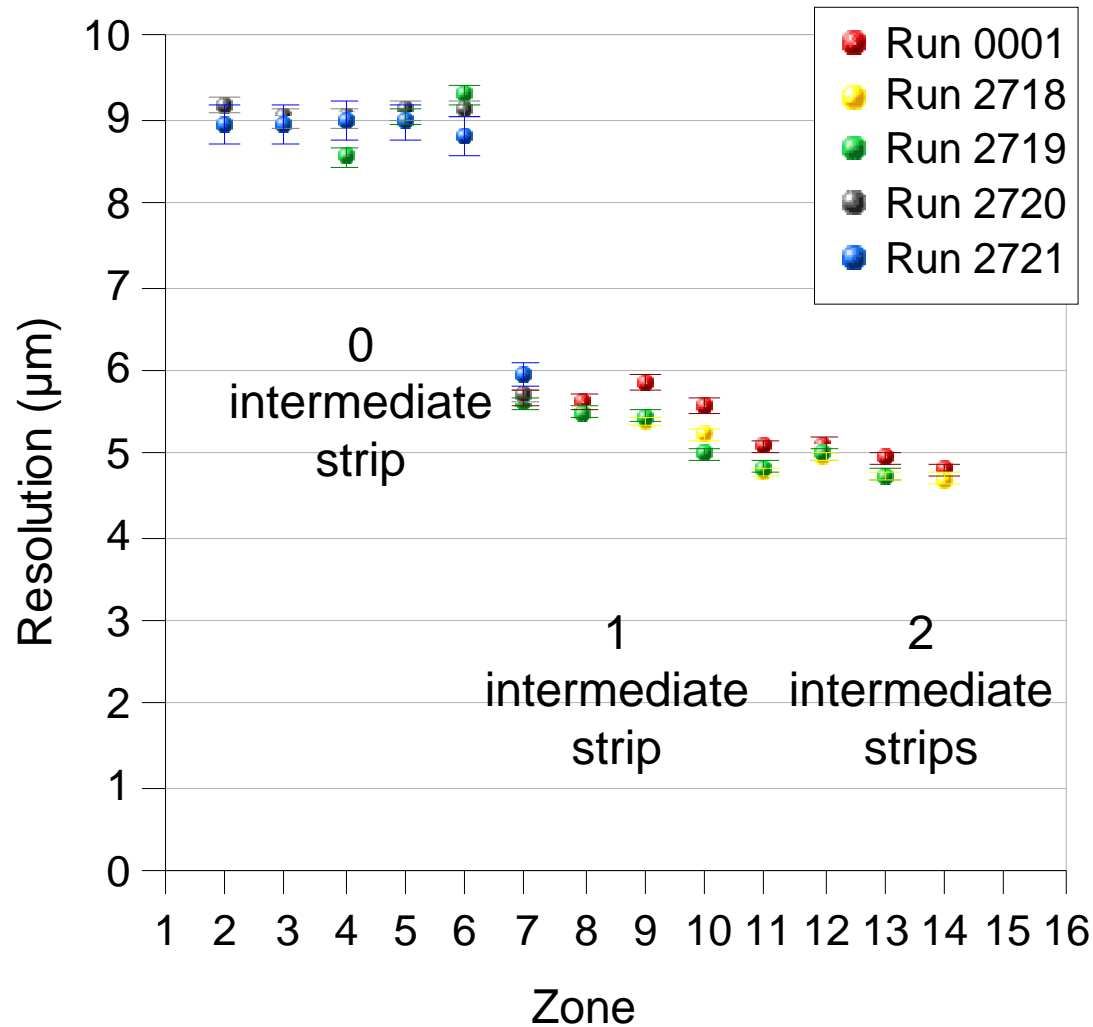


TESTAC:

strip width [μm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

# Spatial resolution vs strip geometry

(Result from test beam  
with test structures)



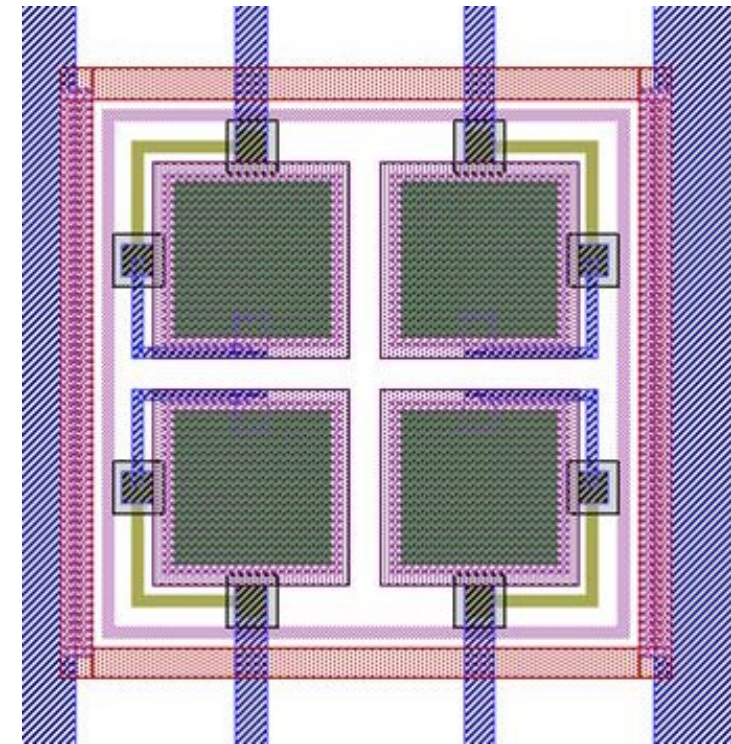
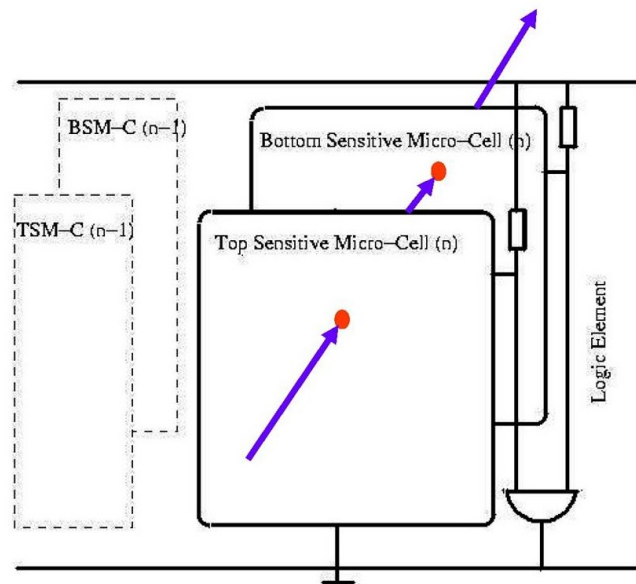
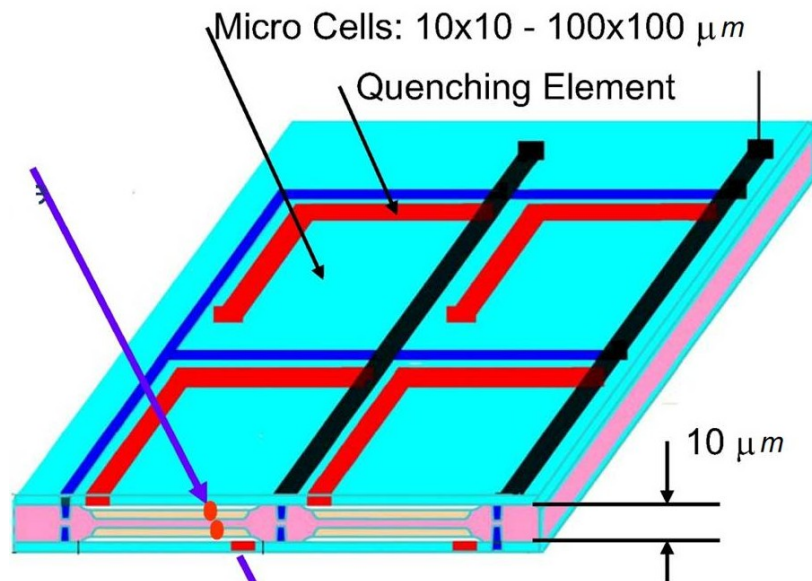
50 μm readout pitch strip

**Interesting result:**

**9μm resolution** if no  
intermediate strip

**5 or 6μm resolution** if 1  
or 2 intermediate strip

# NEW 3D PIXELS: LOW MATERIAL BUDGET & HIGH INTRINSIC GAIN (OSU)



Microcells operating @ breakdown mode  
 Gain up to  $10^{**6}$   
 Thickness down to a about 10microns  
 Size of pixels  $10 \times 10$  up to  $100 \times 100 \mu m$   
 Electronics can be implemented onto the detector

# R&D on Electronics

- **FEE**: new FE readout chip produced in 130nm CMOS technology with full functionality (see next talk)  
Will equip all the test beam prototypes  
Next steps: 256 channels elementary blocks, thinning, go to 90nm.
- **Direct connection of the FE chip onto the strip detector by:**
  - => **bump bonding**, now, with new HPK & SiTR\_130-88
  - => **3D vertical interconnect**: longer term & global effort
- **DAQ Electronics**: starting to develop an overall electronics chain to fully process the Silicon tracking data, using the test beams as training camp.  
Major step forward this year by developing an overall standalone tracking system (see next & talk at the DAQ session)

# R&D on Mechanics

- **Alignment** (essential input for Physics studies)  
Two cases: alignment of a system of Silicon trackers (IFCA)  
alignment in the case of a single layer (ex SET)
- **New modules and light support structures**
- **Mechanics for the test beams**: 3D table, thermal & electrical envelope (see next)
- **Integration**:  
Most of the ongoing work is on the ILD integration of the Silicon system proposed by SiLC ((SIT, SET) + (FTD , ETD))  
Example: very preliminary studies by Torino on SET detector (see next)

Driving schedule: test beams and LOIs

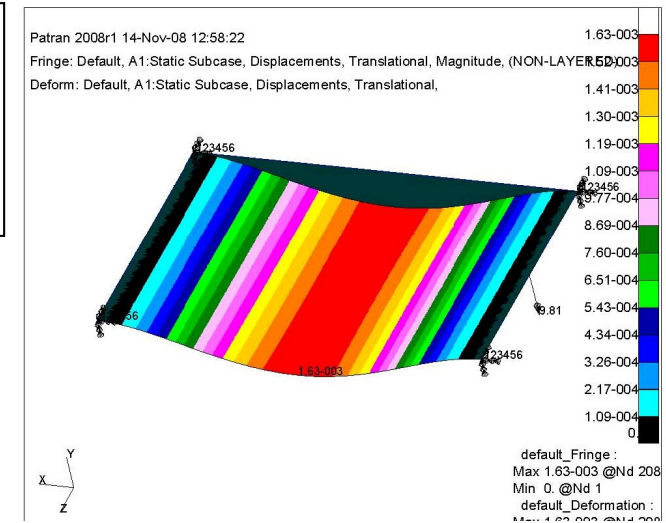
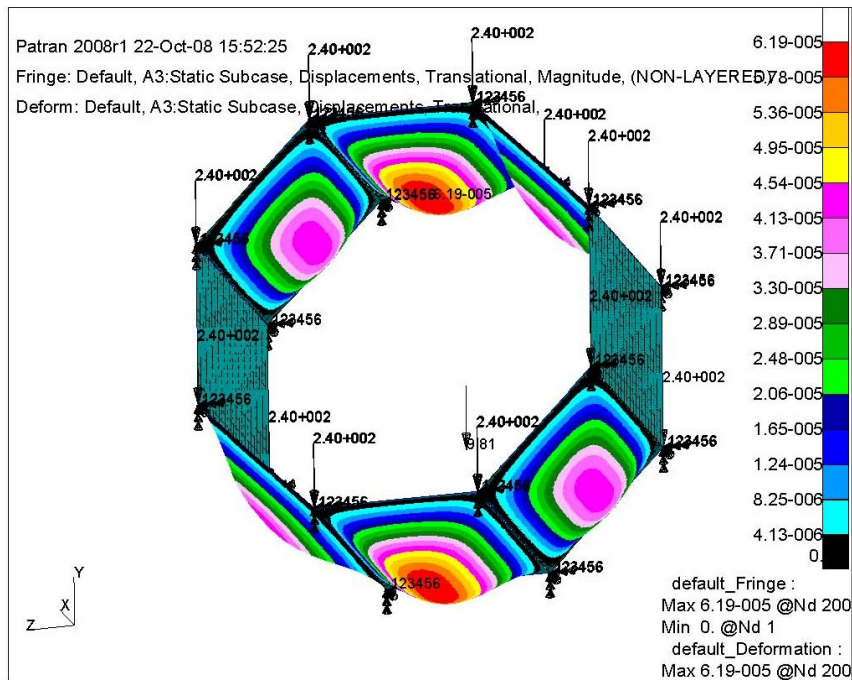
Driving parameters: Lightness, robustness, simple to construct



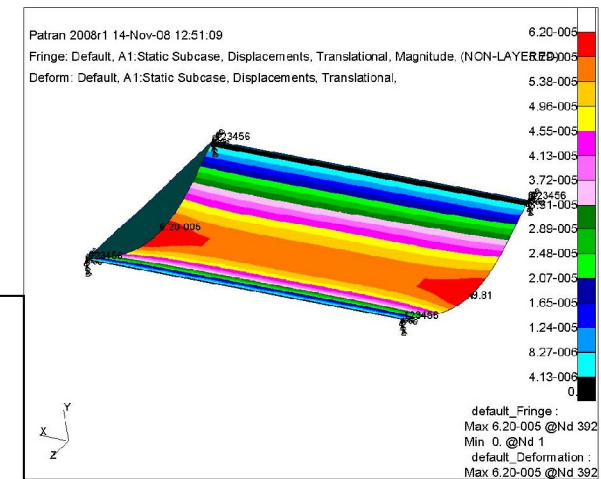
# SET mechanical structure

constrained on short sides;

- 8,9 kg dead load;
- 3 kg payload.
- **MAX deflection: 1,6 mm**



## STATIC DEFLECTION OF ONE PANEL



constrained on long sides;

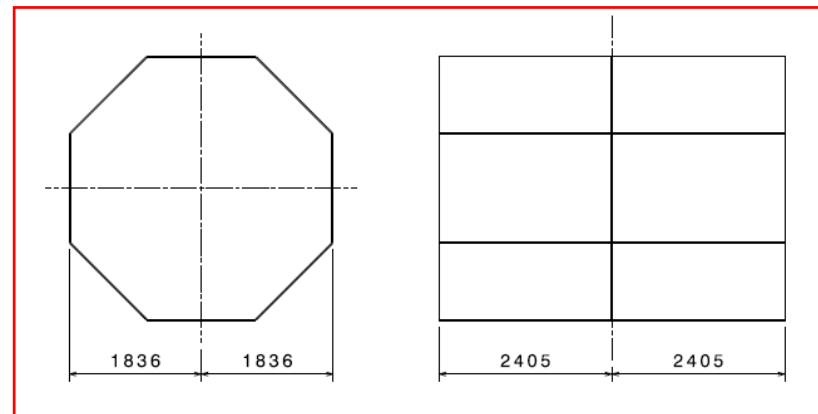
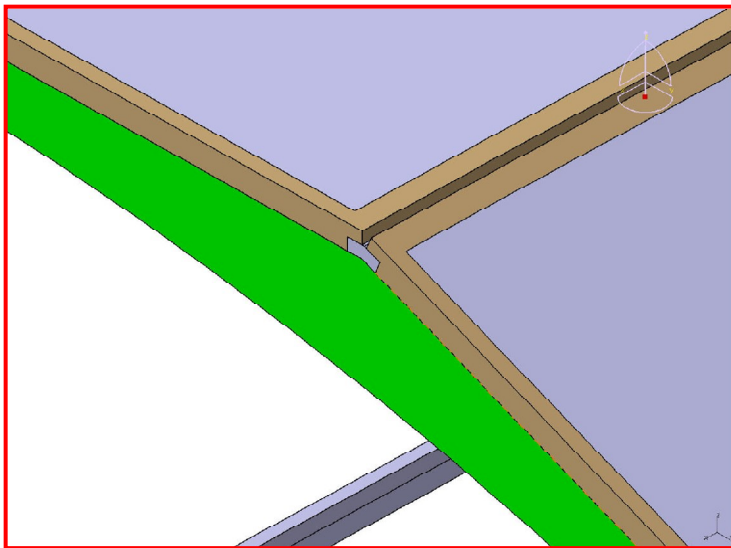
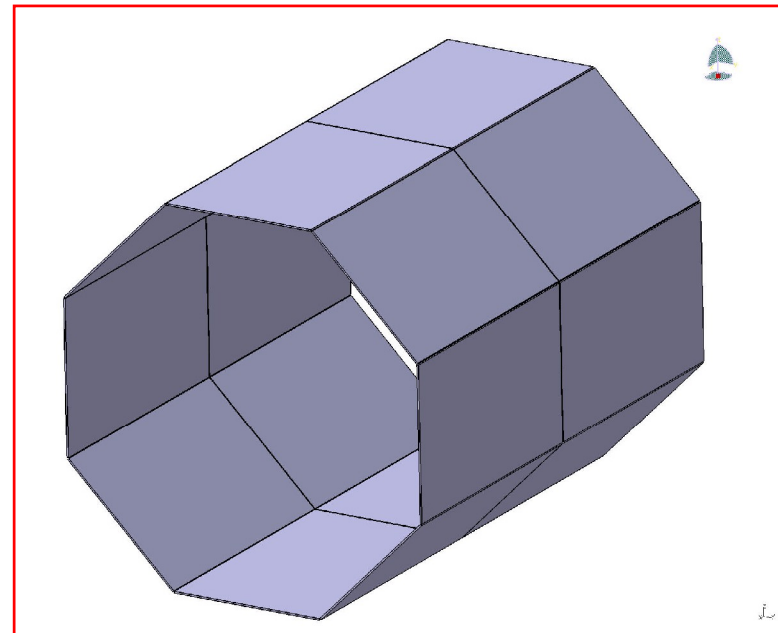
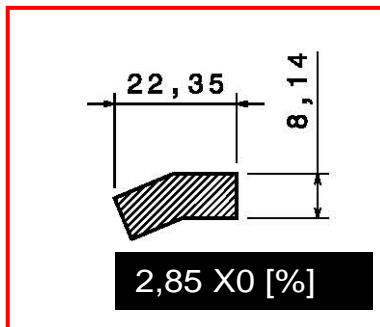
- 8,9 kg dead load;
- 3 kg payload.
- **MAX deflection: 62 micron**

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# SET mechanical structure

(Among SET tasks: the tracking alignment)

Each panel is constrained at 4 sides;  
-> 3 support rings on TPC

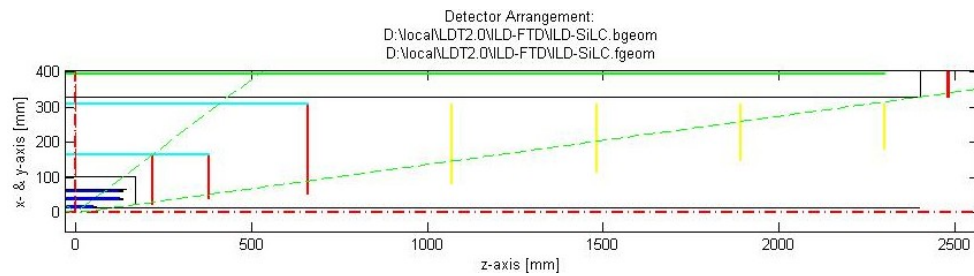


# Detector Simulation studies

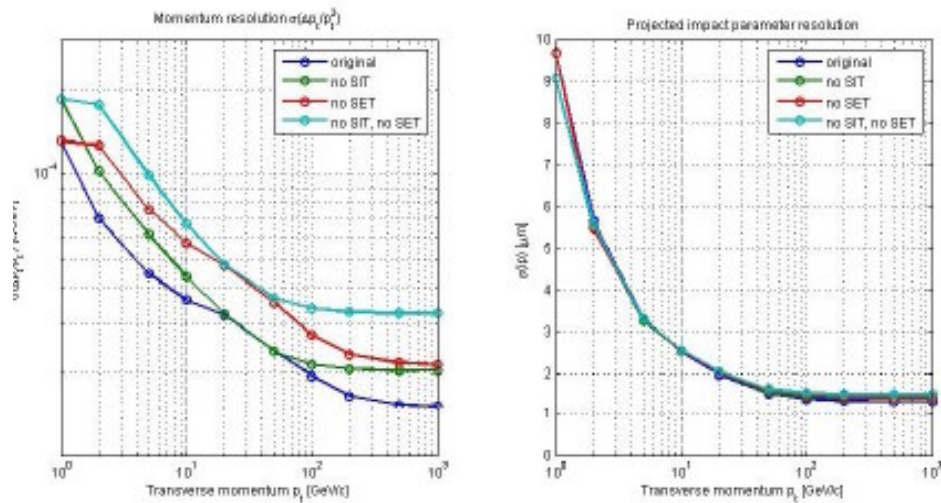
SiLC teams developed or are continuing to develop:

- Three main tools:
  - => LiCToy (fast simu)
  - => MOKKA (all ILD Si components implemented)
  - => ILCROOT (definition of an all Silicon tracker  
and Silicon + gaseous tracker)
- Digitization that can be implemented in one or the other simulation framework

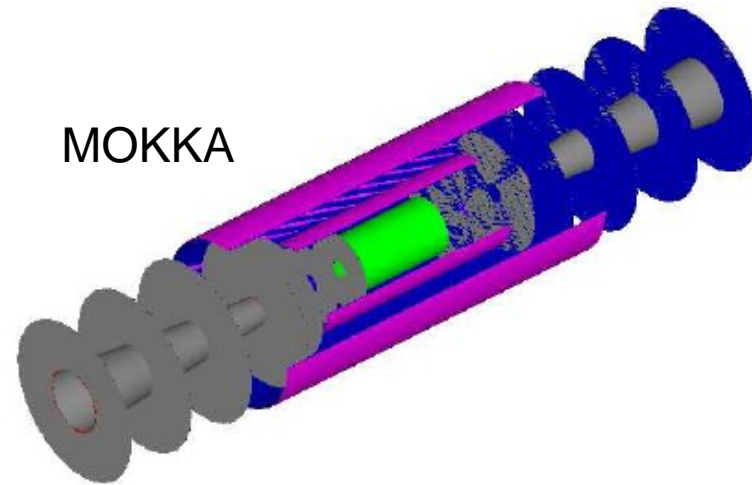
***Essential for LOIs, detector definition & performance studies***



## LICTOY for fast detector studies

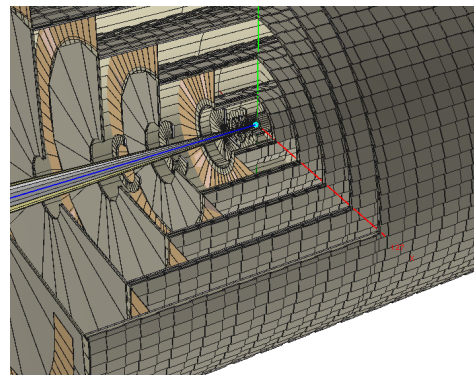
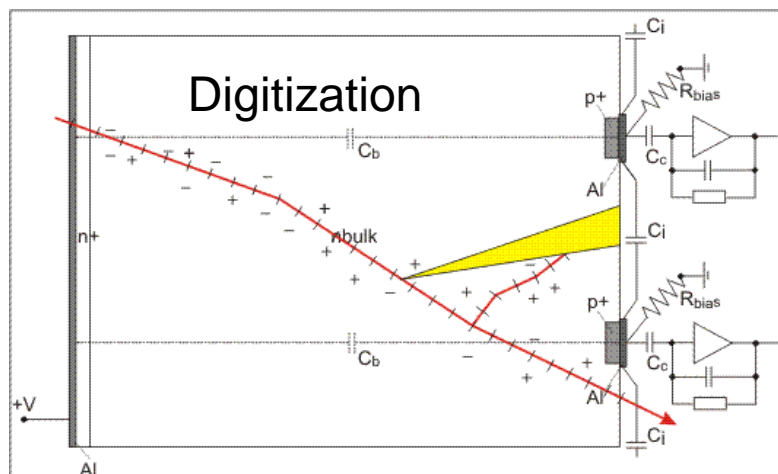
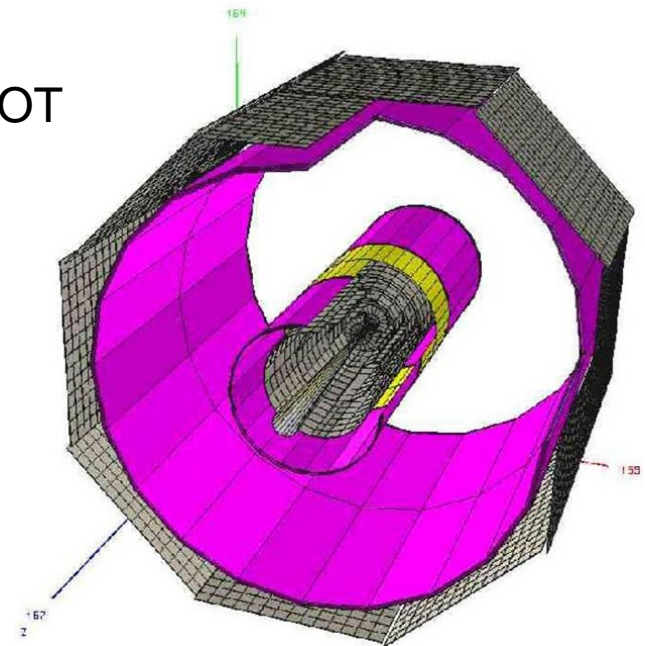


## MOKKA



Detector model for the Silicon Intermediate Tracker and the Forward Tracker Disks of LDC in the MOKKA simulation framework (the green colour component is the VDX).

## ILCROOT



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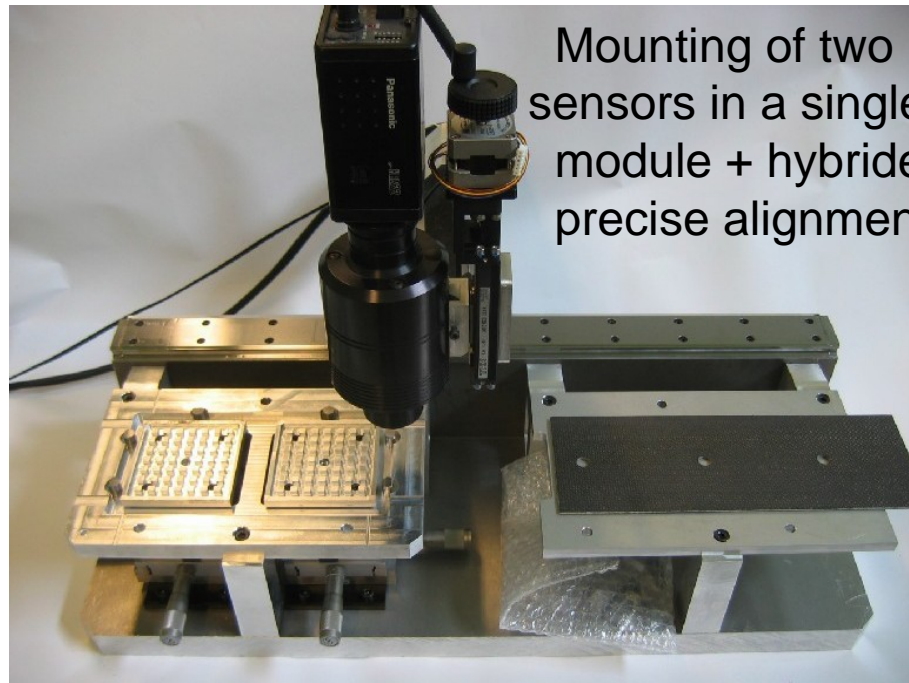


# New Lab test benches in 2008

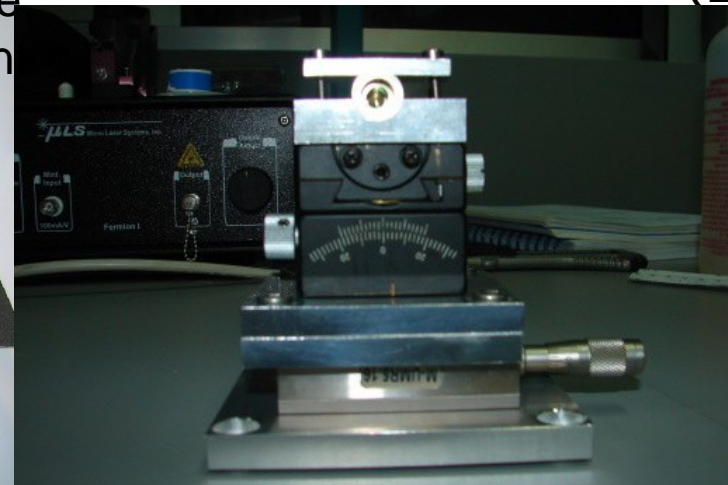
- Development of a new facility to construct new modules and experience new sensors (LPNHE)
- Development of a new alignment facility at IFCA



# Fabrication of module (LPNHE)



Mounting of two  
sensors in a single  
module + hybride  
precise alignment



Automatized gluing  
machine



Bonding at the bonding Lab at CERN  
Soon (hopefully) installed in Paris

# Test beams in 2008

- 1) Test beam at the SPS in June with the test structures (see S. Haensel)
- 2) Preparation of the test beam with the LCTPC at DESY (see S. Haensel)
- 3) Preparation of a brand new complete test beam system
  - => New modules
  - => New test beam mechanics
  - => New FE electronics
  - => New DAQ electronics and software
  - => new alignment prototype

This standalone system can be combined to any other sub-detector and

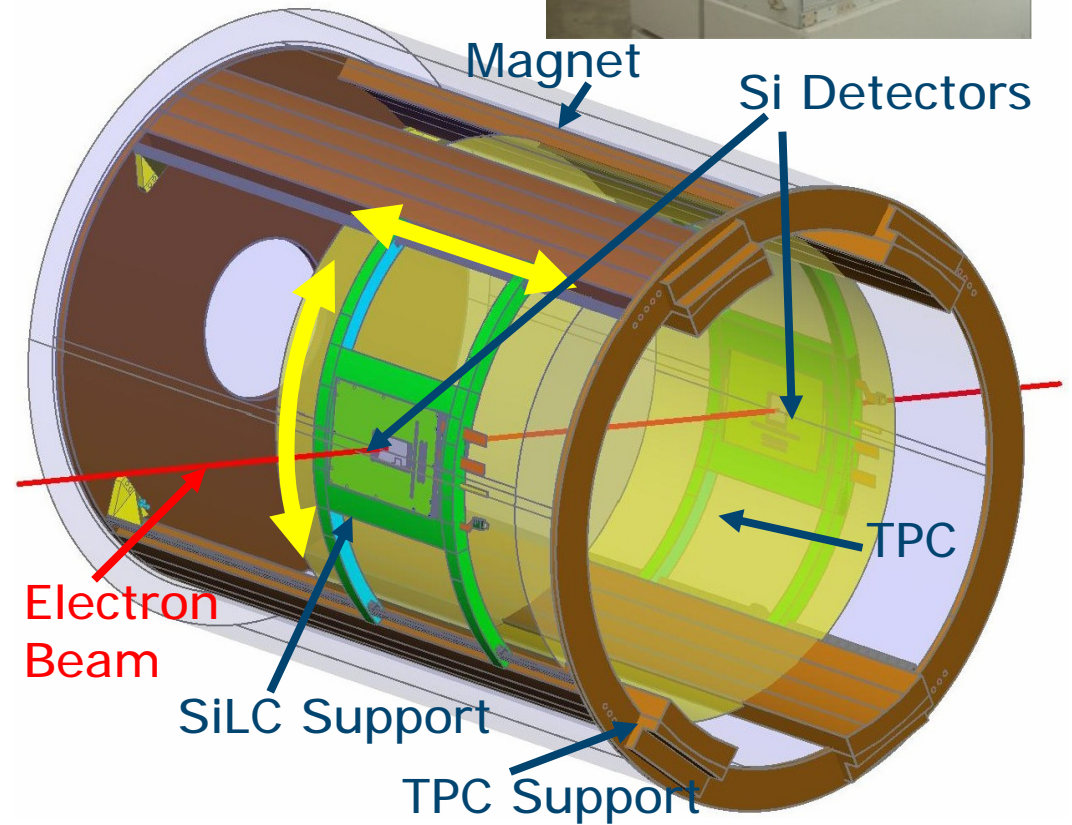
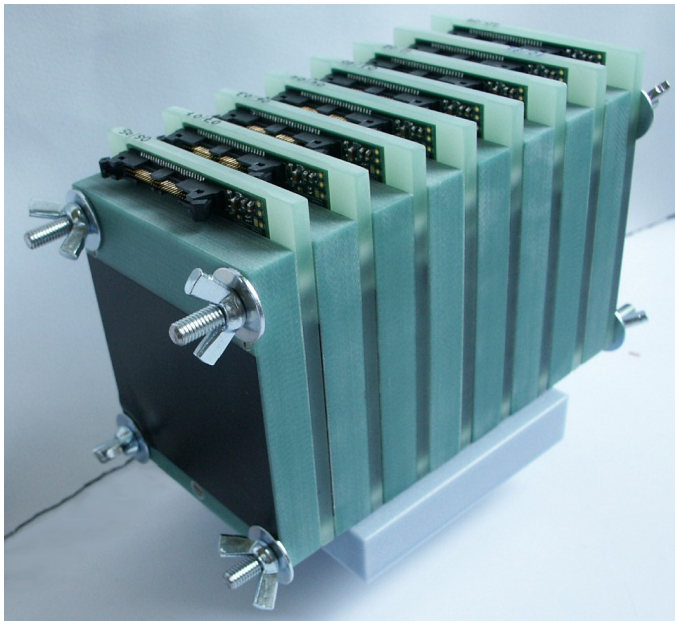
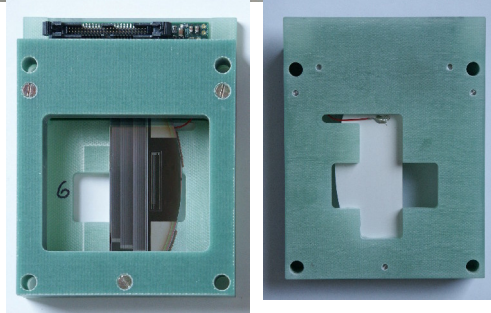
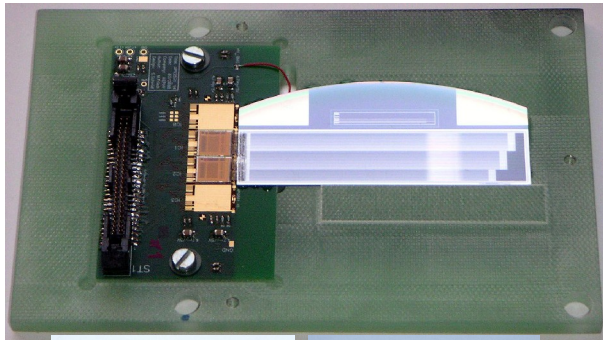
Can go to any test beam

Allows to test new sensors and new chips



# LP-TPC: Silicon Envelope (HEPHY, IEKP, LPNHE)

DESY test beam  
(2009)



Test HPK structures CERN SPS  
(HEPHY+CU Prague), June 2008

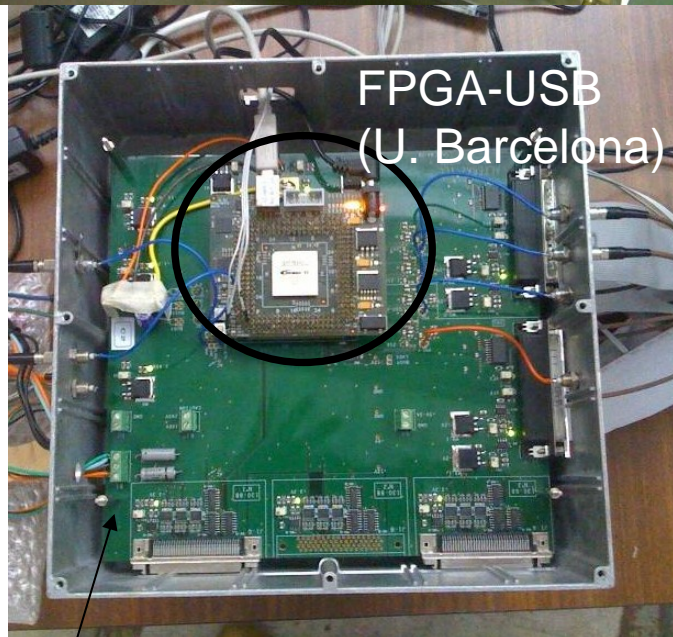
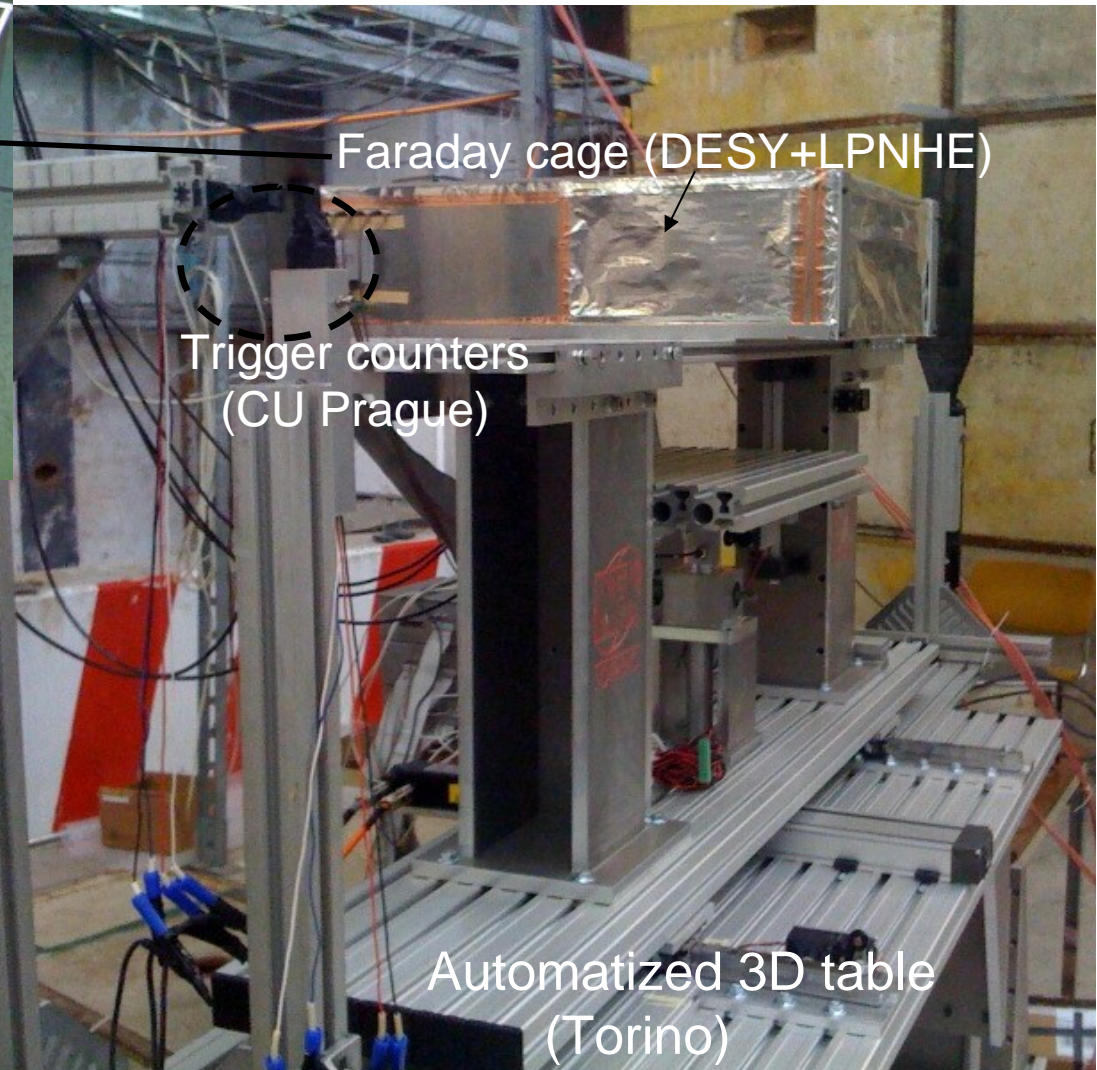
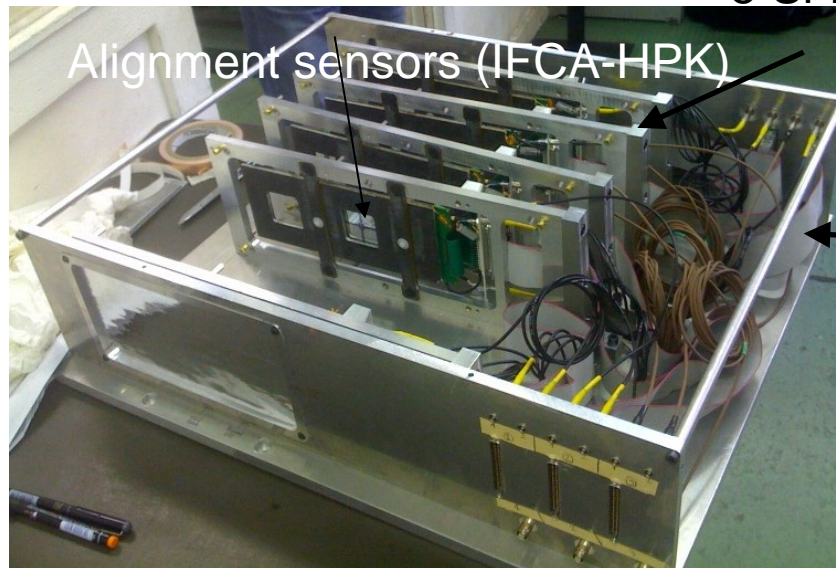
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See S. Haensel's talk



# Test beam at PS-CERN, Nov 1-7 2008

5 Si-HPK strips modules (LPNHE+CERN bonding Lab)



FPGA-board: 2VA1 modules (1024 ch) + 3 SiTR\_130-88 modules (1056 ch) (LPNHE)



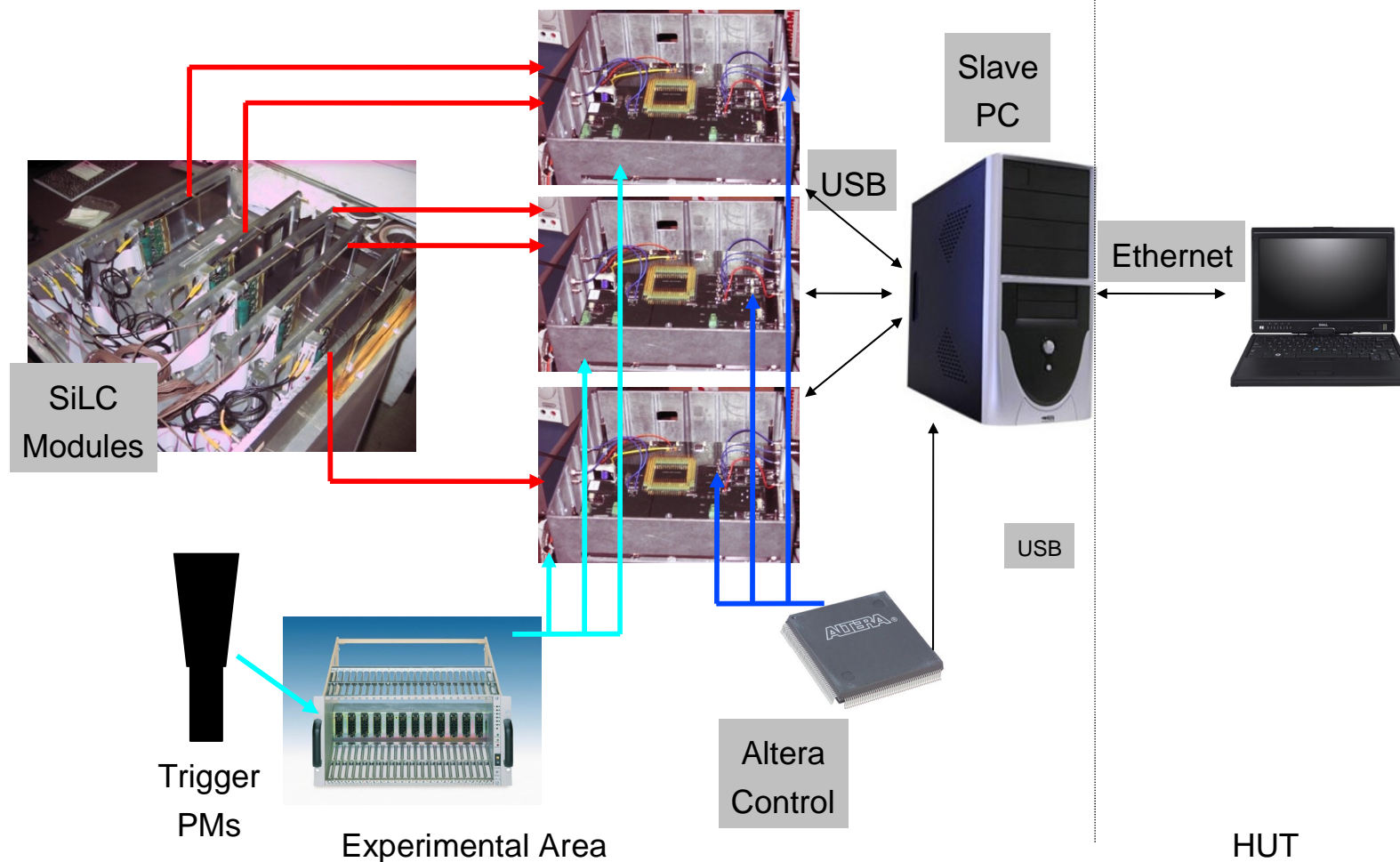


# New test beam DAQ set-up for SiTR\_130-88

SOFTWARE: VHDL, C++, ROOT

Altera  
boxes

Fully standalone tracking system



# SiLC perspectives

- SiLC has been achieving a very successful program of work since LCWS07 on the R&D objectives
- Covering more and more the R&D objectives for the various LOIs: ILD (strong involvement), SiD (collaborative contacts intend to develop further in this direction too), 4<sup>th</sup> concept is now also interested
- An always strong synergy with LHC and upgrades of LHC,
- Extending now to CLIC and also some common interest also with SuperB factories
- Pursuing R&D on presently available technology (short term) but developing also lines of research on novel technologies for the longer term in a participation to global worldwide efforts.
- Reinforcing collaborative efforts with Industry

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