Special Focus Session
On
CMOS MAPS and 3D Silicon

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Pixel Development Group

Introduction

- Monolithic vertical integration (3D) is a relatively new approach to IC development with many options and paths toward successful implementation.
- Recent meetings and presentations at HEP workshops have generated a great deal of discussion and interest in 3D electronics.
- As a result, a significant number of institutions have come together as a consortium to work on related 3D ideas.

Goals

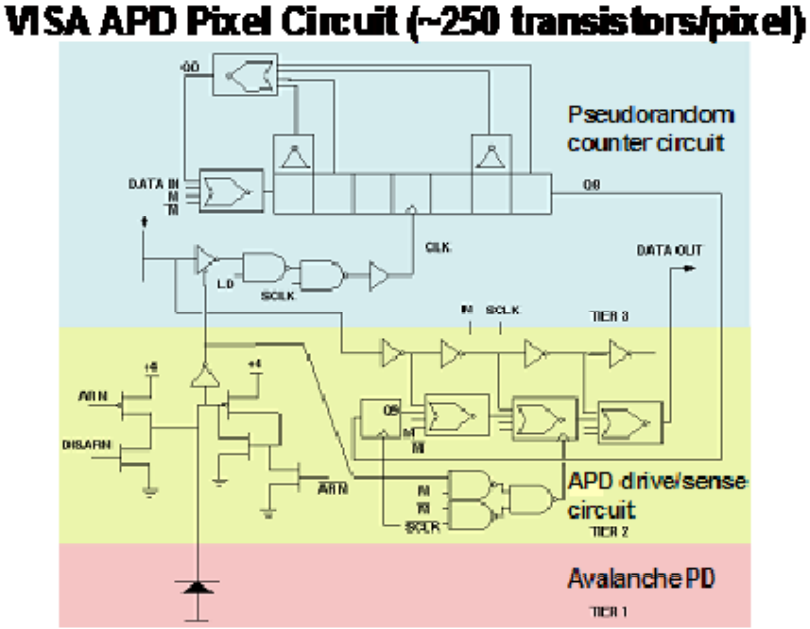
- Explore the range of options available in 3D and understand which scientific applications and spin offs can best benefit from this new technology.
- Share development costs
- Focus on commercial vendors for CMOS and vertical integration, whenever possible, to benefit from their experience and investments in the technology.
- Provide an organized focus for commercial vendors to understand the needs of our community.
- Provide a mechanism for joint funding approval.
- Provide information to outside community through presentations and publication of developments on a yearly basis.

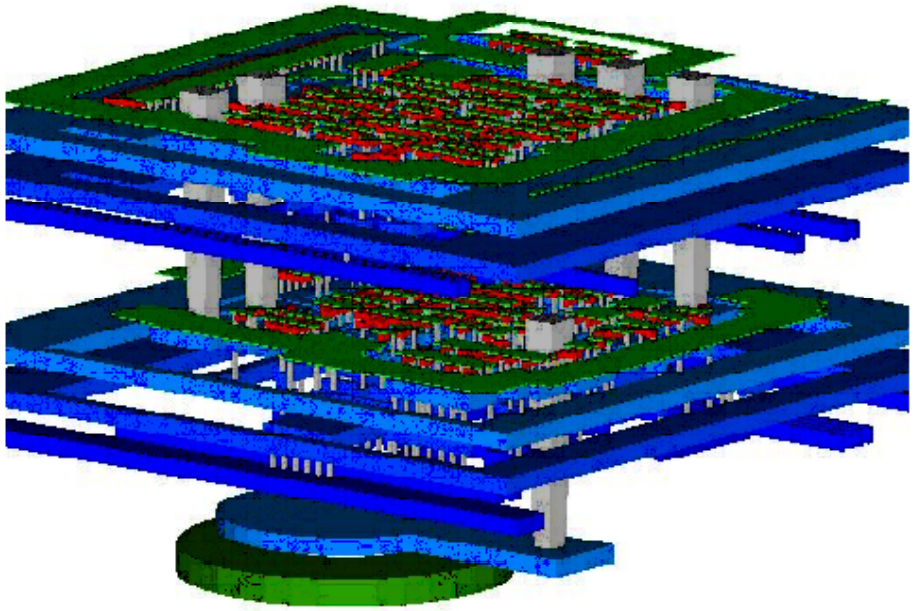
Benefits

- Cost sharing is expected to be by means of multi-project wafer runs and sharing of designs and man power resources.
  - development of cells
  - characterization of devices
  - development and evaluation of new software tools
- Enter into joint contracts with the relevant foundries and post processing vendors.
- Define common testing procedures and hardware.
- Provide for mutual design reviews
- Maintain communication within the consortium through regular meetings and web based technology server.

What is 3D or Vertical Integration?

- It is not 3D sensors which have been described in various HEP talks.
- Vertical integration or 3D for short is defined as "the integration of thinned and bonded silicon integrated circuits with vertical interconnects between IC layers". The definition might be best understood by means of an example as seen in the schematic below which show a three tier IC stack comprised of two layers of electronics and one sensor layer along with the associated 3D CAD layout.





Advantages

- The ability to have high functionality in a small area without going to deeper submicron technologies => small pixels.
- The ability to have very low mass circuits since each circuit layer can be thinned to 7-12 microns.
- The ability to isolate analog and digital functions on different layers.
- The ability to remove PMOS transistors from the sensing layer in a Monolithic Active Pixel Sensors (MAPS).
- The ability to mix technologies and feature sizes in a monolithic structure.

3D Consortium Members

- The consortium is currently comprised of members who have written a Letter of Intent to work together on a MPW run using the Tezzaron 3D IC fabrication process. Other processes have and will be investigated as the need arises. The Tezzaron process will be described a little later.
- There are currently 15 organizations in the consortium.
- Other laboratories within the US are considering joining.

	Institutions	Location	First Contact	
			Last name	e-mail
1	CMP	Grenoble France	Torki	Kholdoun.Torki@imag.fr
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4	IRFU	Saclay France	Degerli	yavuz.degerli@cea.fr
5	LAL	Orsay France	De la Taille	taille@lal.in2p3.fr
6	LPNHE	Paris France	Pham	pham@lpnhe.in2p3.fr
7	University	Bergamo Italy	Re	valerio.re@unibg.it
8	INFN	Pisa Italy	Morsani	fabio.morsani@pi.infn.it
9	INFN	Bologna Italy	Gabrielli	alessandro.gabrielli@bo.infn.it
10	INFN	Rome Italy	Spiriti	spiriti@roma3.infn.it
11	University	Pavia Italy	Ratti	lodovico.ratti@unipv.it
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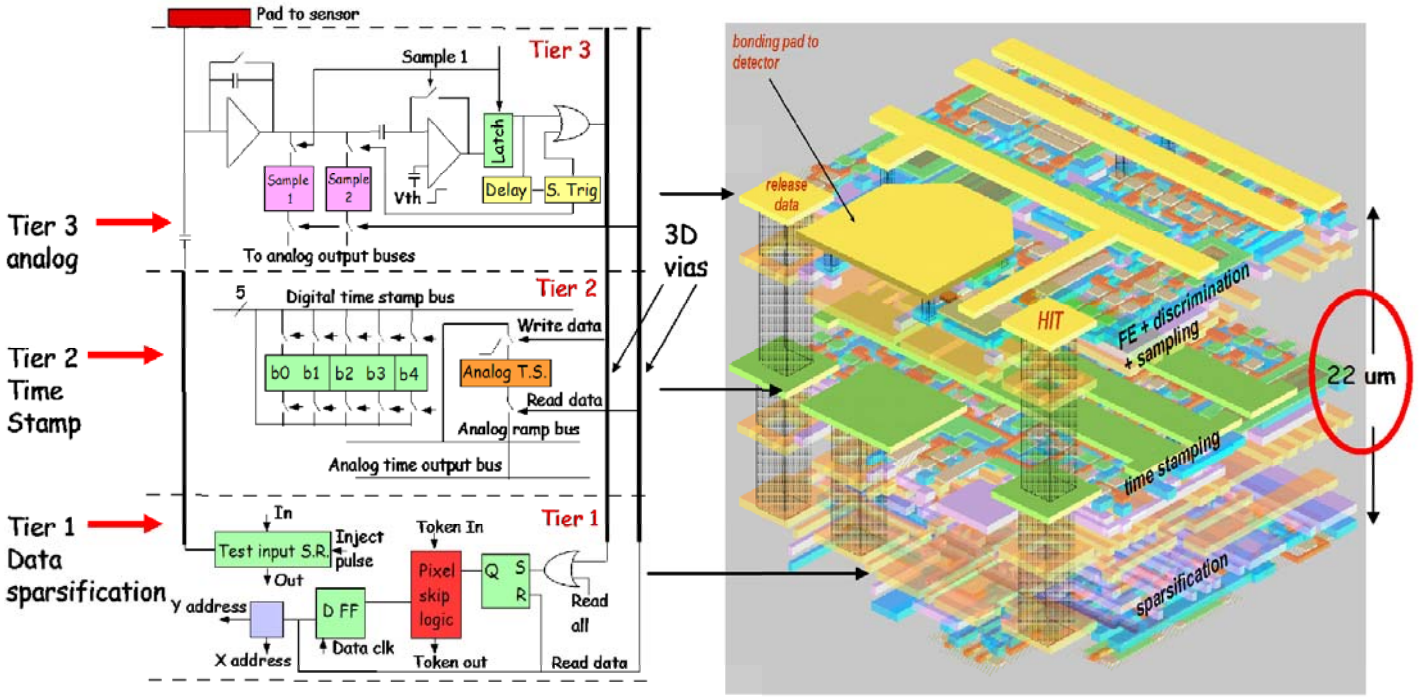
15	Fermilab	Batavia USA	Yarema/Deptuch	yarema@fnal.gov/deptuch@fnal.gov

Early Work In MIT LL

- The first two 3D designs (VIP1, VIP2a) for HEP were demonstrator chips that have most of the functionality needed for an ILC vertex detector.
- These chips were designed in the MIT LL SOI process (0.15 – 0.18 um minimum feature size) which uses a "via last" process.
- A sensor layer was not available in these MPW runs.

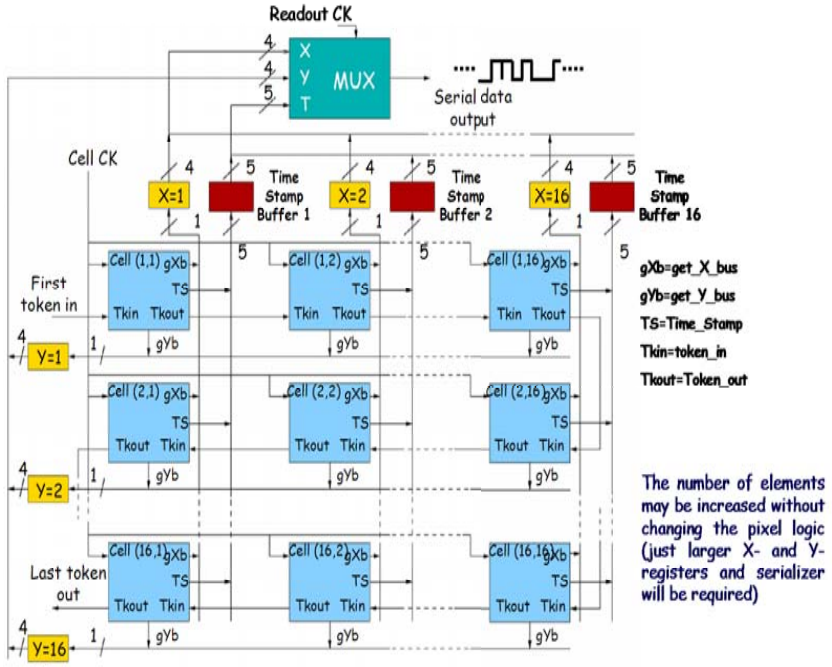


Initial Results

- The VIP1, which is a 4K pixel array with 20 micron pixels, has been shown to work. Results have been presented at other meetings.
- The yield on VIP1 was low. The VIP2a was designed specifically to improve yield with things like redundant contacts and wider traces.
- We found that the SOI transistors in the MIT LL process were not well characterized and not well suited to analog circuit design.
- Focus has moved to working in CMOS with commercial vendors

MAPS design

- A MAPS device with the same architecture and sparsified readout scheme as VIP1 was designed and tested by Valerio Re. The MAPS device was primarily digital in the sense that there was no analog readout or analog test inputs. The device was built in the ST Microelectronics 0.13 um deep-Nwell process.
- Success of the 2D MAPS design is further confirmation that a ILC pixel design with high resolution time stamping and sparsified readout is possible.

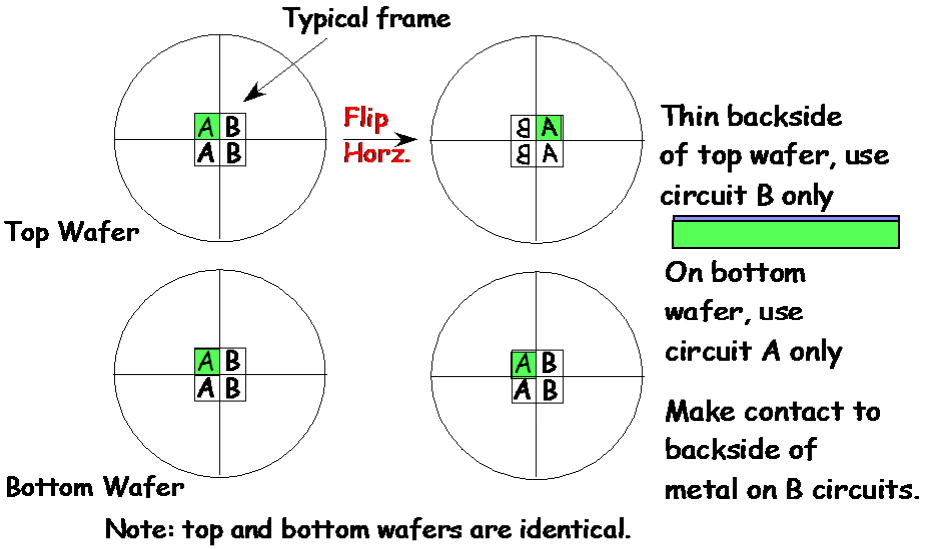


Consortium Plans

- Plans are progressing to have a 3D multi project wafer run through a commercial vendor, Tezzaron.
- The wafers will be fabricated for Tezzaron in the Chartered 130 nm process using a "via first" process.
- Wafers will be stacked into 3D assemblies and finished by Tezzaron.
- An official quote has been received and the cost is being divided into 3 separate purchase orders.

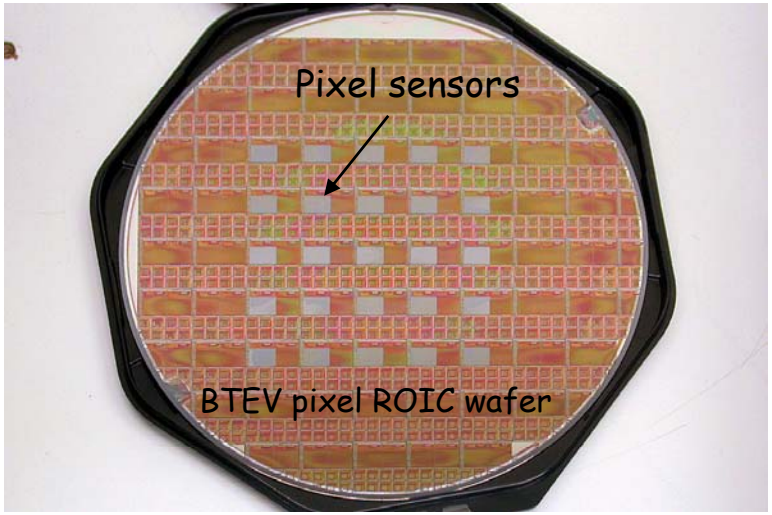
Tezzaron 3D Multi-Project Run

- There will be 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 15.5 x 26 mm)
- The wafers will be bonded face to face.

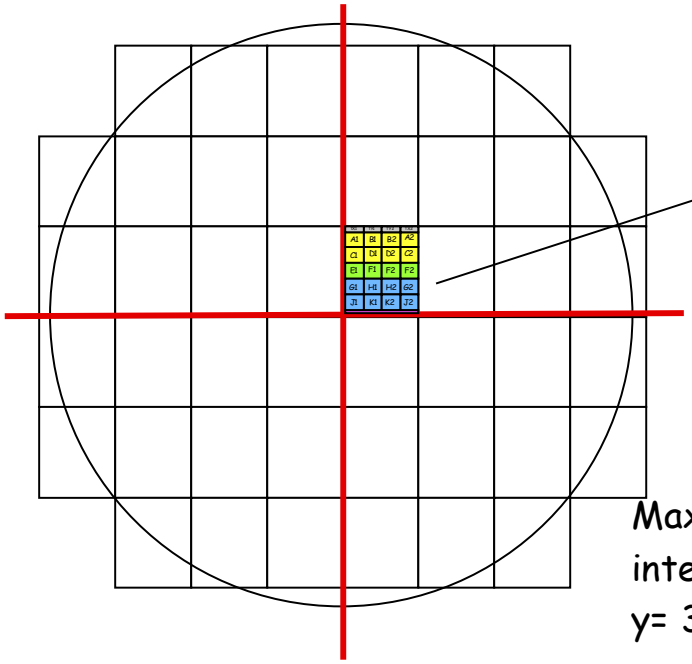


Face to Face Bonding

For devices without integrated sensors, bond pads will be fabricated for bump bonding to sensors to be done later at Ziptronix as shown below.



MPW run Reticule Layout



Wafer Map

TX1	TY1	TY2	TX2
A1	B1	B2	A2
C1	D1	D2	C2
E1	F1	F2	F2
G1	H1	H2	G2
J1	K1	K2	J2

Frame layout

Max frame layout area including internal saw streets: x=25.760 mm y= 30.260 mm.

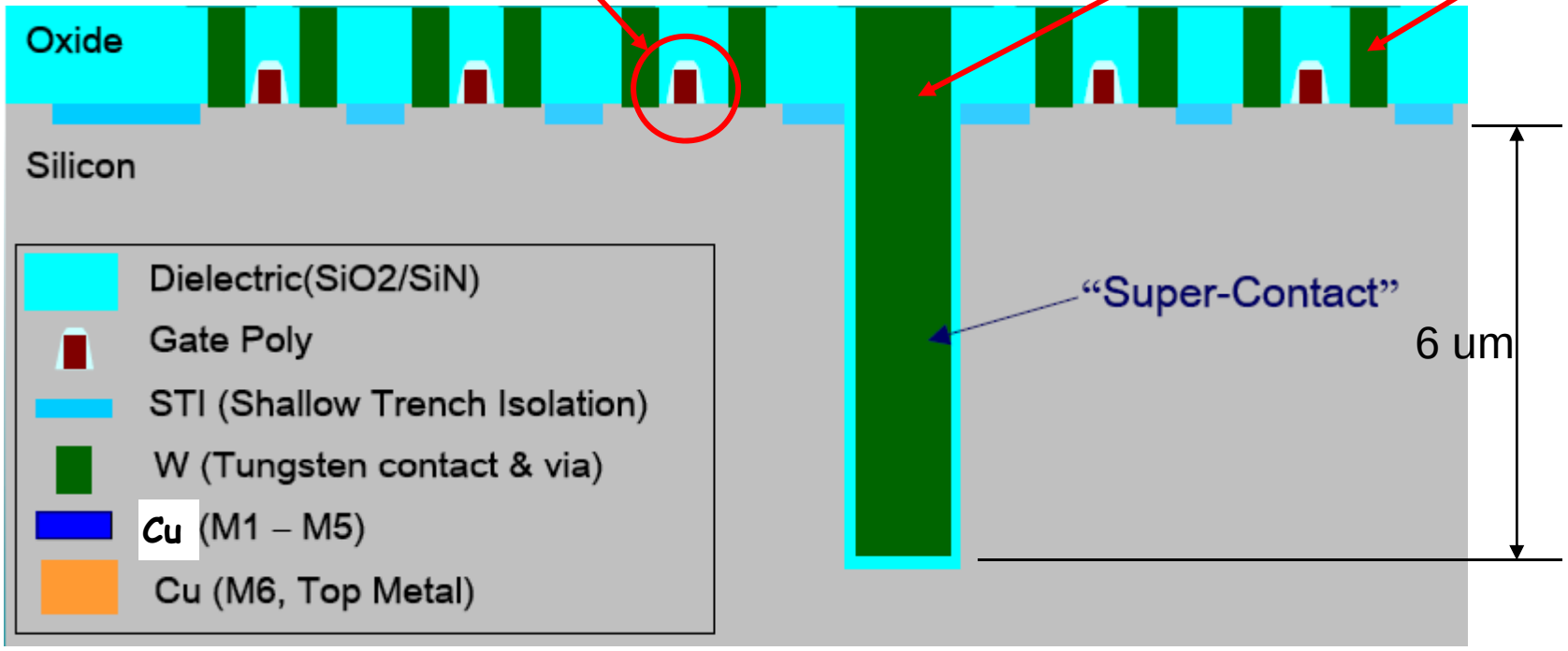
Yellow = France
Green = Italy
Blue = USA
Magenta = alignment
Grey = test chips

Chip X= 6.3 mm
Chip Y= 5.5 mm
Test chip Y=2.0 mm, X=6.3
Streets = 100 um

Alignment area (outside design area) = 250 um x 25.76 mm at top and bottom

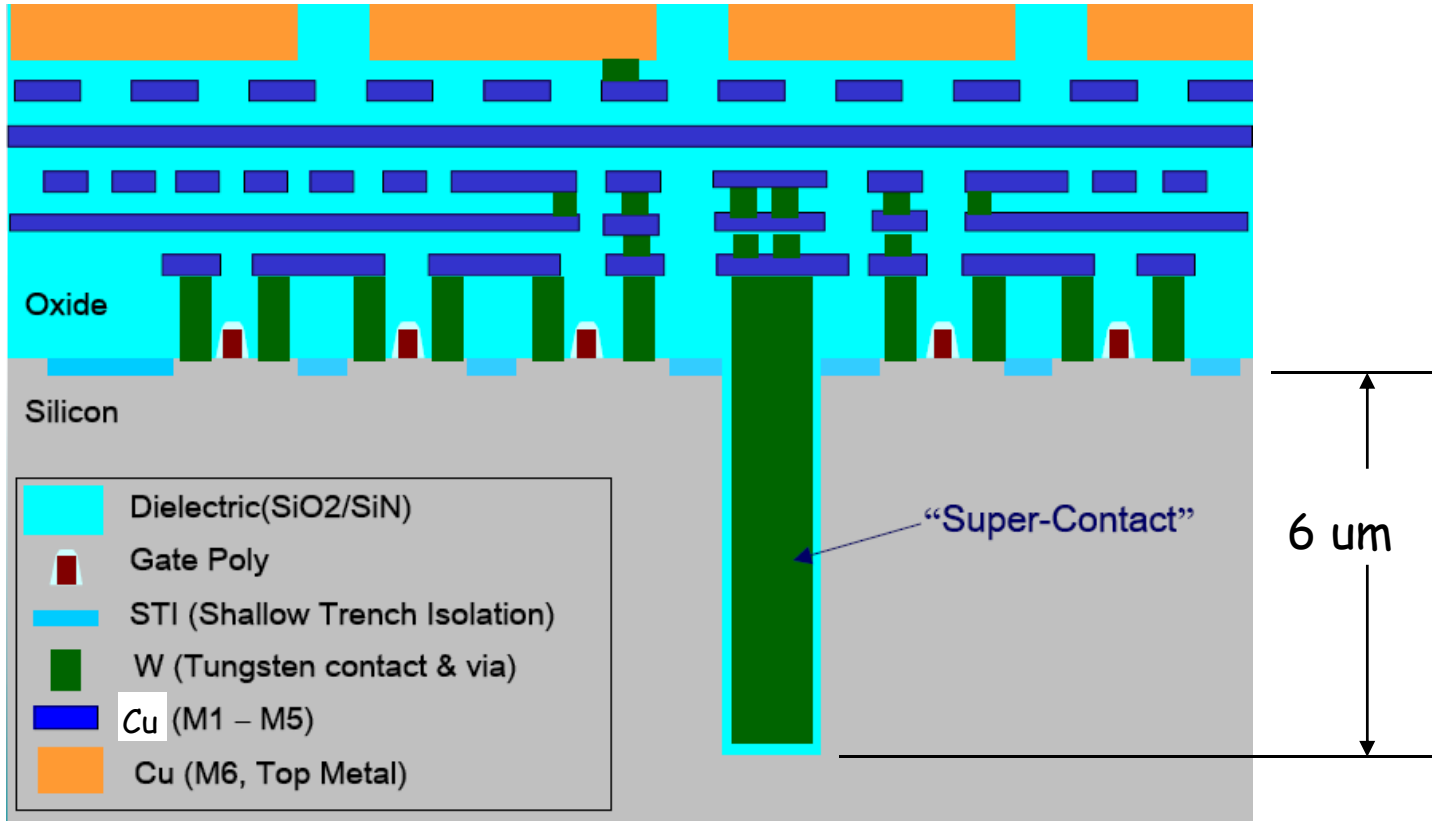
Tezzaron 3D Process

- Through silicon vias are fabricated as a part of the foundry process. "Via first" approach.
- Complete FEOL (transistor fabrication) on all wafers to be stacked
- Form and passivate super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors



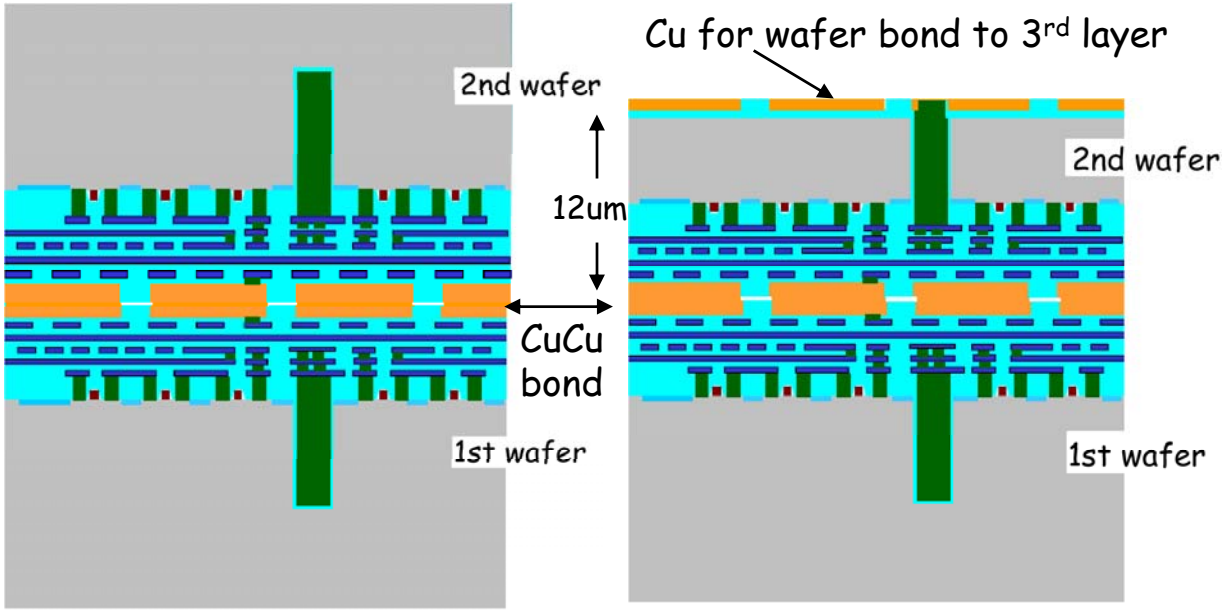
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)



Tezzaron 3D Process

Example: bonding identical wafers



Flip 2nd wafer on top of first wafer.

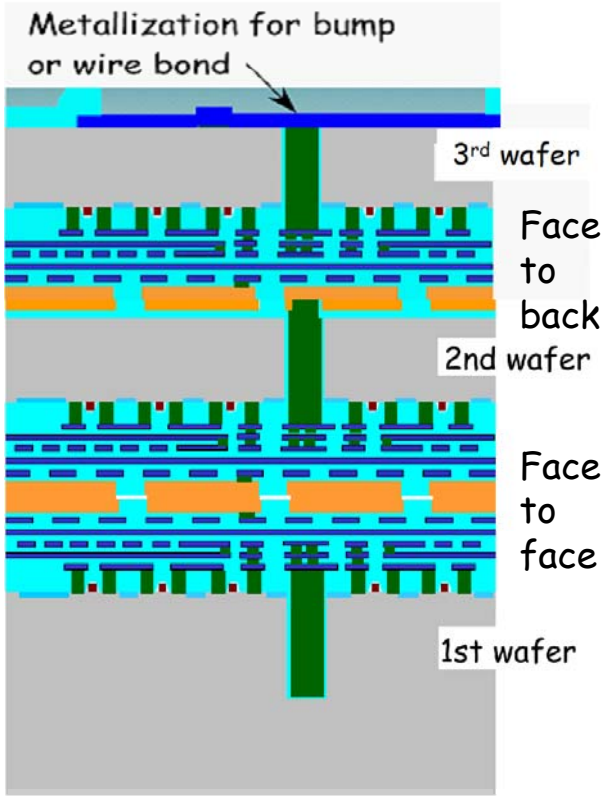
Bond second wafer to first wafer using Cu-Cu thermo-compression bond.

Thin second wafer to about 12um to expose super via.

Add metallization to back of 2nd wafer for bump bond or wire bond.

OR

Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer



Flip 3rd wafer

Bond 3nd wafer to 2rd wafer.

Thin 3rd wafer to expose super via.

Add final passivation and metal for pads

MPW Run Designs

- Several designs are directed toward the ILC.
- Complementary efforts have been initiated building upon the original VIP1 pixel design for the ILC.
  - In Italy the 2D MAPS vertex readout chip will be converted into a 3D design where most if not all the PMOS devices in the sensor layer will be moved to another layer along with other electronics.
  - In France there are two approaches being considered
    - One tier with sensing diodes and analog signal processing and a second tier with time stamping and sparsification from the VIP1 design
    - A sensor layer with analog processing fabricated in a 0.35 um technology and readout based on VIP1 in a separate layer
  - In the US plans are for an improved version of the VIP2a.

MPW Run Designs

- Other designs
  - Plans have started for a multi-national design for an ATLAS pixel upgrade with analog electronics on one layer and digital on a separate layer.
  - New design for a CMS pixel ROIC utilizing the advantages of 3D processing
  - Design for a data driven continuous readout architecture with sparsification and timestamp information for SuperB
  - On-going discussion of a design for light source applications.

Current Developments

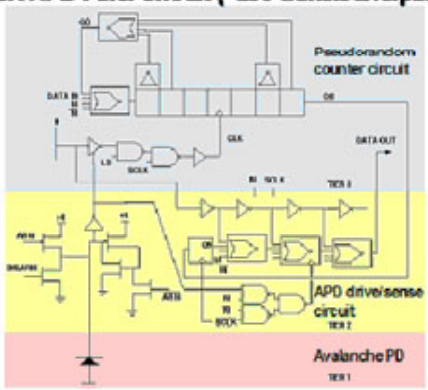
- All organizations now have NDAs with Tezzaron
- Working to resolve Chartered NDA issue for some European organizations.
- Developing standardize wafer bonding patterns for all MPW participants.
- Beginning to develop small library of parts to share with participants.
- Setting up web based server for exchange of information.

3DIC at Fermilab

Consortium for Development of 3D/Vertically Integrated Readout Electronics and Sensors

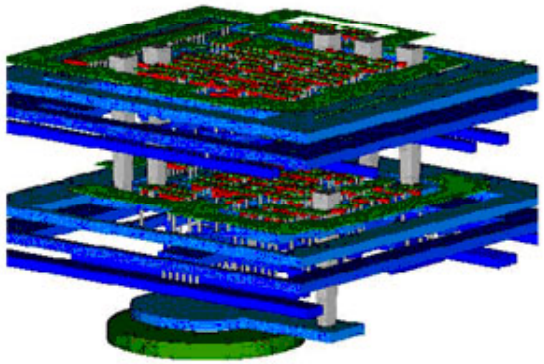
Vertical integration or 3D for short is defined as "the integration of thinned and bonded silicon integrated circuits with vertical interconnects between IC layers"1. The definition might be best understood by means of an example as seen in the schematic below which show a three tier IC stack comprised of two layers of electronics and one sensor layer. This device was fabricated by MIT Lincoln labs. The active electronics in each layer is only 7 microns thick. A CAD layout view of one pixel element is also shown for clarity showing the vertical interconnects.

VISA APD Pixel Circuit (~250 transistors/pixel)



The 3D technology is being explored by industry for many applications including memories, pixel arrays, microprocessors, and FPGAs. This consortium has been form to explore vertical integration for pixel arrays in a number of scientific applications. 3D offers the opportunity to develop low mass circuits with high circuit density along with isolation of various elements such as analog and digital circuits.

Handbook of 3D Integration, edited by Philip Garrou, Christopher Bower, and Peter Ramm, Wiley-VCH, 2008



Summary

- A large number of institutions have come together to work on development of 3D integrated circuits and CMOS sensors using commercial vendors.
- The goals and benefits of the consortium have been outlined.
- The consortium is currently working on its first MPW run with Tezzaron.
- Future MPW runs are expected based on the results of the first MPW.