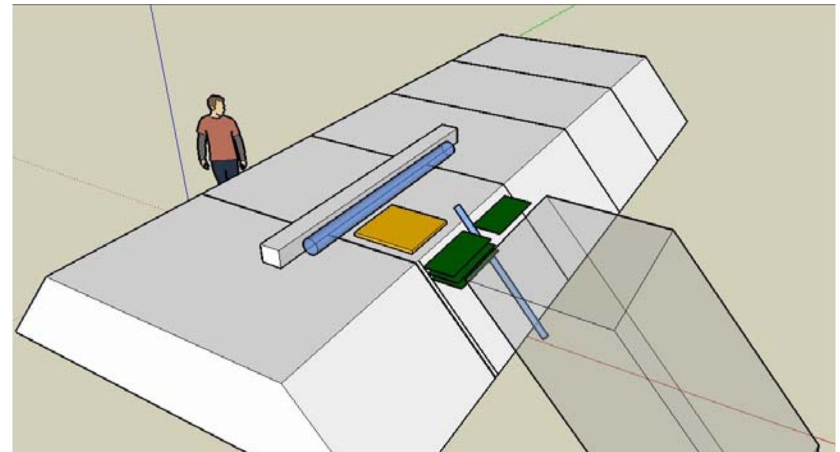
Calorimeter for ILC

Status and Constraints on ECAL electronics

- -Roadmap
- -Mechanics
- -LV Power
- -HV power
- -Data rates
- -DIF
- -info

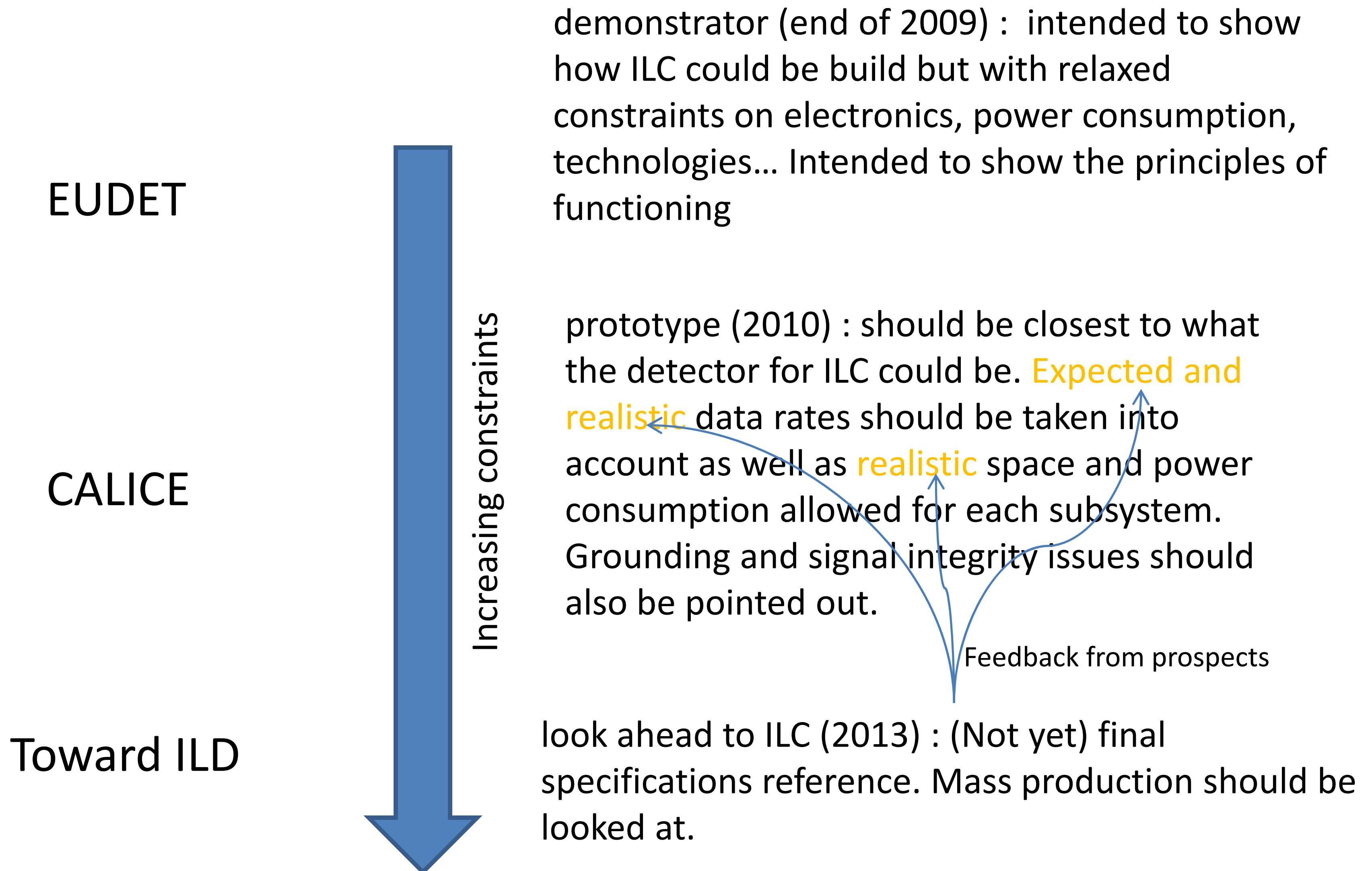


Rémi CORNAT

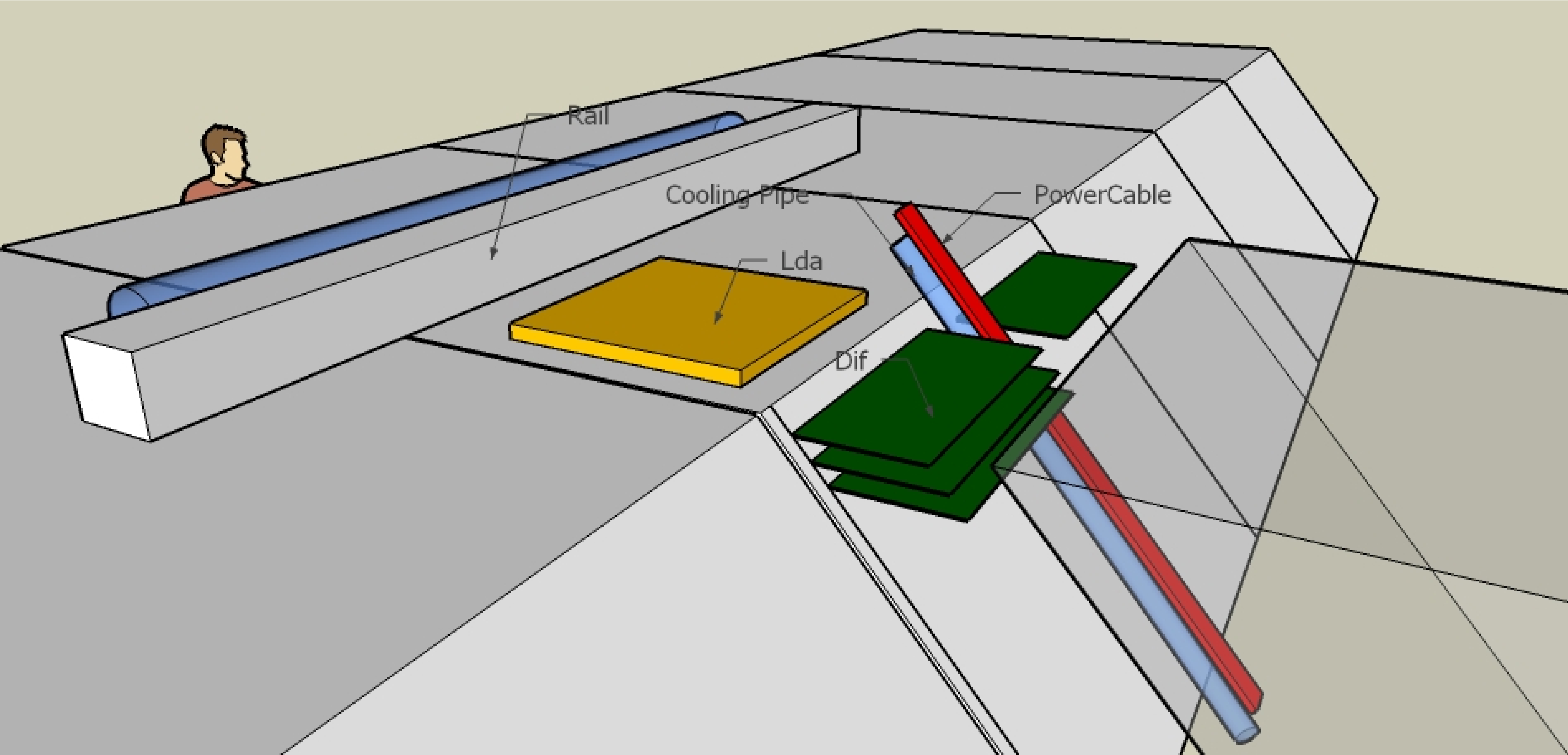
LLR (CNRS/IN2P3)

EUDET meeting
at LAL, June 3rd 2008

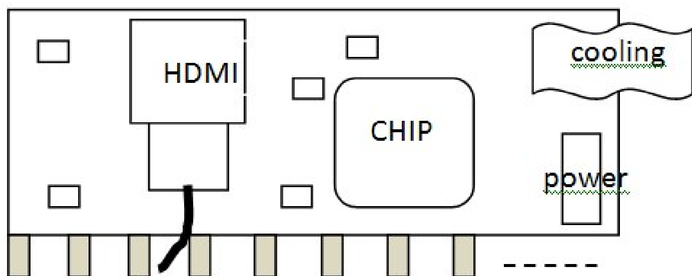
Roadmap



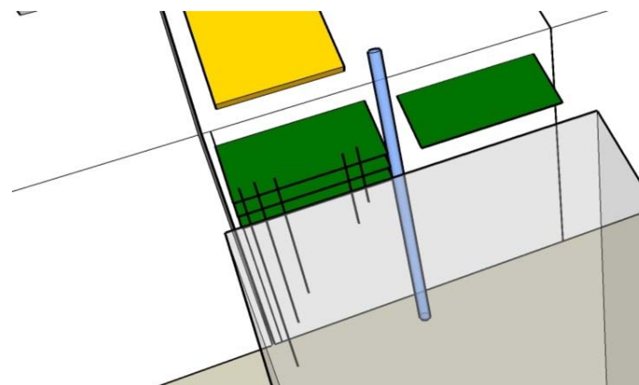
ILD ?



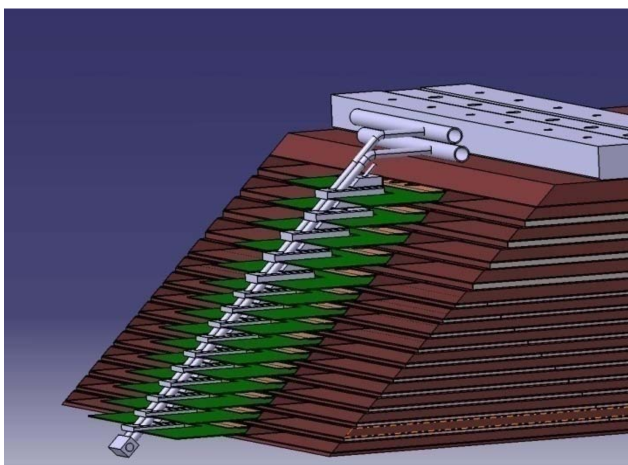
ILD !



DIF is part of last ASU of the SLAB
Allowed space : 6-7 x 3 x 0.6-0.8 cm3 !
Small amount of components allowed

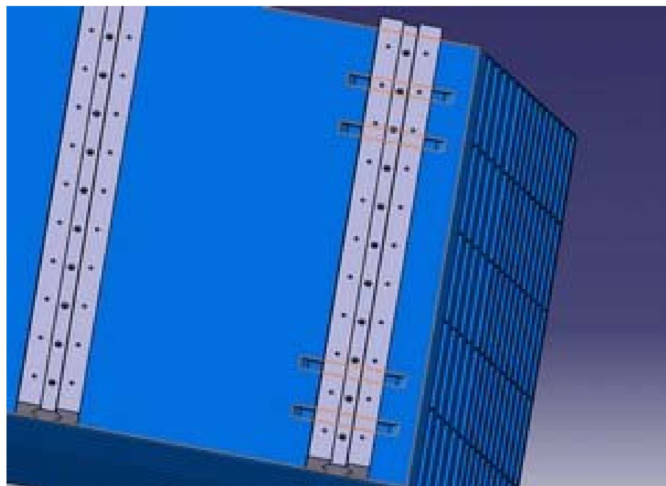


Quite no place for cabling : DAQ + HV + GND
LDA has to receive 30 cables (45 cm linear)
Service space is mostly taken by cooling

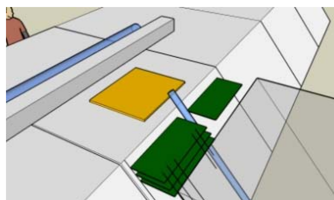


Space for HV and GND is <u>being negotiated</u>

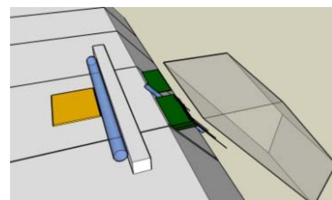
ILD !!



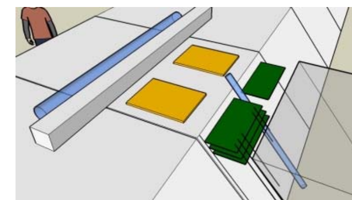
Space for LDA : 10x10 cm2 + connectors and cable curvature, holes (small!) for cables below rails



Outter,

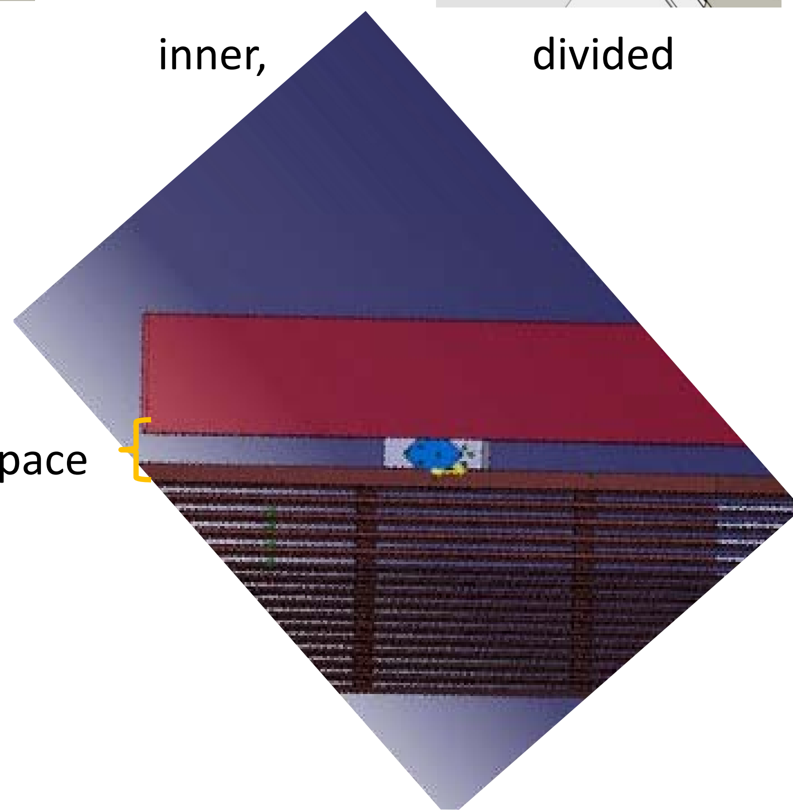


inner,



divided

3 cm in height space



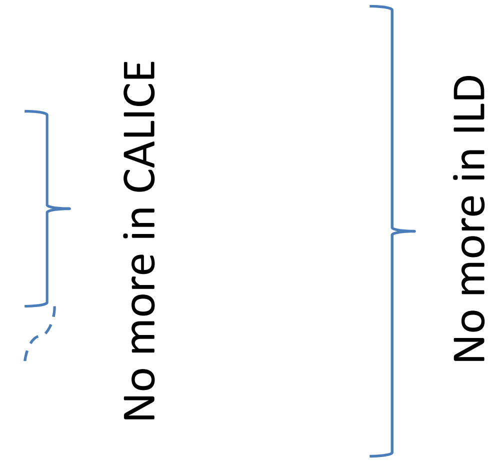
Conclusion on ILD section

- Stringent requirements from ILD
- Relaxed constraints for forthcoming developments (EUDET)
- BUT ILD design have to be kept in mind
  - Provide realistic parts
  - Reusable components (life time of developments)
  - Avoid divergence from ILD baseline when possible
    - Test beam compatibility
    - Features for debugging

So, what about EUDET ?

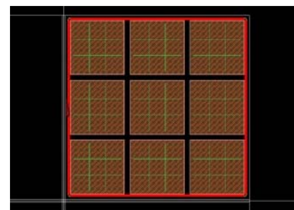
Developers need to monitor/debug/access their parts : development version

- Parts can be un-mounted
- Adapter board
- Relatively large DIF (usb, connectors)
- Accessibility
- Not so low data rate (test beam structure)

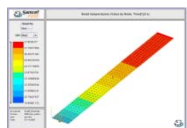


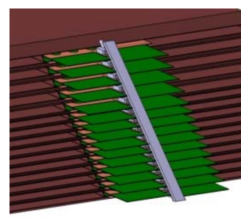
But feasibility is a nonsense if it not demonstrate how ILD goal could be reached
ILD functioning mode : power pulsing, thermal studies, etc…

Status on ECAL



- Wafers
  - Hamamatsu lot being tested : OK
  - 3x3 tests wafers being designed (Xtalk measurements at LPC)
- Mechanics
  - First long structure (Marc, LLR)
  - Thermal studies (LPSC)
  - 3 layers prototype
  - ILD prospects
  - Uncertainties about SLAB thickness (glue, foam, …)





- Electronics
  - Lot of work done in UK (DAQ, gluing tech., DIF,…)
  - SKIROC 2 (Q1'09)
  - 2 DIFs : try to share efforts (USB from DHCAL, SLAB itf)
  - ASU test bench (LPC)
  - System level thoughts (power, data rates and protocols, CCC, CC,…)
    - To be done together
    - Urgent
  - Web site

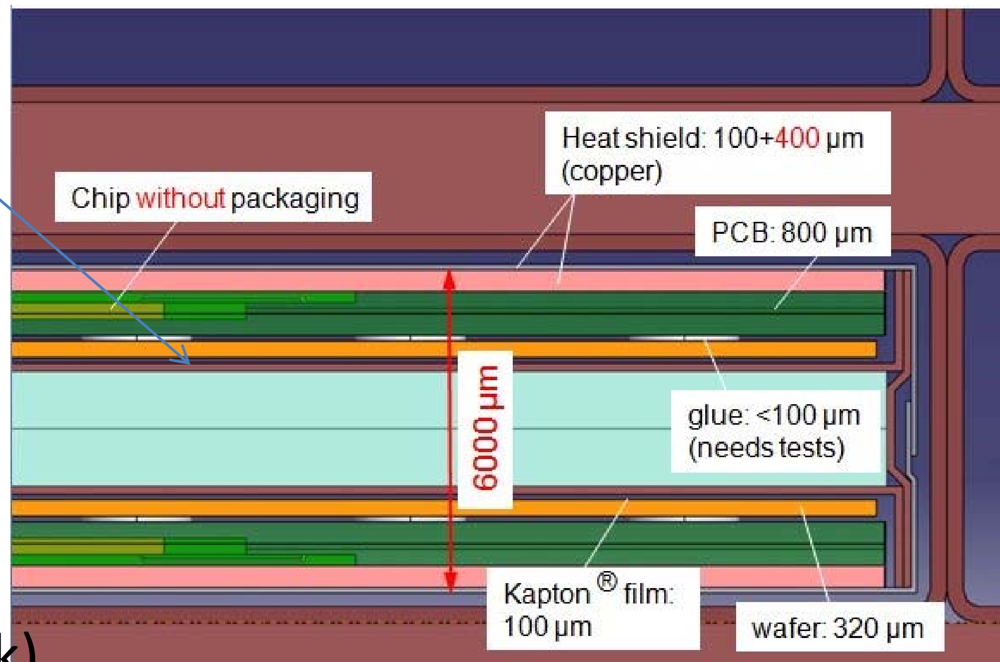
SLAB integration

- Many unknown points
  - Overall thickness
    - Gluing/connection
    - Thermal contacts (foam,…)
  - HV path
  - Cooling outside the structure
    - Dif components placement
      - Place for contacts
      - Thermal dissipation of FPGA
    - Space avaliable for HV, GND (cables & connectors !)
- SLAB structure
  - Production
  - assembly steps

HV (mechanics)

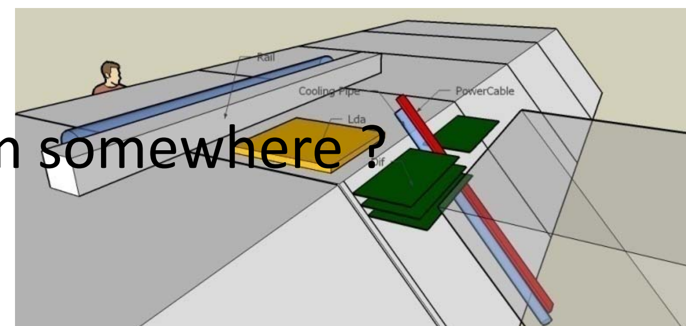
HV on kapton film

Glue ?
Foam ?
Thickness !



Can not be un mounted !
- Find a solution (Aboud's talk)
- Or discard other features for un mounting ASUs

Location and connectors (bus topology) from somewhere ?



LV

- Power pulsing will be tested
  - Power supplies as if it were ILD
  - Distant 8-10 V main PSU, low current capability
  - DIF (of LDA or …) has to provide constant 3 V
    - Regulator
    - Capacitances to locally store power for chips
- Low drop-out regulator (thermal dissipation)

Direct powering : U=q/C, dU= didt/C
dU = 100 mV, di=128*1 mA, dt=9 ms : C = 12 mF

With regulator 8 V – 3 V : U=q/C, dU= didt/C
dU = 4 V, di=128*1 mA, dt=9 ms : C = 300 uF

Place for capacitances on ILD DIF !

Sensors intimacy

6x6 cm2

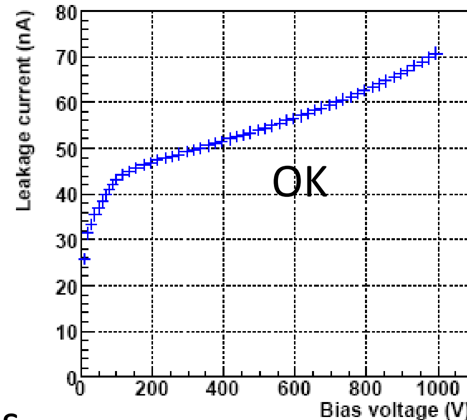
Contact : remi.cornat@in2p3.fr

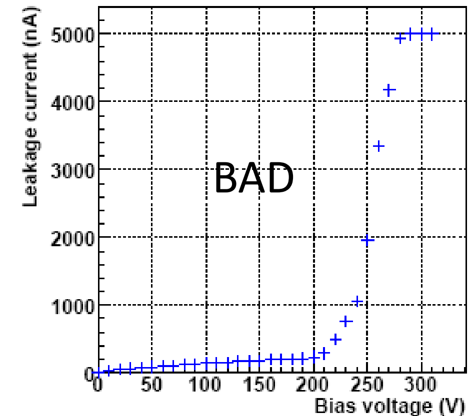
Find a low cost but effective sensor

Why ? 3000 m2 to be produced !

- Validate sensor processing prior to gluing
- 3 production batches (2005-2007)
  - Russian (Moscow State University)
  - Czech (Institute of Physics)
  - Korean

- Low leakage current (<10 nA/cm2)
- Full depletion for maximum energy deposition
- Stable in time and for gluing
- Small dead area : large size





I(Vbias) : leakage
C(Vbias) : depletion

Yield : ~55% ok

New Hamamatsu sensor supposed not to have guardring but cost is high : **for tests only**

Actually it has a guardring…!

New specifications
- 256 channels
- 0.55x0.55 cm2 pads
- 18x18 cm2 total area

some problems about gluing : chemical incompatibility with passivation, new passivation used

Crosstalk issue : under study (3x3 pads test wafers being designed with new guardring structures

Calorimeter for ILC

DAQ / CCC

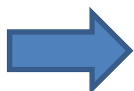
Forthcoming test beams need specific setup (external trigger, fast commands, data rate,…)

Different from ILD constraints

Over constraints the design : distribution of isochronous signals, higher data rate, …

Idea : take benefit of the number of pins of the HDMI connector to ***separate*** TB specific functionalities and strict ILD mode functions

- Isochronous ExtTrigger (Very Fast commands) , ChipFull (Detector feed back), TBclock (Very fine synchronization) on separate pairs (TB only)
- Additional read-out pairs (enabled in TB mode) to increase read-out rate (TB only)
- Keep the 3 standard pairs (ILD mode + TB)
  - ILDclock (Fast clock for “coarse” synchronization : ~ 2-8 x BX rate)
  - Din (SC, Fast commands)
  - Dout (SC, read-out)



- Easier switching between modes
- Reusable blocks (those dedicated to ILD mode) for future CALICE “module 0”
- Feasibility of ILD (no need new firmware, …) by disabling extra features and having ILD “compliant” design (and working without being disturbed by TB functions : power cons., clk freq, etc…)

CALICE Calorimeter for ILC

Conclusion

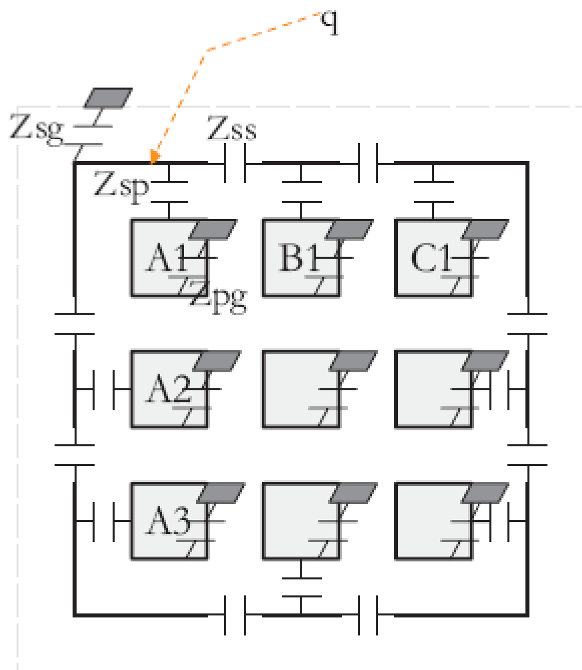
- Do not forget constraints driven by ILD
- EUDET have relaxed constraints but it is a demonstrator on how ILD could be
  - TB requirements : compromises have to be found

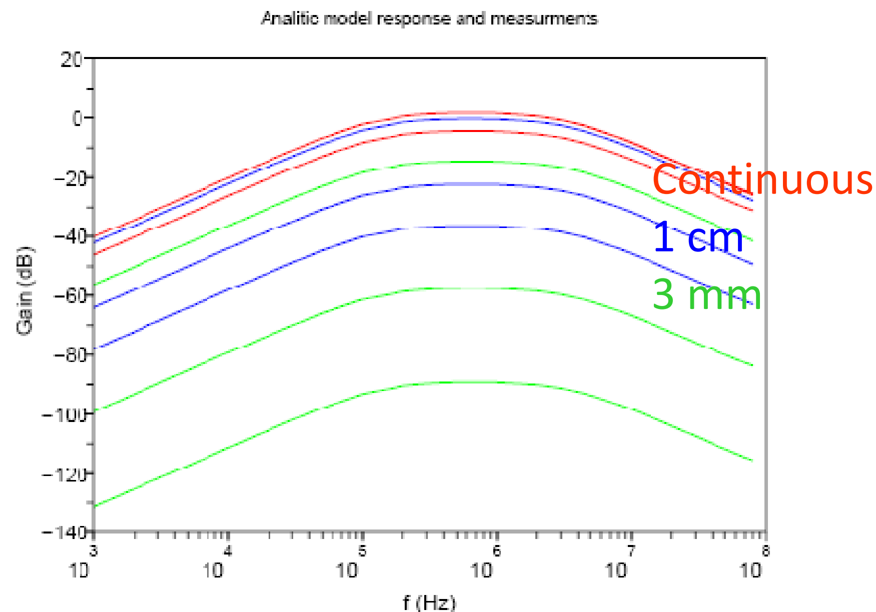
- A lot of ongoing efforts on technical aspects
- Most critical points :
  - Chip integration in PCB
  - SLAB assembly (gluing, thermal coupling, assembly procedure …)
  - Square events
- Hamamatsu (realistic design) wafer will be sent to various locations
  - UK : gluing test
  - LPC : crosstalk measurements
  - Prague : leakage measurements

Backup slides about square events

Analytic model of guarding crosstalk

Modéle pur guardrings





$$T = T_{elec} \times T_{pix} \times (T_{seg} \times T_{ss})^{N_{seg}} \times T_{seg} \times T_{inj}$$

Measurement electronics — Crosstalk — Charge injector

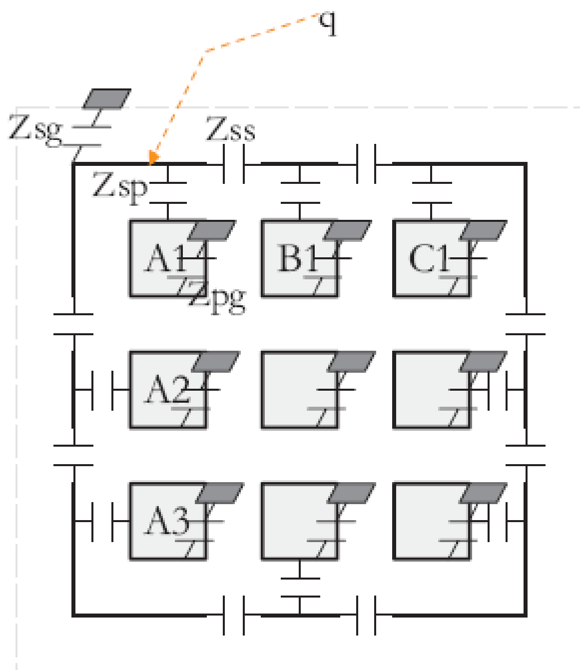
Figure 11: Model response (set for copper-epoxy model)

Pixel	Continuous	1 cm	3 mm
A1 (ref)	0	0	-14.5
A2	-6	-21.6	-75
A3	0	-34.6	-138

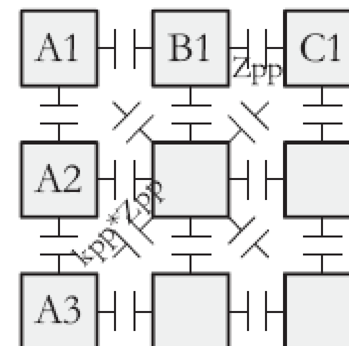
Couplings are modeled with quadripoles filters
the number of segment Nseg appears

Includes the whole measurement chain (band pass filter)

Electrical simulation : SPICE



Pixel crosstalk		
0	-23.6	-46.6
-23.6	-37.5	-58.6
-46.6	-58.8	-72.3



+

Within the same simulation

=

Continuous			1 cm			3 mm		
0	-4.4	0	0	-18.3	-35.6	-11.5	-36.0	-49.8
-4.4	-14.1	-4.4	-18.3	-34.2	-51.2	-36.0	-49.0	-71.1
0	-4.4	0	-35.6	-51.2	-64.3	-49.8	-71.1	-85.7

dB

Guradring + pixel to pixel contribution to crosstalk are included

Copper-Epoxy hardware models

How to be confident in all these simulations ?

Investigate on segmented design without real wafers ! (first)

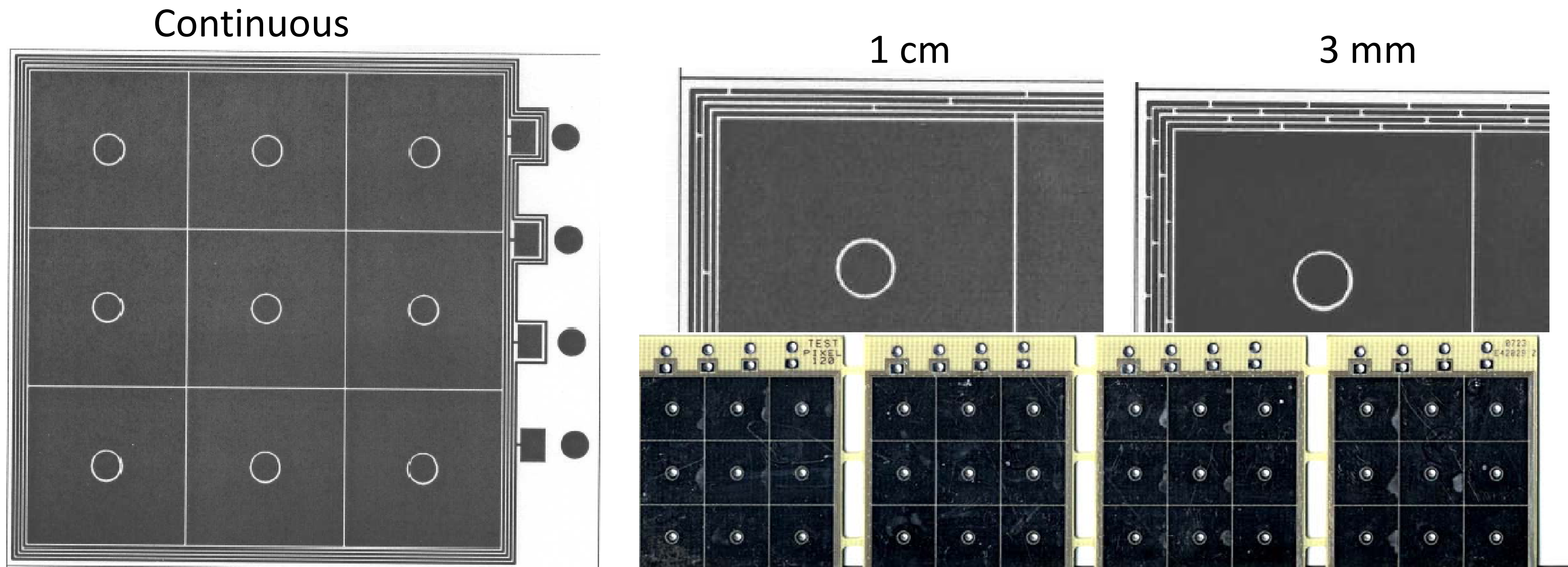
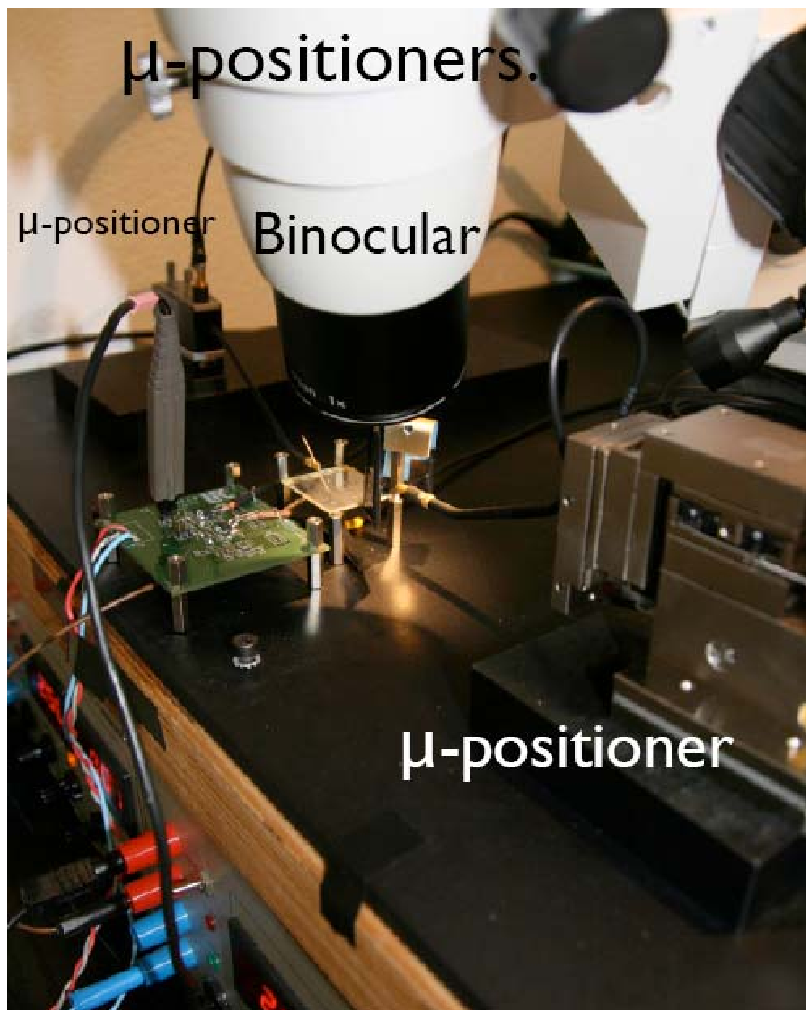


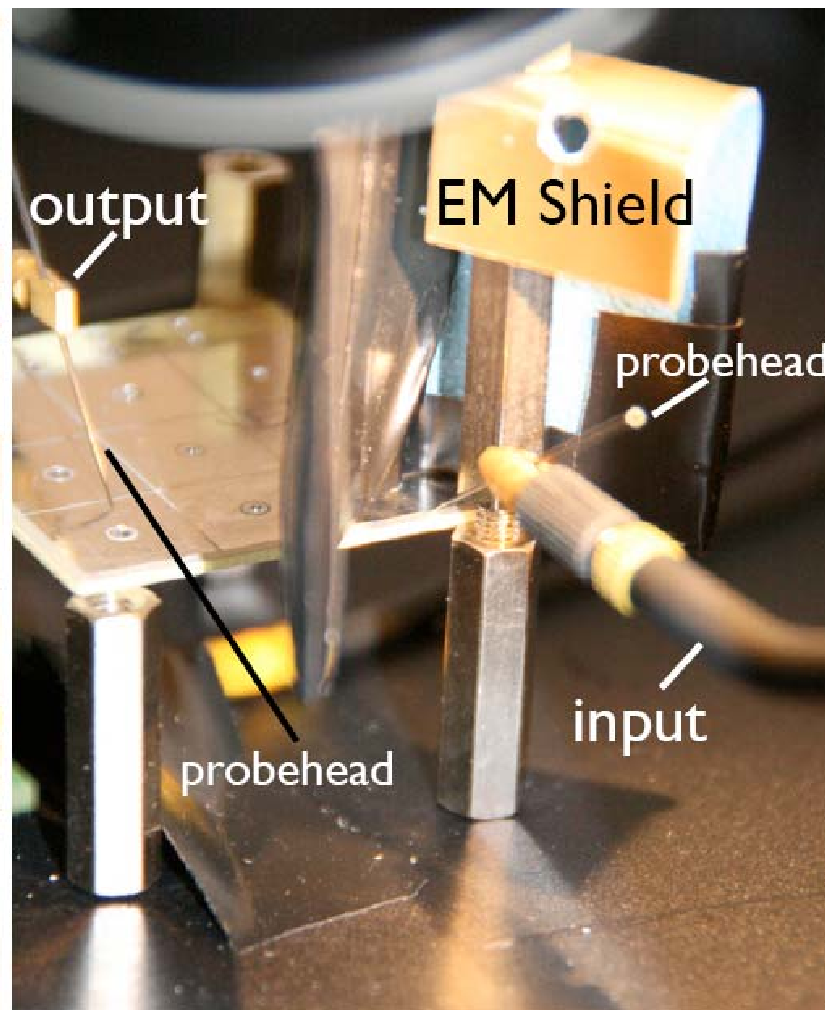
Figure 6: Copper epoxy made wafer model featuring 3x3 pixels and 4 continuous guardrings.

Then perform measurements on real wafers if the crosstalk hypothesis is verified

Test bench LPC

For crosstalk measurements on sensors (real or not)





M. Benyamna/R. Cornat/F. Morisseau

Measurements of printed circuit models

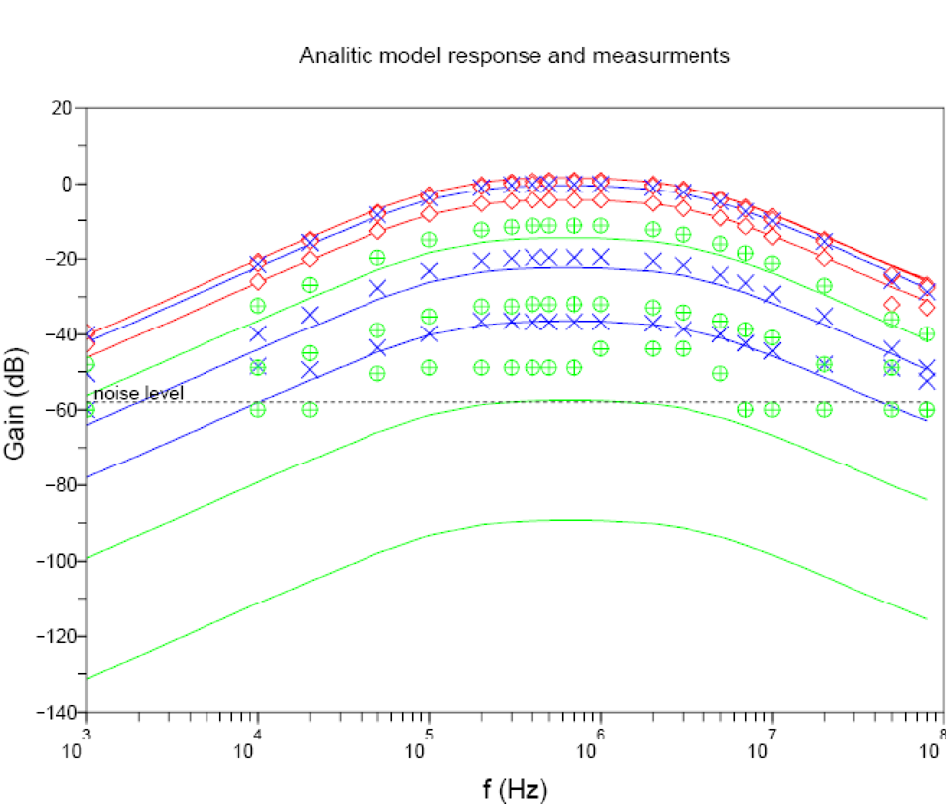
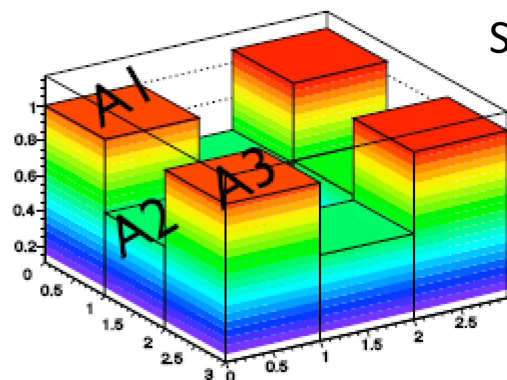
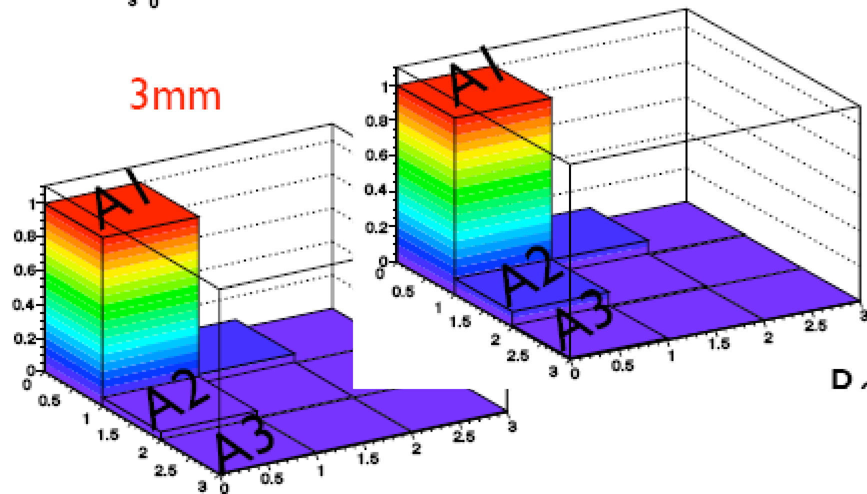


Figure 15: Model response and measurments made on hardware model

Continuous



Same as in TB data



Raw data (no corrections applied) fit well with analytic model response

- Limited by noise level of measurement electronics (to be improved)
- Except for 3 mm segments

Conclusion on printed circuit models

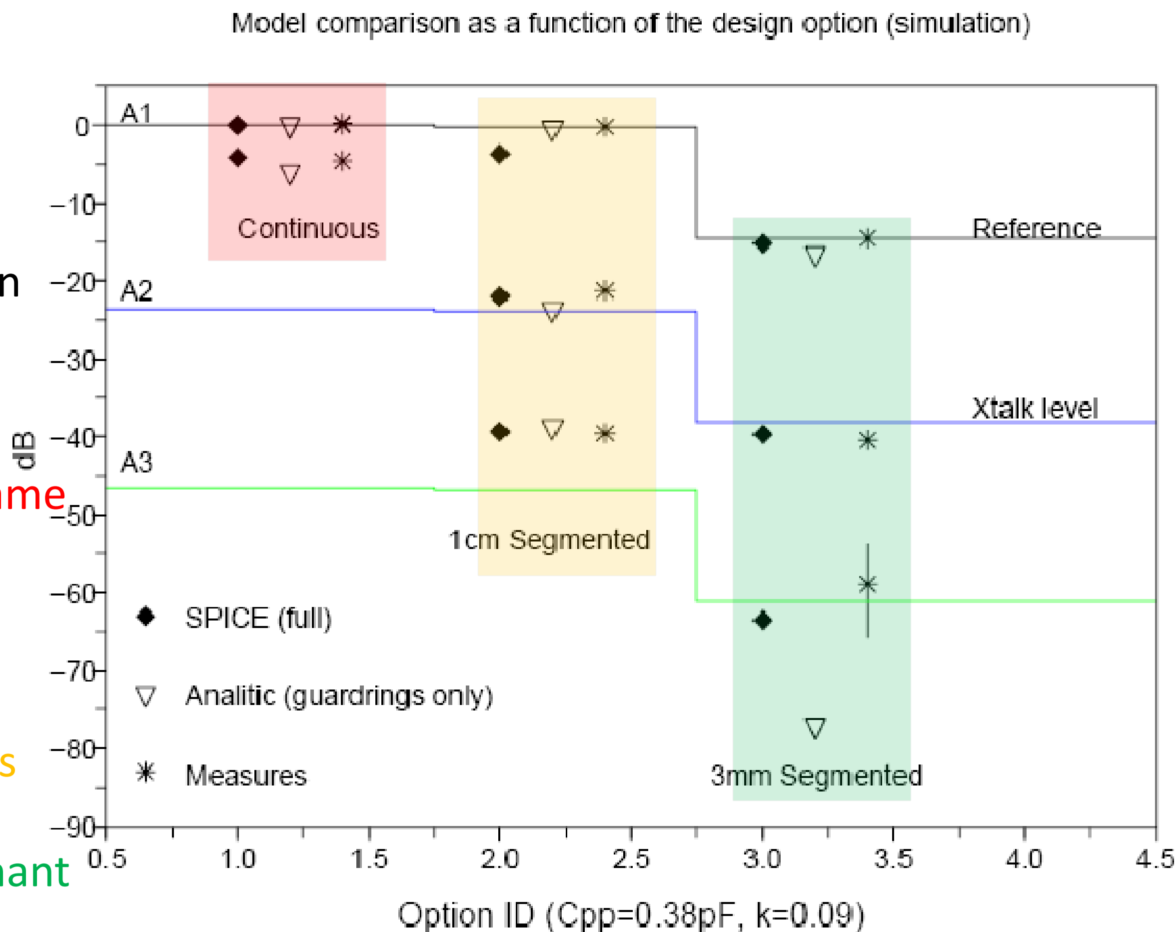
Electrical simulation includes :
•Guardring crosstalk
•Pixel to pixel crosstalk

Analytic model explains guardring related crosstalk
•Crosscheck Electrical simulation
•Gives expected contribution

Guardring crosstalk measured for continuous shape has the same behavior as in the TB data

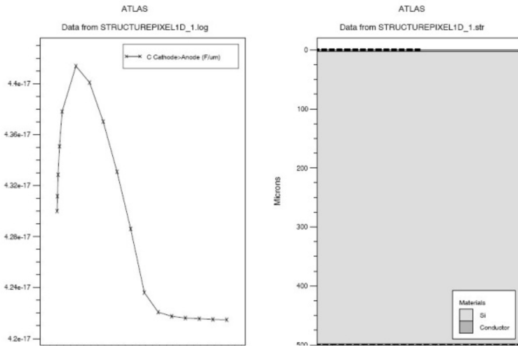
Guardring and pixel to pixel crosstalk have the same contribution for 1cm segments

Pixel to pixel crosstalk dominant for 3mm segments



Segmented topology should limit square events effects to the pixel to pixel crosstalk

Silicon Simulation

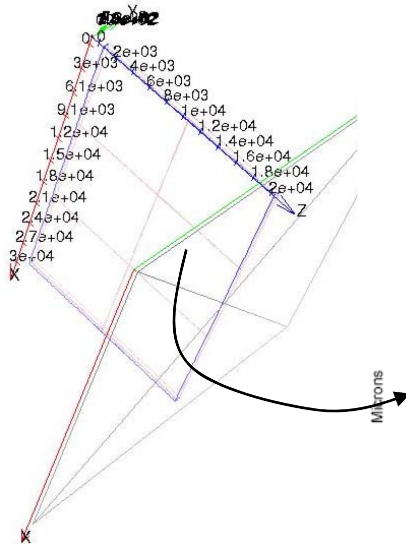


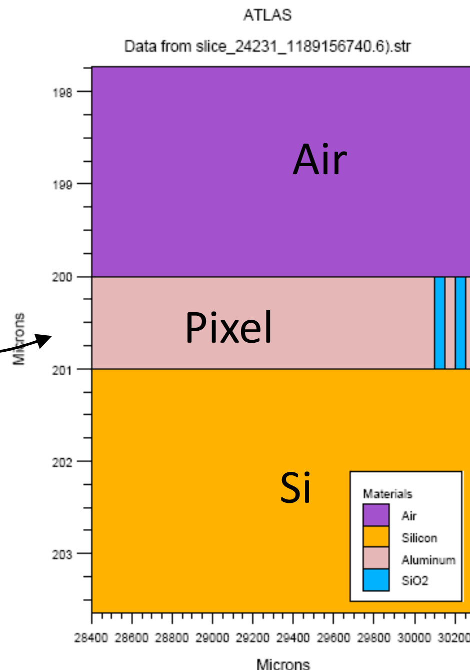
First step to check capacitance values between pixels, guardrings, substrate

Then back annotate to SPICE simulation

ATLAS
Data from 4STRUCTURE_6PIXEL3D_4guard_1.str

Simulated Cap. Values are within a 20% range from expected values calculated with first order formula





3D simulation are ongoing to take into account border effects

Second step to verify if guardrings still act as guardrings…

Extrapolation to real sensors

Name	First order formula	Set 1	Set 2	Set 3
Cpp		0.4 - 0.6 pF	0.8 - 1 pF	0.8 - 1 pF
Cpg	$\varepsilon_r \varepsilon_0 \cdot \frac{L_p^2}{W_t}$	4 - 5 pF	20 pF	33 pF
Csp		$\approx 60\, pF/m$	$\approx 80\, pF/m$	$\approx 80\, pF/m$
Csg	$\varepsilon_r \varepsilon_0 \cdot \frac{L_s * t_s}{W_t}$	0.06 pF/cm	0.1 pF/cm	0.17 pF/cm
Css		0.04 pF	0.1	0.1
k_{pp}		0.086	0.04	0.04

Table 3: Model parameters related to the geometry of the DUT and crosstalk coupling

First order formula to compute the parameters of the models

Si 500 µm

Continuous			1 cm			3 mm		
0	0	0	0	-21	-43	-11	-40	-68
0	0	0	-21	-42	-62	-40	-57	-83
0	0	0	-43	-62	-80	-68	-83	-98

Si 300 µm

Continuous			1 cm			3 mm		
0	0	0	0	-20	-37	-4	-36	-67
0	0	0	-20	-44	-58	-36	-56	-85
0	0	0	-37	-58	-70	-67	-85	-103

Same trend as for printed circuit boards

But simulations assume a local hit : what if multiple hits (EM shower) ?

Are guardrings still act as guardrings (protection against breakdown) when segmented ?

Test sensors (OnSemi CZ)

Layout made at LLR