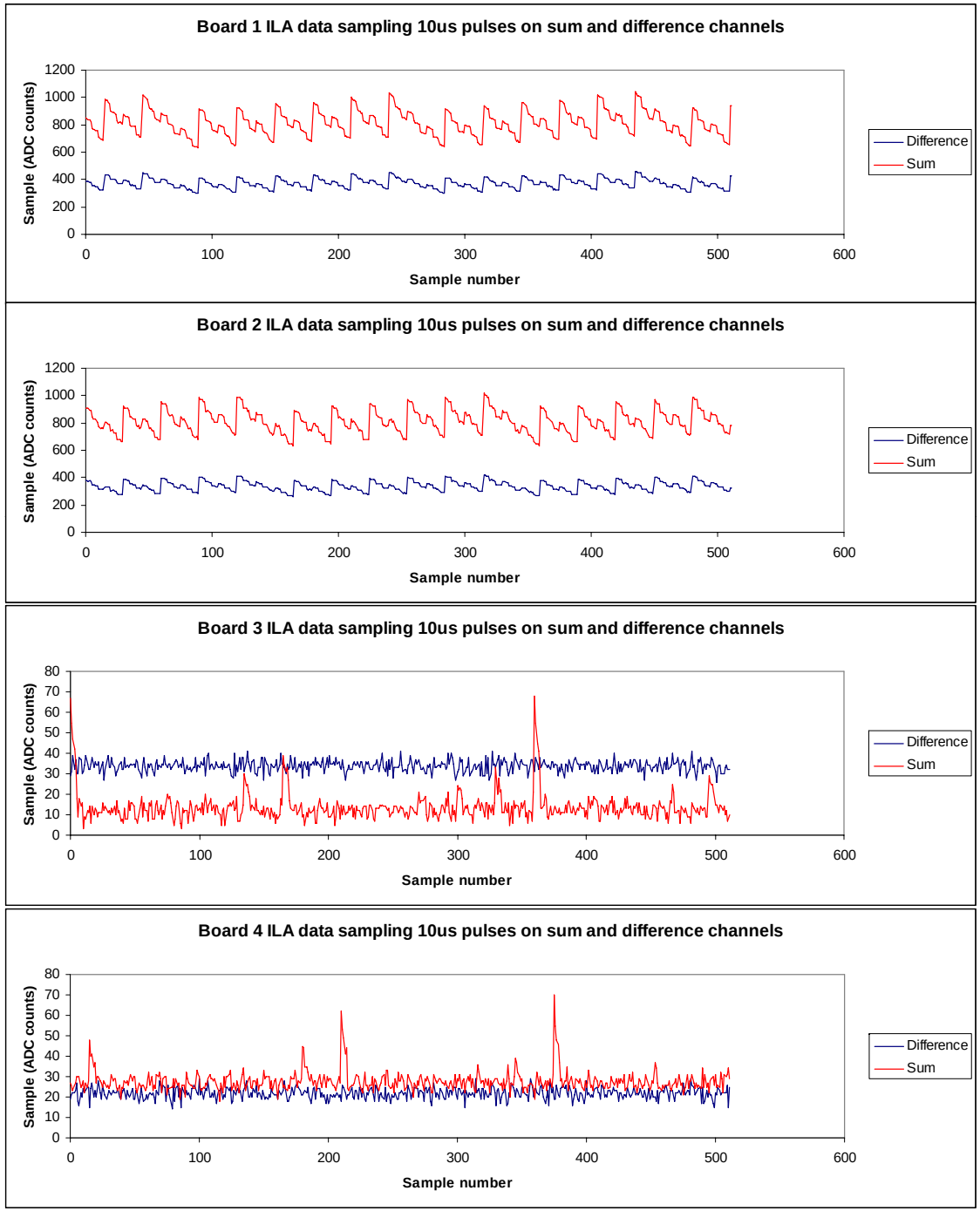
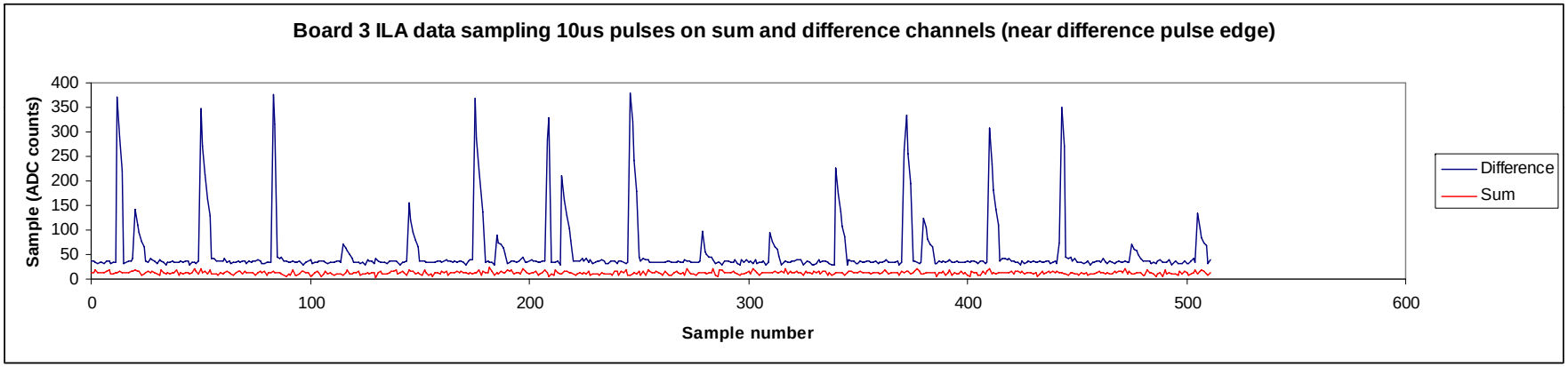
Digital board tests

- Difference seen between original boards (1 & 2) and new boards (3 & 4)
- Input 80mV square pulse to difference channel
- Input 160mV square pulse to sum channel
- Generated clocks and trigger on separate digital board
- Delayed trigger to sample away from pulse edges
- Sampled via ILA


Board 1 ILA data sampling 10us pulses on sum and difference channels
Sample (ADC counts)
Sample number
Difference
Sum
Board 2 ILA data sampling 10us pulses on sum and difference channels
Sample (ADC counts)
Sample number
Difference
Sum
Board 3 ILA data sampling 10us pulses on sum and difference channels
Sample (ADC counts)
Sample number
Difference
Sum
Board 4 ILA data sampling 10us pulses on sum and difference channels
Sample (ADC counts)
Sample number
Difference
Sum

- Using board 3, reduced trigger delay while watching ILA
- Near pulse edge, observe larger samples
- Only high frequencies reaching ADC?



Charge normalisation LUT tests

- Scanned input pulse amplitudes and feedback gain to produce the following: