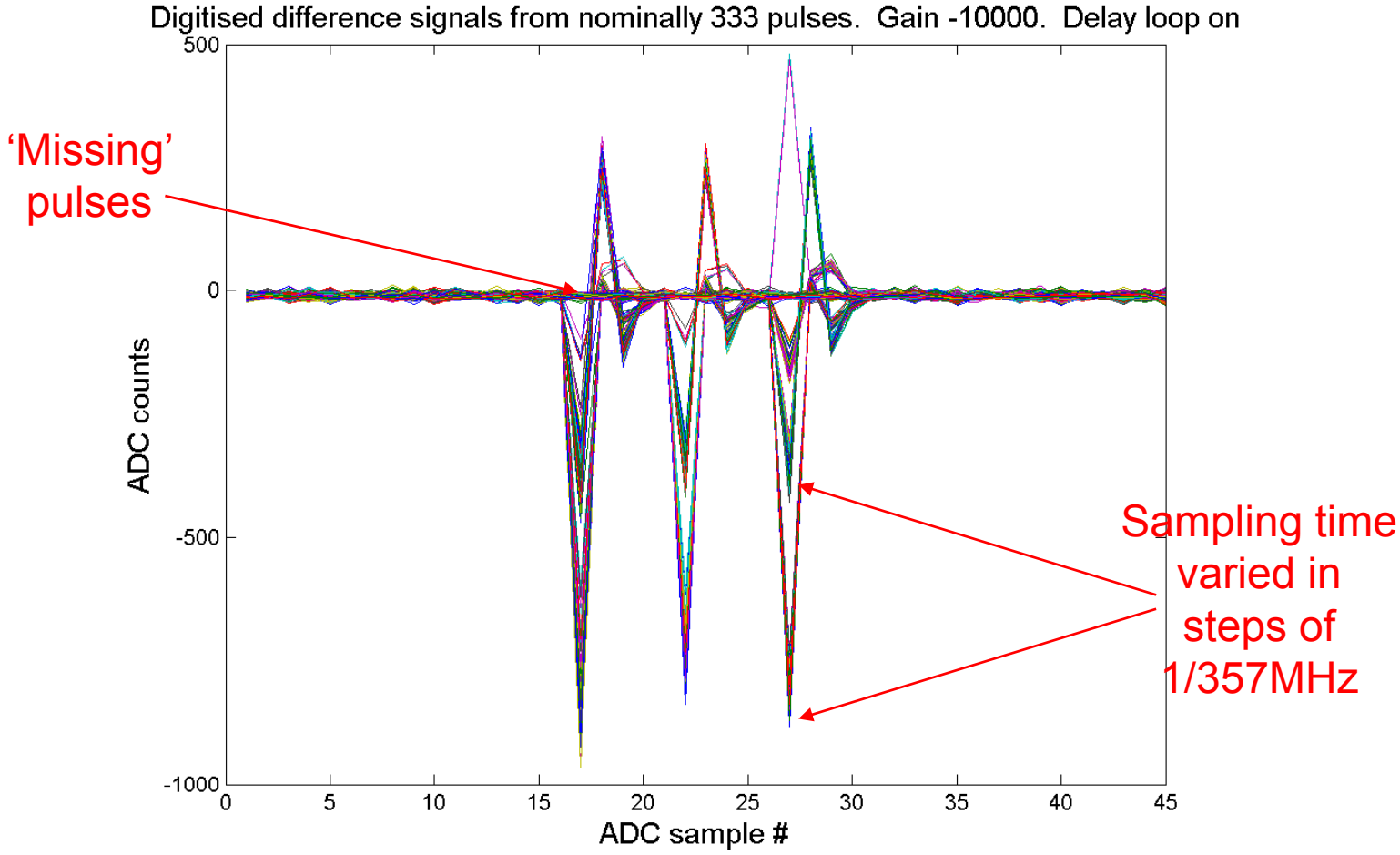
First report from FONT4 at ATF

Week of the 21st of April 2008

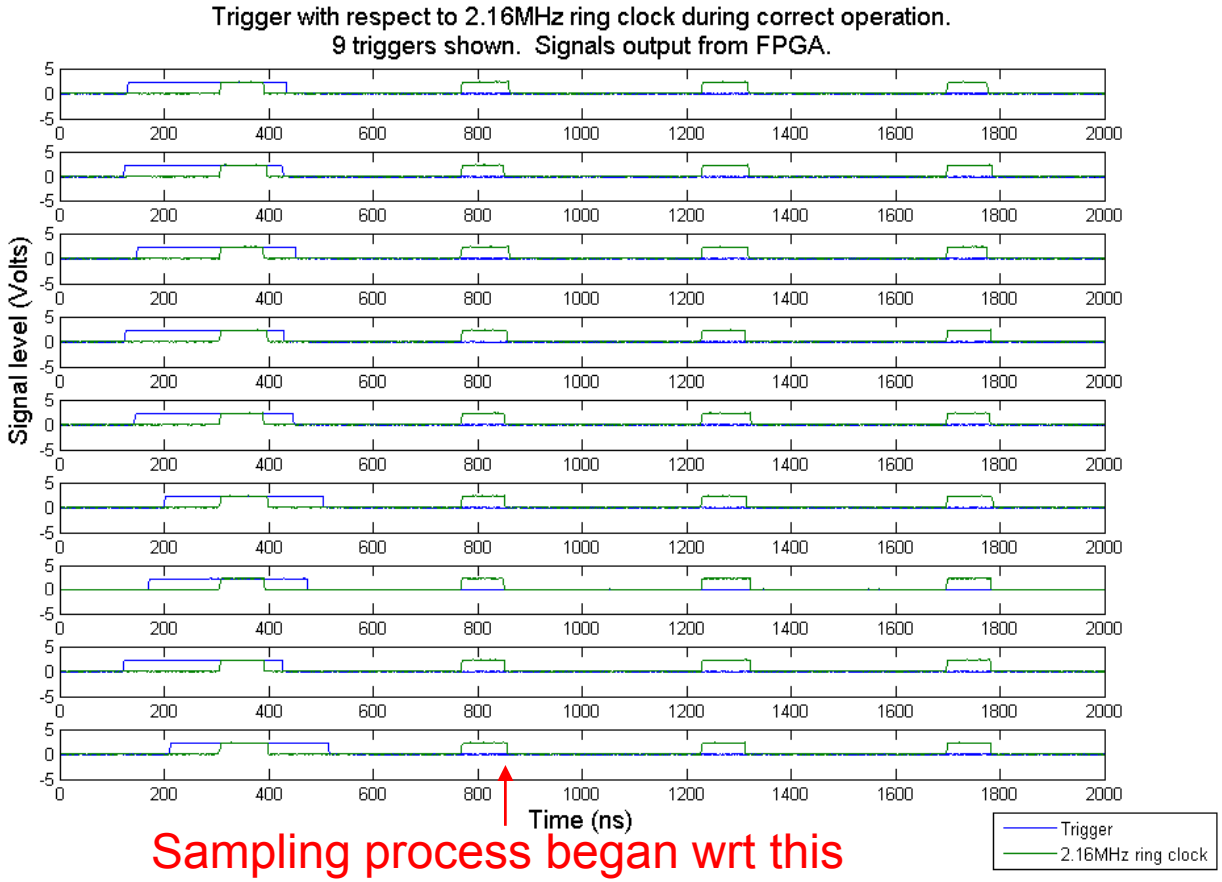
April 29th 2008

Sampling errors from March 2008

- Two independent sampling issues from March 08 trip



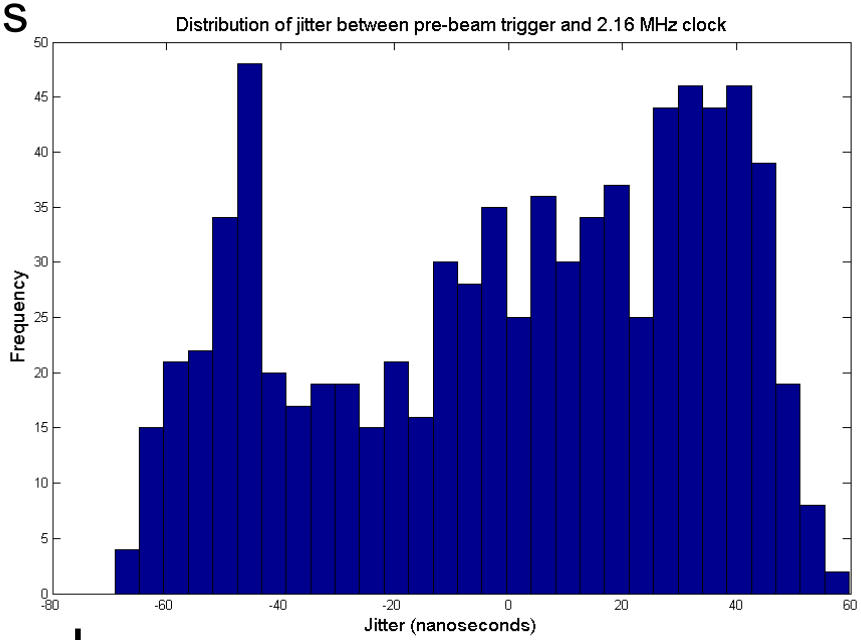
Digital board triggering



- Trigger selects correct ring clock cycle

Trigger jitter causes missing pulses

- Pre-beam trigger jitter wrt 2.16MHz ring clock ±60ns
  - c.f ring clock period of 463ns

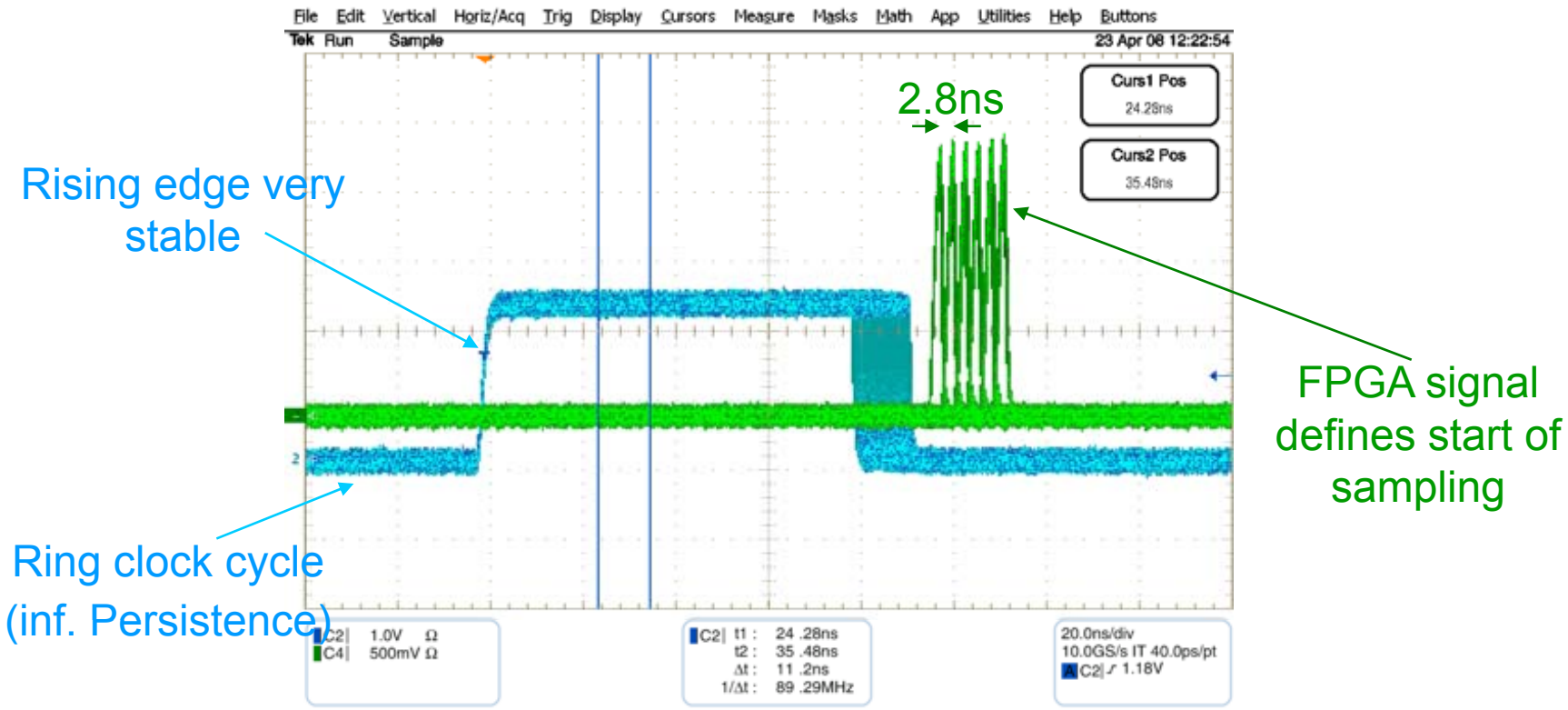


- Trigger close to ring clock edge

  → Wrong ring clock cycle sometimes selected
- Solution: implement trigger delay in firmware (to do)

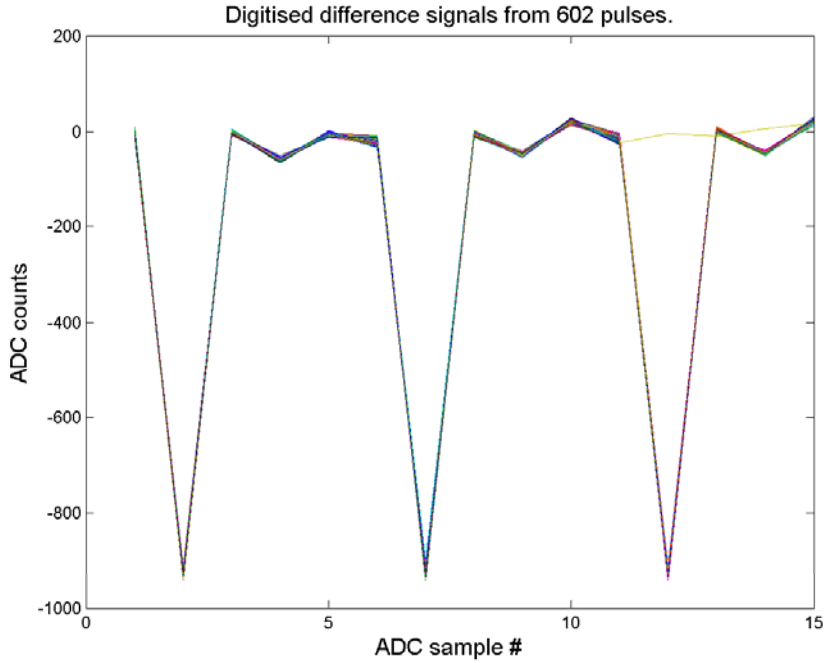
Sample time variation in 2.8ns steps

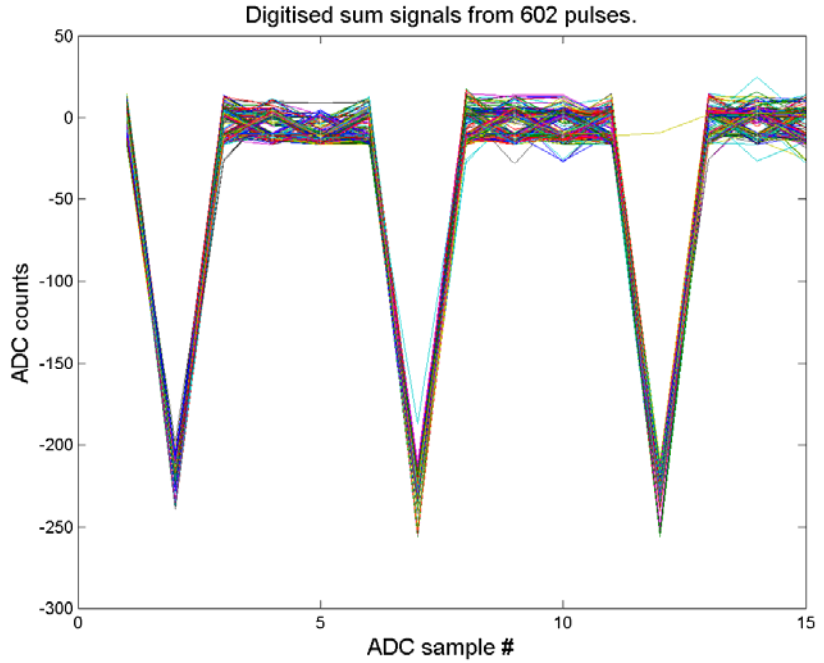
- We use 2.16MHz ring clock to begin sampling process
  - In March, cycles of 357MHz counted wrt falling edge
- ±6ns jitter on this edge (see below scope trace)



Experiment modification

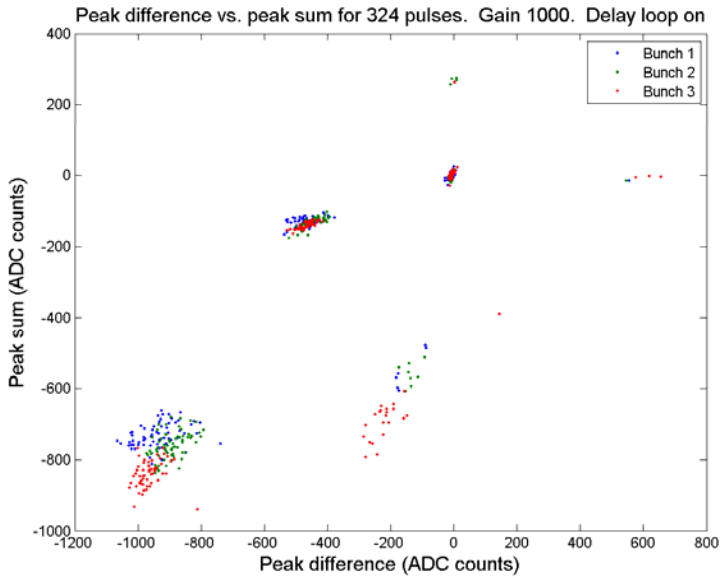
- Carefully timed pre-beam trigger
- Modified FPGA firmware (modification #1)
  - Sampling now begins wrt 2.16MHz rising edge
- Sampling issues resolved

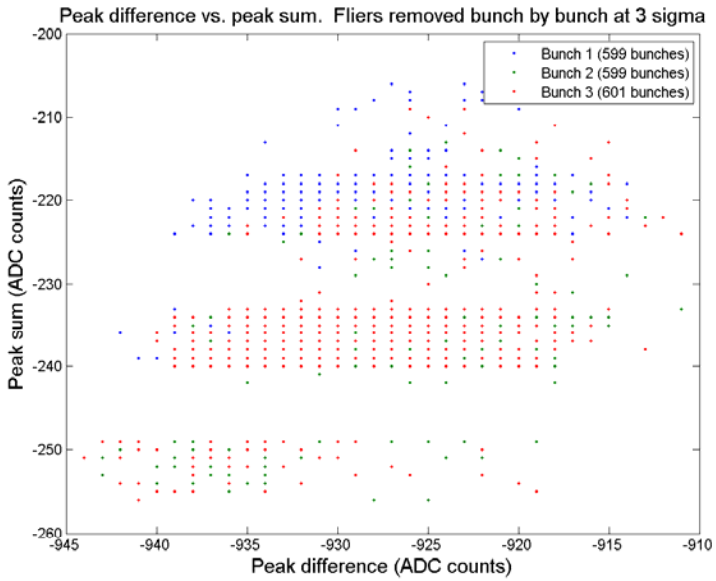




Further sampling analysis

- March data (left), modified firmware #1 (right)

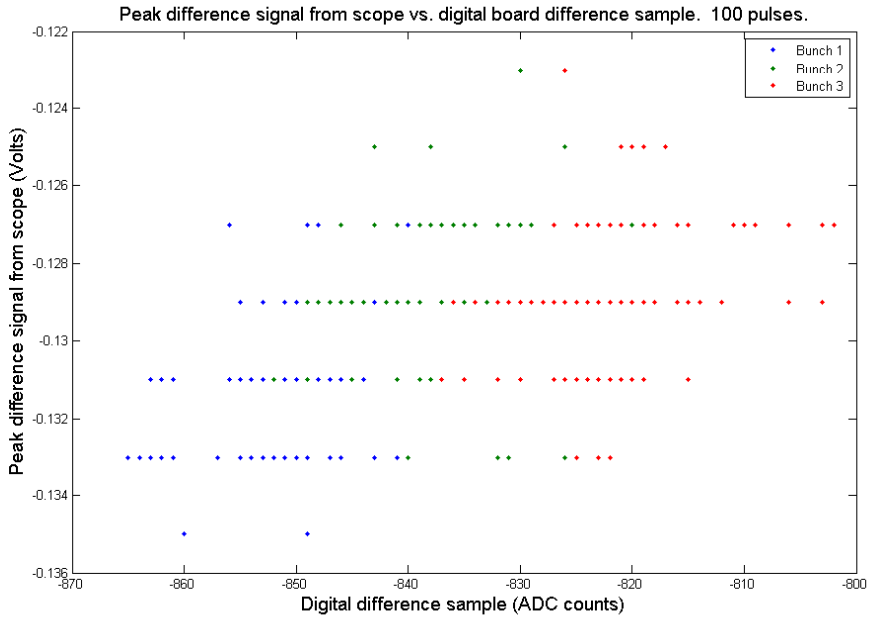




- New results much more sensible!

Further sampling analysis

- Split BPM processor output
  - Sampled with scope
  - Sampled with digital board

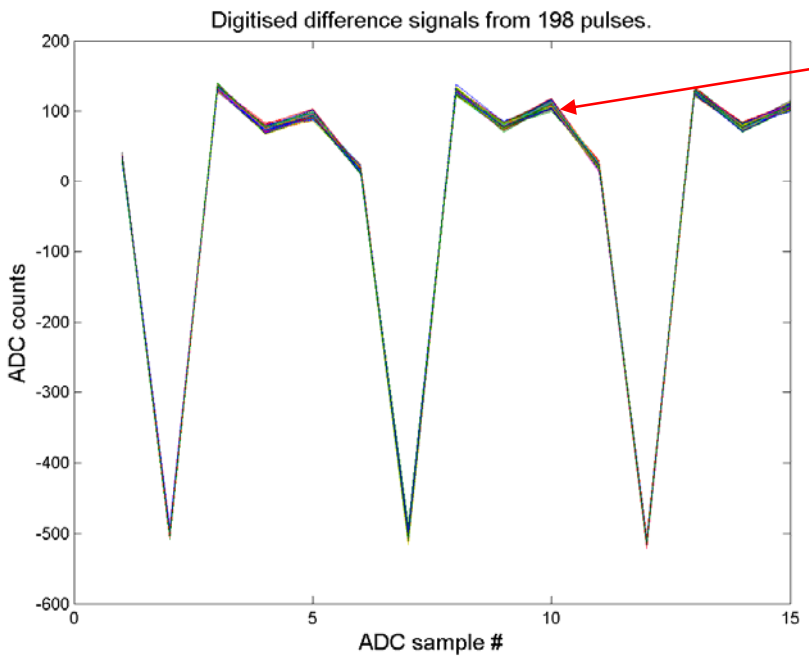


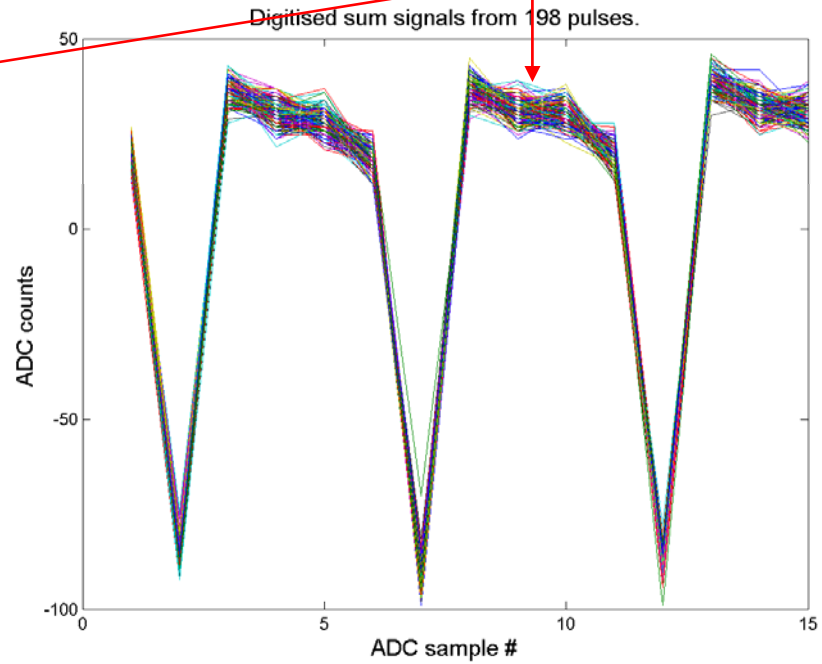
- Looks reasonable
  - More detailed analysis with integration and/or gaussian fitting

Investigation of digital board 3

- Prior to trip, difference between digital board 1st and 2nd generations noted
  - Ran board 3 with modified firmware #1
  - Slight difference from board 1, but still works

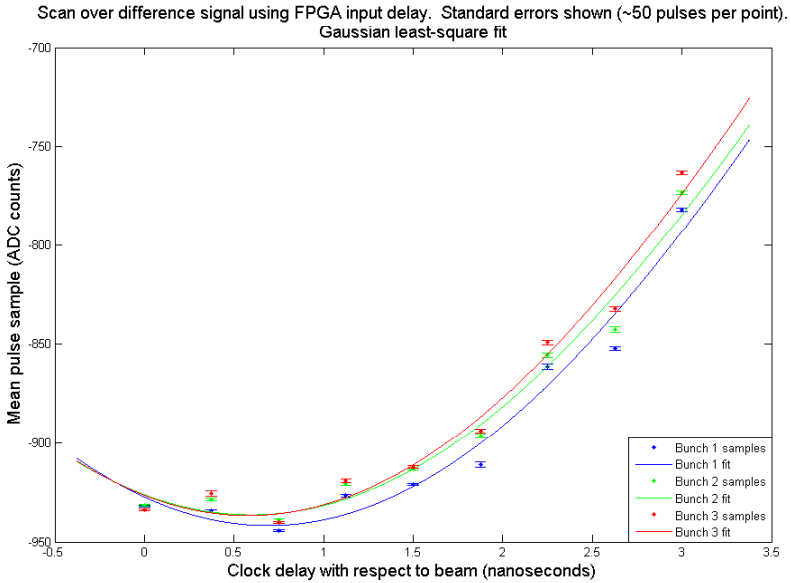
'Slanting' not present on board 1 data

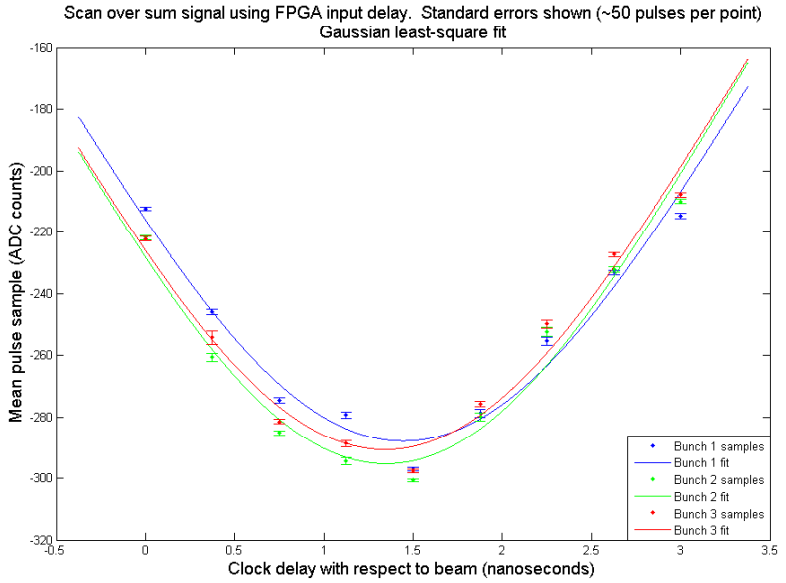




BPM processor pulse scan

- Scanned sum and difference signals by delaying clocks with respect to beam (used modified firmware #1)

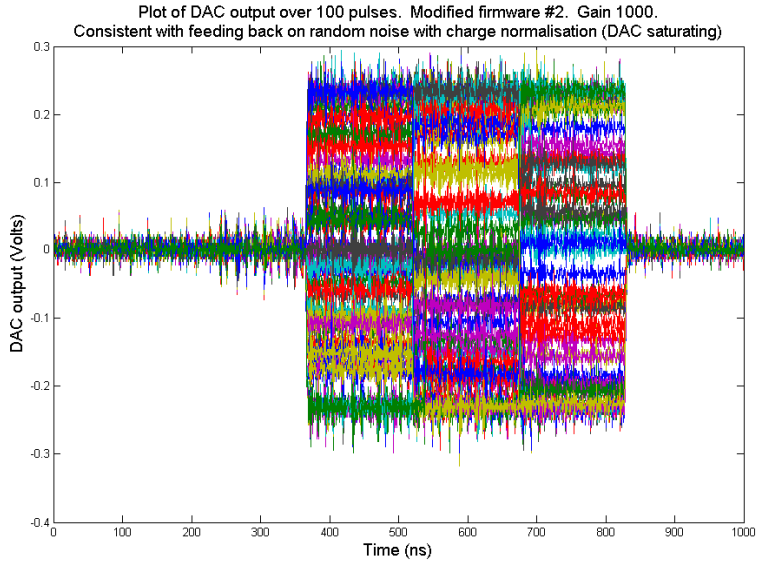




  - Systematic variation beyond standard errors visible
  - Gaussian fits give σ_Δ = 5.5 – 5.7 ns and σ_Σ = 2.7 ns
  - c.f scope data fits σ_Δ = 4.13 ns and σ_Σ = 2.68 ns
  - Consistent Δ vs. Σ time offset of 0.76ns (due to BPM processor)

Feedback investigation

- Now for the bad news…
- Ran feedback without driving kicker while monitoring DAC
  - Modified firmware at Glenn's suggestion (modified firmware #2)
  - Intended to correct for DAC timing issues



- Most likely explanation is wrong sample sent to DAC

Priorities before May

1. Main priority is DAC timing
   - MUST ensure that correct feedback signal is generated
   - I will pursue this via simulation and tests using ATF signals
   - I'll also liaise with Glenn on this
2. Digital DAQ issues
   - A jury-rigged DAQ was used this trip
   - It still had issues in that it didn't operate consistently
   - Some conditional effect is the cause: it operated 100% in March!
3. Trigger delay in firmware