

Ns Timescale Beam Feedback Systems

for warm and cold linear colliders

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Intra-train Beam Feedback

Bunch-by-bunch feedback within bunchtrain

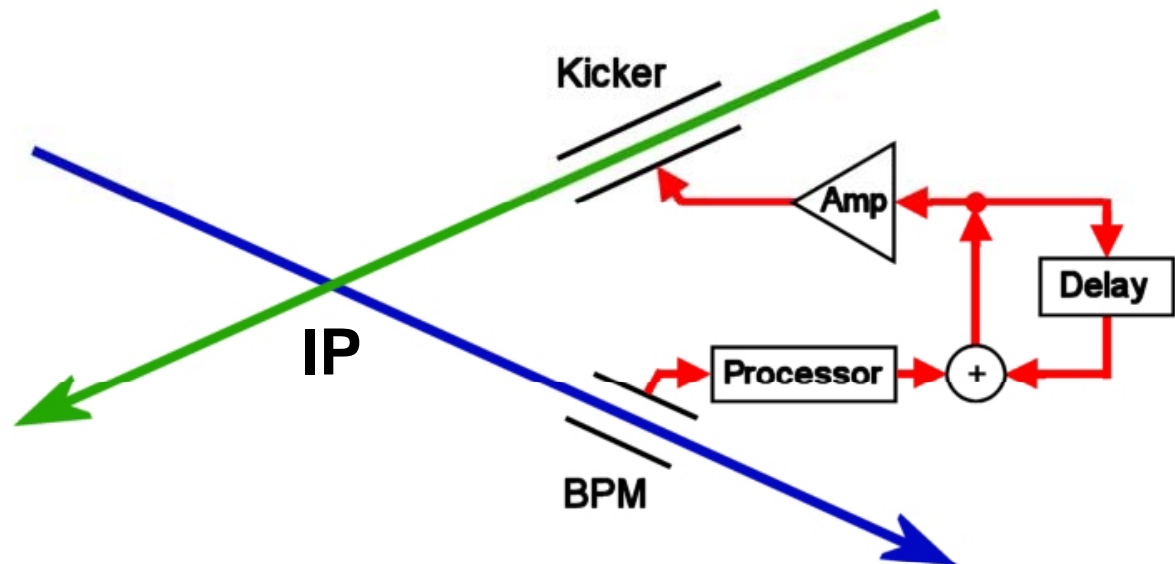
- **Interaction point collision feedback**
- **Linac train-straightener**
- **Ring-to-main linac feed forward ...**
- **Each system feedback needs to be integrated into global machine feedback strategy**

Intra-train feedback system - concept

Last line of defence against relative beam misalignment

Measure vertical position of outgoing beam and hence beam-beam kick angle

Use fast amplifier and kicker to correct vertical position of incoming beam



FONT:
Feedback On
Nanosecond Timescales

FONT Collaboration

Oxford + Daresbury:

Philip Burrows

Glenn Christian

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Ben Constance

Robert Apsimon

SLAC, KEK, DESY, CERN

Philip Burrows



Eurotev Goals

Design/operation of IP feedback system in context of 'start-to-end' simulations

- covered in ILPS work package (see Resta Lopez talks)

Prototype intra-train FB hardware system

- covered in BDS work package

Context

When Eurotev was first considered the linear collider world looked different:

NLC/JLC: 192 bunches separated by 1.4 ns

TESLA: 2820 bunches separated by 337 ns

CLIC: c. 100 bunches separated by c. 0.7 ns

For bunch-by-bunch FB the 'warm' machines are much more challenging!

FONT work started in context of ALL ANALOGUE FB;

DIGITAL FB work was started after adoption of 'cold' technology for ILC

FONT Analogue Feedback Systems

- NLCTA: 65 MeV beam, 170ns train, 87ps bunch spacing

FONT1 (2001-2):

First demonstration of closed-loop FB: latency 67ns
10/1 beam position correction

FONT2 (2003-4):

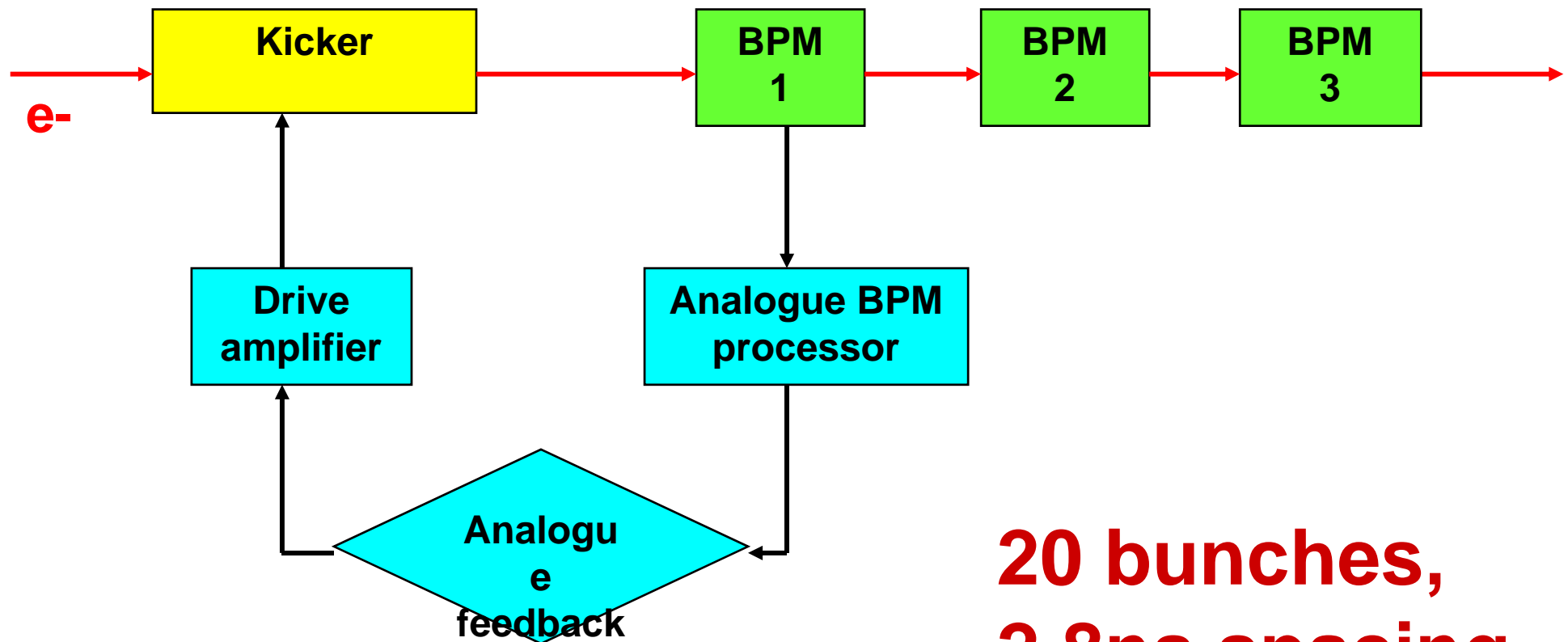
Improved demonstration of FB: latency 54ns
real time charge normalisation with logarithmic amplifiers
beam flattener to straighten train profile
solid-state amplifier

- ATF: 1.3 GeV beam, 56ns train, 2.8ns bunch spacing

FONT3 (2004-5):

Ultra-fast demonstration of FB: latency 23 ns
3 stripline BPMs
high-power solid-state amplifier

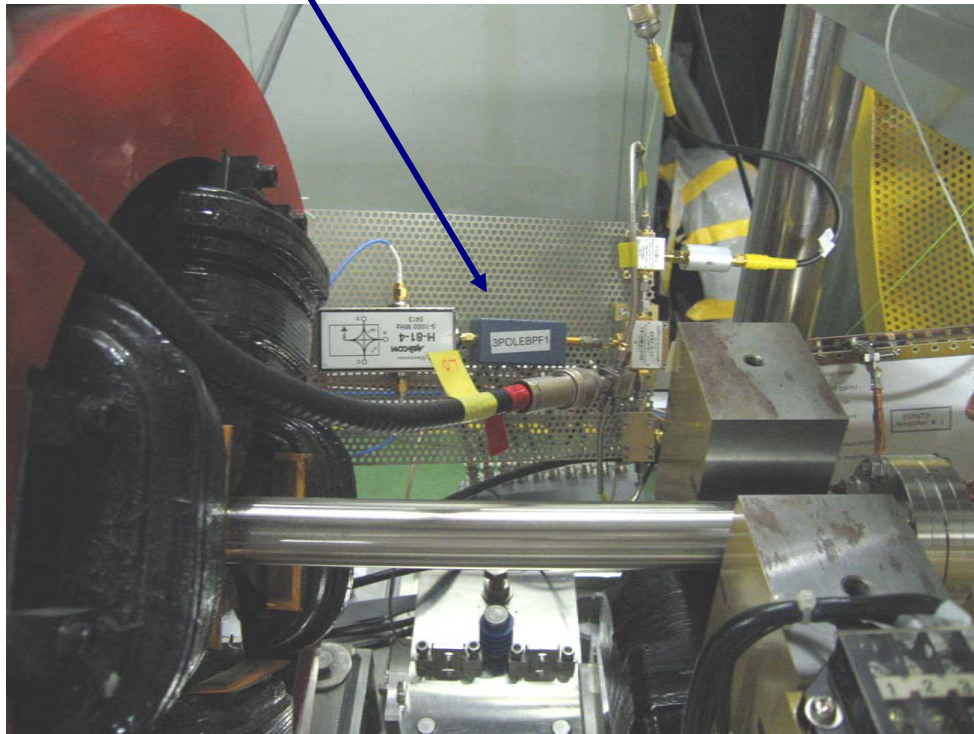
FONT3 prototype at KEK/ATF



**20 bunches,
2.8ns spacing**

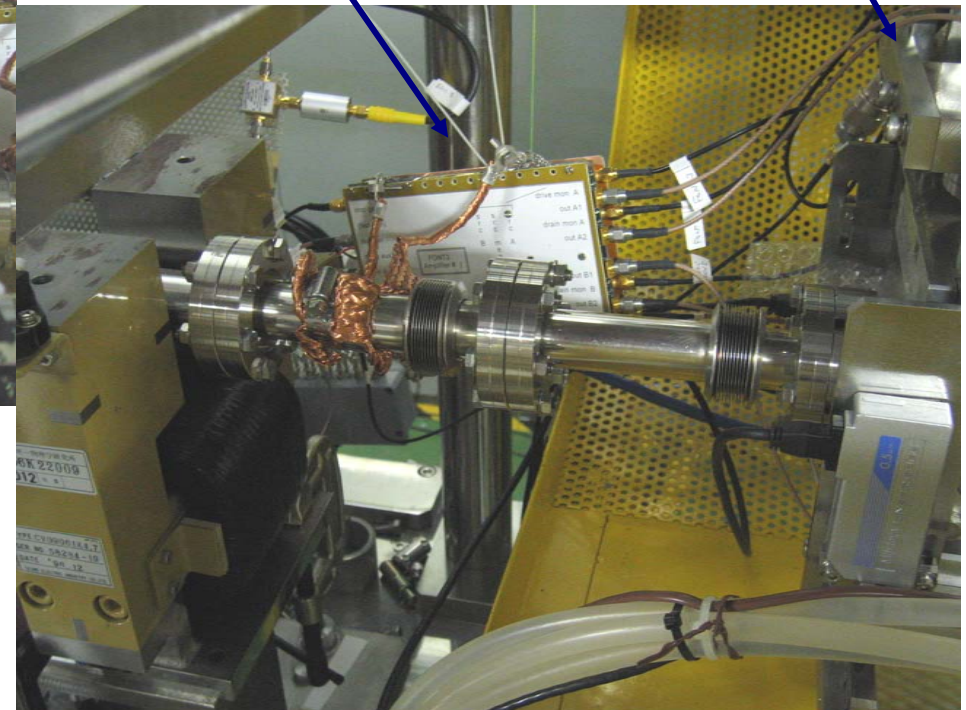
FONT3: BPM processor + amplifier/feedback installation in ATF beamline

BPM processor board



Amplifier/FB board

FEATHER kicker



FONT3: latency budget

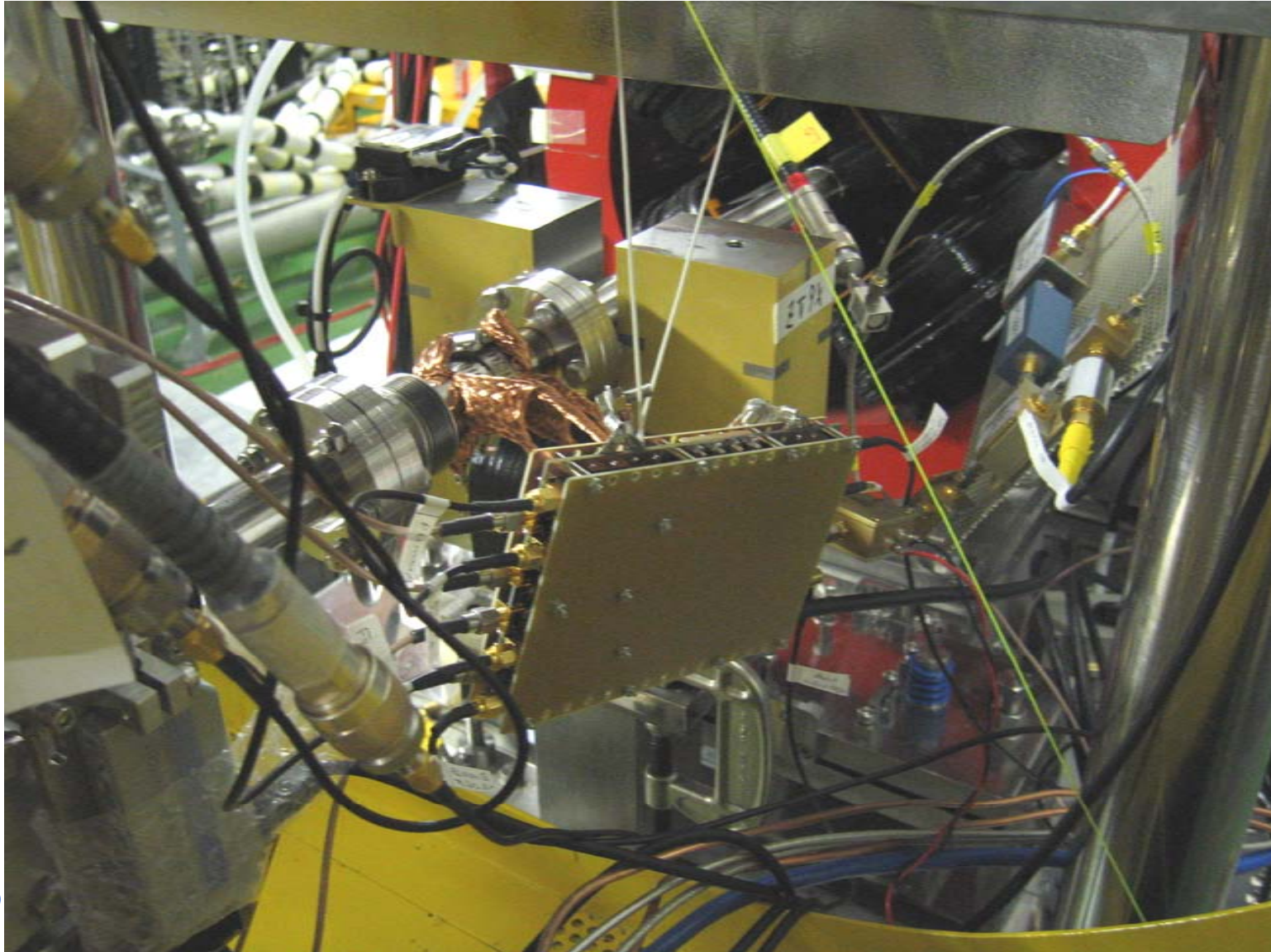
- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 6ns
- **Irreducible latency: 10ns**

- BPM processor: 5ns
- Amplifier + FB: 5ns
- **Electronics latency: 10ns**

- **Total latency budget: 20ns**

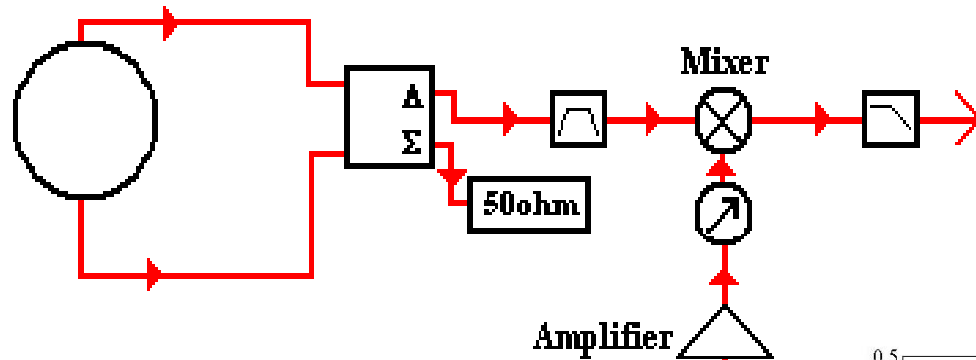
Will allow $56/20 = 2.8$ periods during bunchtrain

FONT3: Beamline Installation



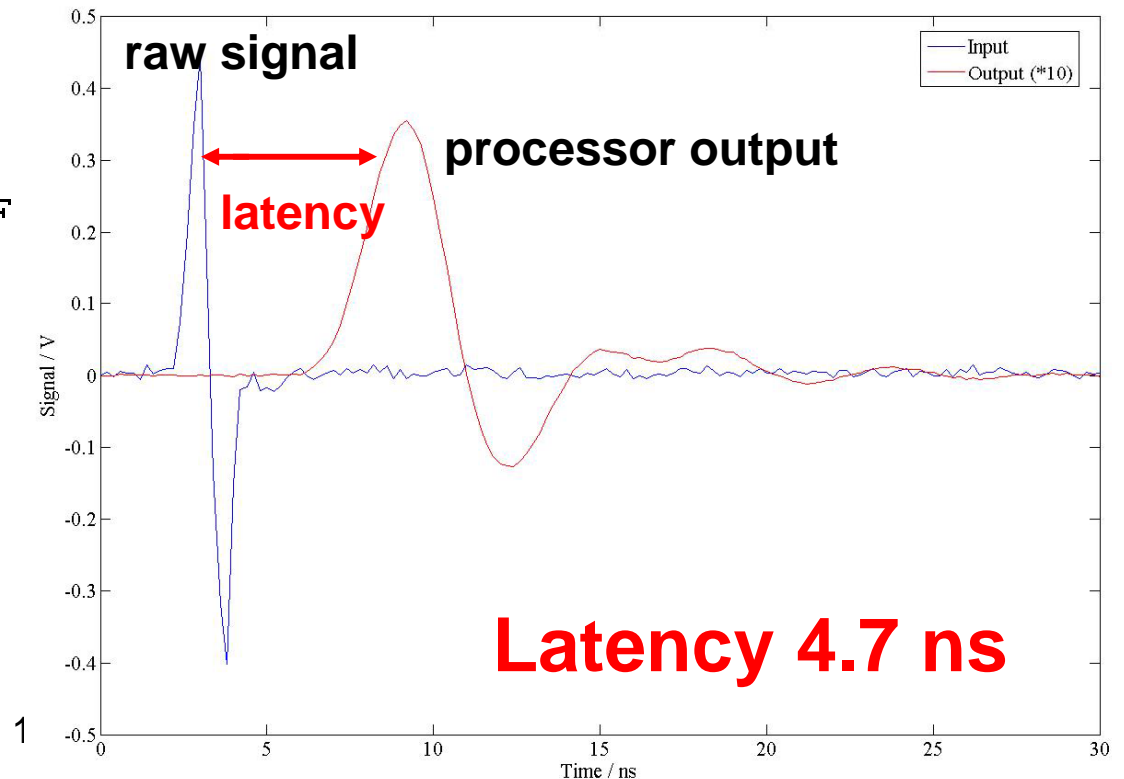
FONT3: BPM processor latency measurement

(single bunch, March 2005 beam tests)



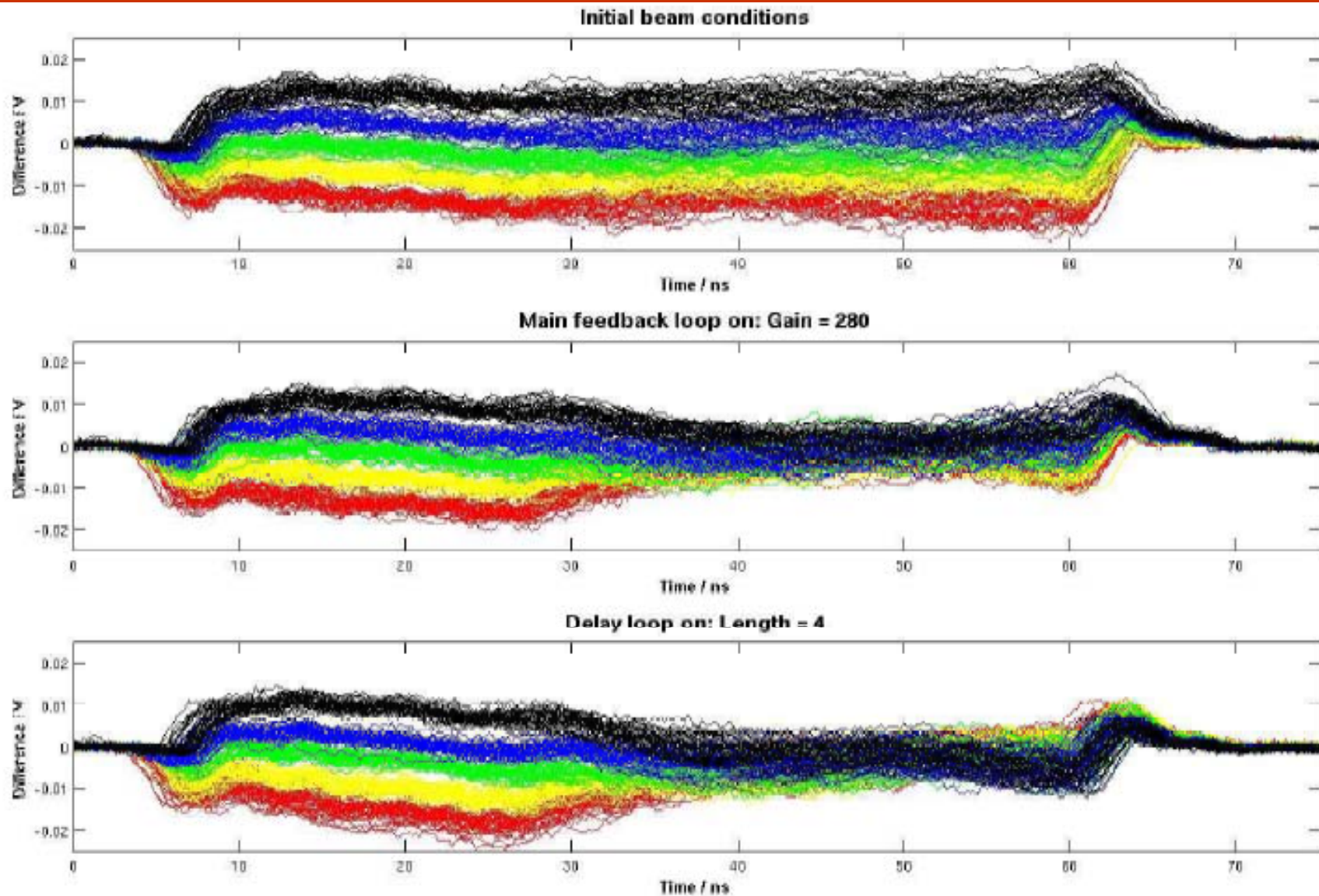
Single
stage
down-mix
to baseband

Amplifier
Locked
714MHz
from ATF

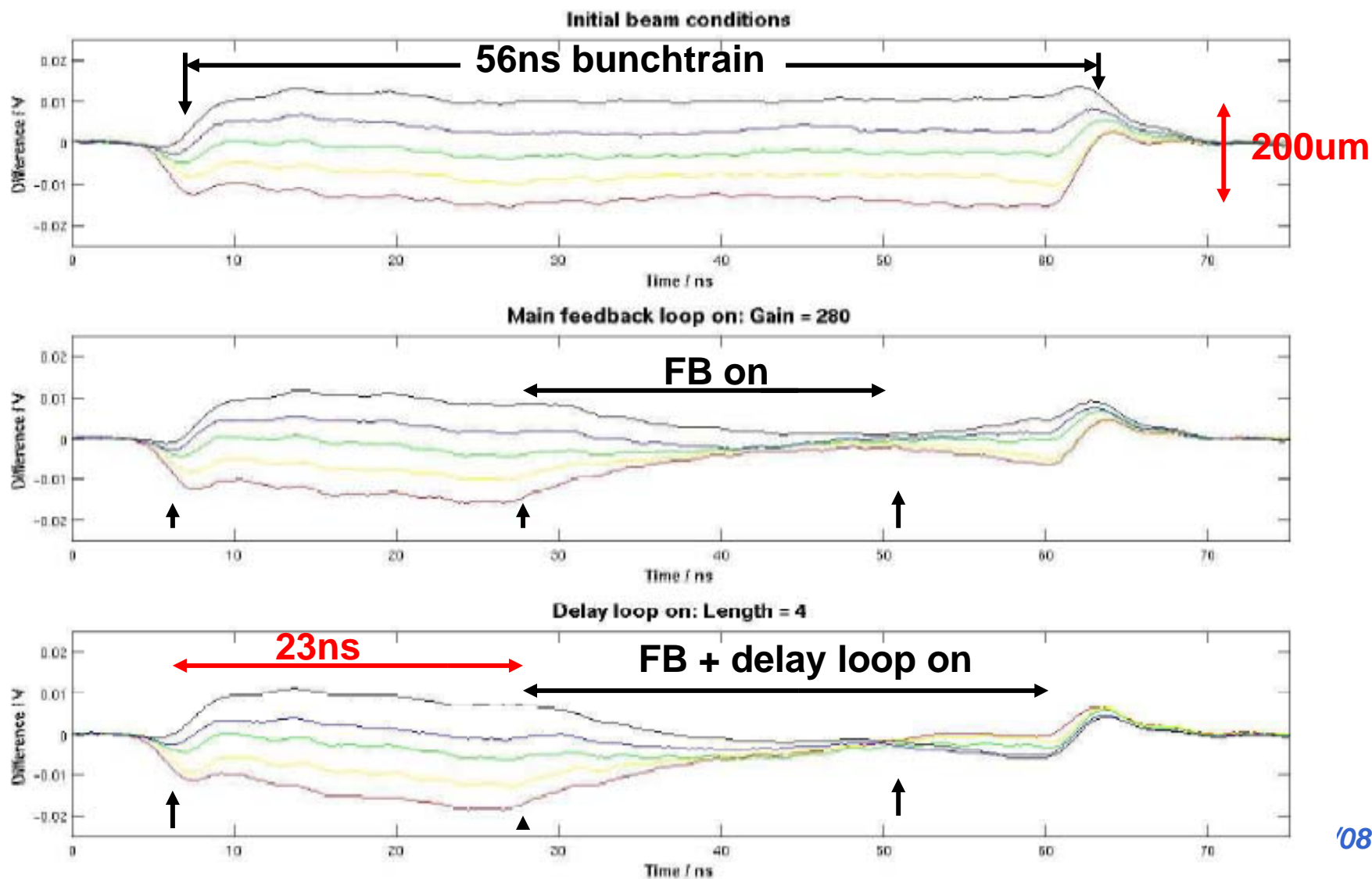


FONT3: Results (June 2005)

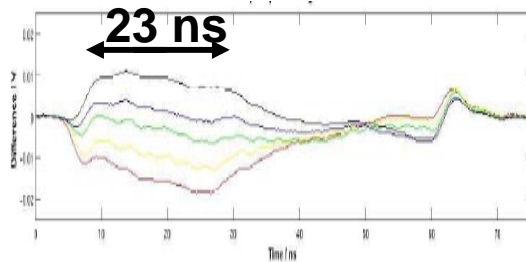
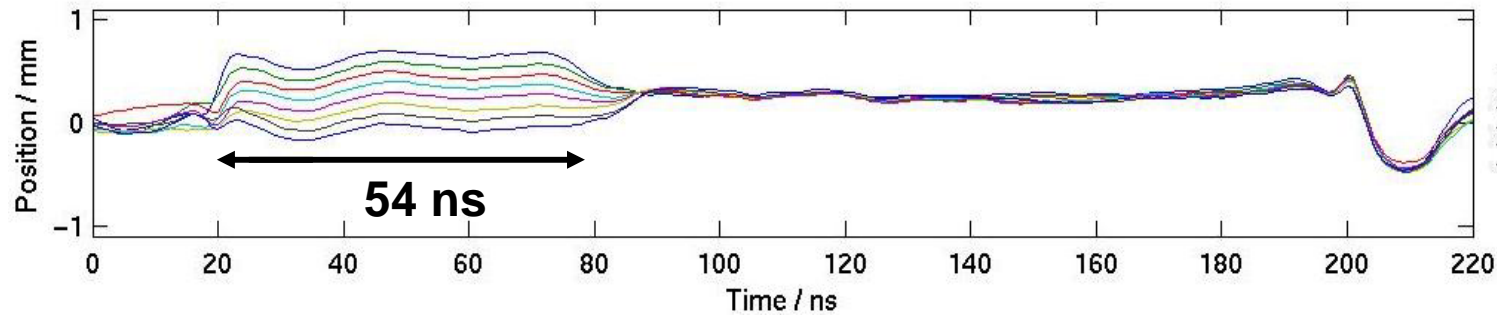
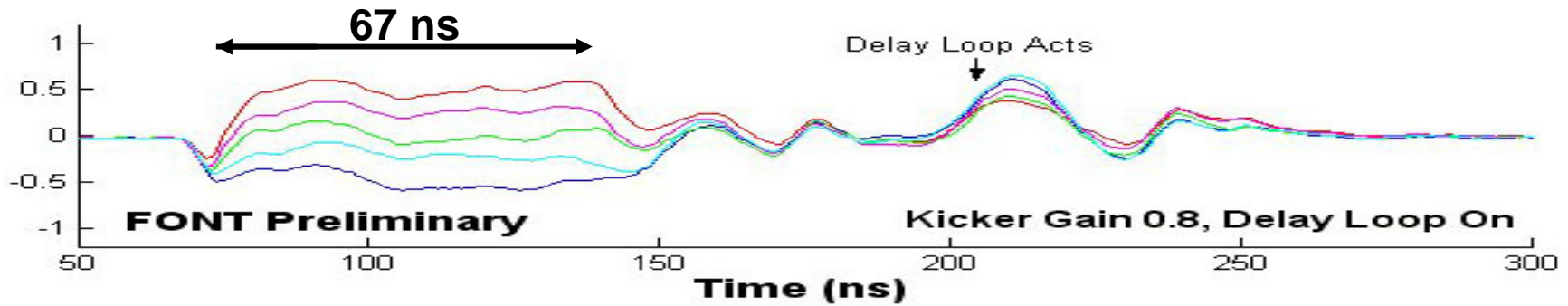
40 pulses per position setting



FONT3: Results (June 2005): Delay-loop feedback w. latency 23 ns

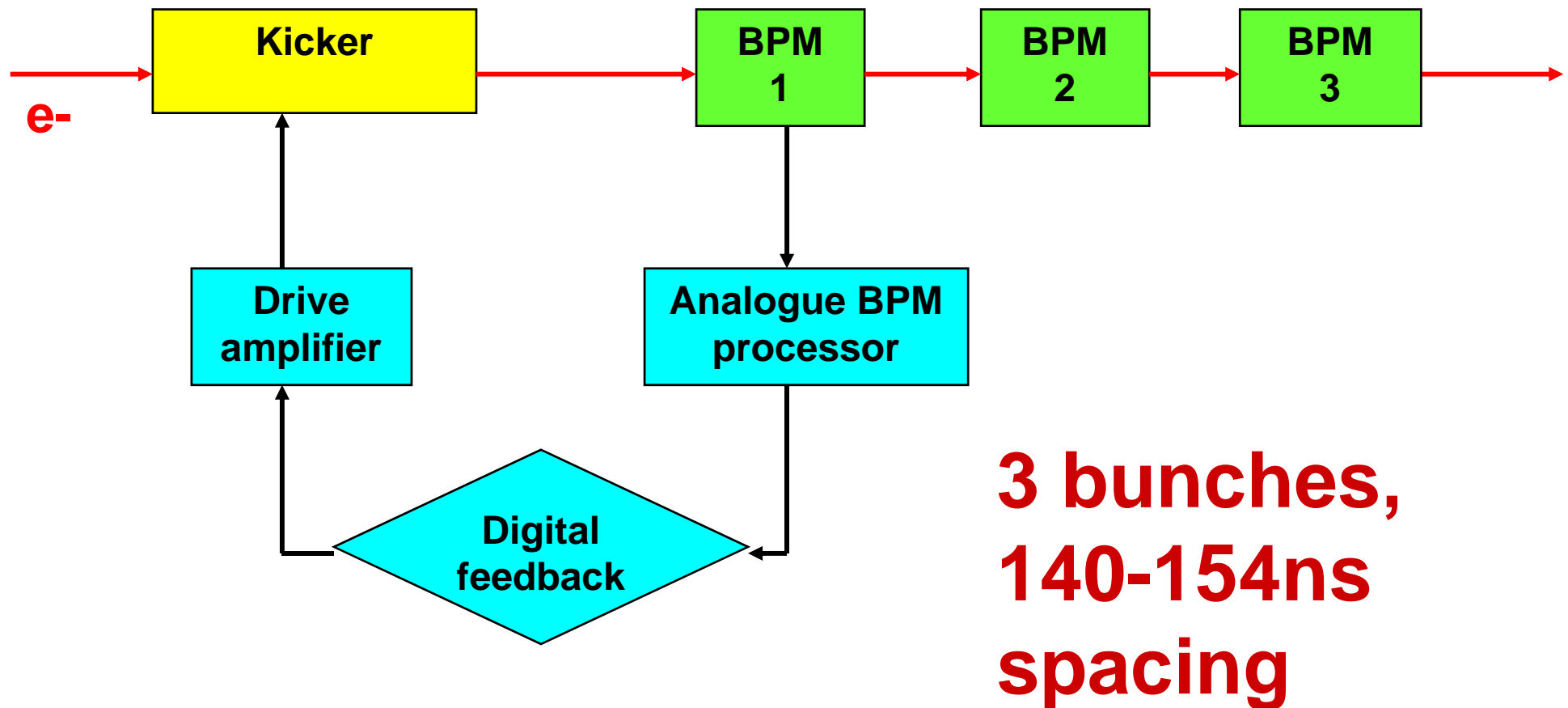


Analogue FB: Summary

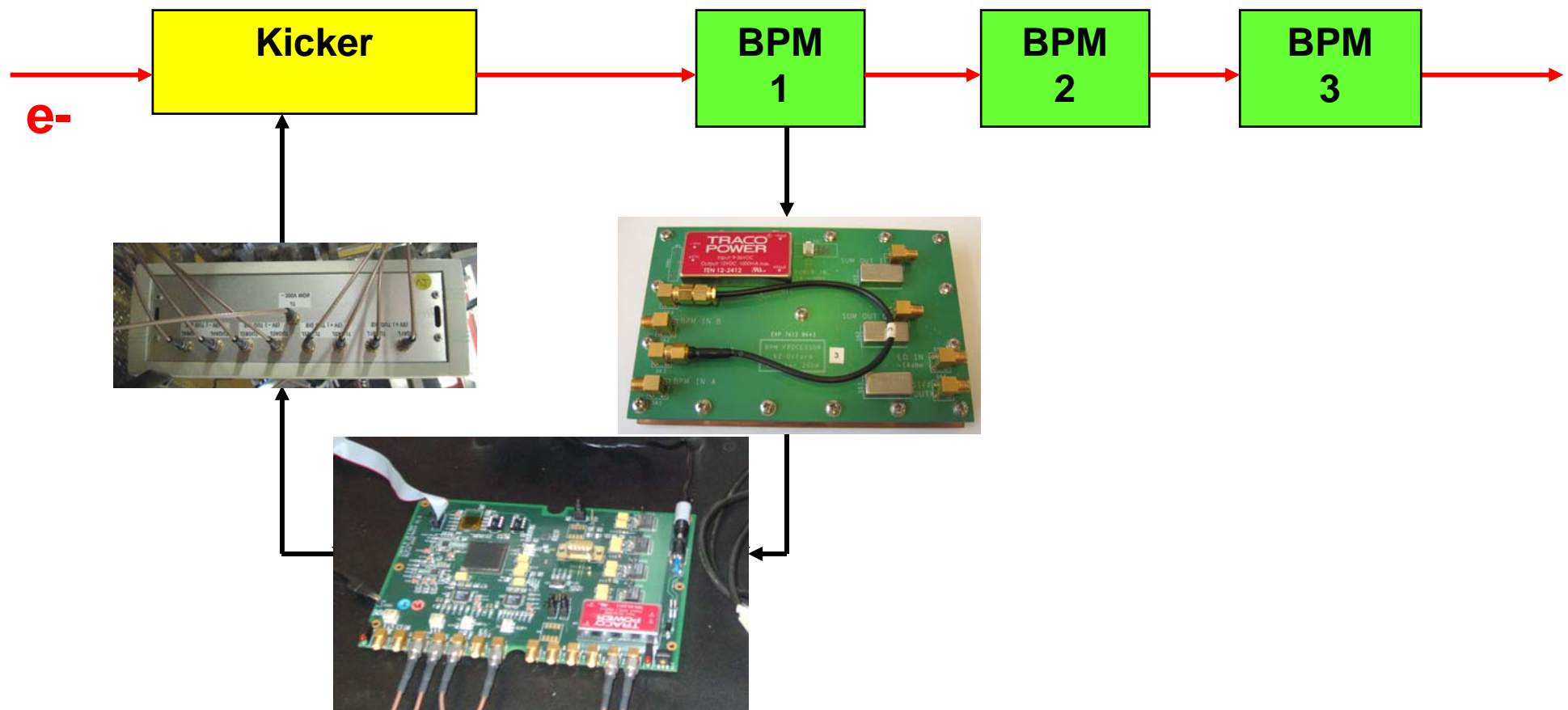


Even fast enough for CLIC intra-train FB!

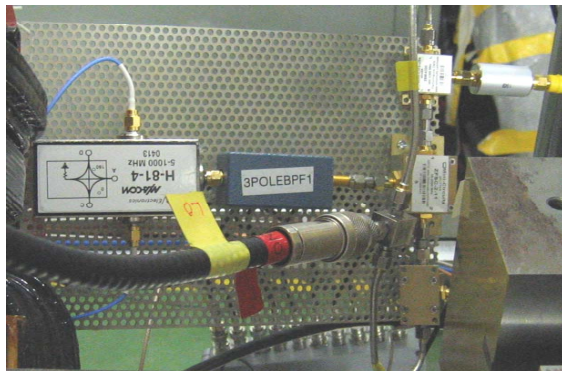
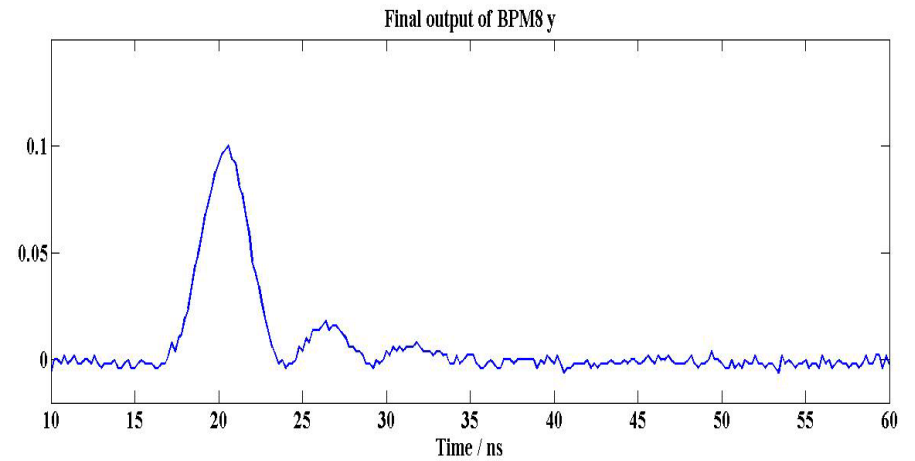
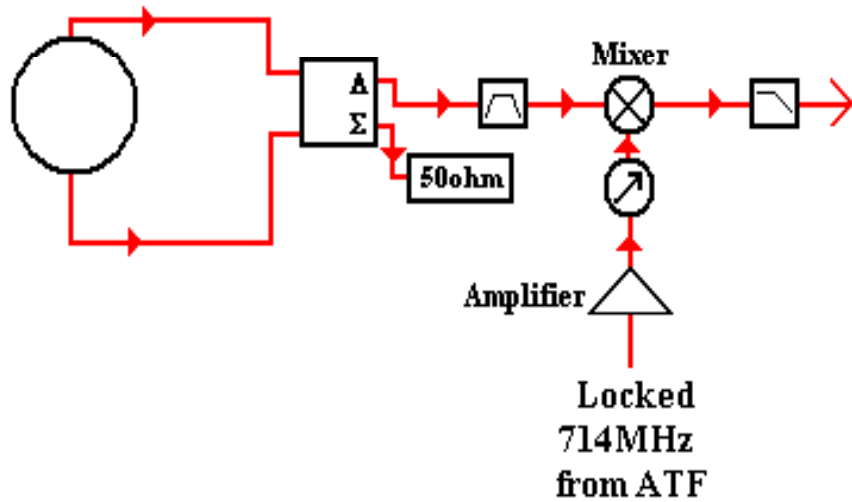
FONT4 prototype at KEK/ATF



FONT4 prototype at KEK/ATF



BPM processor



2005

Philip Burrows



2006

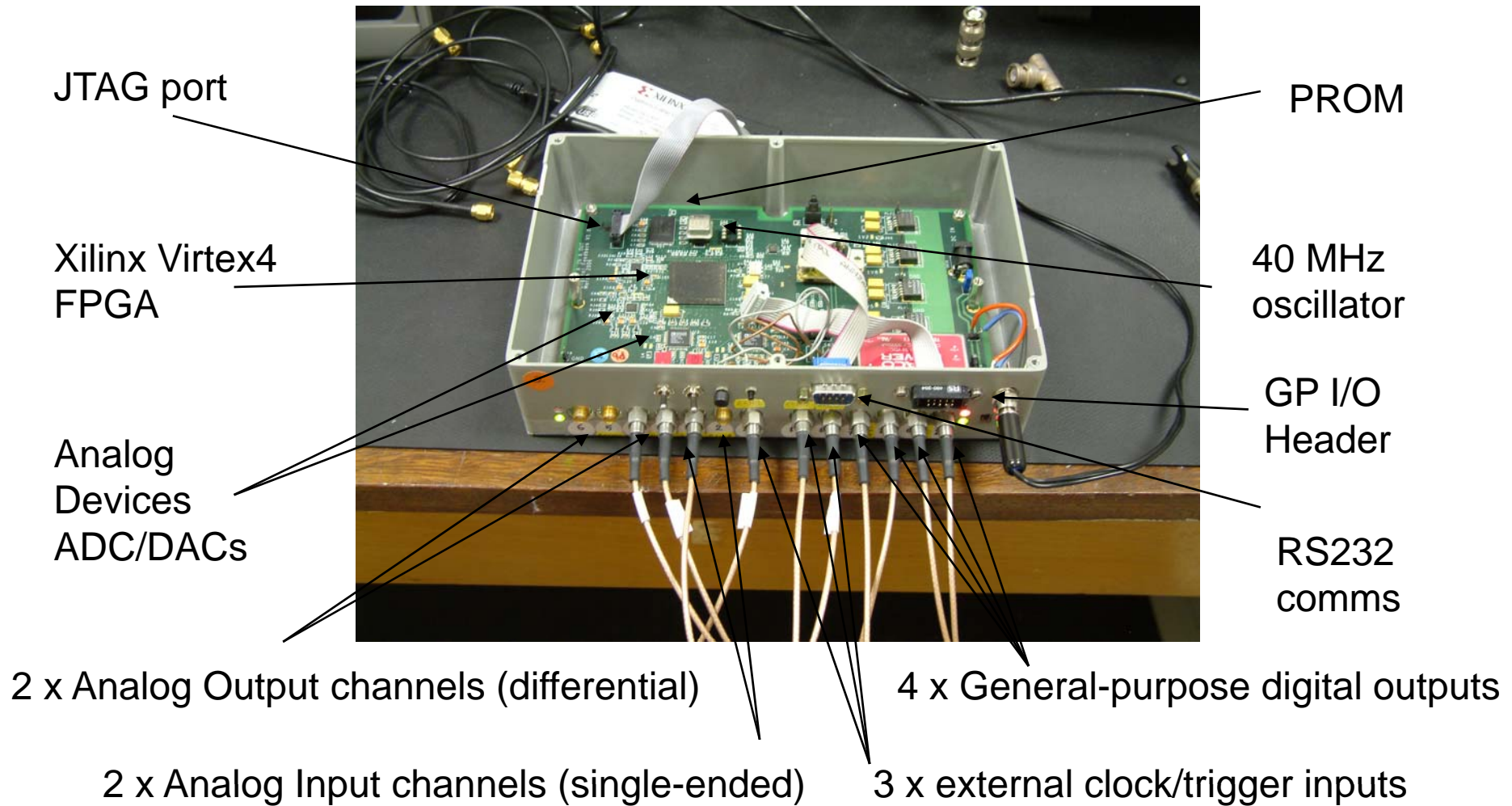
18



2007

Eurotev Workshop, Uppsala 27/08/08

Digital Feedback Board



Kicker driver amplifier

Specifications:

- **+/- 15A (kicker terminated with 50 Ohm)**
- **+/- 30A (kicker shorted at far end)**
- **35ns risetime (to 90%)**
- **pulse length 10 us (specified for 20-60 bunches)**
- **repetition rate 10 Hz**

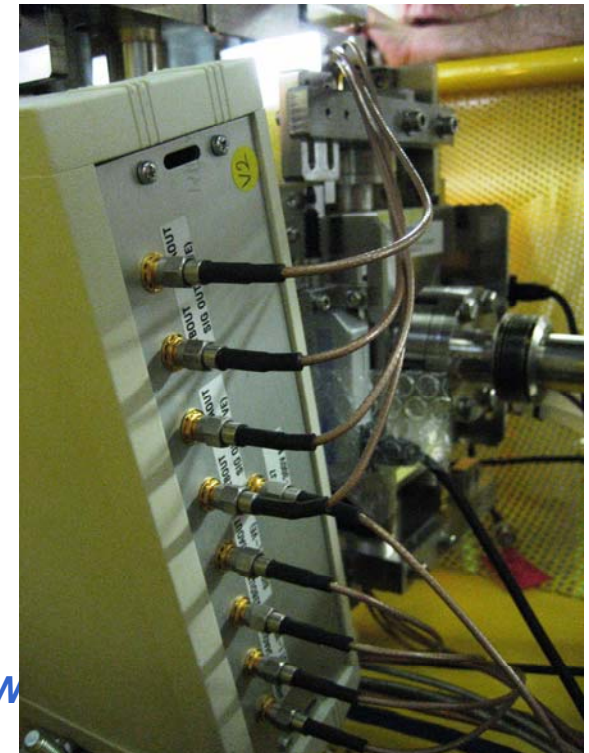
Outline design done in Oxford

Order placed with TMD Technologies Sept 06

Two prototype units delivered Dec 06

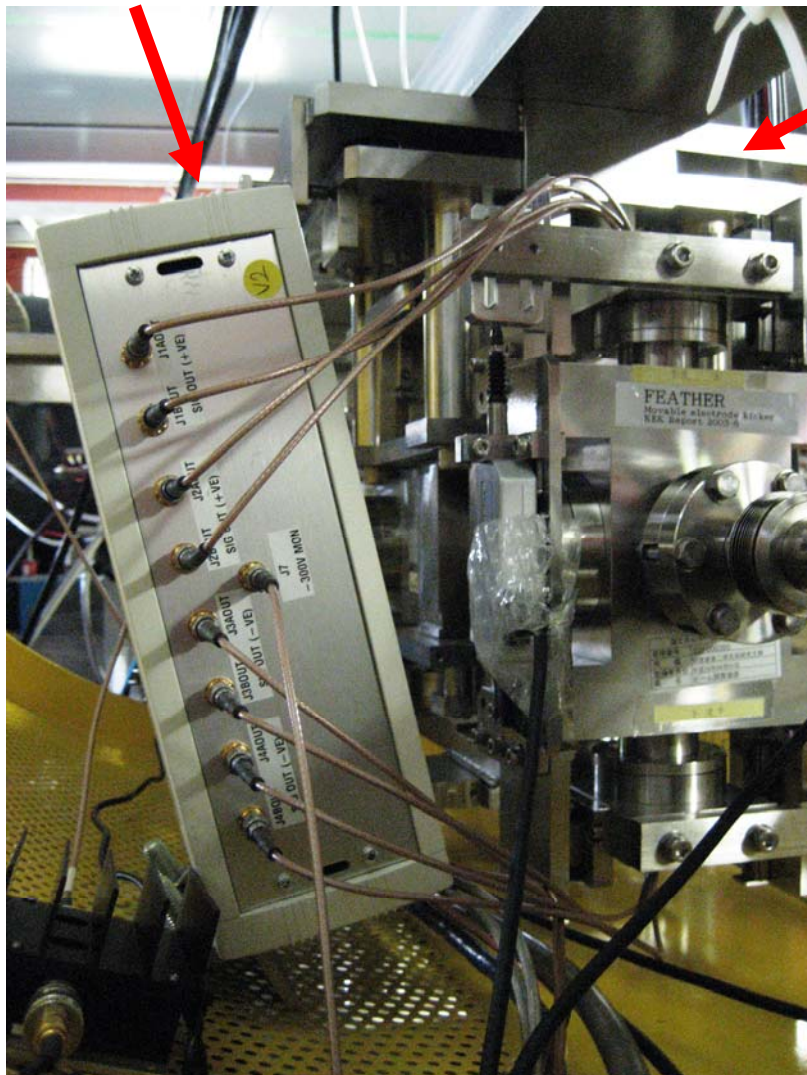
Tested numerous times with beam in 2007

and 2008

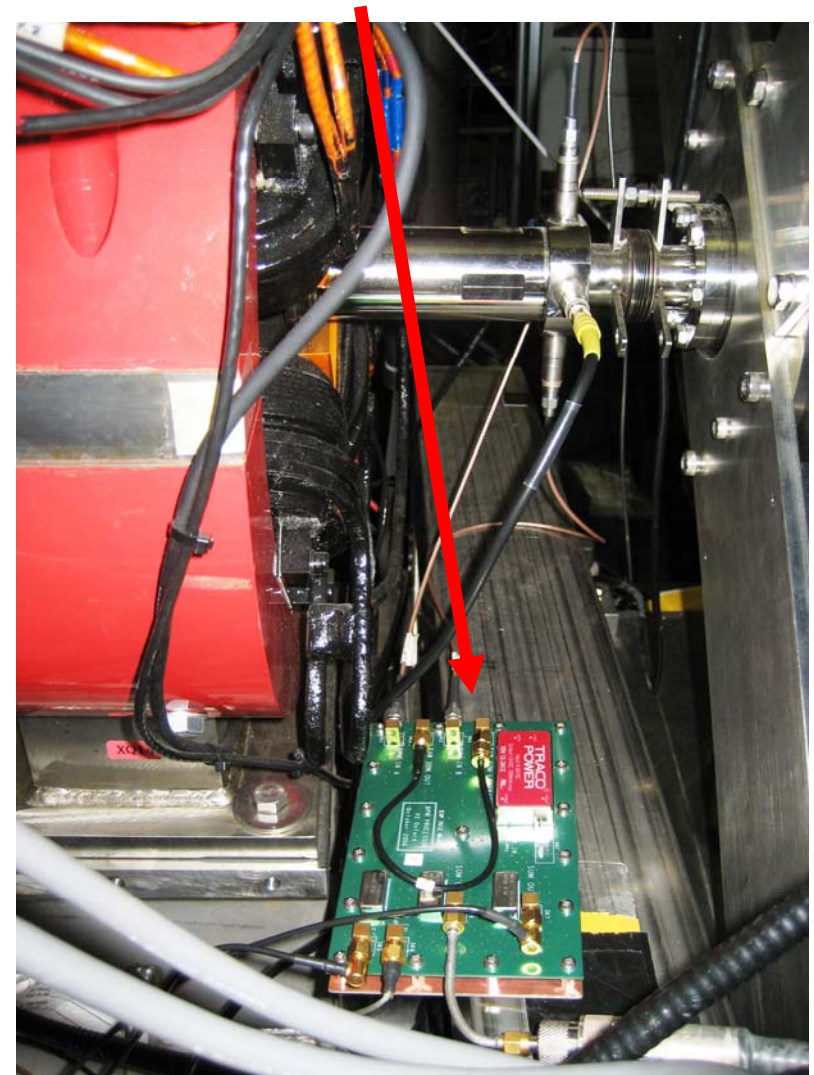


FONT4: beamline at KEK ATF

Amplifier



FEATHER Kicker



Latency estimate

- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 10ns
- **Irreducible latency: 14ns**

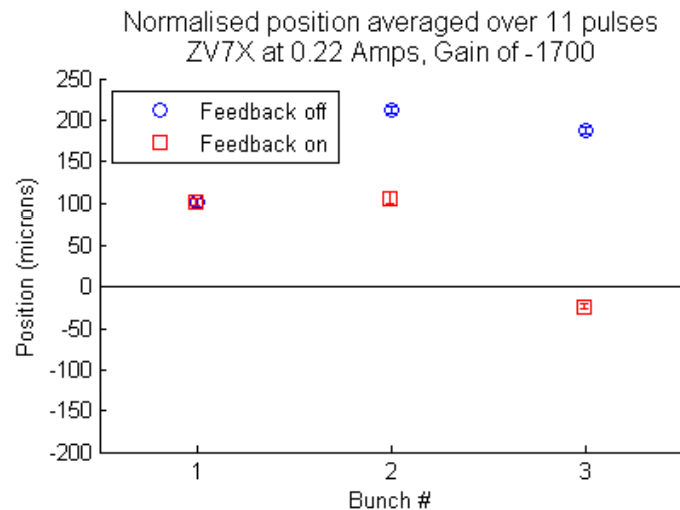
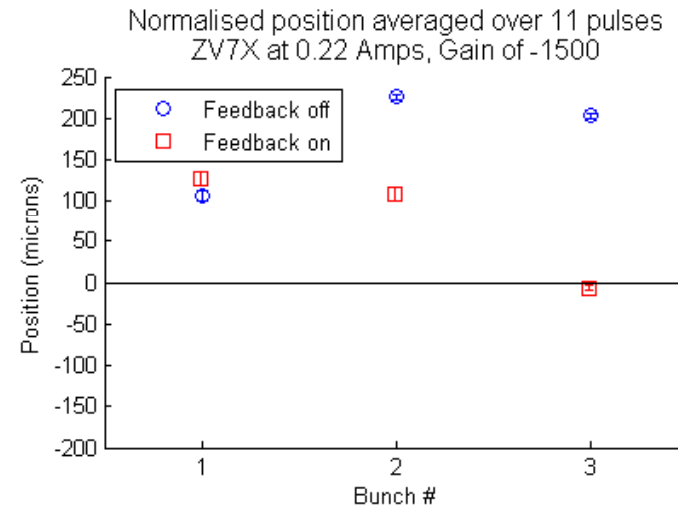
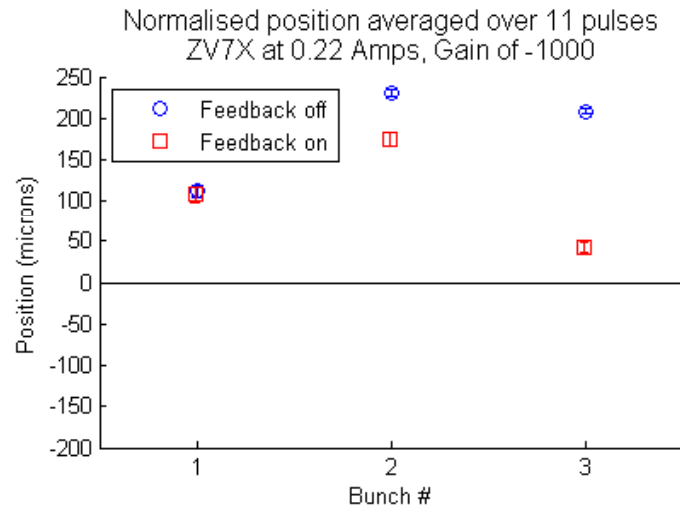
- BPM processor: 10ns
- **ADC/DAC (3.5 89 MHz cycles) 40ns**
- **Signal processing (9 357 MHz cycles) 28ns**
- **FPGA i/o 3ns**
- Amplifier 35ns
- Kicker fill time 3ns
- **Electronics latency: 119ns**

- **Total latency budget: 133ns**

May 2008 Feedback Tests

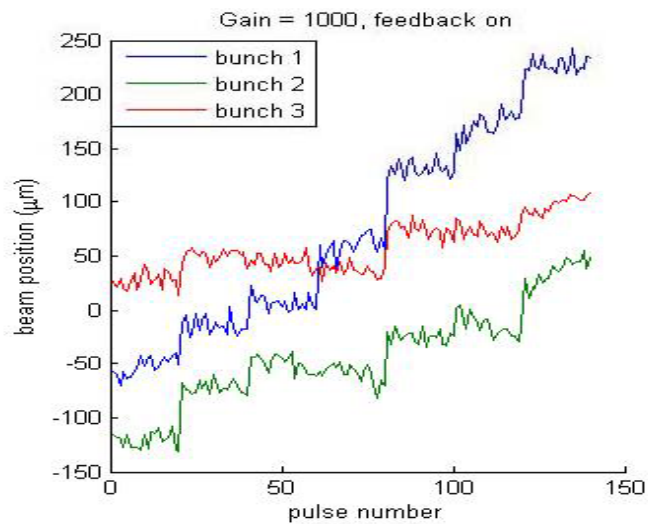
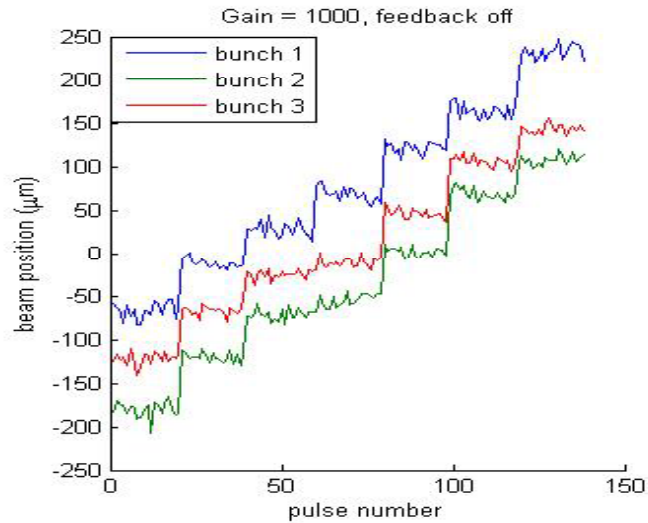
- **Beam steered using ZV7X corrector, eg.
0.22A, 0.245A, 0.27A, 0.295A, 0.32A, 0.35A, 0.38A**
- **Nominal +/-150 um range around zero (as seen in FB BPM)**
- **gain settings: 1000 (low), 1500 (medium), 1700 (high), 2000 (v. high)**
- **Two modes of feedback:
no delay loop, with delay loop**
- **Recorded analogue and digital data**
- **Data analysis in progress – all results preliminary!**

Example (1) of May 2008 Results

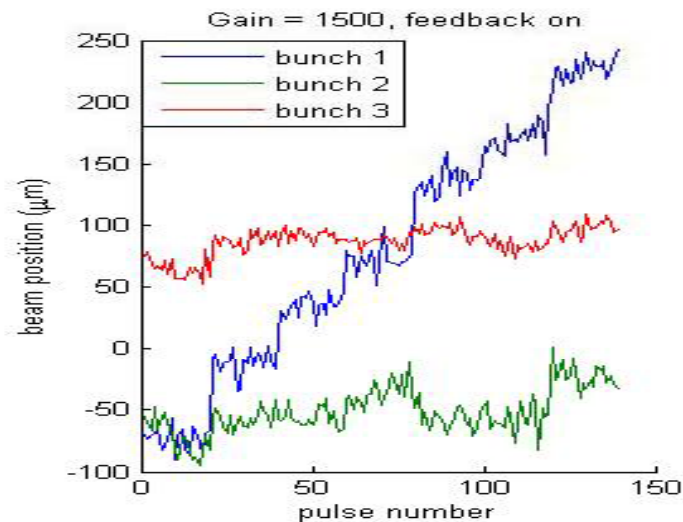
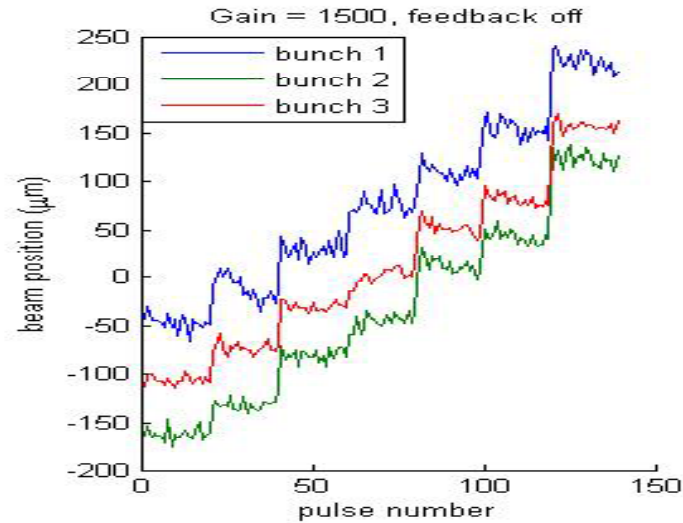


PRELIMINARY

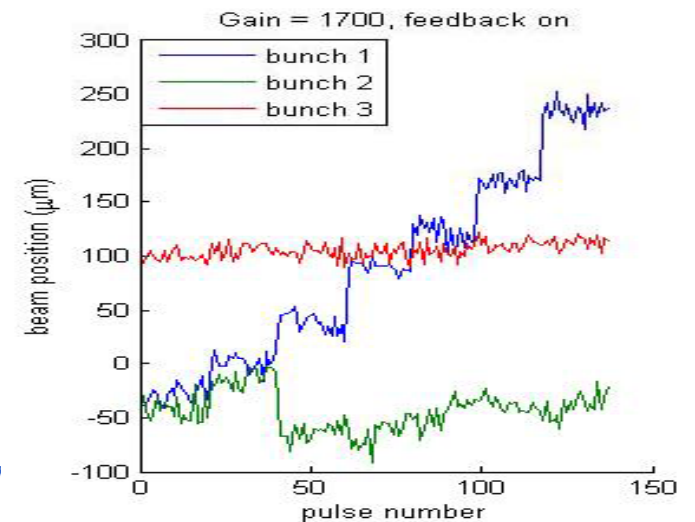
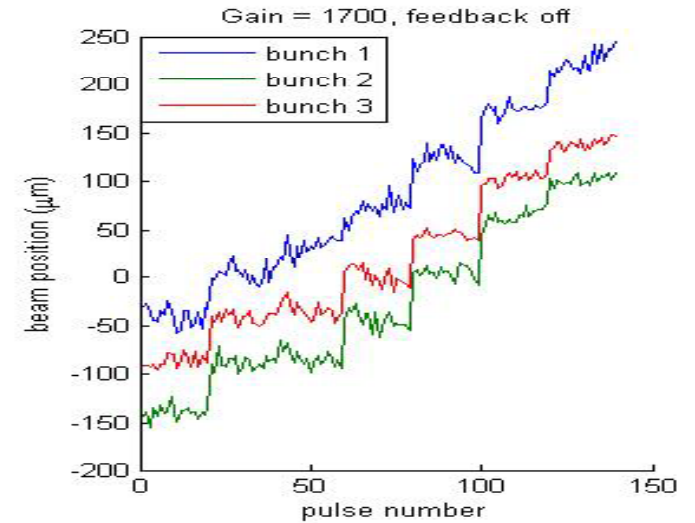
Example (2) of May 2008 Results



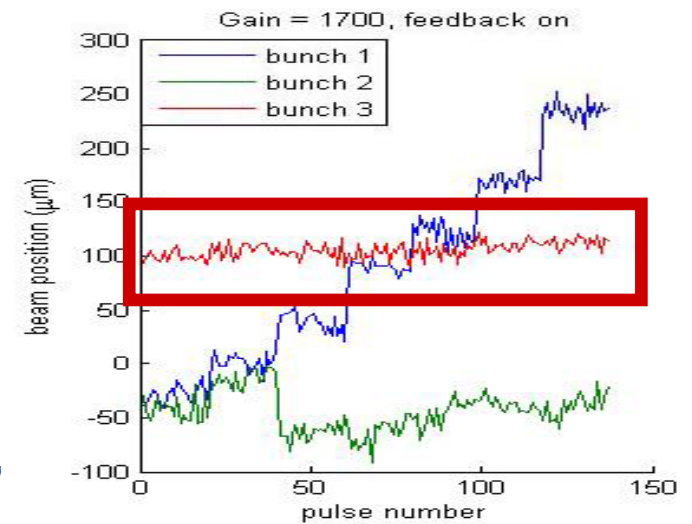
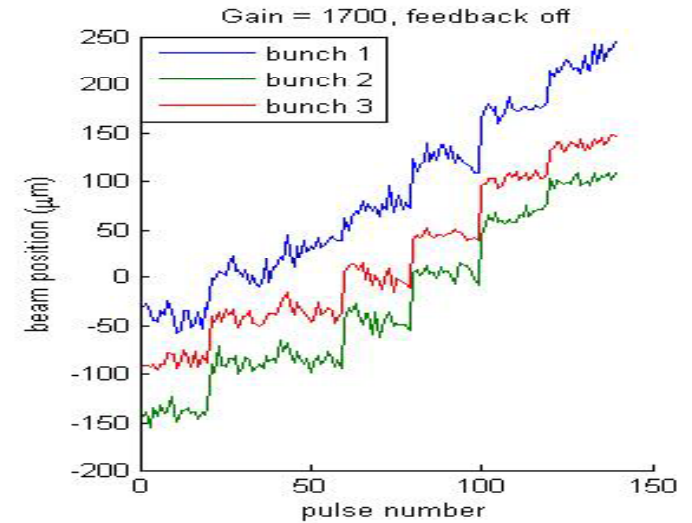
Example (2) of May 2008 Results



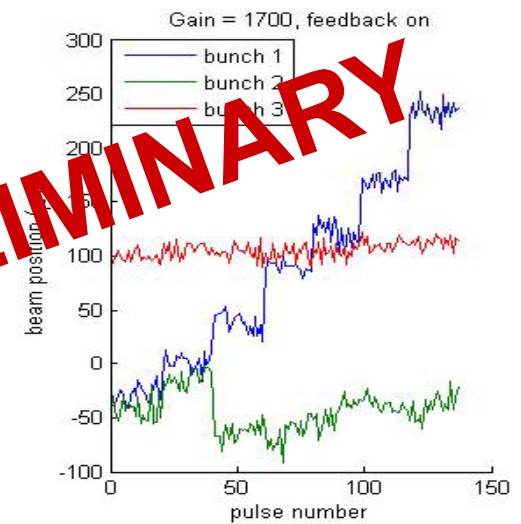
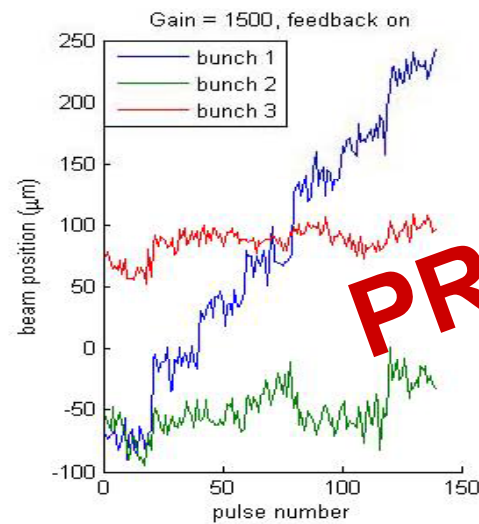
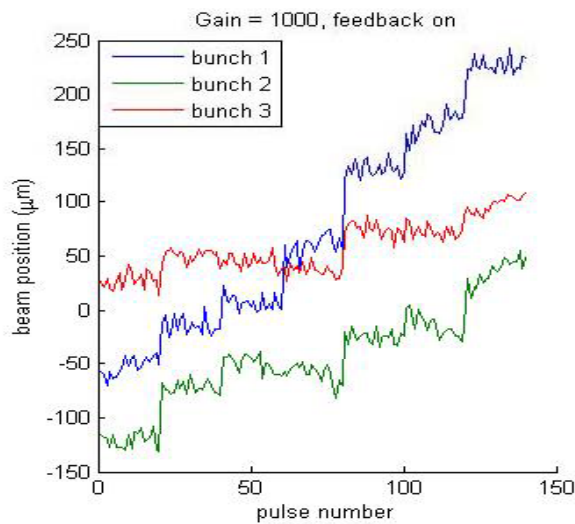
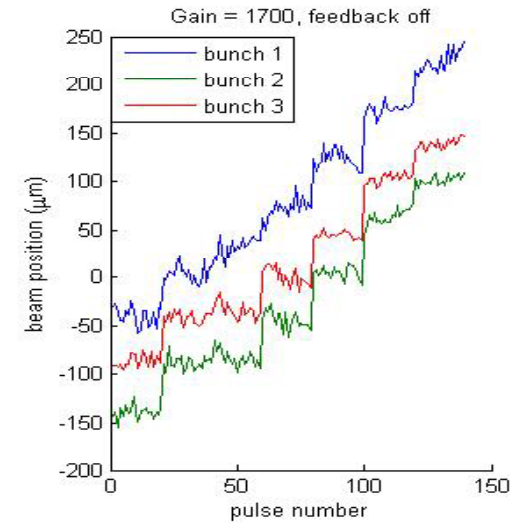
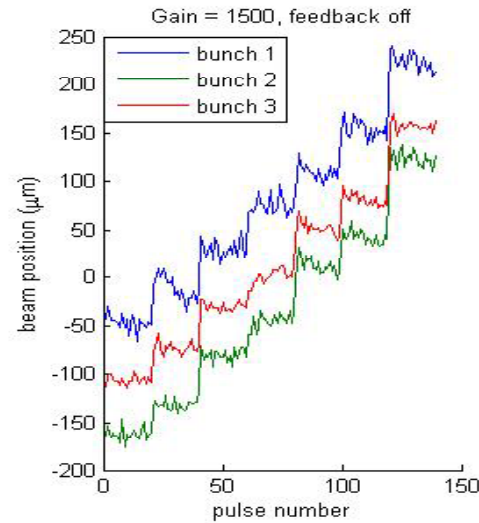
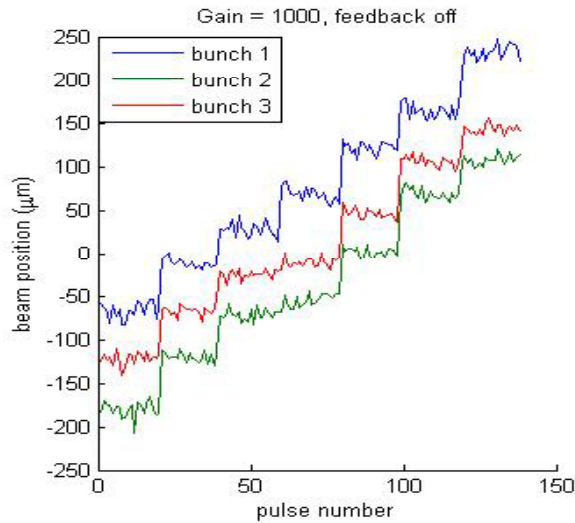
Example (2) of May 2008 Results



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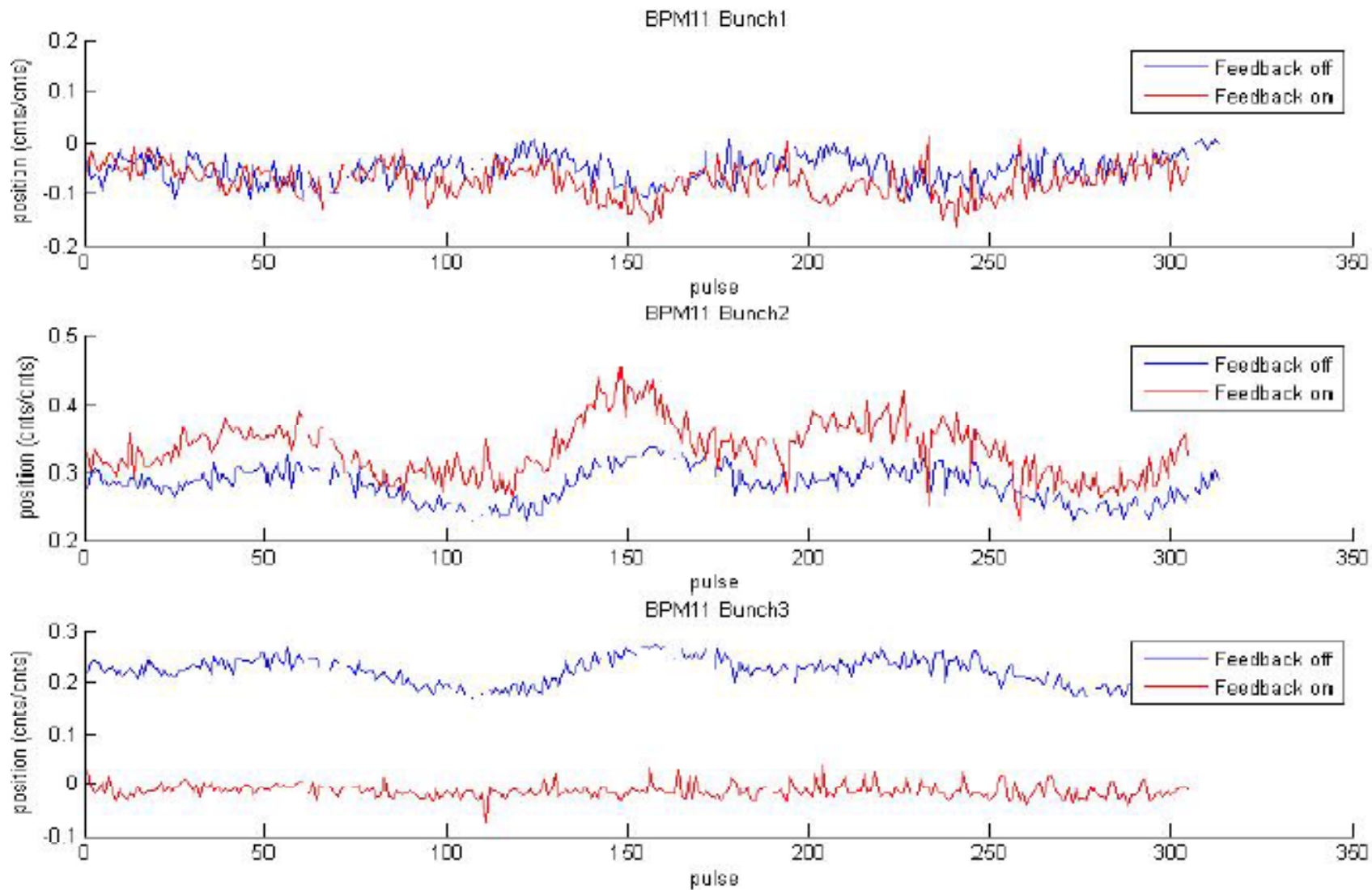


Example (2) of May 2008 Results

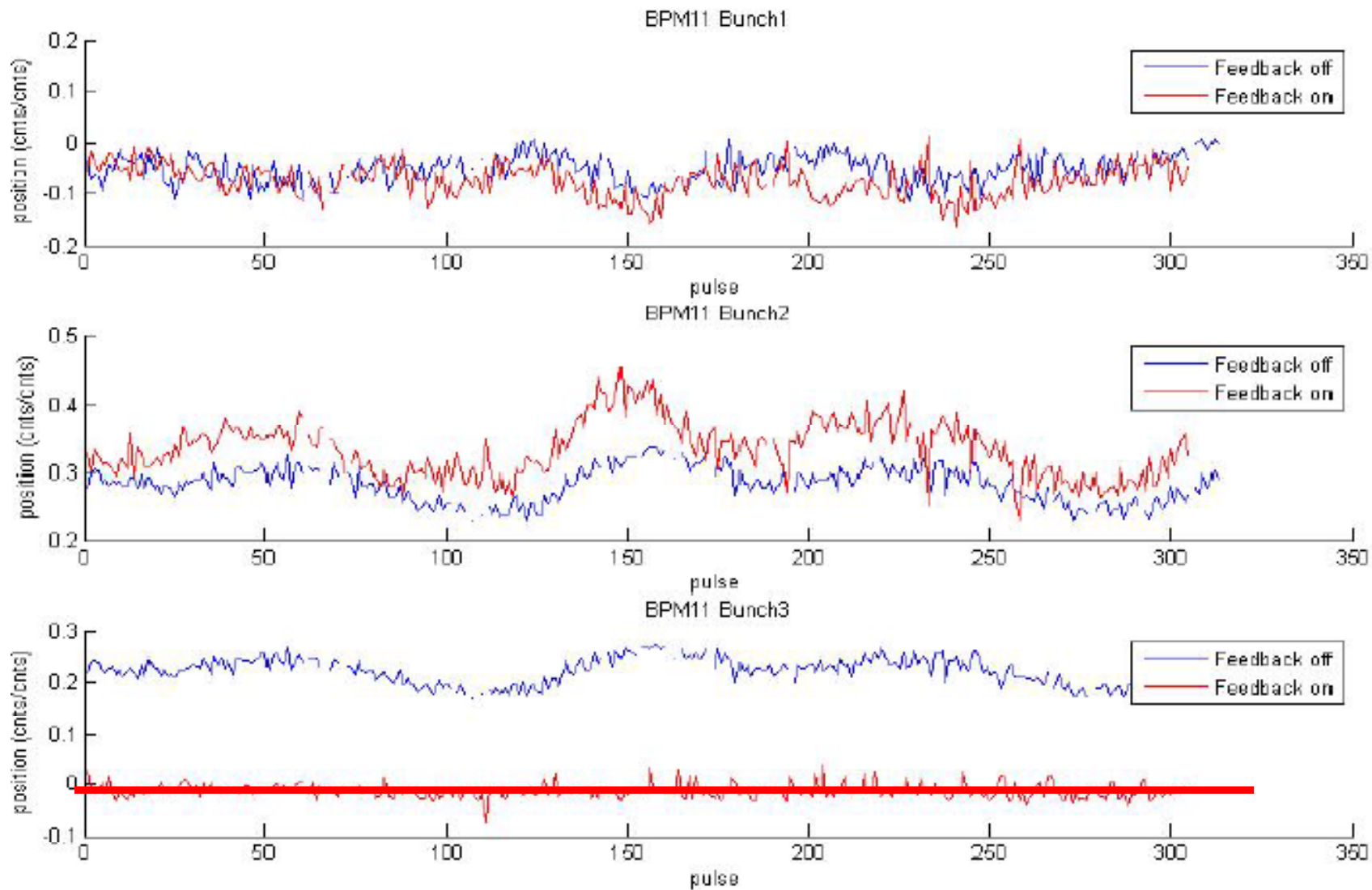


PRELIMINARY

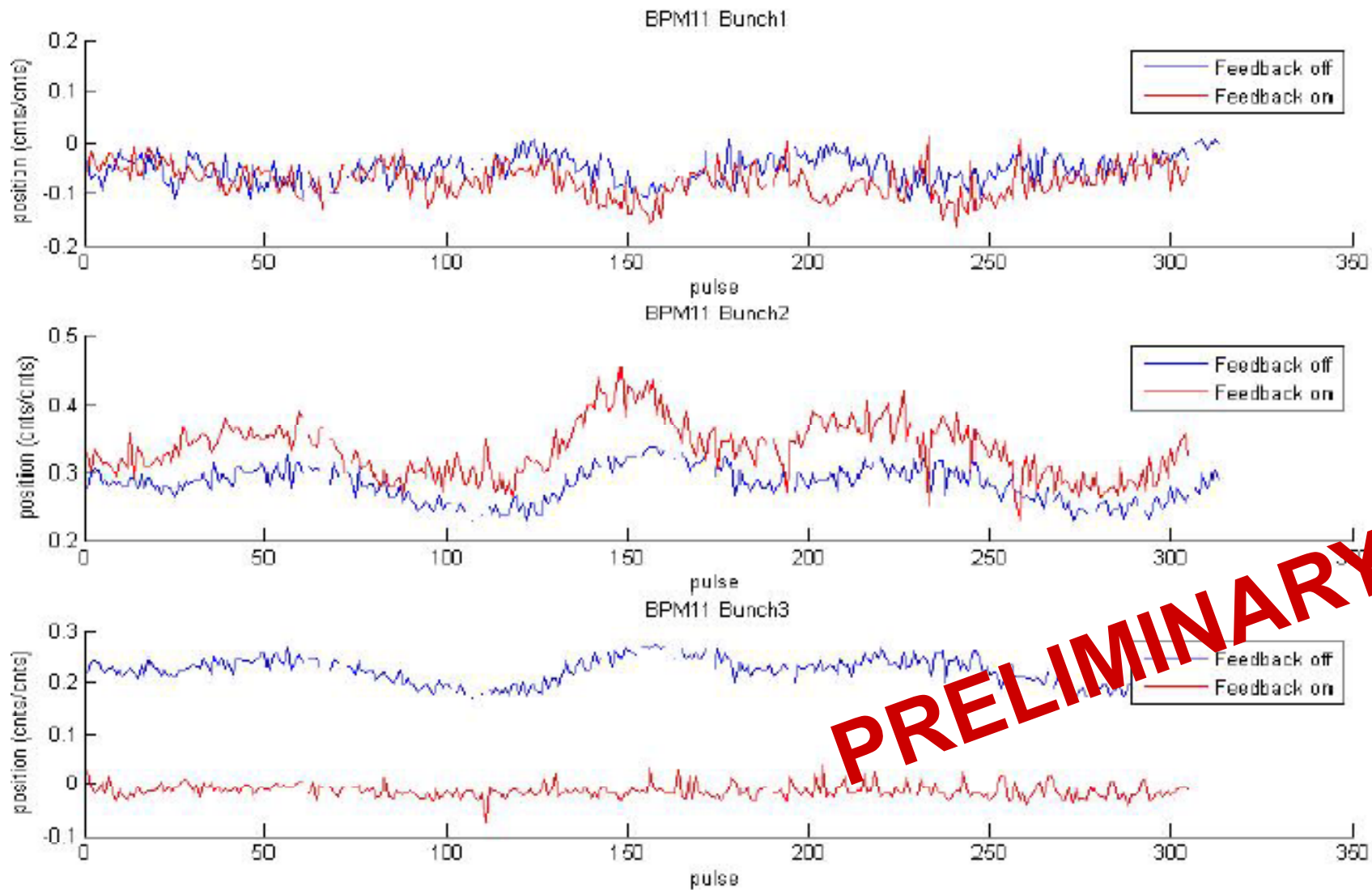
Example (3) of May 2008 Results



Example (3) of May 2008 Results

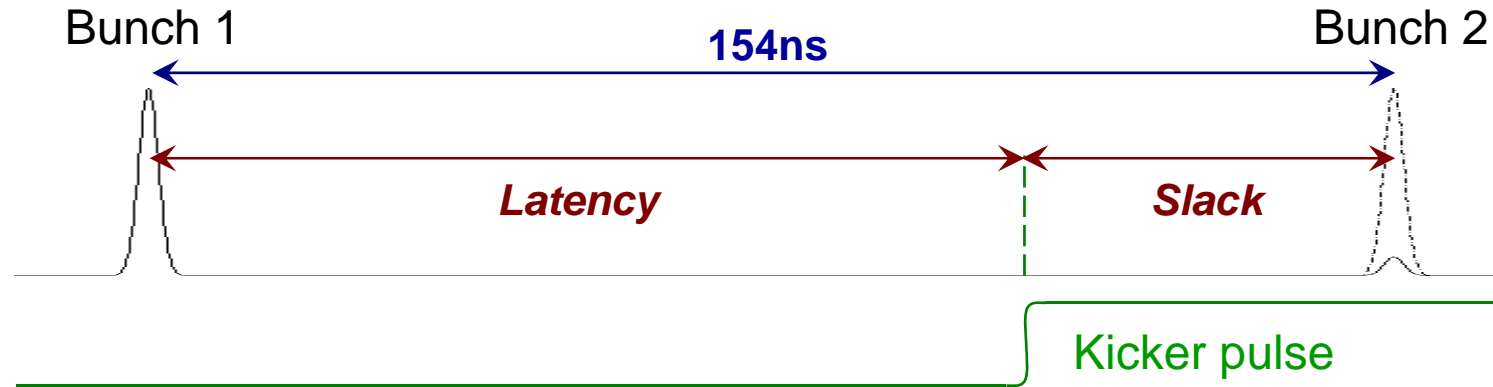


Example (3) of May 2008 Results

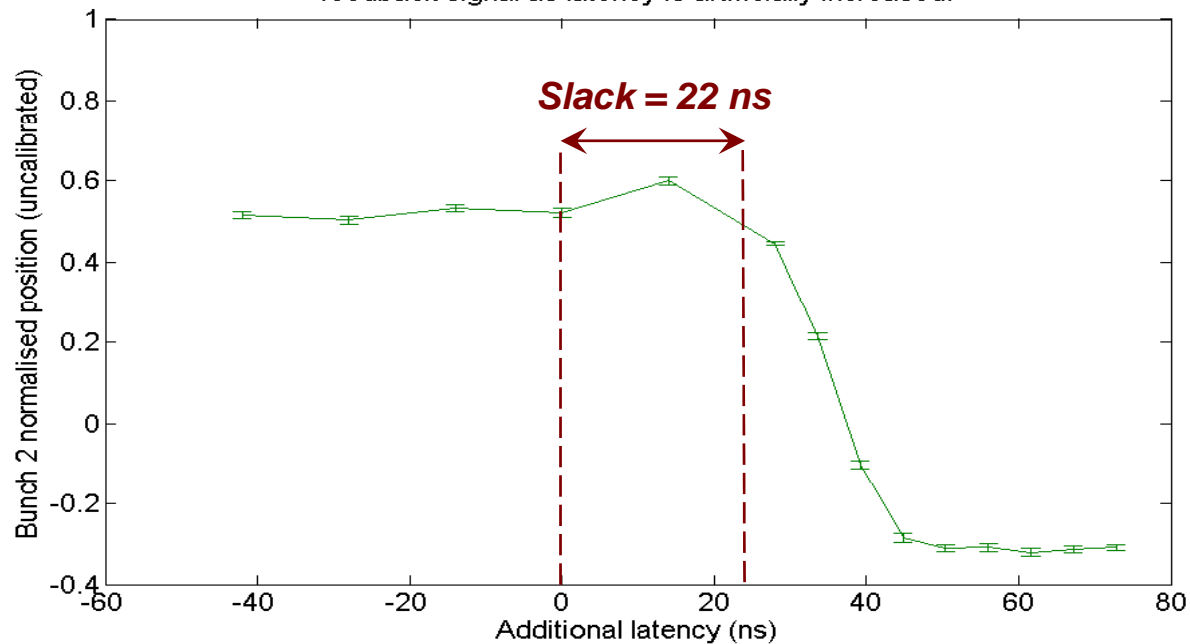


PRELIMINARY

Latency measurement



Position of bunch 2 in response to a constant magnitude feedback signal as latency is artificially increased.



Latency
= 154 - slack
= 132 ns
+ 8ns (1/Q)

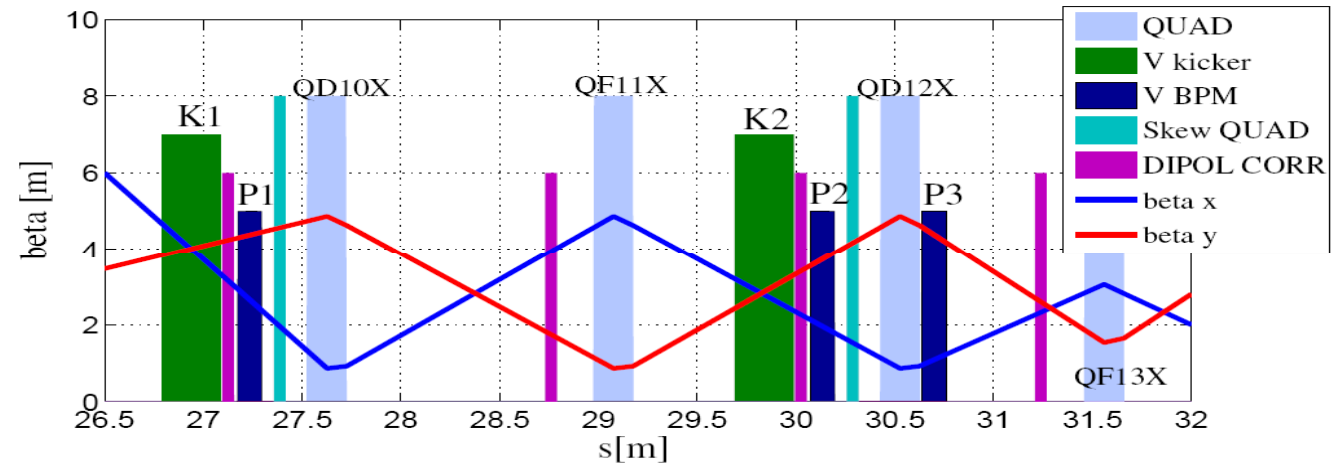
Conclusions

- **Linear collider prototype intra-train feedback systems have been designed, built, commissioned and tested with beam**
- **Latency 23 ns achieved with ALL-ANALOGUE FB**
- could be further developed for CLIC
- **Latency of 140ns achieved with DIGITAL FB**
- production ILC system being built for ATF2

ATF2 FB system

Dedicated system:

- **2 stripline kickers + fast drive amplifiers**
- **3 stripline BPMs + fast analogue front-end electronics**
- **9-channel digital FB processor**



Conclusions

Eurotev goals have been achieved!